

**K1S2816BCM****U $\bar{t}$ RAM****Document Title****8Mx16 bit Page Mode Uni-Transistor Random Access Memory****Revision History**

<b><u>Revision No.</u></b>	<b><u>History</u></b>	<b><u>Draft Date</u></b>	<b><u>Remark</u></b>
0.0	Initial Draft - Design Target	April 12, 2004	Preliminary
0.1	Revised - Updated "TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$ Controlled)" in page 8 and added tWHP( $\overline{WE}$ High Pulse Width) parameter as Min.5ns - Added comment on standby current(IsB1) measure condition as "Standby mode is supposed to be set up after at least one active operation after power up. IsB1 is measured after 60ms from the time when standby mode is set up." - Changed IsB1 value(< 85°C) from 200 $\mu$ A into 250 $\mu$ A	July 12, 2004	Preliminary
1.0	Finalize - Changed tOH from 5ns to 3ns	April 06, 2005	Final

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# K1S2816BCM

# U<sub>t</sub>RAM

## 8M x 16 bit Page Mode Uni-Transistor CMOS RAM

### FEATURES

- Process Technology: CMOS
- Organization: 8M x16 bit
- Power Supply Voltage: 1.7~2.0V
- Three State Outputs
- Compatible with Low Power SRAM
- Support 4 page read mode
- Package Type: TBD

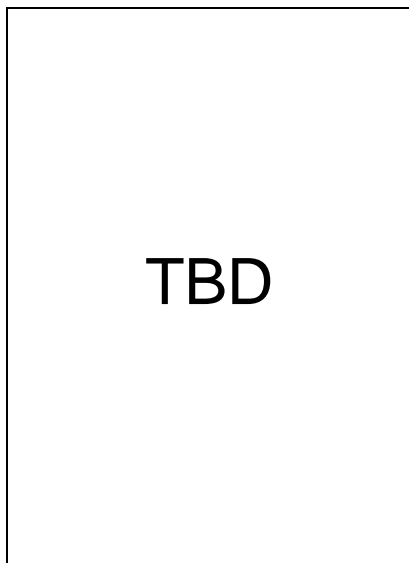
### GENERAL DESCRIPTION

The K1S2816BCM is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device supports 4 page read operation and Industrial temperature range. The device supports dual chip selection for user interface. The device also supports internal Temperature Compensated Self Refresh mode for the standby power saving at room temperature range.

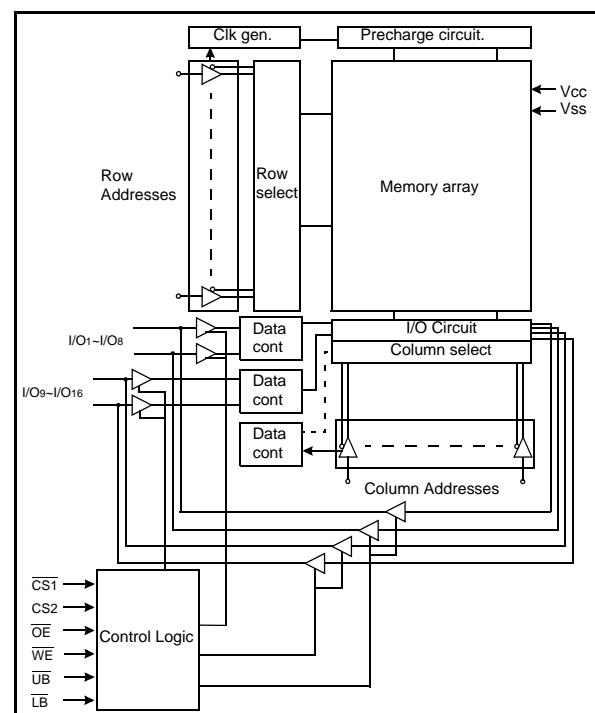
### PRODUCT FAMILY

Product Family	Operating Temp.	Vcc Range	Speed (trc)	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Max.)	Operating (I <sub>CC2</sub> , Max.)	
K1S2816BCM-I	Industrial(-40~85°C)	1.7~2.0V	70ns	130μA(<40°C)	40mA	TBD
				250μA(<85°C)		

### PIN DESCRIPTION



### FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
$\overline{CS1}, \overline{CS2}$	Chip Select Inputs	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O <sub>9~16</sub> )
A <sub>0</sub> ~A <sub>22</sub>	Address Inputs	$\overline{LB}$	Lower Byte(I/O <sub>1~8</sub> )
I/O <sub>1</sub> ~I/O <sub>16</sub>	Data Inputs/Outputs	NC	No Connection <sup>1)</sup>

1) Reserved for future use

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# K1S2816BCM

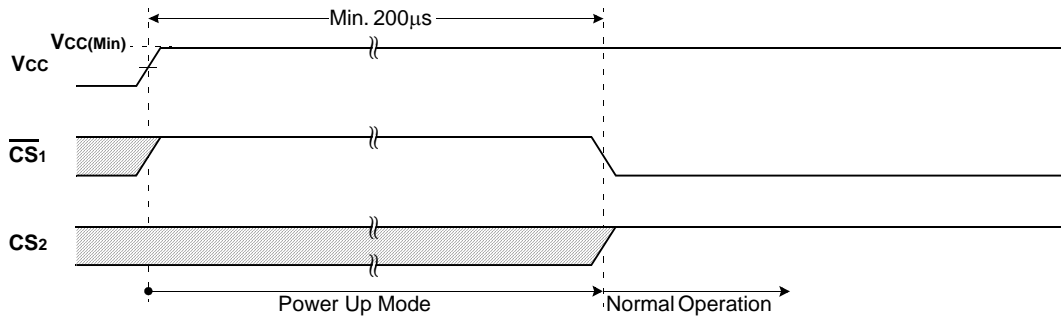
# U<sub>t</sub>RAM

## POWER UP SEQUENCE

During the Power Up mode, the standby current can not be guaranteed. To get the stable standby current level, at least one cycle of active operation should be implemented regardless of wait time duration. To get the appropriate device operation, be sure to keep the following power up sequence.

1. Apply power.
2. Maintain stable power ( $V_{CC} \text{ min.} = 1.7V$ ) for a minimum  $200\mu s$  with  $\overline{CS1} = \text{high}$  or  $CS2 = \text{low}$ .

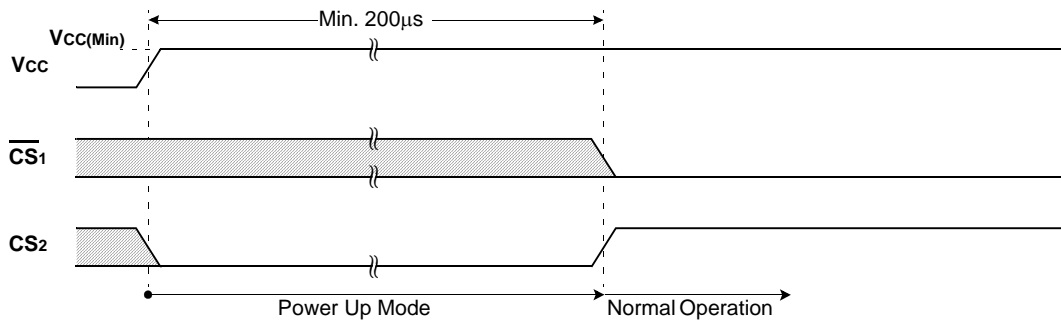
### TIMING WAVEFORM OF POWER UP(1) ( $\overline{CS1}$ controlled)



#### POWER UP(1)

1. After  $V_{CC}$  reaches  $V_{CC}(\text{Min.})$ , wait  $200\mu s$  with  $\overline{CS1}$  high. Then the device gets into the normal operation.

### TIMING WAVEFORM OF POWER UP(2) ( $CS2$ controlled)



#### POWER UP(2)

1. After  $V_{CC}$  reaches  $V_{CC}(\text{Min.})$ , wait  $200\mu s$  with  $CS2$  low. Then the device gets into the normal operation.

**K1S2816BCM****U $\bar{t}$ RAM****FUNCTIONAL DESCRIPTION**

$\overline{\text{CS1}}$	$\text{CS2}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	I/O <sub>1-8</sub>	I/O <sub>9-16</sub>	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Deselected	Standby
X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X <sup>1)</sup>	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X <sup>1)</sup>	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X <sup>1)</sup>	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X <sup>1)</sup>	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X <sup>1)</sup>	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

**ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>**

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V <sub>ss</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.2 to V <sub>CC</sub> +0.3V	V
Voltage on V <sub>CC</sub> supply relative to V <sub>ss</sub>	V <sub>CC</sub>	-0.2 to 2.5V	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	T <sub>A</sub>	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

**K1S2816BCM****U<sub>t</sub>RAM****PRODUCT LIST**

Industrial Temperature Product(-40~85°C)	
Part Name	Function
K1S2816BCM	70ns, 1.8V

**RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>**

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	1.7	1.85	2.0	V
Ground	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	0.8 x V <sub>CC</sub>	-	V <sub>CC</sub> +0.2 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.2 <sup>3)</sup>	-	0.4	V

1. T<sub>A</sub>=-40 to 85°C, otherwise specified.
2. Overshoot: V<sub>CC</sub>+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

**CAPACITANCE<sup>1)</sup>(f=1MHz, T<sub>A</sub>=25°C)**

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

**DC AND OPERATING CHARACTERISTICS**

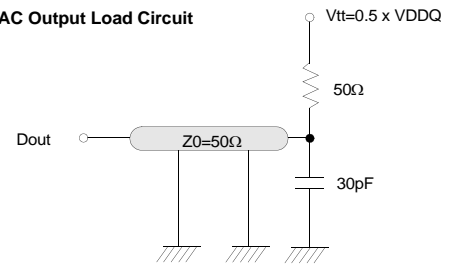
Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{LB}=\overline{UB}=V_{IH}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Average operating current	I <sub>CC2</sub>	Cycle time=t <sub>RC</sub> +3t <sub>PC</sub> , I <sub>IO</sub> =0mA, 100% duty, $\overline{CS1}=V_{IL}$ , CS2=V <sub>IH</sub> , $\overline{LB}=V_{IL}$ or/and $\overline{UB}=V_{IL}$ , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	40	mA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =0.1mA	-	-	0.2	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-0.1mA	1.4	-	-	V	
Standby Current(CMOS)	I <sub>SB1</sub> <sup>1)</sup>	Other inputs=0~V <sub>CC</sub> 1) $\overline{CS1} \geq V_{CC}-0.2V$ , CS2≥V <sub>CC</sub> -0.2V( $\overline{CS1}$ controlled) or 2) 0V ≤ CS2 ≤ 0.2V(CS2 controlled)	< 40°C	-	-	130	μA
			< 85°C	-	-	250	μA

1. Standby mode is supposed to be set up after at least one active operation.after power up.

I<sub>SB1</sub> is measured after 60ms from the time when standby mode is set up.

**K1S2816BCM****U<sub>t</sub>RAM****AC OPERATING CONDITIONS****TEST CONDITIONS**(Test Load and Test Input/Output Reference)Input pulse level: 0.2 to V<sub>cc</sub>-0.2V

Input rising and falling time: 3ns

Input and output reference voltage: 0.5 x V<sub>cc</sub>Output load (See right): C<sub>L</sub>=30pF**AC Output Load Circuit****AC CHARACTERISTICS** (V<sub>cc</sub>=1.7~2.0V, T<sub>A</sub>=-40 to 85°C)

	Parameter List	Symbol	Speed Bins		Units
			70ns		
			Min	Max	
Read	Read Cycle Time	t <sub>RC</sub>	70	-	ns
	Address Access Time	t <sub>AA</sub>	-	70	ns
	Chip Select to Output	t <sub>CO</sub>	-	70	ns
	Output Enable to Valid Output	t <sub>OE</sub>	-	35	ns
	$\overline{UB}$ , $\overline{LB}$ Access Time	t <sub>BA</sub>	-	70	ns
	Chip Select to Low-Z Output	t <sub>LZ</sub>	10	-	ns
	$\overline{UB}$ , $\overline{LB}$ Enable to Low-Z Output	t <sub>BLZ</sub>	10	-	ns
	Output Enable to Low-Z Output	t <sub>OLZ</sub>	5	-	ns
	Chip Disable to High-Z Output	t <sub>HZ</sub>	0	25	ns
	$\overline{UB}$ , $\overline{LB}$ Disable to High-Z Output	t <sub>BHZ</sub>	0	25	ns
	Output Disable to High-Z Output	t <sub>OHZ</sub>	0	25	ns
	Output Hold from Address Change	t <sub>OH</sub>	3	-	ns
	Page Cycle	t <sub>PC</sub>	25	-	ns
Page Access Time	t <sub>PA</sub>	-	20	ns	
Write	Write Cycle Time	t <sub>WC</sub>	70	-	ns
	Chip Select to End of Write	t <sub>CW</sub>	60	-	ns
	Address Set-up Time	t <sub>AS</sub>	0	-	ns
	Address Valid to End of Write	t <sub>AW</sub>	60	-	ns
	$\overline{UB}$ , $\overline{LB}$ Valid to End of Write	t <sub>BW</sub>	60	-	ns
	Write Pulse Width	t <sub>WP</sub>	55 <sup>1)</sup>	-	ns
	$\overline{WE}$ High Pulse Width	t <sub>WHP</sub>	5	-	ns
	Write Recovery Time	t <sub>WR</sub>	0	-	ns
	Write to Output High-Z	t <sub>WHZ</sub>	0	25	ns
	Data to Write Time Overlap	t <sub>DW</sub>	30	-	ns
	Data Hold from Write Time	t <sub>DH</sub>	0	-	ns
	End Write to Output Low-Z	t <sub>OW</sub>	5	-	ns

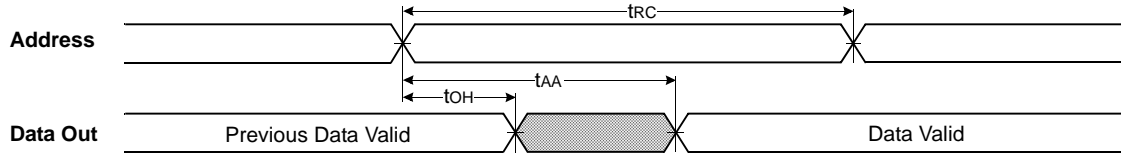
1. t<sub>WP</sub>(min)=70ns for continuous write operation over 50 times.

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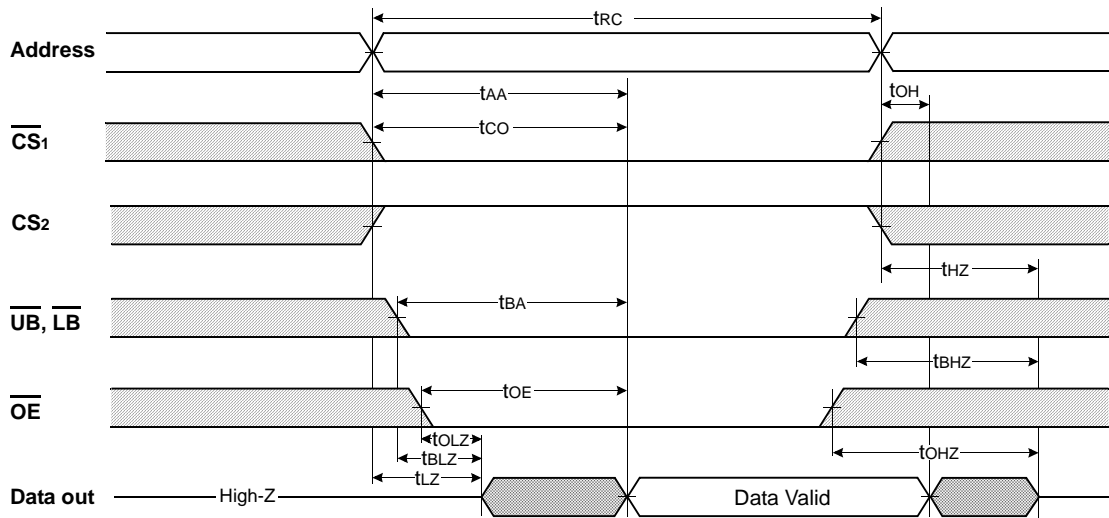
# U $\bar{t}$ RAM

## TIMING DIAGRAMS

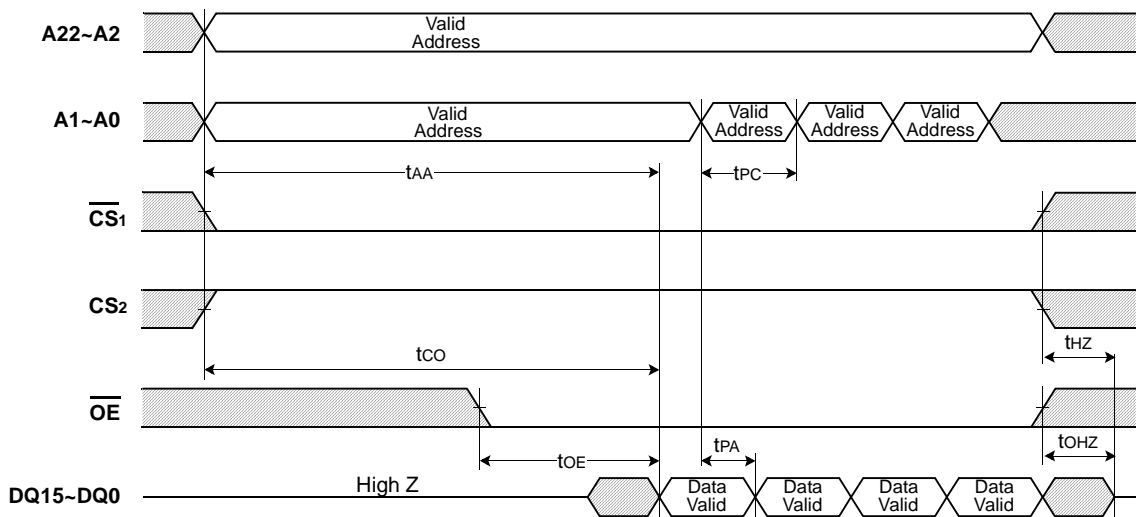
**TIMING WAVEFORM OF READ CYCLE(1)**(Address Controlled,  $\overline{CS1}=\overline{OE}=V_{IL}$ ,  $CS2=\overline{WE}=V_{IH}$ ,  $\overline{UB}$  or/and  $\overline{LB}=V_{IL}$ )



**TIMING WAVEFORM OF READ CYCLE(2)**( $\overline{WE}=V_{IH}$ )



**TIMING WAVEFORM OF PAGE CYCLE(READ ONLY)**



(READ CYCLE)

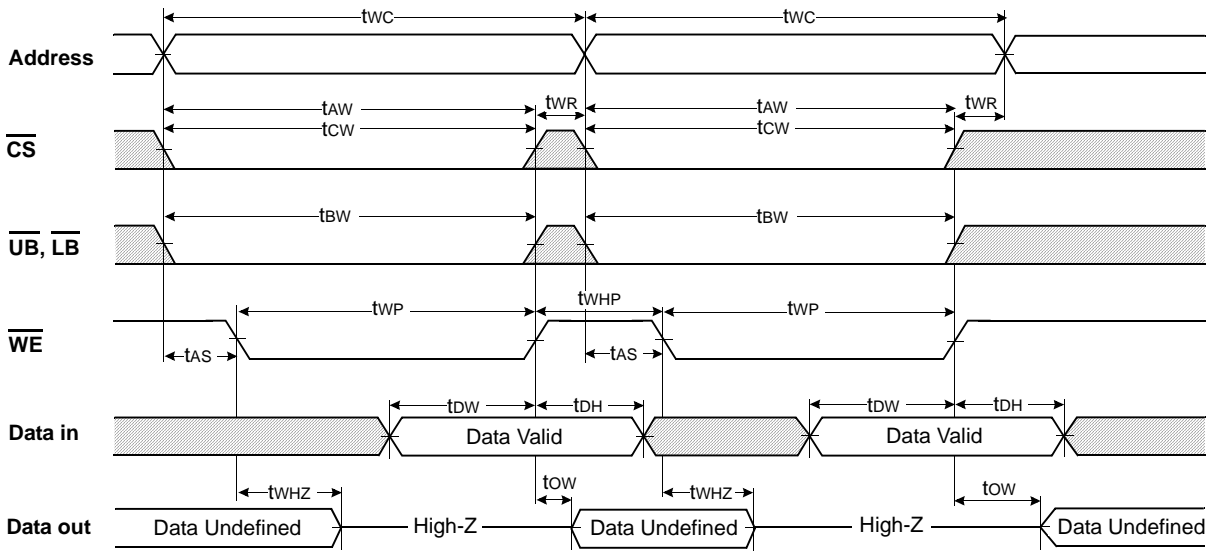
1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.
3.  $t_{OE}(\text{max})$  is met only when  $\overline{OE}$  becomes enabled after  $t_{AA}(\text{max})$ .
4. If invalid address signals shorter than min.  $t_{RC}$  are continuously repeated for over 4 $\mu$ s, the device needs a normal read timing( $t_{RC}$ ) or needs to sustain standby state for min.  $t_{RC}$  at least once in every 4 $\mu$ s.



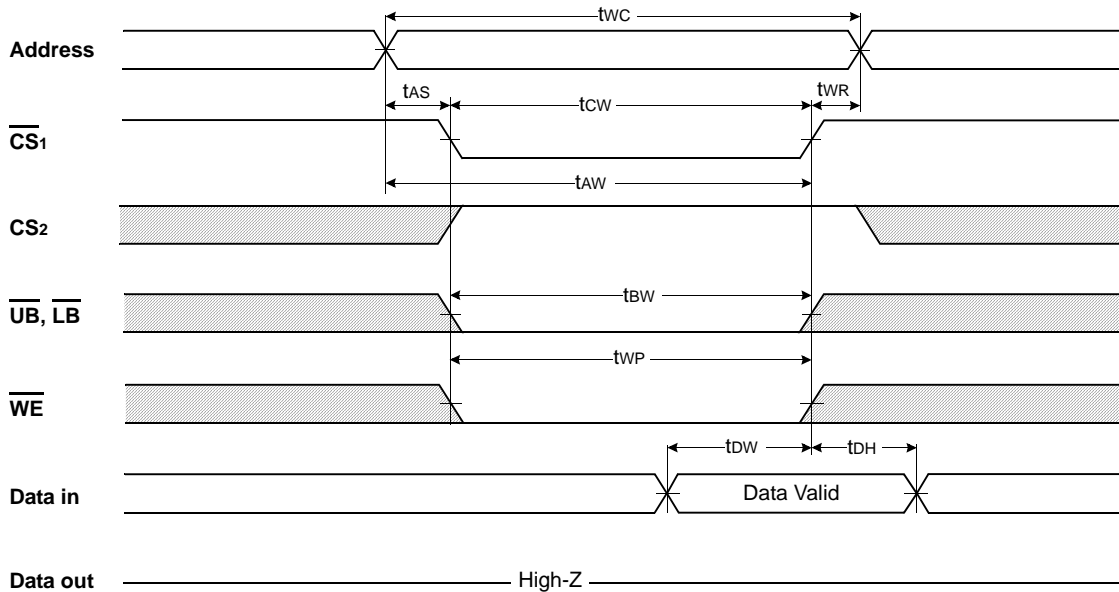
# K1S2816BCM

# U<sub>t</sub>RAM

## TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$ Controlled)



## TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS1}$ Controlled)

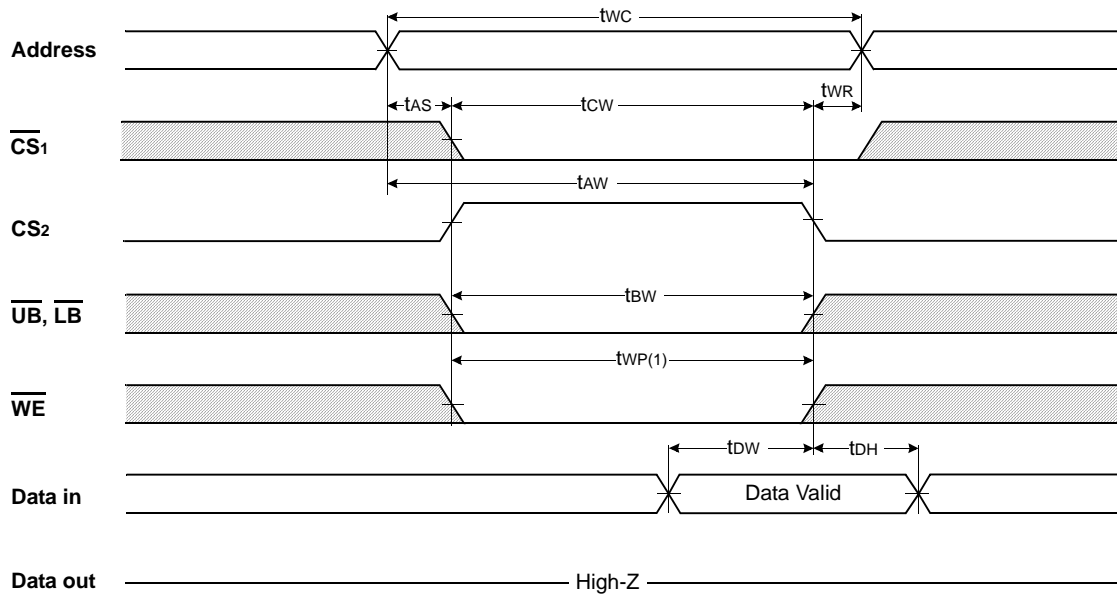
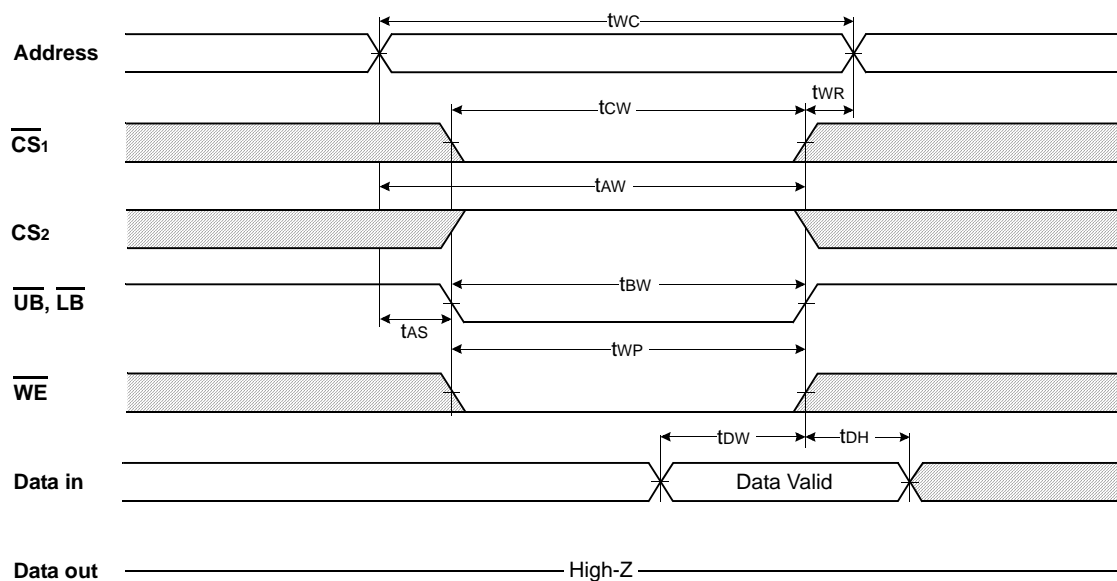




## K1S2816BCM

U $\bar{t}$ RAM

## TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)

TIMING WAVEFORM OF WRITE CYCLE(4) ( $\overline{UB}$ ,  $\overline{LB}$  Controlled)

## NOTES (WRITE CYCLE)

1. A write occurs during the overlap( $t_{WP}$ ) of low  $\overline{CS1}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS1}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS1}$  goes high and  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS1}$  going low to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  is applied in case a write ends with  $\overline{CS1}$  or  $\overline{WE}$  going high.
5.  $t_{WP}(\min)=70\text{ns}$  for continuous write operation over 50 times.

**K1S2816BCM**

**U<sub>t</sub>RAM**

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**PACKAGE DIMENSION**

**TBD**