

# MOS FIELD EFFECT TRANSISTORS 2SK2499, 2SK2499-Z

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### DESCRIPTION

The 2SK2499 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

#### FEATURES

- Low On-Resistance  
 $R_{DS(on)1} = 9 \text{ m}\Omega$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 25 \text{ A}$ )  
 $R_{DS(on)2} = 14 \text{ m}\Omega$  ( $V_{GS} = 4 \text{ V}$ ,  $I_D = 25 \text{ A}$ )
- Low  $C_{iss}$   $C_{iss} = 3400 \text{ pF TYP.}$
- High Avalanche Capability.
- Built-in G-S Protection Diode

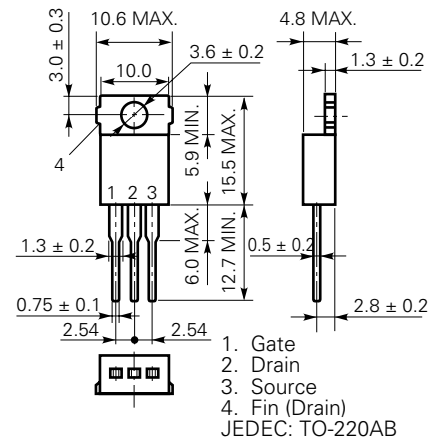
#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25 \text{ }^\circ\text{C}$ )

Drain to Source Voltage	$V_{DSS}$	60	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 50$	A
Drain Current (pulse)*	$I_{D(pulse)}$	$\pm 200$	A
Total Power Dissipation ( $T_c = 25 \text{ }^\circ\text{C}$ )	$P_{T1}$	75	W
Total Power Dissipation ( $T_A = 25 \text{ }^\circ\text{C}$ )	$P_{T2}$	1.5	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current**	$I_{AS}$	50	A
Single Avalanche Energy**	$E_{AS}$	250	mJ

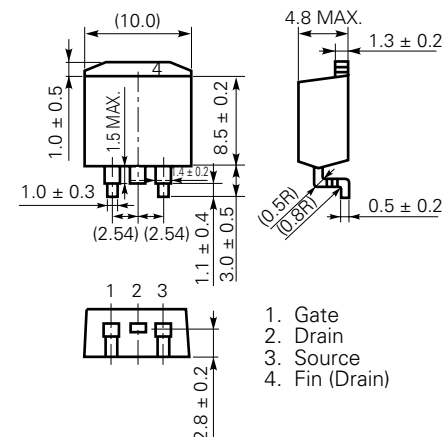
\* PW - 10  $\mu\text{s}$ , Duty Cycle - 1 %

\*\* Starting  $T_{ch} = 25 \text{ }^\circ\text{C}$ ,  $R_G = 25 \text{ }\Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0$

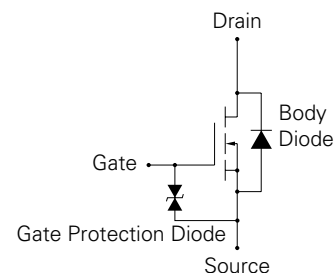
#### PACKAGE DIMENSIONS (in millimeters)



#### MP-25 (TO-220)



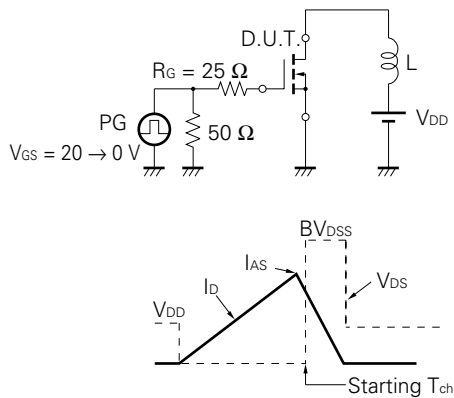
#### MP-25Z (SURFACE MOUNT TYPE)



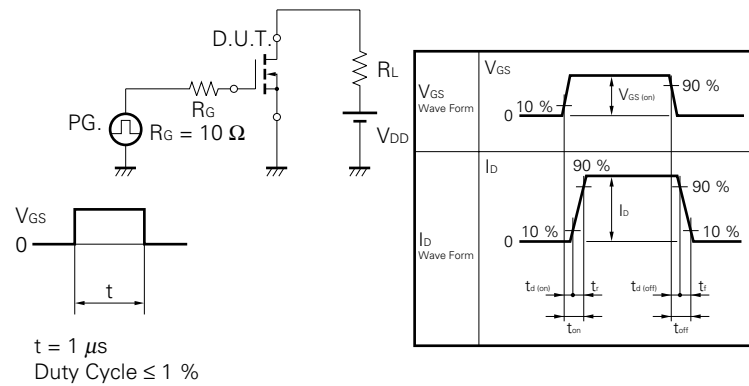
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-State Resistance	R <sub>DS(on)1</sub>		7.3	9.0	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A
	R <sub>DS(on)2</sub>		11	14	mΩ	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 25 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0	1.5	2.0	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	20	58		S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 25 A
Drain Leakage Current	I <sub>DSS</sub>			10	μA	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		3 400		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		1 600		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		770		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		55		ns	I <sub>D</sub> = 25 A
Rise Time	t <sub>r</sub>		360		ns	V <sub>GS(on)</sub> = 10 V
Turn-Off Delay Time	t <sub>d(off)</sub>		480		ns	V <sub>DD</sub> = 30 V
Fall Time	t <sub>f</sub>		360		ns	R <sub>G</sub> = 10 Ω
Total Gate Charge	Q <sub>G</sub>		152		nC	I <sub>D</sub> = 50 A
Gate to Source Charge	Q <sub>GS</sub>		11		nC	V <sub>DD</sub> = 48 V
Gate to Drain Charge	Q <sub>GD</sub>		60		nC	V <sub>GS</sub> = 10 V
Body Diode Forward Voltage	V <sub>F(S-D)</sub>		0.92		V	I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		105		ns	I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		265		nC	di/dt = 100 A/μs

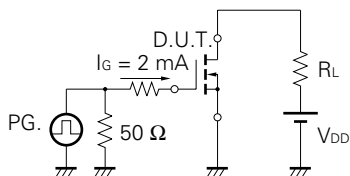
**Test Circuit 1 Avalanche Capability**



**Test Circuit 2 Switching Time**

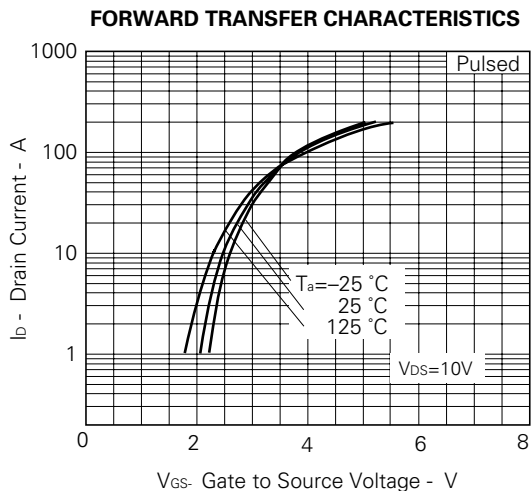
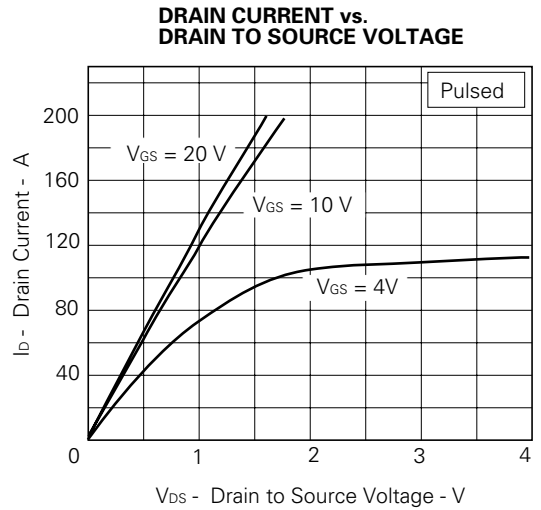
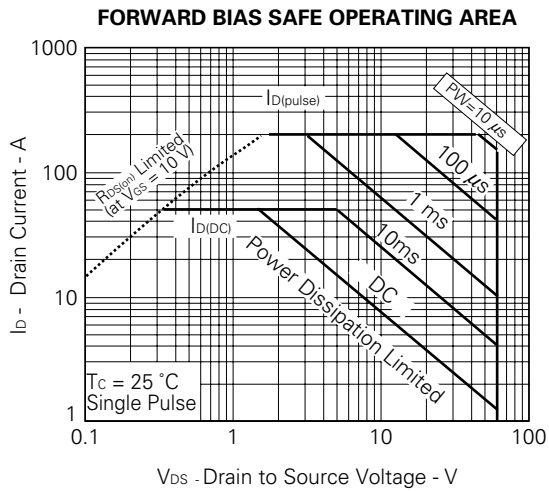
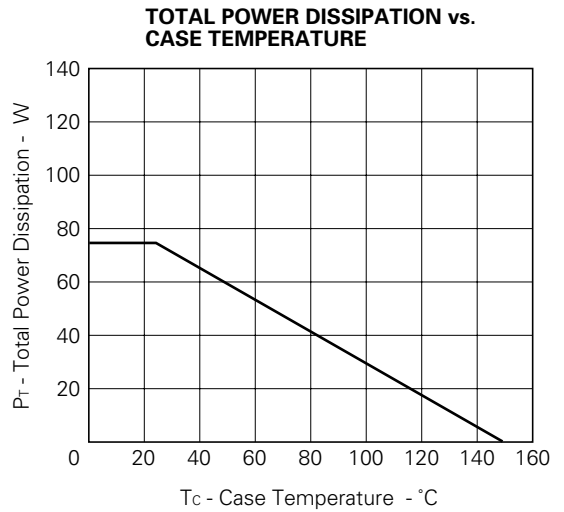
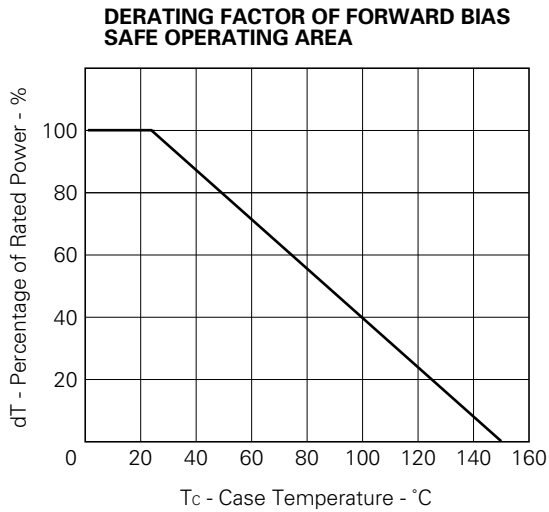


**Test Circuit 3 Gate Charge**

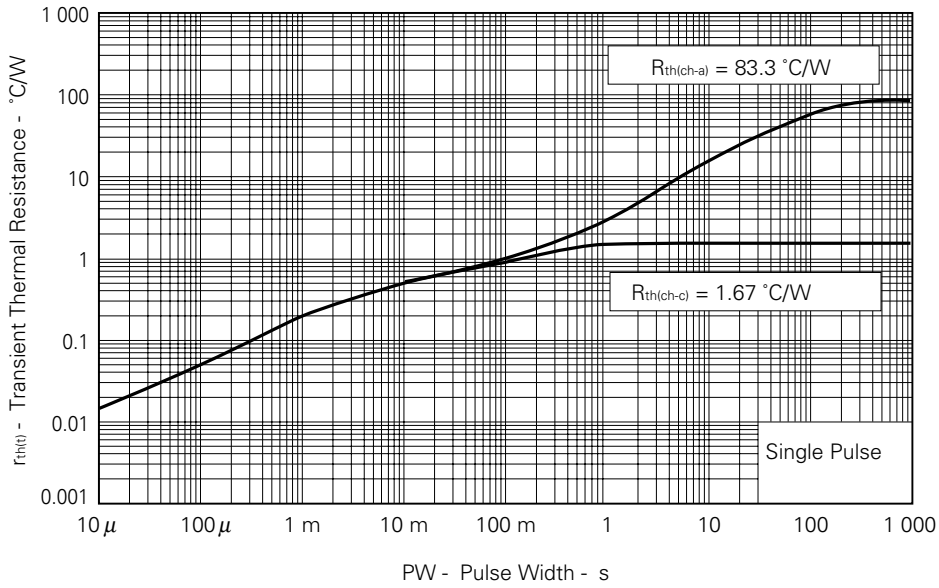


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

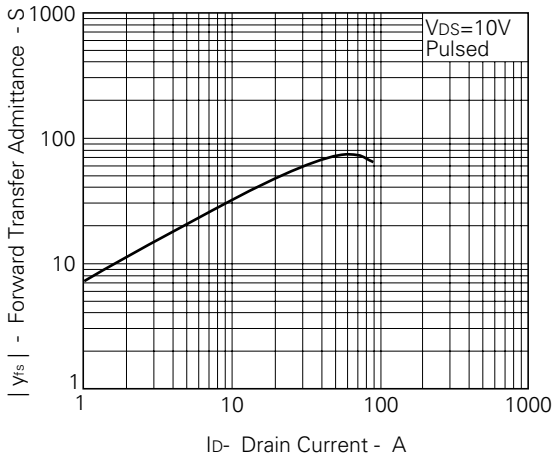
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)



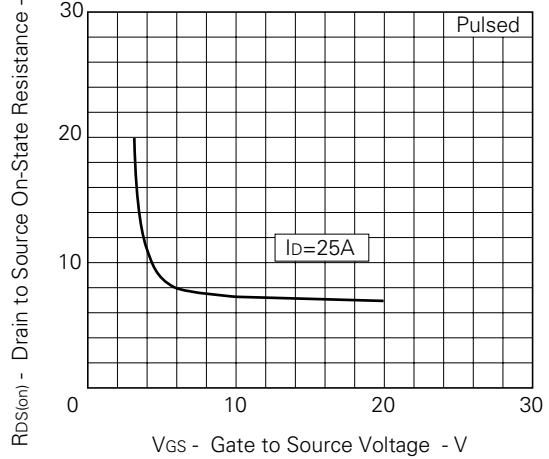
**TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH**



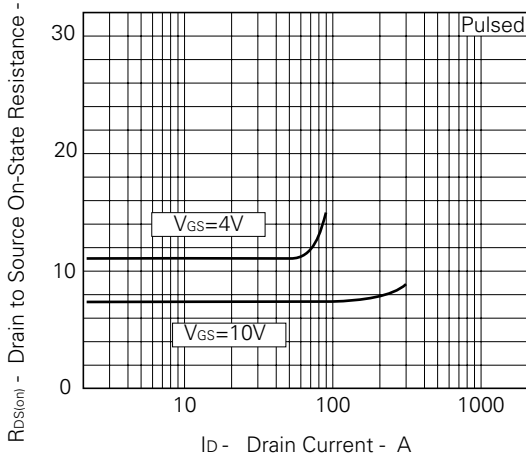
**FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT**



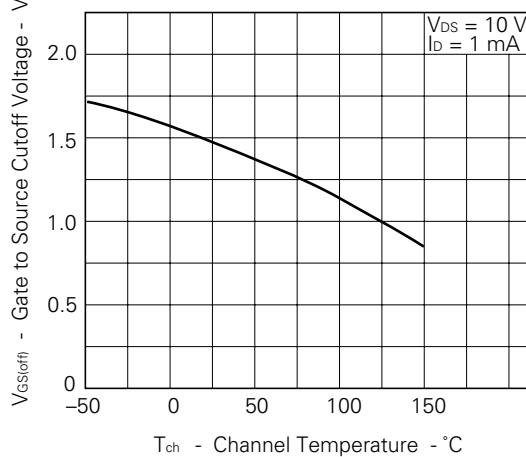
**DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE**



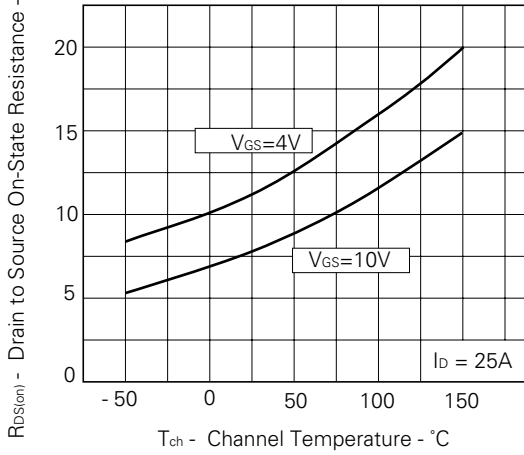
**DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT**



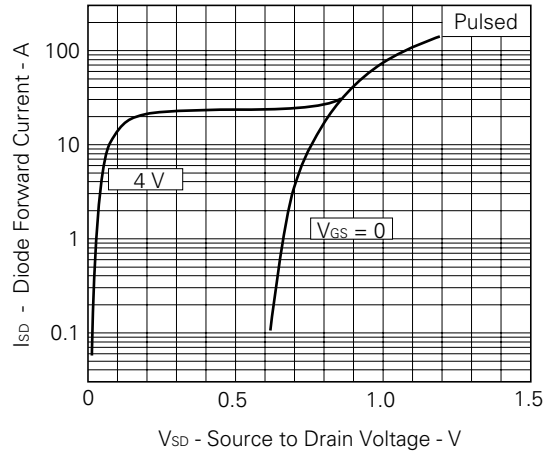
**GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE**



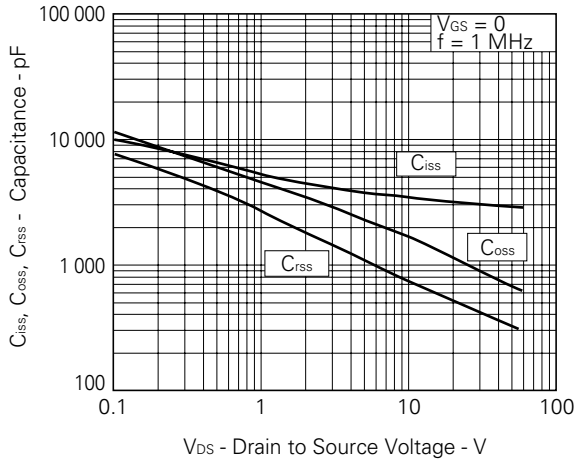
**DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE**



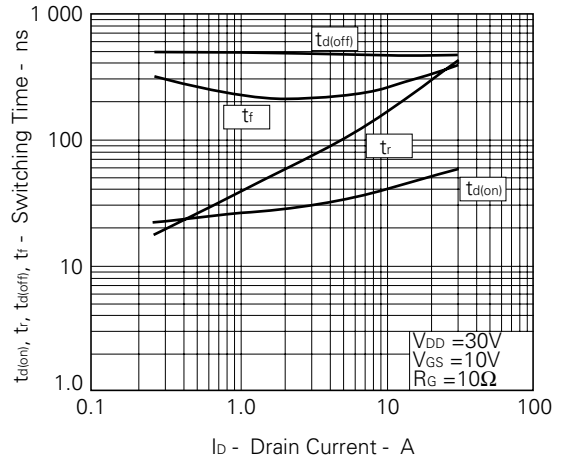
**SOURCE TO DRAIN DIODE FORWARD VOLTAGE**



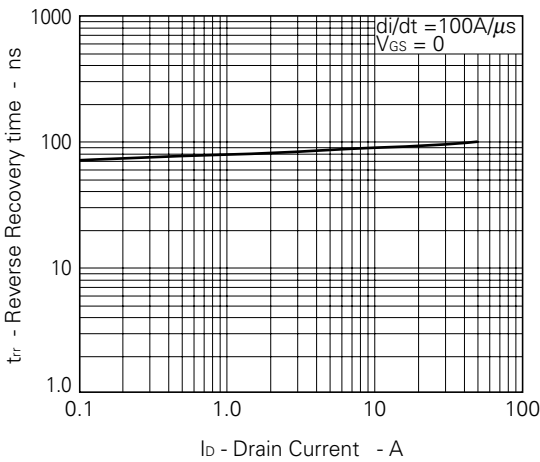
**CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE**



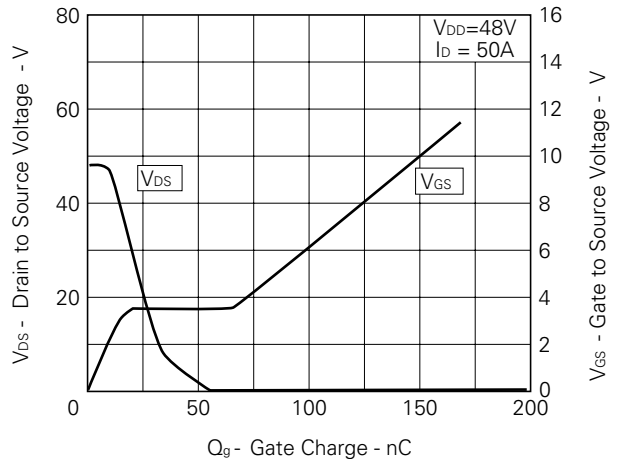
**SWITCHING CHARACTERISTICS**



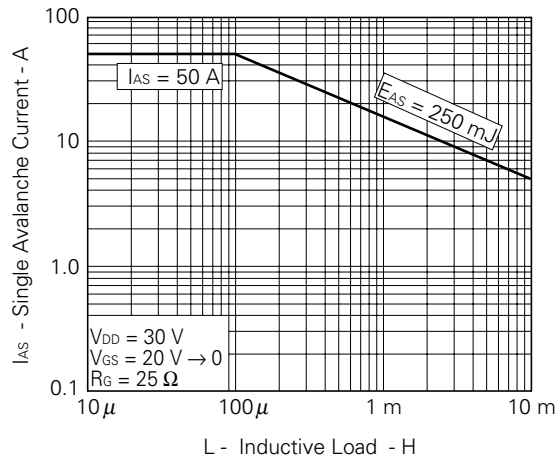
**REVERSE RECOVERY TIME vs. DRAIN CURRENT**



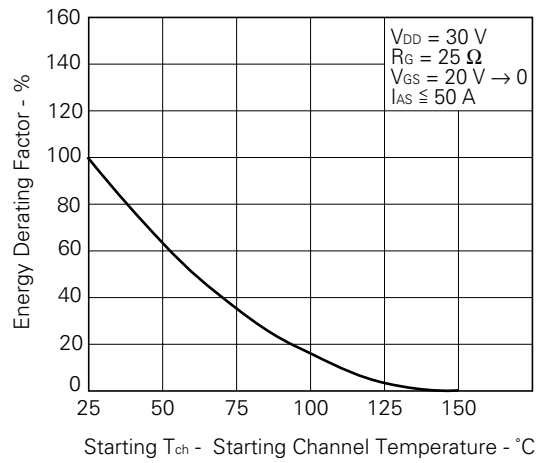
**DYNAMIC INPUT/OUTPUT CHARACTERISTICS**



**SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD**



**SINGLE AVALANCHE ENERGY DERATING FACTOR**



**REFERENCE**

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding \_\_\_\_\_ the rated voltage may be applied to this device.

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Anti-radioactive design is not implemented in this product.