Ordering number:ENN6121

N-Channel Silicon MOSFET

2SK2919

Ultrahigh-Speed Switching Applications

Features

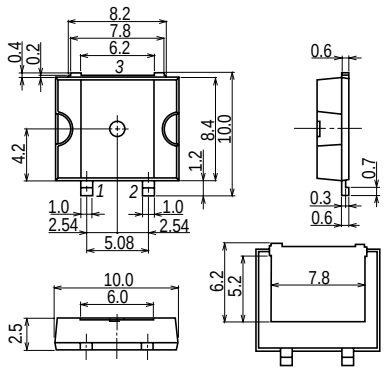
- Low ON resistance.
- Ultrahigh-speed switching.
- On-chip high-speed diode (t_{rr}=100ns).

Package Dimensions

unit:mm

2128

[2SK2919]



1 : Gate
2 : Source
3 : Drain
SANYO : ZP

Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		600	V
Gate-to-Source Voltage	V_{GSS}		±30	V
Drain Current (DC)	I_D		2	A
Drain Current (Pulse)	I_{DP}		8	A
Allowable Power Dissipation	P_D	Tc=25°C	35	W
Channel Temperature	Tch		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	600			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=480V, V_{GS}=0			1.0	mA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0			±100	nA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=1mA	2.0		3.0	V
Forward Transfer Admittance	| yfs |	V_{DS}=10V, I_D=1A	0.8	1.5		S
Static Drain-to-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=1A		3.2	4.3	Ω
Input Capacitance	Ciss	V_{DS}=20V, f=1MHz		400		pF
Output Capacitance	Coss	V_{DS}=20V, f=1MHz		55		pF
Reverse Transfer Capacitance	Crss	V_{DS}=20V, f=1MHz		15		pF

Note) Be careful in handling the 2SK2919 because it has no protection diode between Gate-to-Source.

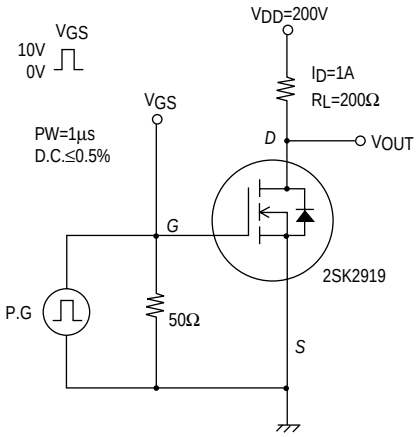
Continued on next page.

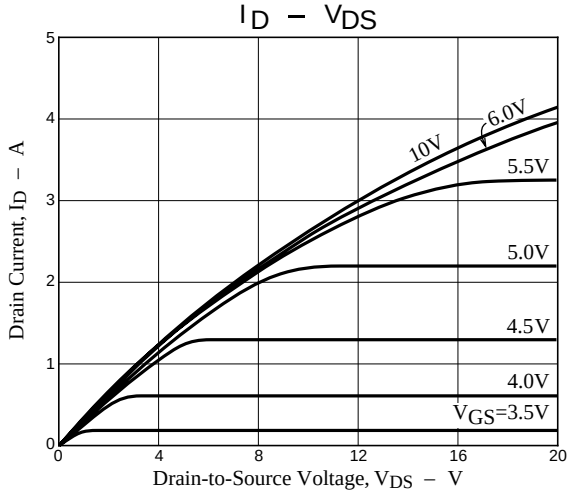
SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

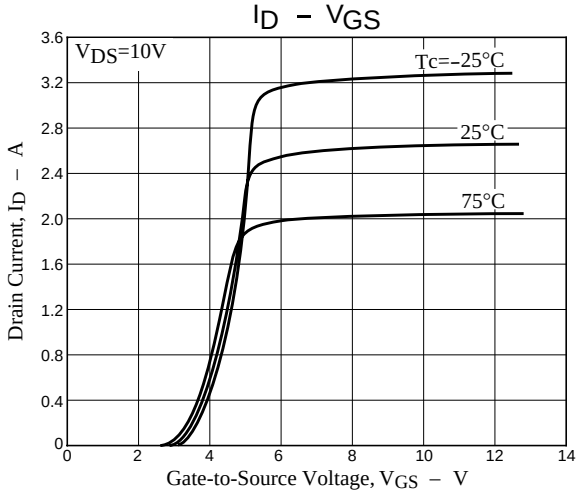
Continued from preceding page.

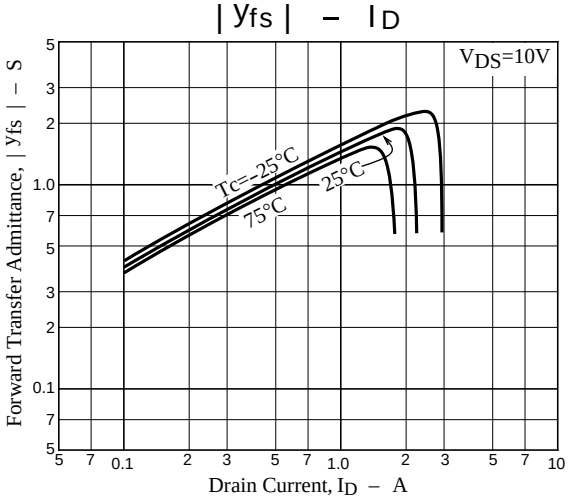
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit		10		ns
Rise Time	t_r	See specified Test Circuit		12		ns
Turn-OFF Delay Time	$t_{d(off)}$	See specified Test Circuit		65		ns
Fall Time	t_f	See specified Test Circuit		40		ns
Diode Forward Voltage	V_{SD}	I_S=2A, V_{GS}=0			1.5	V
Diode Reverse recovery time	t_{rr}	IS=2A, di/dt=100Aμs		100		ns

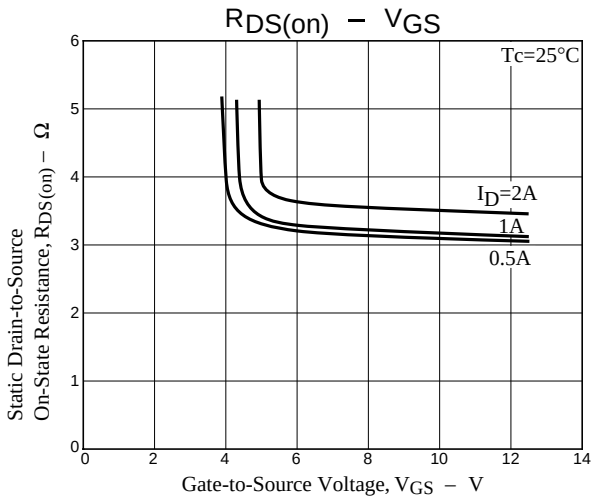
Switching Time Test Circuit



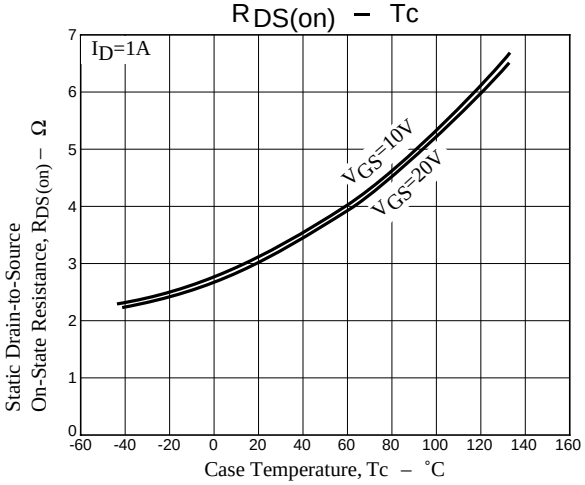




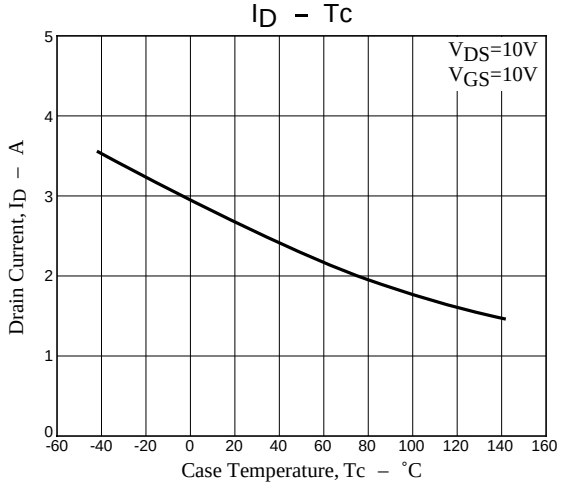




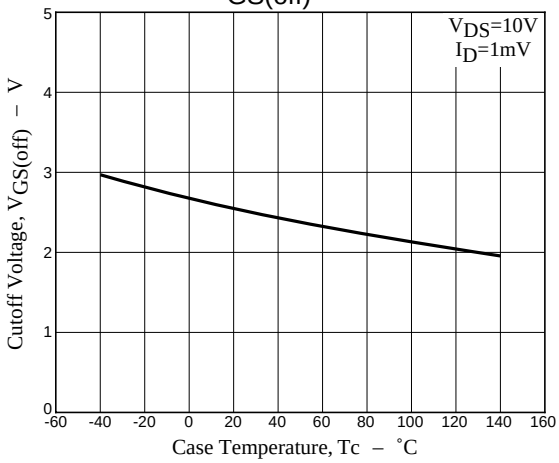
$R_{DS(on)}$ – Tc



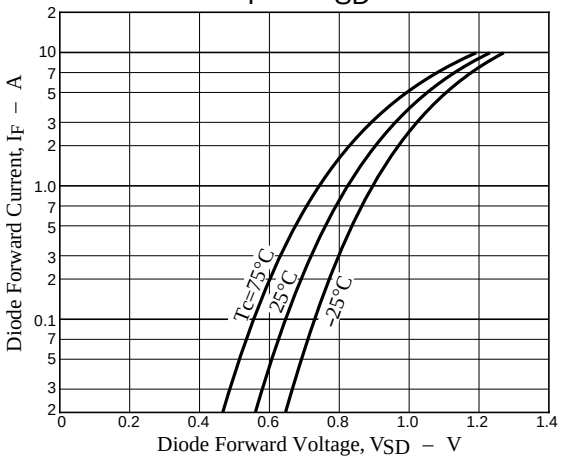
I_D – Tc



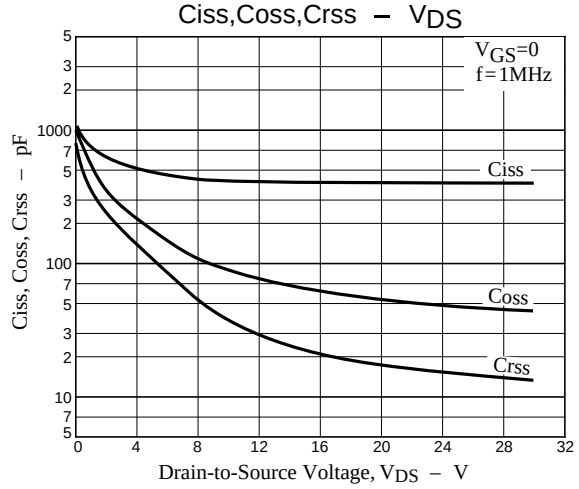
$V_{GS(off)}$ – Tc



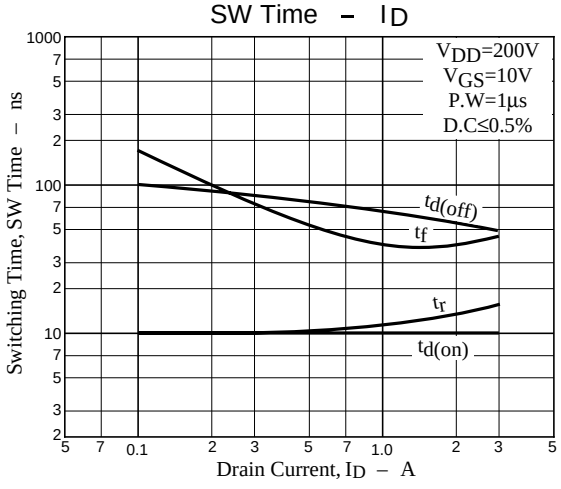
I_F – V_{SD}



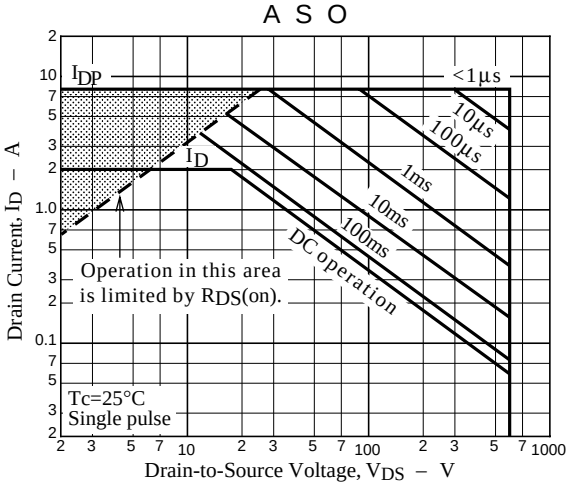
Ciss,Coss,Crss – V_{DS}



SW Time – I_D



A S O



P_D – Tc