TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π−MOSV)

2SK2993

Chopper Regulator, DC−DC Converter and Motor Drive Applications

Unit: mm

- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 82 mΩ (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 20 S (typ.)
- Low leakage current : I_{DSS} = 100 μA (max) (V_{DS} = 250 V)
- Enhancement−mode : V_{th} = 1.5~3.5 V (V_{DS} = 10 V, I_D = 1 mA)

Maximum Ratings (Ta = 25°C)

Characteristics S		ymbol	Rating	Unit
Drain−source voltage		V_{DSS}	250	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	250	V
Gate−source voltage		V_{GSS} ±	20	V
Drain current	DC (Not e 1)	I_D	20	A
	Pulse (Note 1)	I_{DP}	60	
Drain power dissipation (Tc = 25°C)		P_D 100		W
Single pulse avalanche energy (Not e 2)		E_{AS} 423		mJ
Avalanche current		I_{AR}	20	A
Repetitive avalanche energy (Note 3)		E_{AR} 10		mJ
Channel temperature		T_{ch} 150		°C
Storage temperature range		T_{stg}	−55~150 °	C

Thermal Characteristics

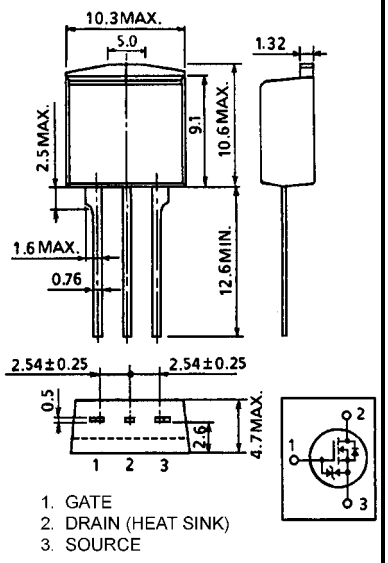
Characteristics S	ymbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$ 1.	25	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$ 83.	3	°C / W

Note 1: Please u se d evices o n co ndition t hat t he channel te mperature is below 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 1.79 mH, I_{AR} = 20 A, R_G = 25 Ω

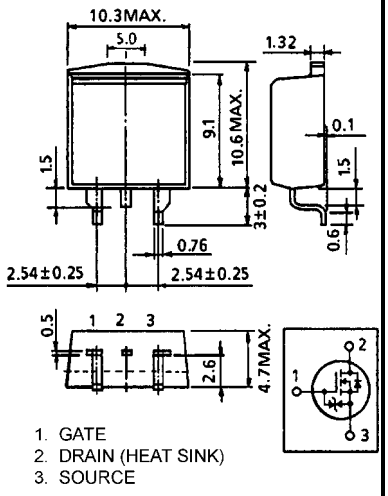
Note 3: Repetitive rating; Pulse width limited by maximum channel temperature.

This transistor is an electrostatic sensitive device.
Please handle with caution.



JEDEC	—
JEITA	—
TOSHIBA	2-10S1B

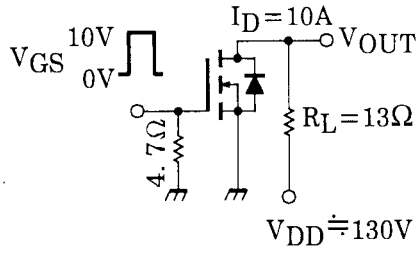
Weight: 1.5 g (typ.)



JEDEC	—
JEITA	—
TOSHIBA	2-10S2B

Weight: 1.5 g (typ.)

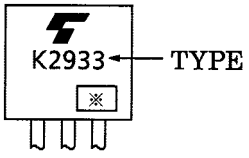
Electrical Characteristics (Ta = 25°C)

Characteristics S		ymbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut−off current		I_{DSS}	V_{DS} = 250 V, V_{GS} = 0 V	—	—	100	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	250	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	1.5	—	3.5	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 10 A	—	82	105	mΩ
Forward transfer admittance		$\|Y_{fs}\|$ V	$_{DS}$ = 10 V, I_D = 10 A	10	20	—	S
Input capacitance		C_{iss} —	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		4000	—	pF
Reverse transfer capacitance		C_{rss}		—	300	—	
Output capacitance		C_{oss}		— 1000		—	
Switching time	Rise time	t_r —			15	—	ns
	Turn−on time	t_{on}		—	35	—	
	Fall time	t_f		—	30	—	
	Turn−off time	t_{off}		— 180		—	
Total gate charge (gate−source plus gate−drain)		Q_g	V_{DD} ≈ 200 V, V_{GS} = 10 V, I_D = 20 A	— 100		—	nC
Gate−source charge		Q_{gs}		—	70	—	
Gate−drain (“miller”) Charge		Q_{gd}		— 30		—	

Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristics S	ymbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Not e 1)	I_{DR} —		—	—	20	A
Pulse drain reverse current (Not e 1)	I_{DRP} —		—	—	60	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 20 A, V_{GS} = 0 V	—	—	−2.0	V
Reverse recovery time	t_{rr}	I_{DR} = 20 A, V_{GS} = 0 V dI_{DR} / dt = 100 A / μs	—	300	—	ns
Reverse recovery charge	Q_{rr}		— 3.	3 —		μC

Marking

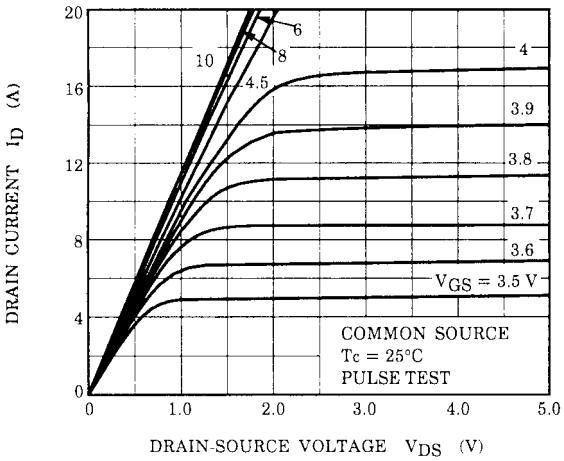


※ Lot Number

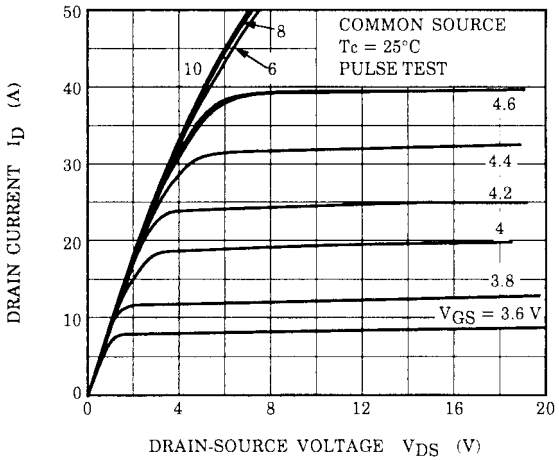
□ □ — Month (Starting from Alphabet A)

Year (Last Number of the Christian Era)

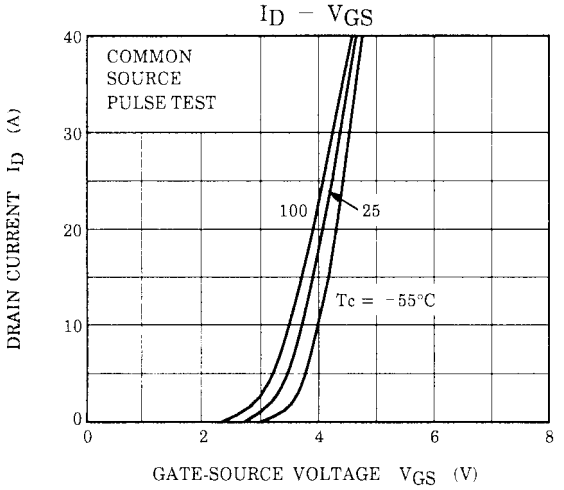
I_D – V_{DS}



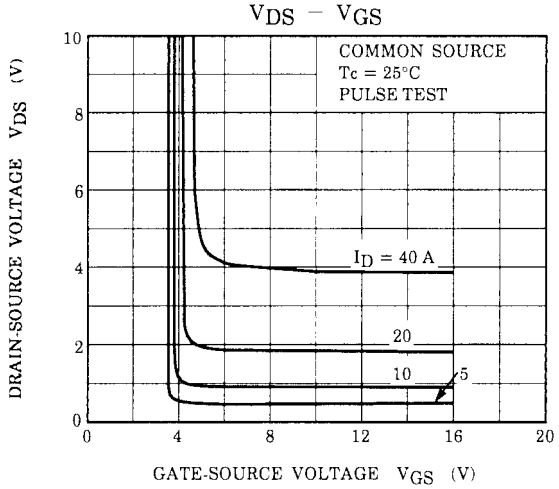
I_D – V_{DS}



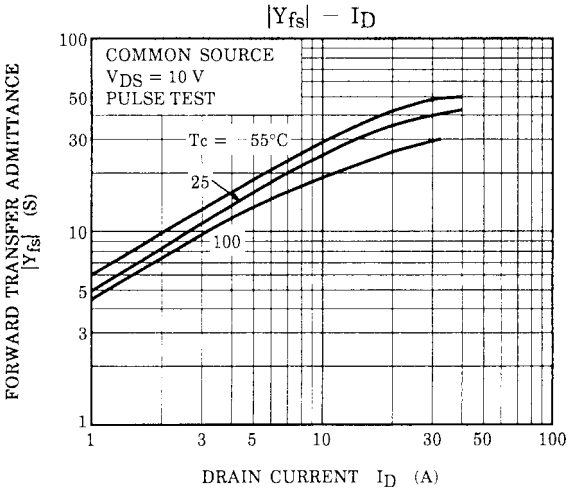
I_D – V_{GS}



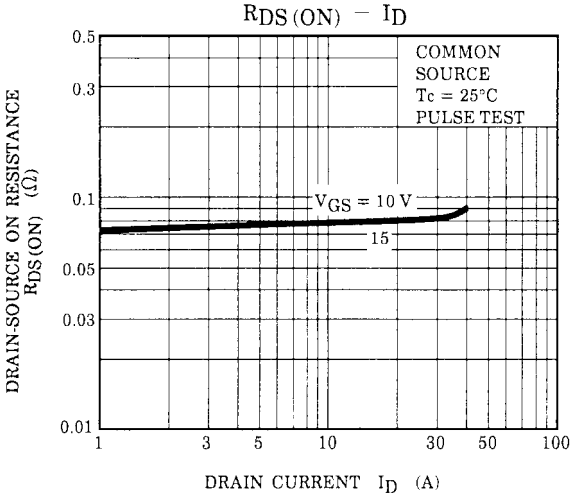
V_{DS} – V_{GS}



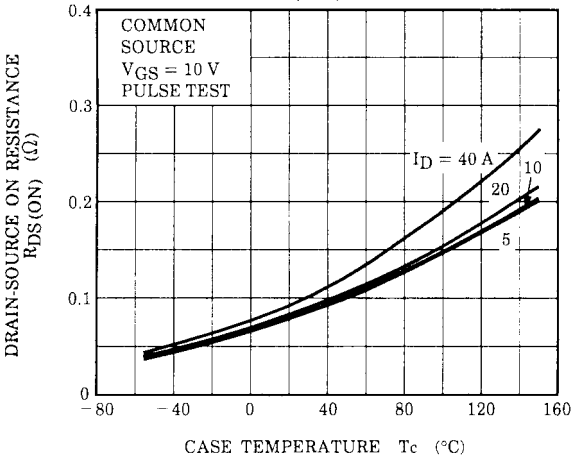
$|Y_{fs}|$ – I_D



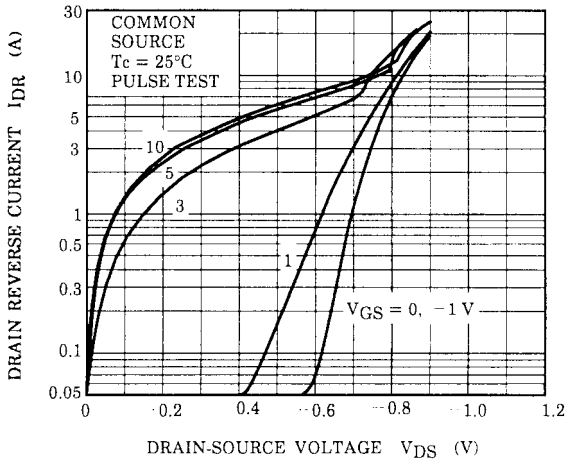
$R_{DS\,(ON)}$ – I_D



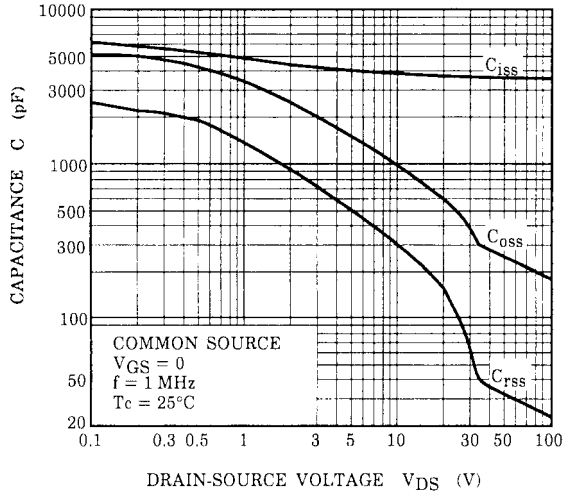
$R_{DS\,(ON)}$ – Tc



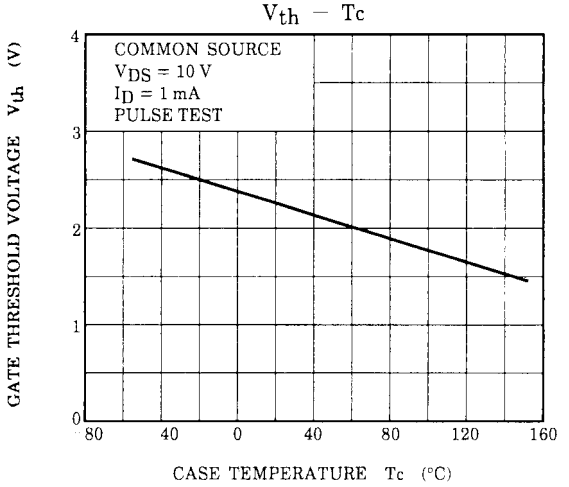
I_{DR} – V_{DS}



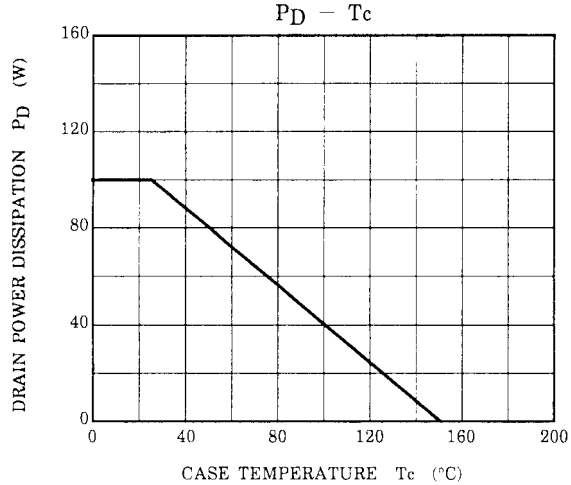
CAPACITANCE – V_{DS}



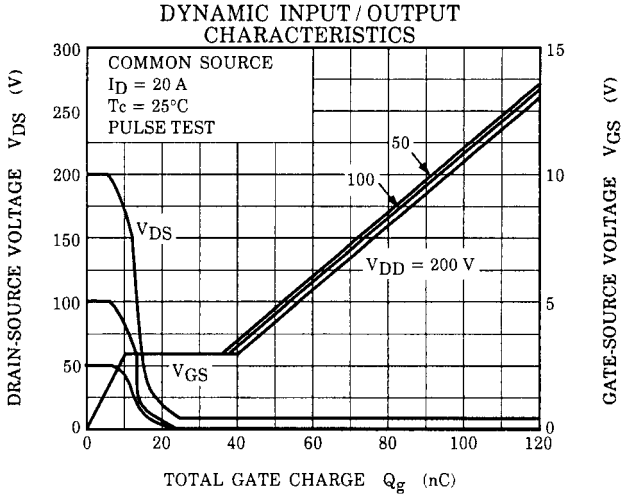
V_{th} – Tc



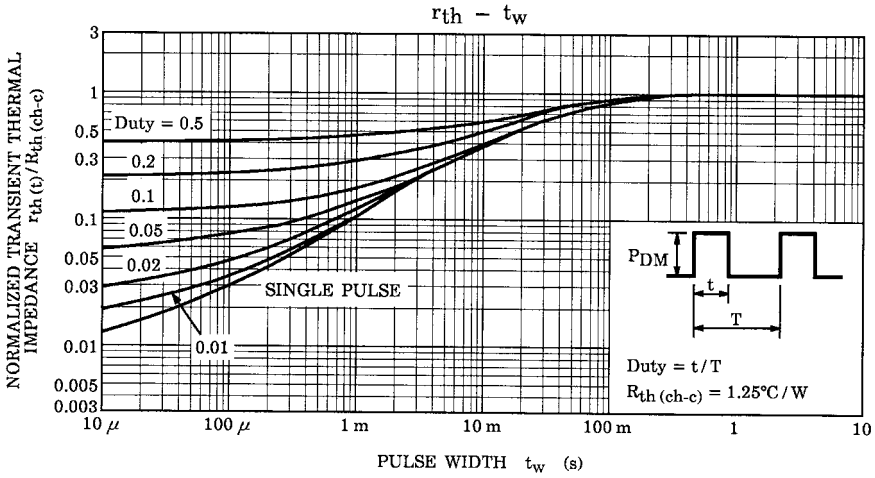
P_D – Tc



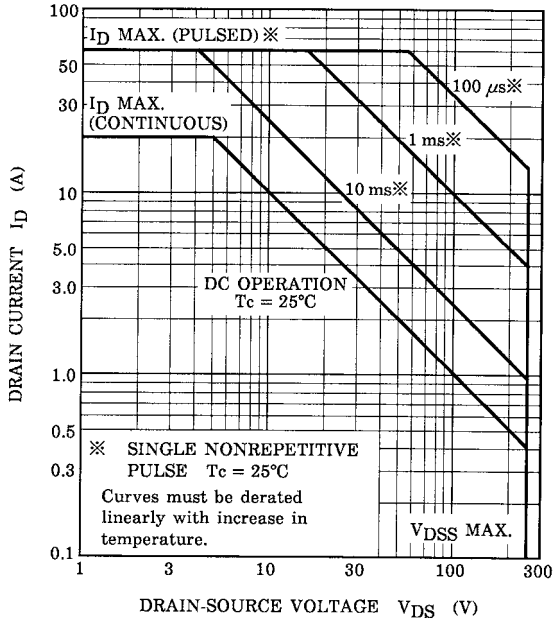
DYNAMIC INPUT / OUTPUT CHARACTERISTICS



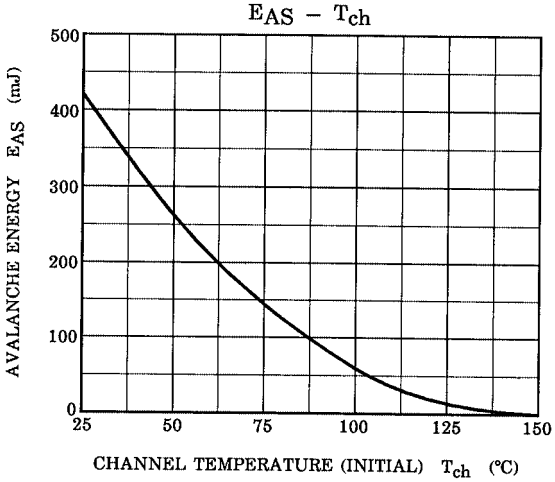
r_{th} – t_w

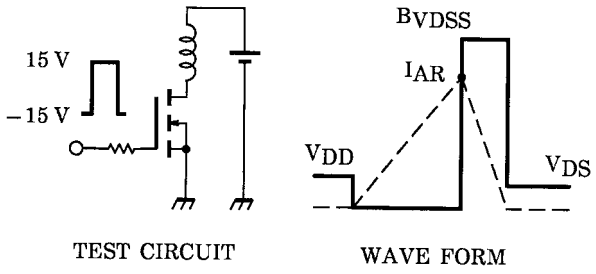


SAFE OPERATING AREA



E_{AS} – T_{ch}





TEST CIRCUIT WAVE FORM

R_G = 25 Ω
V_{DD} = 90 V, L = 1.79 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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