2SK3192

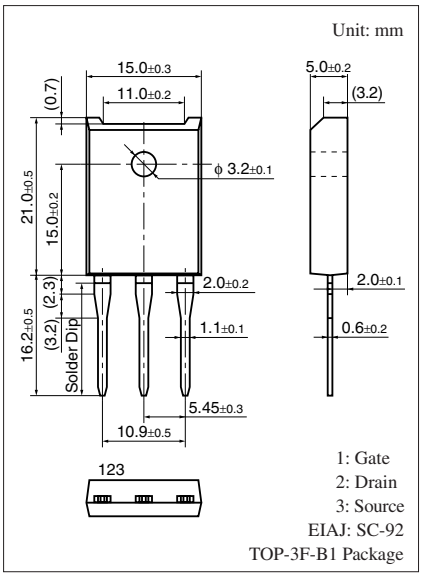
Silicon N-channel power MOSFET

■ Features

- Avalanche energy capability guaranteed
- High-speed switching
- Low ON resistance R_{on}
- No secondary breakdown

■ Applications

- PDP
- Switching mode regulator



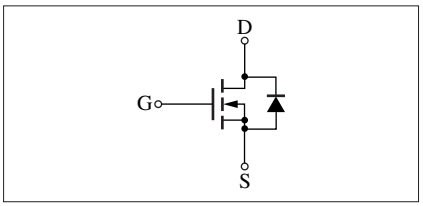
Marking Symbol: K3192

■ Absolute Maximum Ratings $T_C = 25°C$

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	V_{DSS}	250	V
Gate-source surrender voltage	V_{GSS}	±30	V
Drain current	I_D	±30	A
Peak drain current	I_{DP}	±120	A
Avalanche energy capability *	EAS	925	mJ
Power dissipation	P_D	100	W
$T_a = 25°C$		3	
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	−55 to +150	°C

Note) *: L = 1.74 mH, I_L = 30 A, V_{DD} = 50 V, 1 pulse, T_a = 25°C

Internal Connection



■ Electrical Characteristics $T_C = 25°C \pm 3°C$

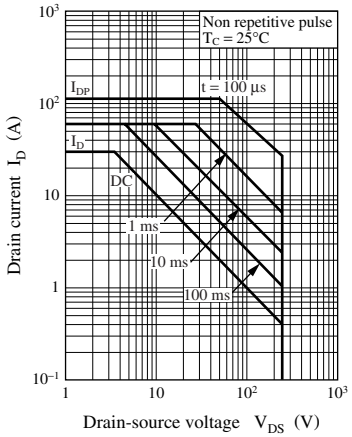
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	I_D = 1 mA, V_{GS} = 0	250			V
Drain-source cutoff current	I_{DSS}	V_{DS} = 200 V, V_{GS} =			0 0	μA
Gate-source cutoff current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0			±1	μA
Gate threshold voltage	V_{th}	V_{DS} = 10 V, I_D = 1 mA	2		4	V
Drain-source ON resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A		50	68	mΩ
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 15 A	8	15		S
Short-circuit forward transfer capacitance (Common source)	C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz		4 200		pF
Short-circuit output capacitance (Common source)	C_{oss}			1 600		pF
Reverse transfer capacitance (Common source)	C_{rss}			650		pF
Turn-on delay time	$t_{d(on)}$	V_{DD} = 100 V, I_D = 15 A, R_L = 6.7 Ω		45		ns
Rise time	t_r	V_{GS} = 10 V		115		ns
Turn-off delay time	$t_{d(off)}$			330		ns
Fall time	t_f			130		ns

■ Electrical Characteristics (continued) $T_C = 25°C \pm 3°C$

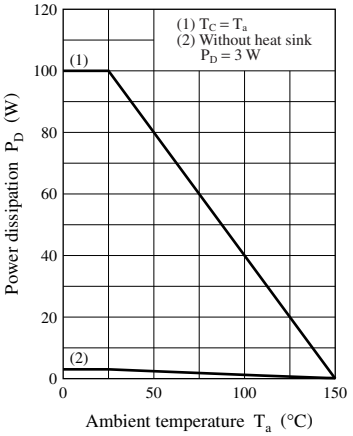
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Diode forward voltage	V_{DSF}	I_{DR} = 30 A, V_{GS} = 0			−1.5	V
Reverse recovery time	t_{rr}	L = 230 µH, V_{DD} = 100 V		260		ns
Reverse recovery charge	Q_{rr}	I_{DR} = 15 A, di/dt = 100 A/µs		1.6		µC
Gate charge load	Q_g	V_{DD} = 100 V, I_D = 15 A		95		nC
Gate-source charge	Q_{gs}	V_{GS} = 10 V		34		nC
Gate-drain charge	Q_{gd}			12		nC
Thermal resistance (ch-c)	$R_{th(ch-c)}$				1.25	°C/W
Thermal resistance (ch-a)	$R_{th(ch-a)}$				41.7	°C/W

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

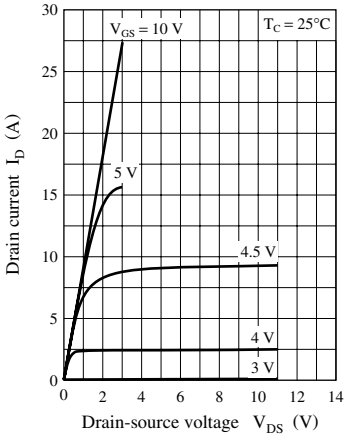
Safe operation area



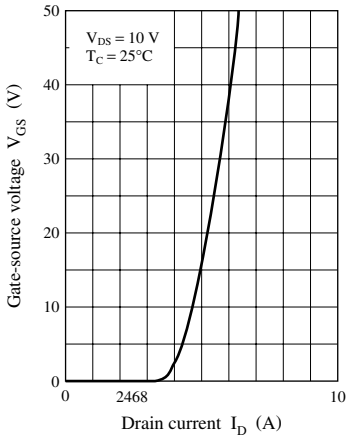
P_D — T_a



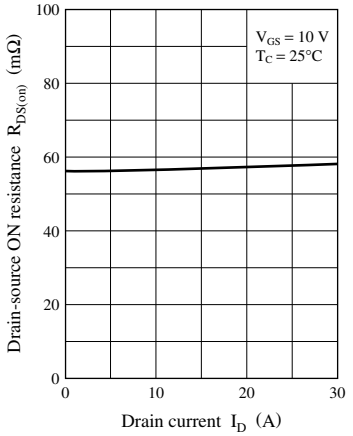
I_D — V_{DS}



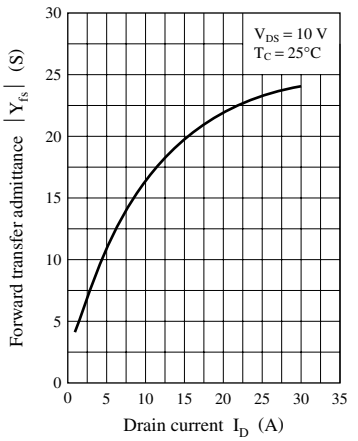
V_{GS} — I_D



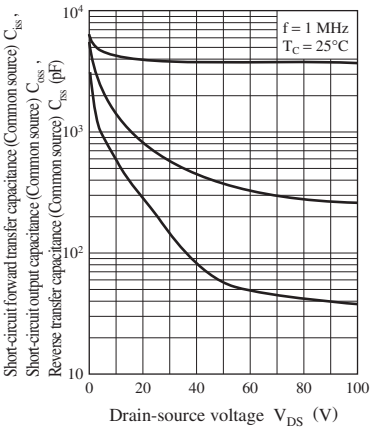
$R_{DS(on)}$ — I_D



$|Y_{fs}|$ — I_D



C_{iss} , C_{oss} , C_{rss} — V_{DS}



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