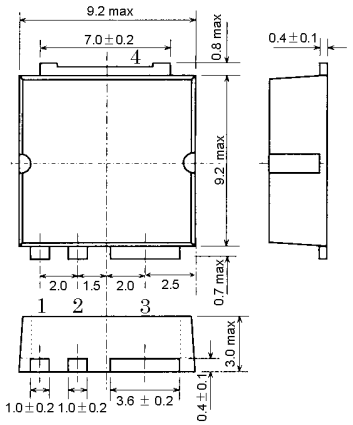
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSII)

2SK3442

Switching Regulator, DC-DC Converter and Motor Drive Applications

- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 15 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 28 S (typ.)
- Low leakage current: I_{DSS} = 100 μA (V_{DS} = 100 V)
- Enhancement mode: V_{th} = 2.0~4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



1. GATE : G
2. SOURCE 1 : S1
3. SOURCE 2 : S2
4. DRAIN : D

JEDEC	—
JEITA	SC-97
TOSHIBA	2-9F1B

Weight: 0.74 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	100	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	100	V
Gate-source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I_D	45	A
	Pulse (Note 1)	I_{DP}	180	
Drain power dissipation (Tc = 25°C)		P_D	125	W
Single pulse avalanche energy (Note 2)		E_{AS}	468	mJ
Avalanche current		I_{AR}	45	A
Repetitive avalanche energy (Note 3)		E_{AR}	12.5	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	1.00	°C/W

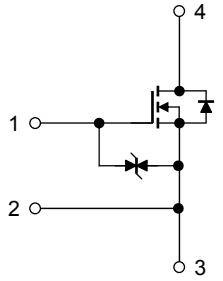
Notice:
Please use the S1 pin for gate input signal return. Make sure that the main current flows into the S2 pin.

Note 1: Ensure that the channel temperature does not exceed 150°C.

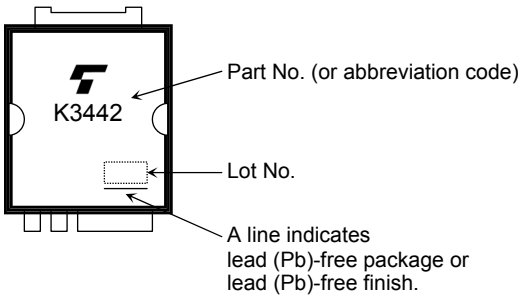
Note 2 V_{DD} = 25 V, T_{ch} = 25°C (initial), L = 373 μH, R_G = 25 Ω, I_{AR} = 45 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

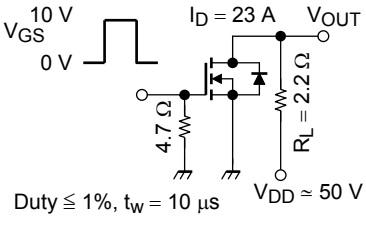
This transistor is an electrostatic-sensitive device. Please handle with caution.



Marking



Electrical Characteristics (Note 4) (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±25 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-off current		I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	100	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 23 A	—	15	20	mΩ
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 23 A	14	28	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	4100	—	pF
Reverse transfer capacitance		C_{rss}		—	340	—	
Output capacitance		C_{oss}		—	980	—	
Switching time	Rise time	t_r		—	15	—	ns
	Turn-on time	t_{on}		—	45	—	
	Fall time	t_f		—	20	—	
	Turn-off time	t_{off}		—	95	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ 80 V, V_{GS} = 10 V, I_D = 45 A	—	85	—	nC
Gate-source charge		Q_{gs}		—	50	—	
Gate-drain (“miller”) charge		Q_{gd}		—	35	—	

Note 4: Connect the S1 and S2 pins together, and ground them except during switching time measurement.

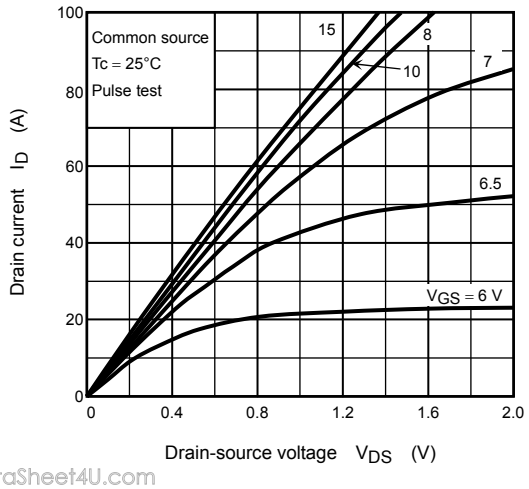
Source-Drain Ratings and Characteristics (Note 5) (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1, Note 5)	$I_{DR}1$	—	—	—	45	A
Pulse drain reverse current (Note 1, Note 5)	$I_{DRP}1$	—	—	—	180	A
Continuous drain reverse current (Note 1, Note 5)	$I_{DR}2$	—	—	—	1	A
Pulse drain reverse current (Note 1, Note 5)	$I_{DRP}2$	—	—	—	4	A
Forward voltage (diode)	V_{DS2F}	I_{DR} = 45 A, V_{GS} = 0 V	—	—	−1.5	V
Reverse recovery time	t_{rr}	I_{DR} = 45 A, V_{GS} = 0 V, dI_{DR}/dt = 50 A/μs	—	160	—	ns
Reverse recovery charge	Q_{rr}		—	512	—	nC

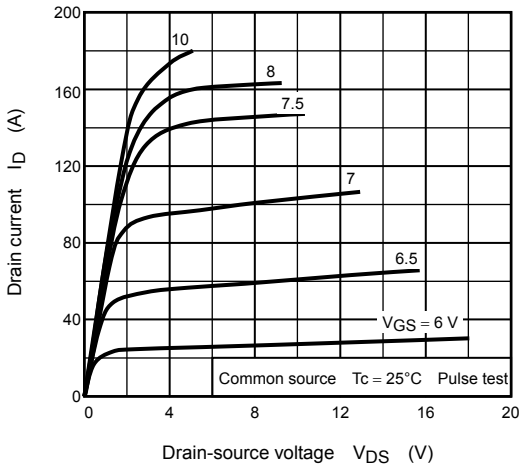
Note 5: $I_{DR}1$, $I_{DRP}1$: Current flowing between the drain and the S2 pin. Ensure that the S1 pin is left open.
$I_{DR}2$, $I_{DRP}2$: Current flowing between the drain and the S1 pin. Ensure that the S2 pin is left open.

Unless otherwise specified, connect the S1 and S2 pins together, and ground them.

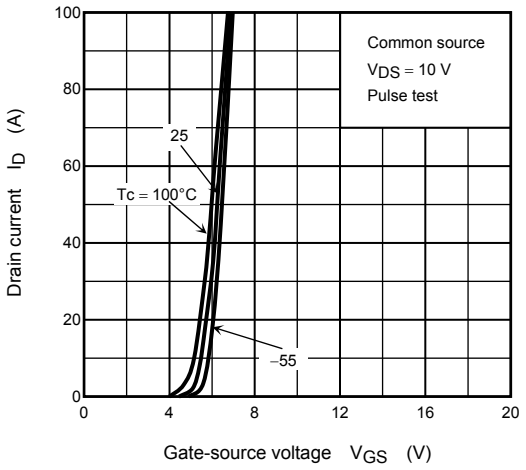
$I_D - V_{DS}$



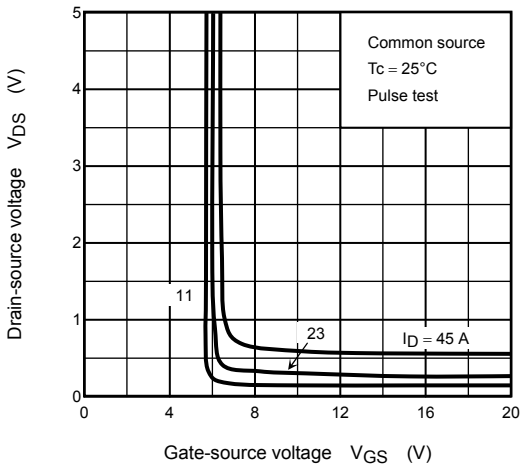
$I_D - V_{DS}$



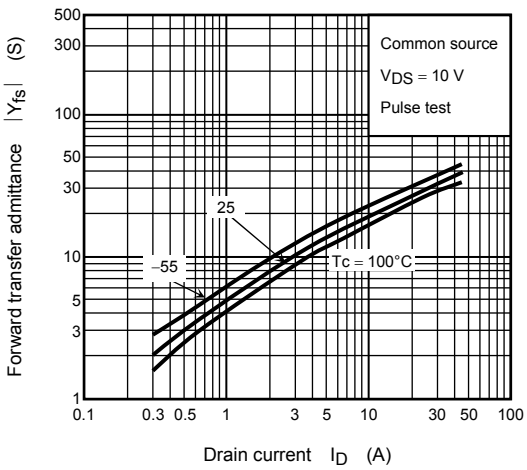
$I_D - V_{GS}$



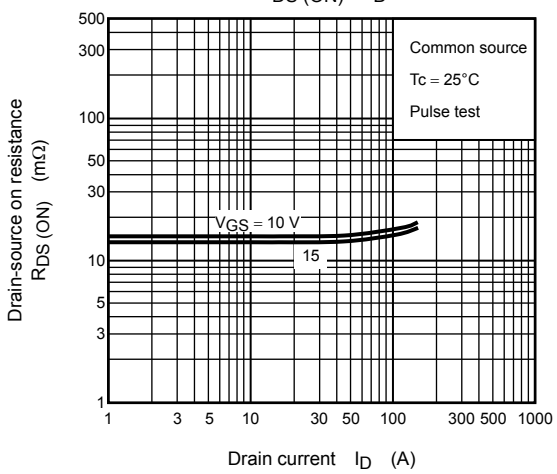
$V_{DS} - V_{GS}$



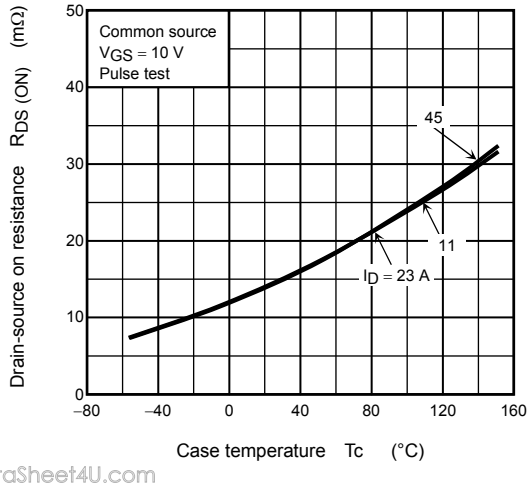
$|Y_{fs}| - I_D$



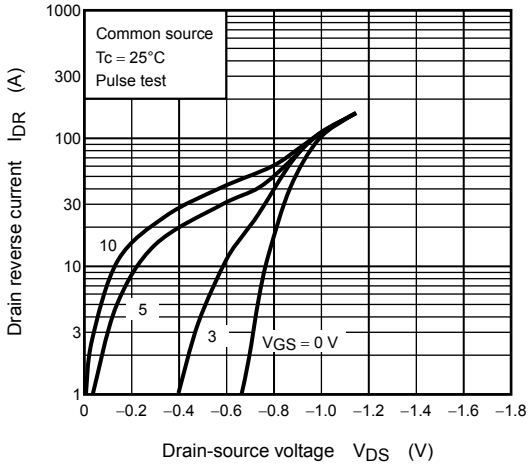
$R_{DS\ (ON)} - I_D$



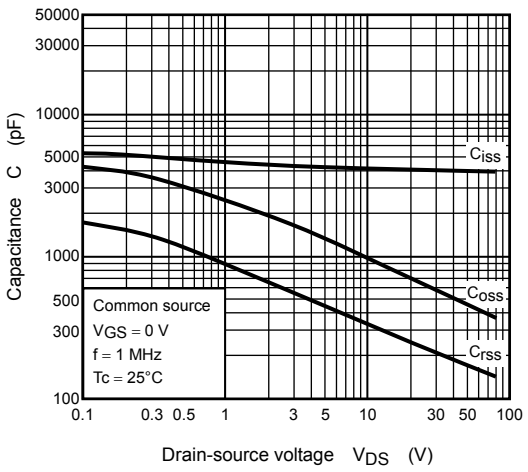
$R_{DS\ (ON)}$ – Tc



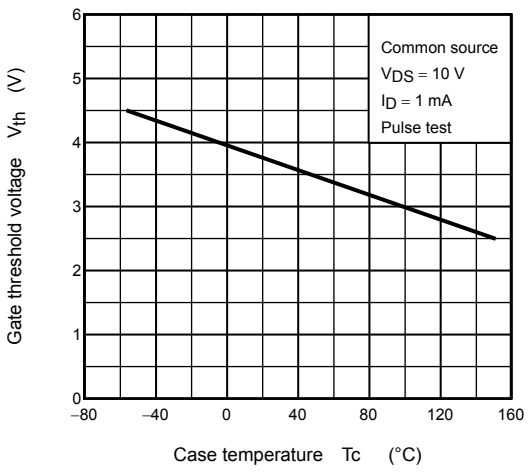
I_{DR} – V_{DS}



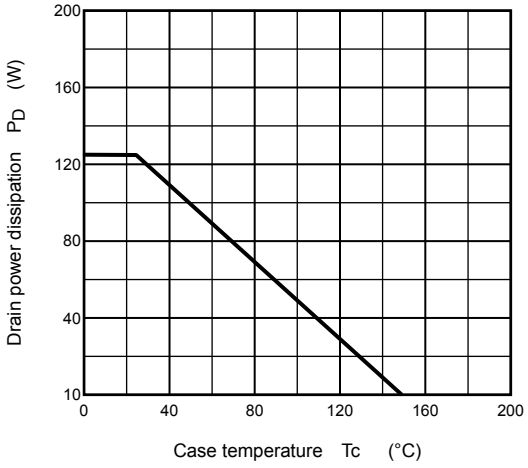
Capacitance – V_{DS}



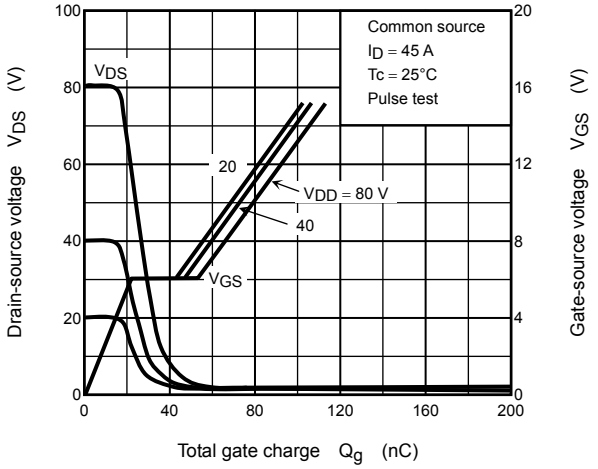
V_{th} – Tc



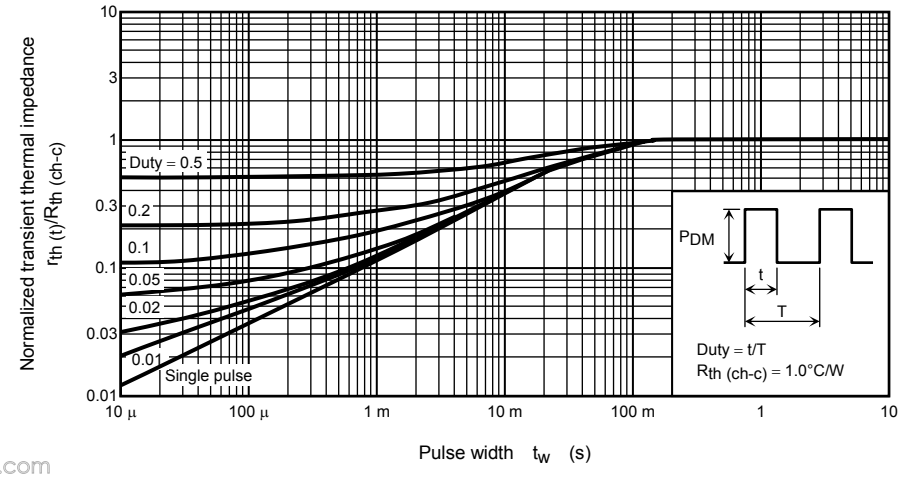
P_D – Tc



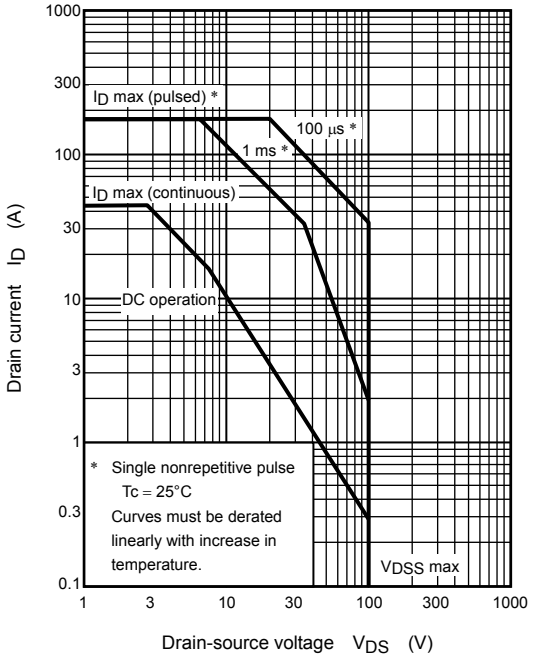
Dynamic input/output characteristics



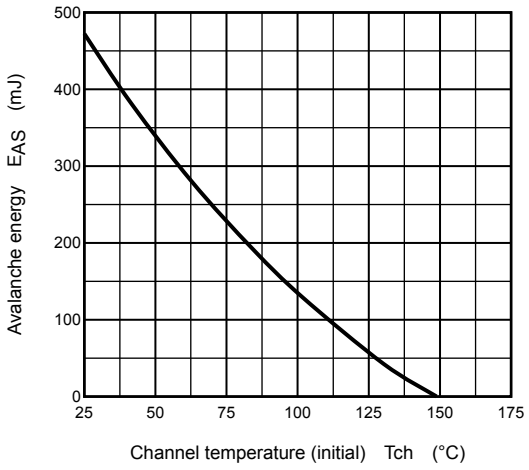
$r_{th} - t_w$

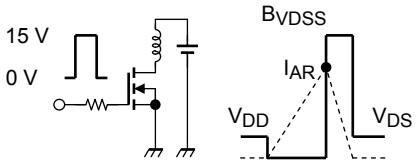


Safe operating area



$E_{AS} - T_{ch}$





Test circuit Wave form

$R_G = 25\ \Omega$
$V_{DD} = 25$ V, L = 373 μH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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20070701-EN

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