DATA SHEET

NEC

# MOS FIELD EFFECT TRANSISTOR
# 2SK3467

## SWITCHING
## N-CHANNEL POWER MOS FET
## INDUSTRIAL USE

### DESCRIPTION

The 2SK3467 is N-Channel MOS FET device that features a low on-state resistance and excellent switching characteristics, designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

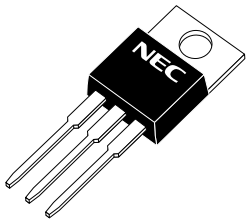
### ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---|---|
| 2SK3467 | TO-220AB |
| 2SK3467-ZK | TO-263(MP-25ZK) |

### FEATURES

- 4.5 V drive available
- Low on-state resistance
  $R_{DS(on)1}$ = 6.0 mΩ MAX. ($V_{GS}$ = 10 V, $I_D$ = 40 A)
- Low gate charge
  $Q_G$ = 55 nC TYP. ($I_D$ = 80 A, $V_{DD}$ = 16 V, $V_{GS}$ = 10 V)
- Built-in gate protection diode
- Surface mount device available

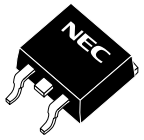
(TO-220AB)




### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C)

| | | | |
|---|---|---|---|
| Drain to Source Voltage ($V_{GS}$ = 0 V) | $V_{DSS}$ | 20 | V |
| Gate to Source Voltage ($V_{DS}$ = 0 V) | $V_{GSS}$ | ±20 | V |
| Drain Current (DC) ($T_C$ = 25°C) | $I_{D(DC)}$ | ±80 | A |
| Drain Current (Pulse) **Note** | $I_{D(pulse)}$ | ±320 | A |
| Total Power Dissipation ($T_A$ = 25°C) | $P_{T1}$ | 1.5 | W |
| Total Power Dissipation ($T_C$ = 25°C) | $P_{T2}$ | 76 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +150 | °C |

(TO-263)




**Note** PW ≤ 10 μs, Duty Cycle ≤ 1%



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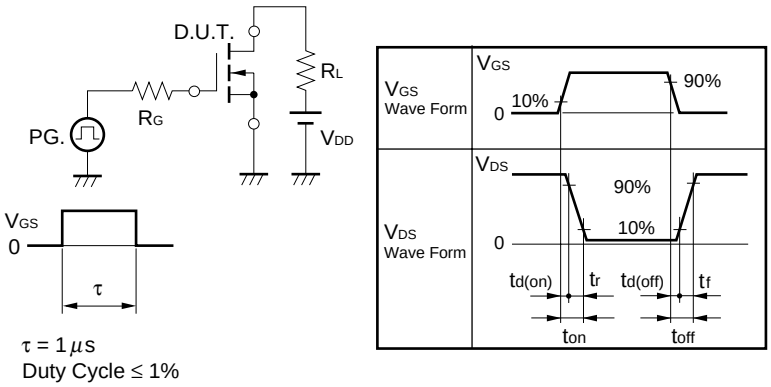
## ELECTRICAL CHARACTERISTICS($T_A$ = 25°C)

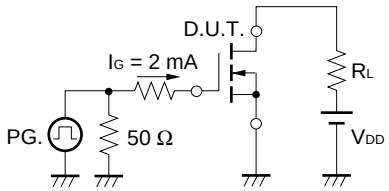
| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Zero Gate voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | | | 10 | μA |
| Gate Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| Gate Cut-off Voltage | $V_{GS(off)}$ | $V_{DS}$ = 10 V, $I_D$ = 1 mA | 1.5 | | 2.5 | V |
| Forward Transfer Admittance | $\|y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 40 A | 20 | | | S |
| Drain to Source On-state Resistance | $R_{DS(on)1}$ | $V_{GS}$ = 10 V, $I_D$ = 40 A | | 4.8 | 6.0 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = 4.5 V, $I_D$ = 40 A | | 6.7 | 9.5 | mΩ |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V | | 2800 | | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | | 1200 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 600 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$ = 10 V , $I_D$ = 40 A | | 16 | | ns |
| Rise Time | $t_r$ | $V_{GS(on)}$ = 10 V | | 23 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $R_G$ = 10 Ω | | 74 | | ns |
| Fall Time | $t_f$ | | | 31 | | ns |
| Total Gate Charge | $Q_G$ | $V_{DD}$ = 16 V | | 55 | | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{GS}$ = 10 V | | 9 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $I_D$ = 80 A | | 17 | | nC |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | $I_F$ = 80 A, $V_{GS}$ = 0 V | | 1.0 | | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 80 A, $V_{GS}$ = 0 V | | 44 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 100 A/μs | | 40 | | nC |

### TEST CIRCUIT 1 SWITCHING TIME



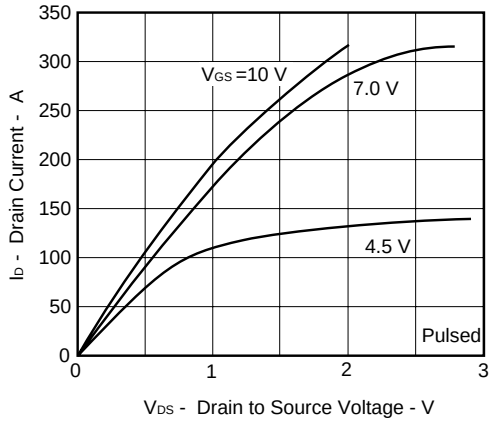

τ = 1 μs
Duty Cycle ≤ 1%

### TEST CIRCUIT 2 GATE CHARGE

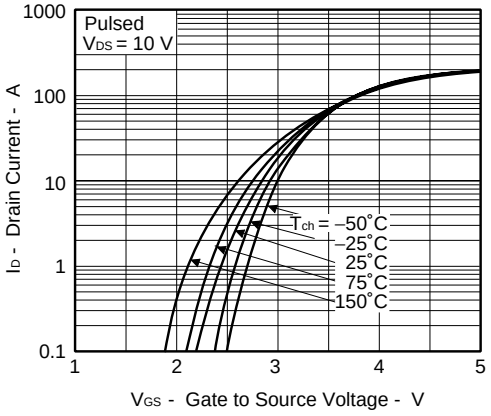


## TYPICAL CHARACTERISTICS ($T_A$ = 25°C)

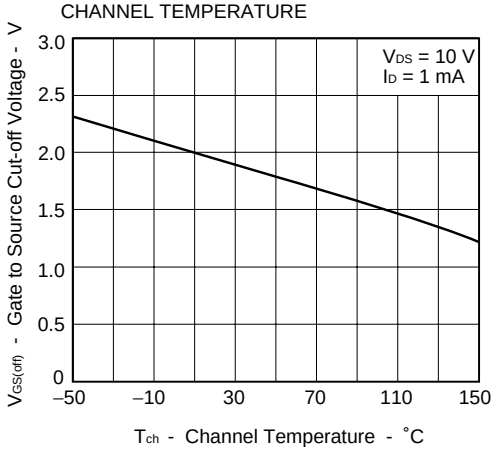
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



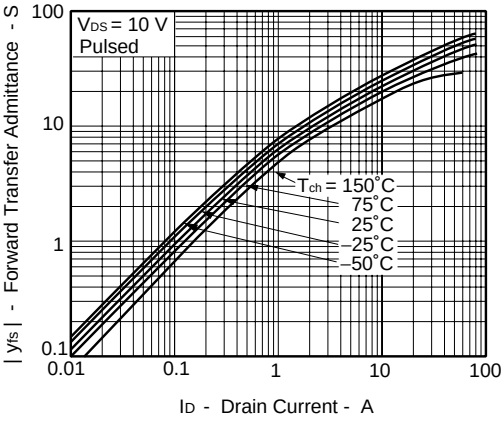

FORWARD TRANSFER CHARACTERISTICS



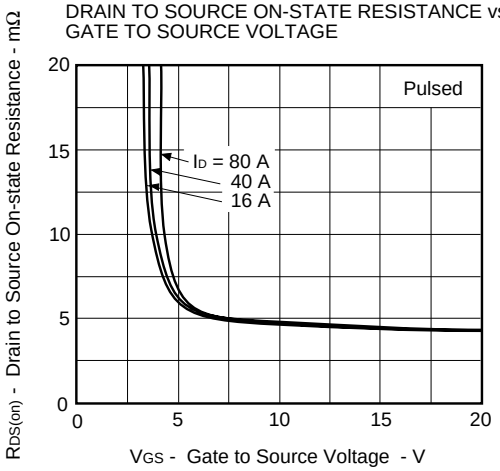

GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



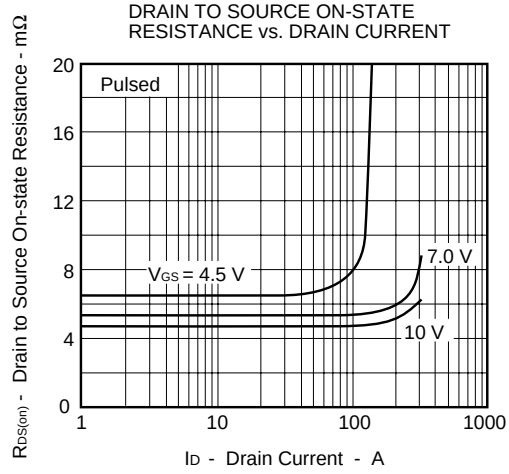

FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



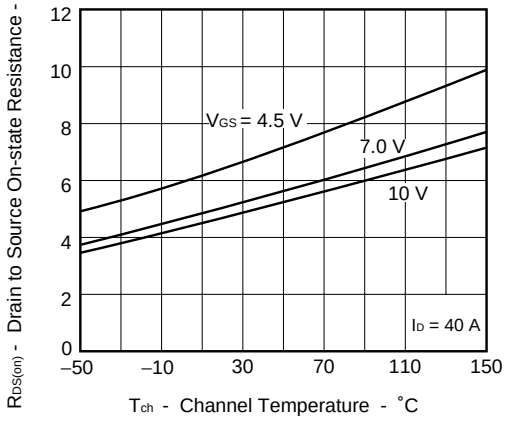

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



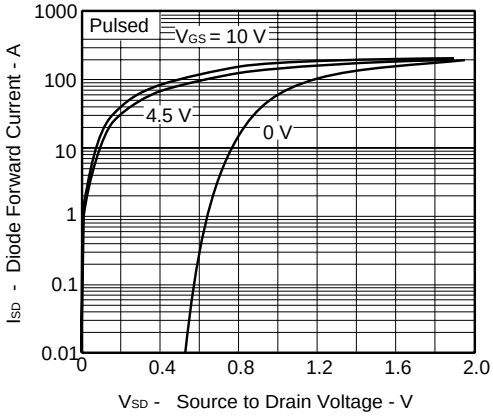

DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



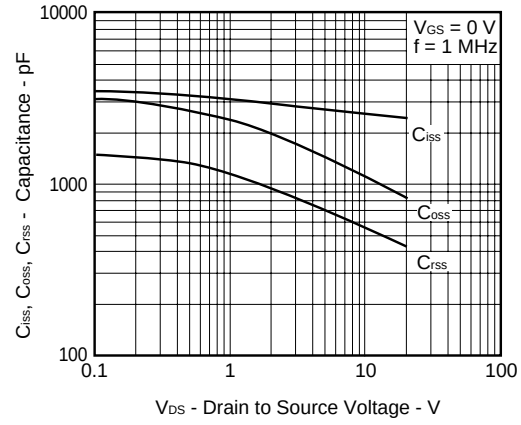
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



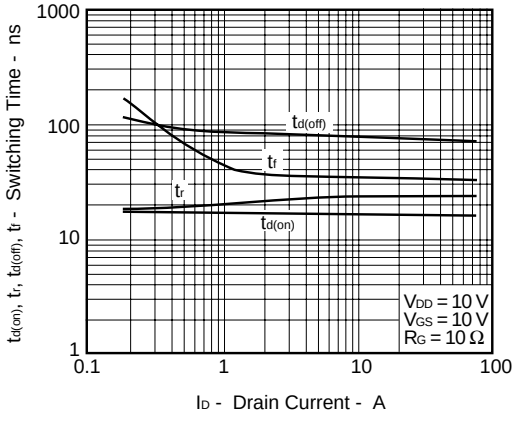

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



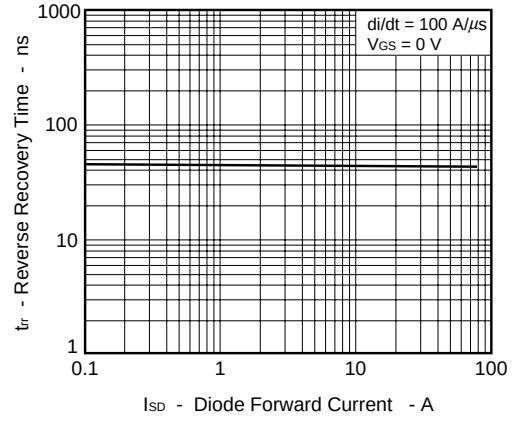

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



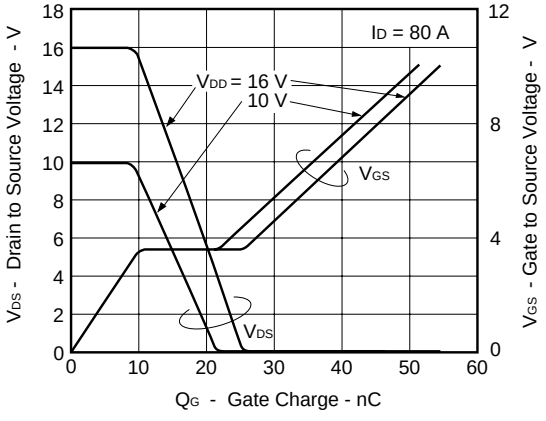

SWITCHING CHARACTERISTICS



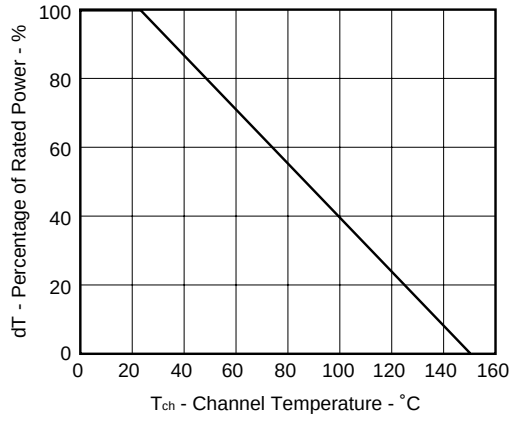

REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



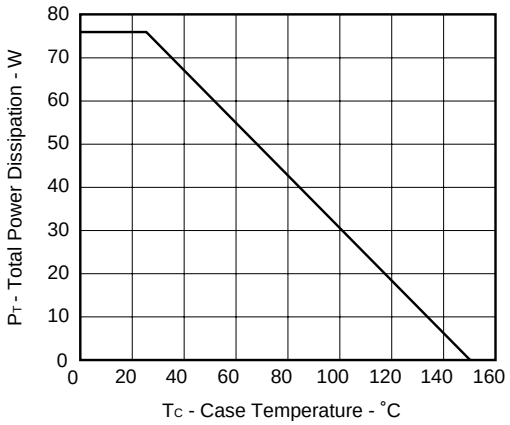

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



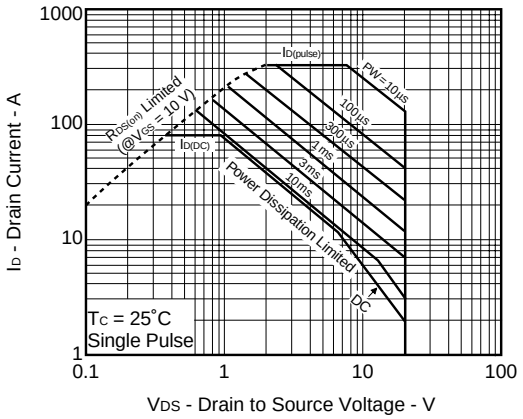
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



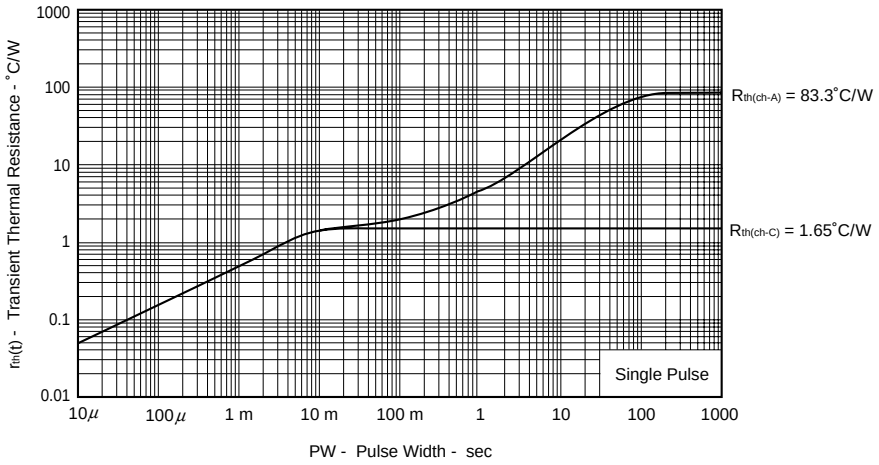

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE




FORWARD BIAS SAFE OPERATING AREA

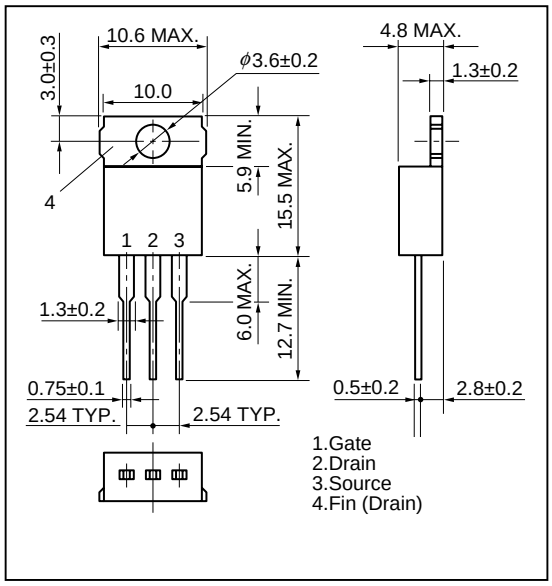



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

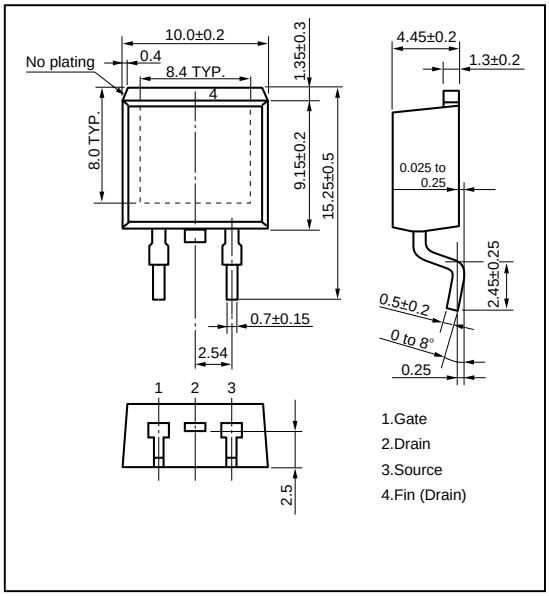


**PACKAGE DRAWINGS (Unit : mm)**

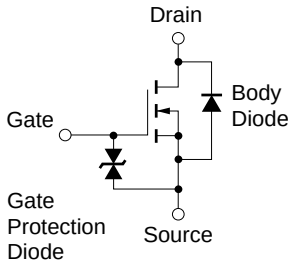
**1)TO-220AB (MP-25)**




**2)TO-263 (MP-25ZK)**




**EQUIVALENT CIRCUIT**




**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

**[MEMO]**

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