

## SWITCHING N-CHANNEL POWER MOS FET

**DESCRIPTION**

The 2SK3511 is N-channel MOS Field Effect Transistor designed for high current switching applications.

**FEATURES**

- Super low on-state resistance:  
 $R_{DS(on)} = 12.5 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 42 \text{ A}$ )
- Low  $C_{iss}$ :  $C_{iss} = 5900 \text{ pF TYP.}$
- Built-in gate protection diode

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)**

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	75	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 83$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 260$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_T$	100	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_T$	1.5	W
Channel Temperature	$T_{ch}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C
Single Avalanche Current <sup>Note2</sup>	$I_{AS}$	52	A
Single Avalanche Energy <sup>Note2</sup>	$E_{AS}$	250	mJ

**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1\%$

**2.** Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 35 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$

**THERMAL RESISTANCE**

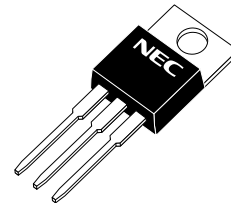
Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.25	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

**ORDERING INFORMATION**

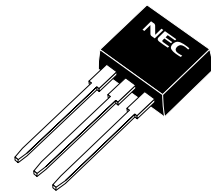
PART NUMBER	PACKAGE
2SK3511	TO-220AB
2SK3511-S	TO-262
2SK3511-ZJ	TO-263
2SK3511-Z	TO-220SMD <sup>Note</sup>

**Note** TO-220SMD package is produced only in Japan.

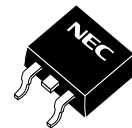
(TO-220AB)



(TO-262)



(TO-263, TO-220SMD)

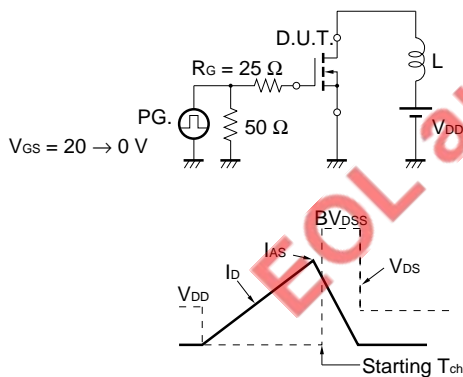


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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

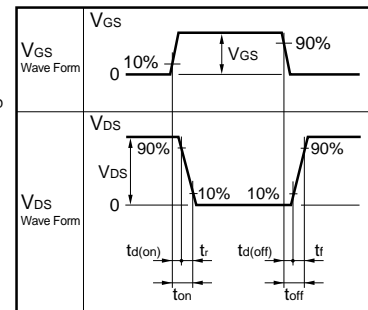
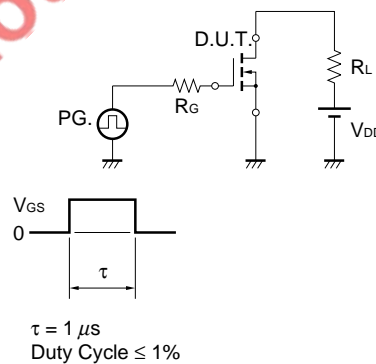
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	2.0	3.0	4.0	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 42 A	21	45		S
Drain to Source On-state Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 42 A		9.5	12.5	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		5900		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		810		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		400		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 38 V, I <sub>D</sub> = 42 A		30		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V		21		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		72		ns
Fall Time	t <sub>f</sub>			12		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 60 V		100		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V		24		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 83 A		35		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 83 A, V <sub>GS</sub> = 0 V		1.1		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 83 A, V <sub>GS</sub> = 0 V		70		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		200		nC

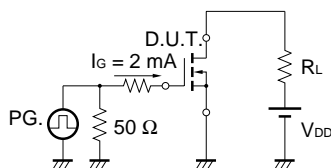
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

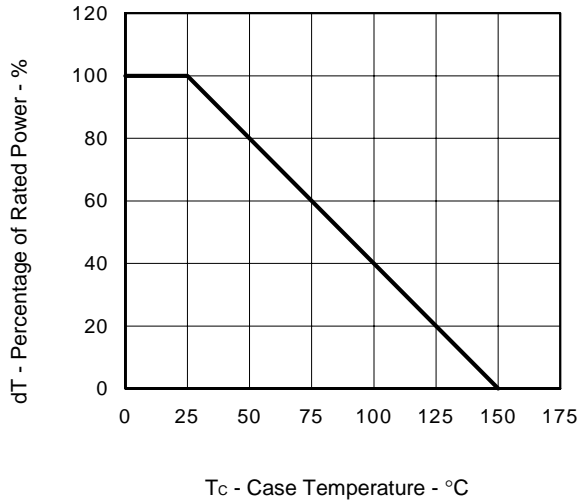


**TEST CIRCUIT 3 GATE CHARGE**

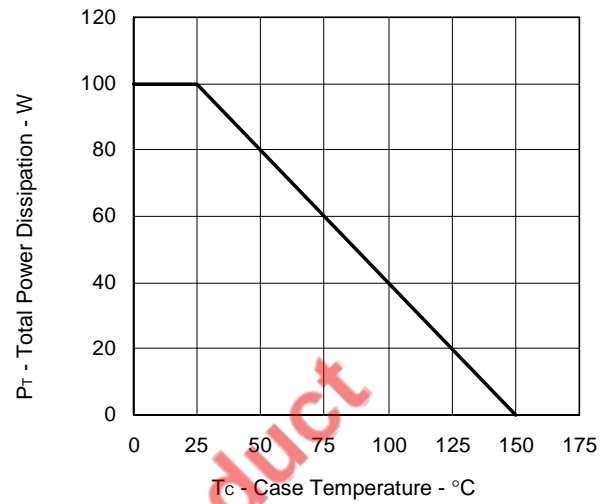


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

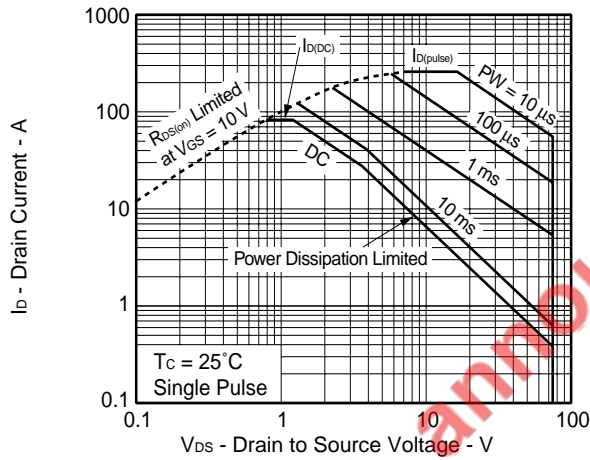
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



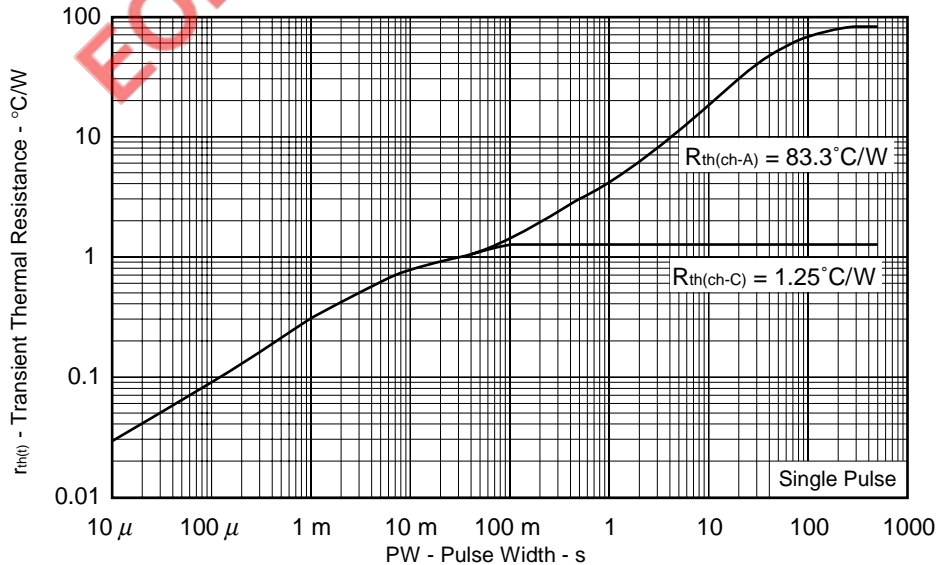
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



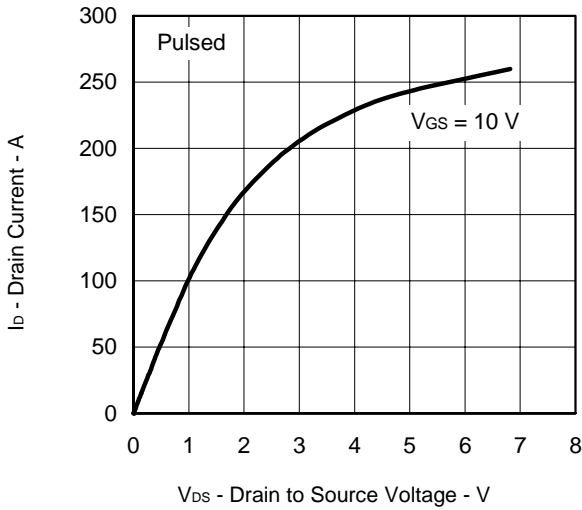
FORWARD BIAS SAFE OPERATING AREA



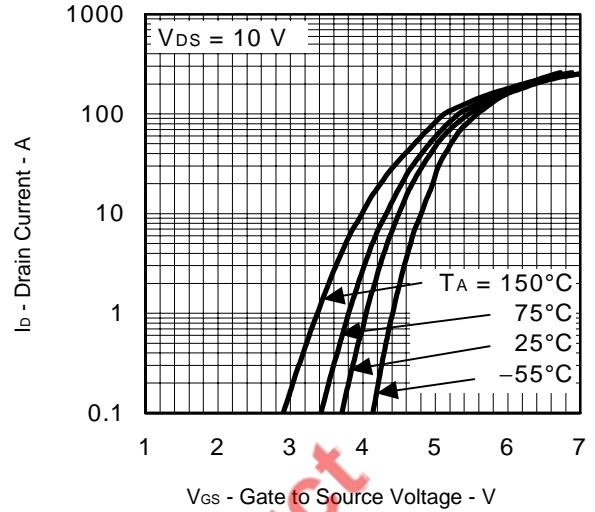
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



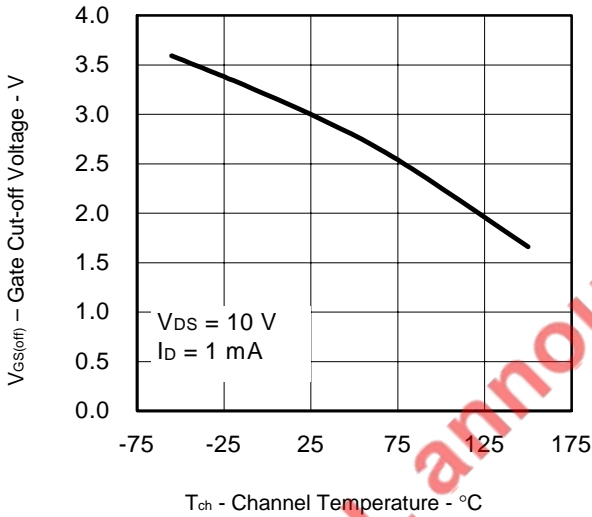
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



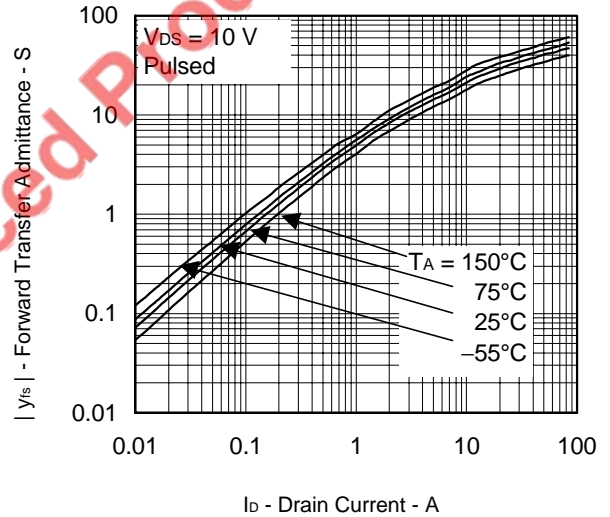
FORWARD TRANSFER CHARACTERISTICS



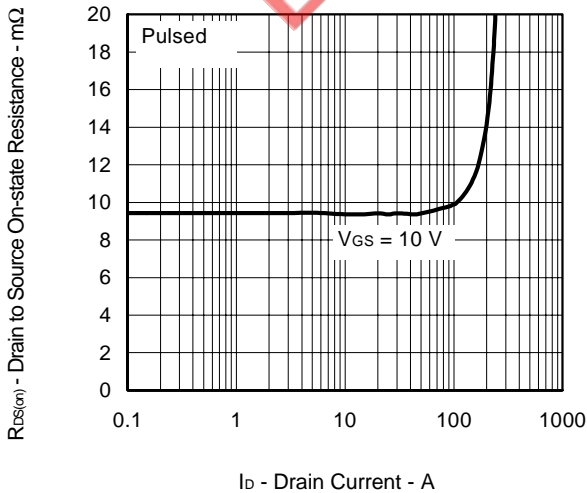
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



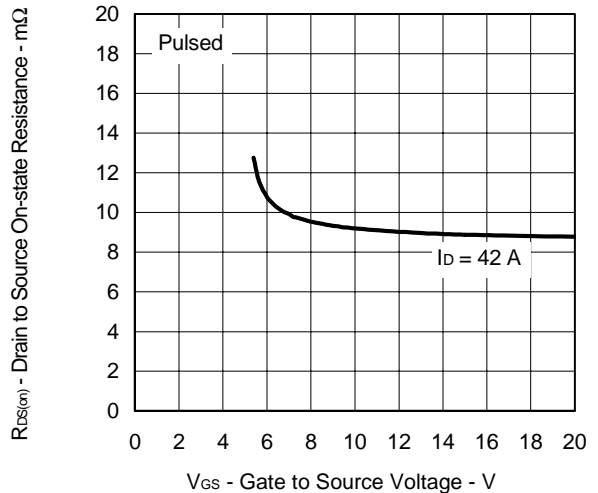
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



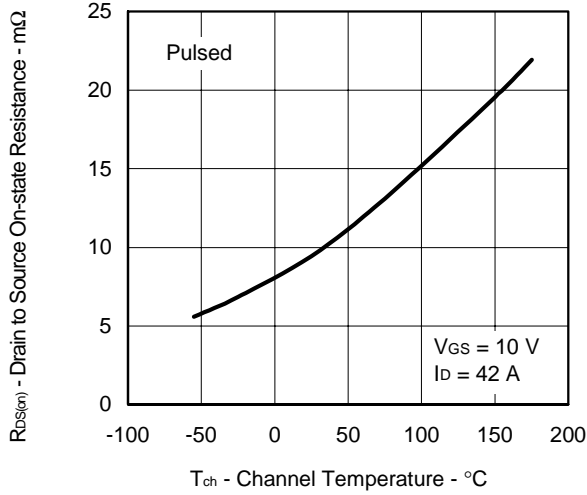
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



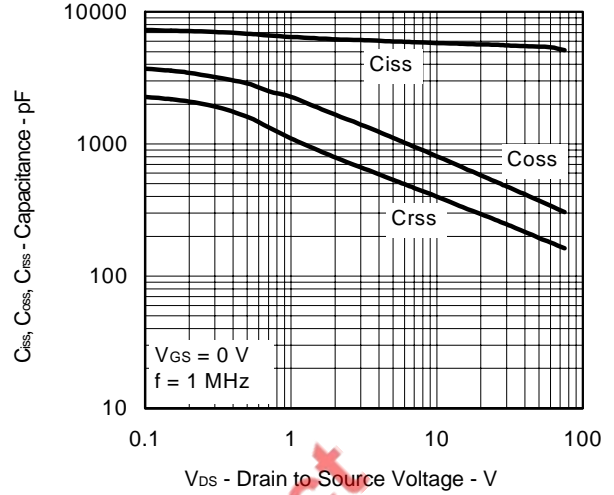
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



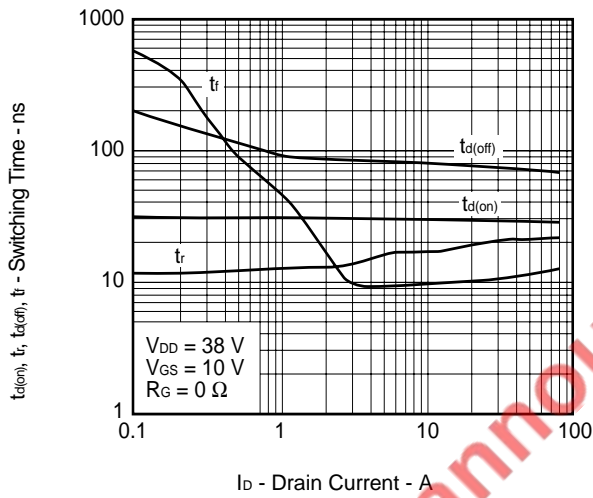
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



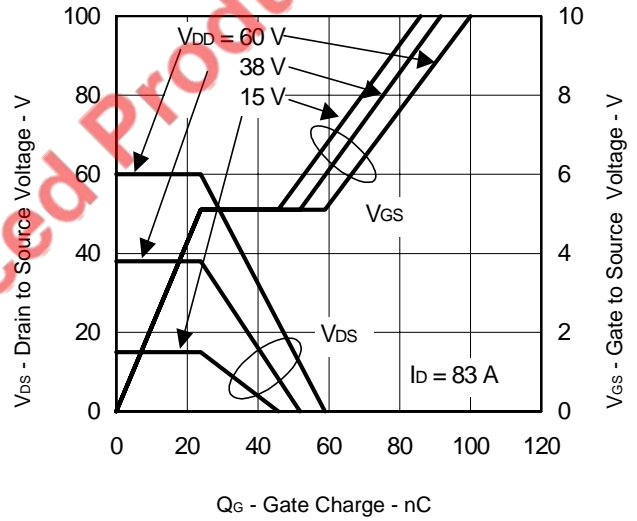
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



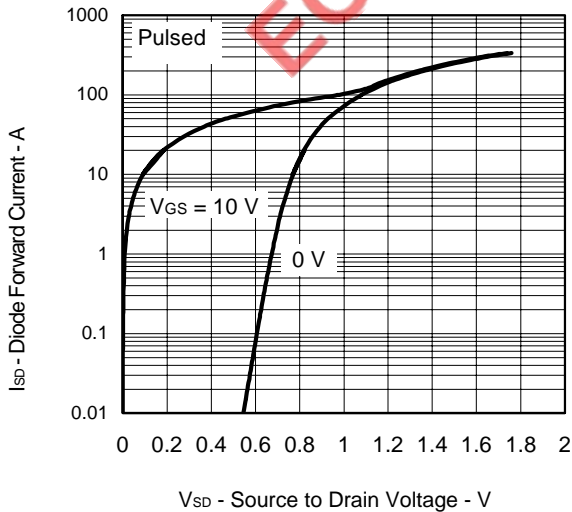
SWITCHING CHARACTERISTICS



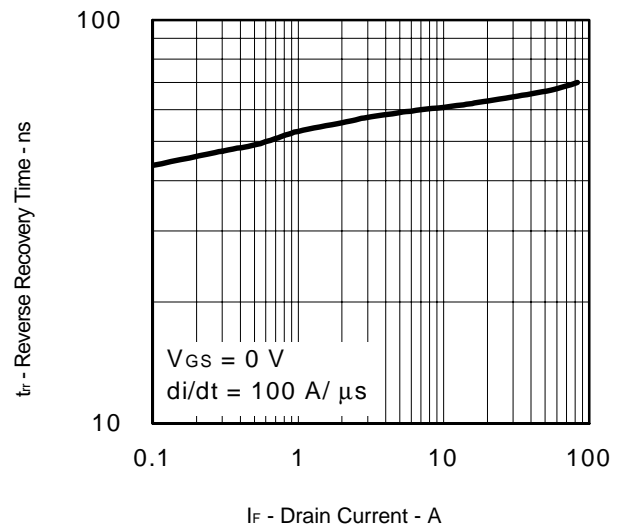
DYNAMIC INPUT/OUTPUT CHARACTERISTICS

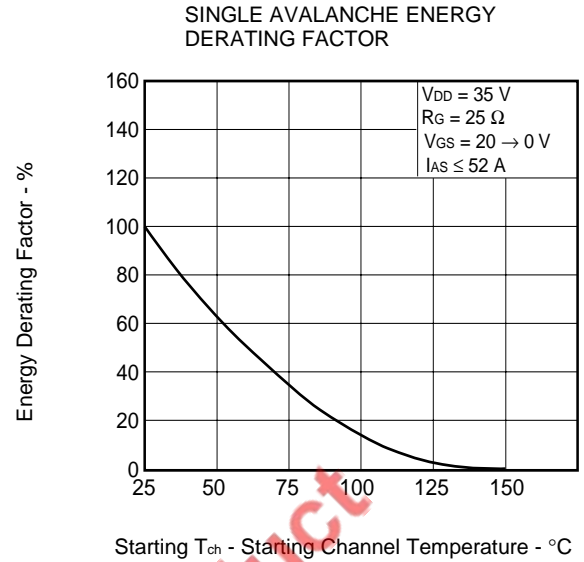
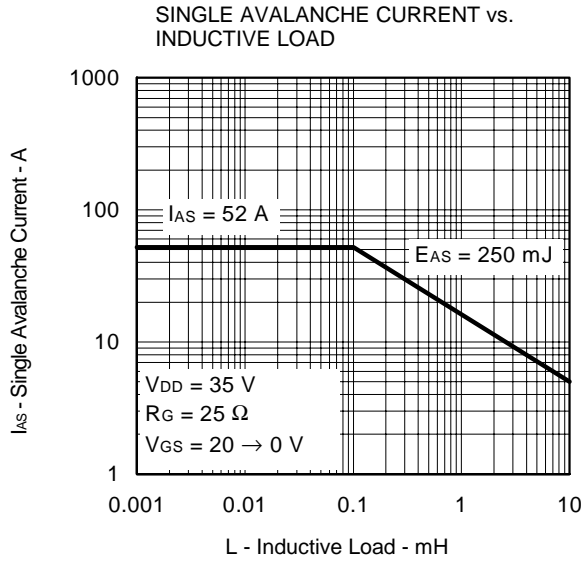


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DRAIN CURRENT

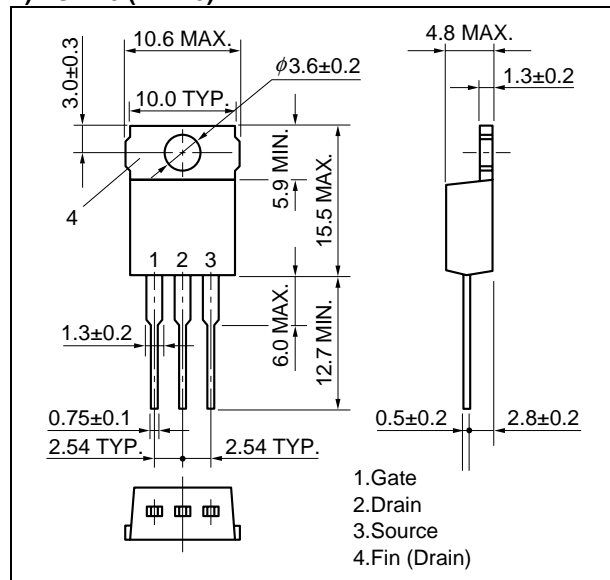




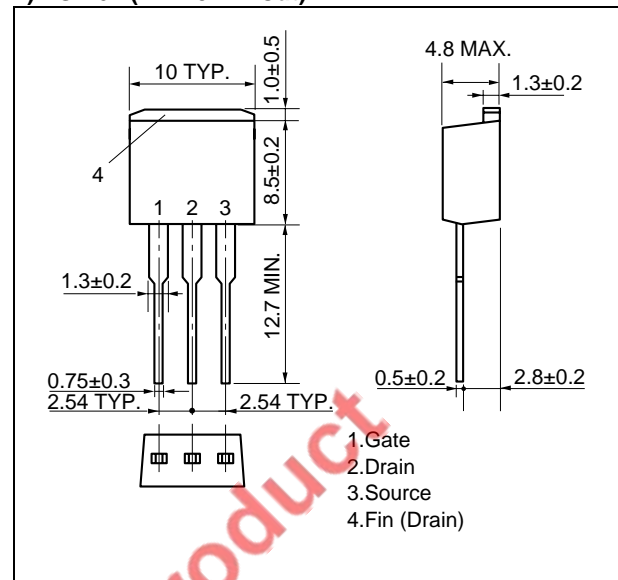
EOL announced Product

PACKAGE DRAWINGS (Unit: mm)

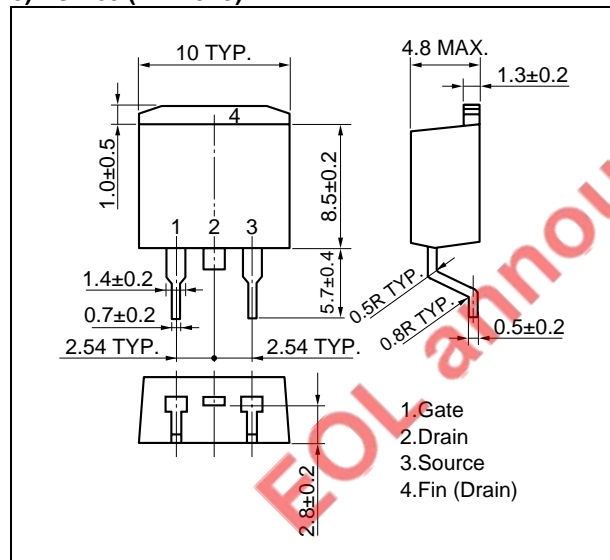
1) TO-220 (MP-25)



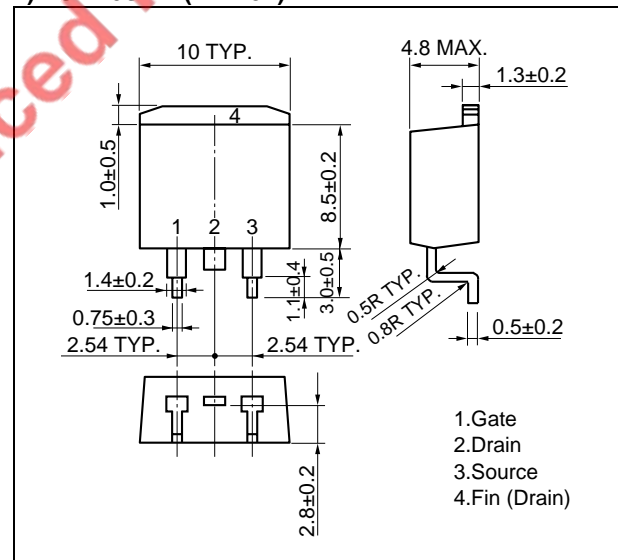
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)

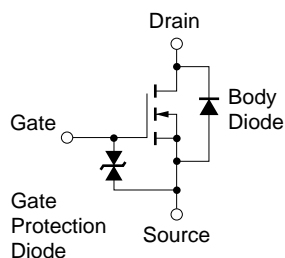


4) TO-220SMD (MP-25Z) <sup>Note</sup>



**Note** This Package is only produced in Japan.

EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.