2SK3652

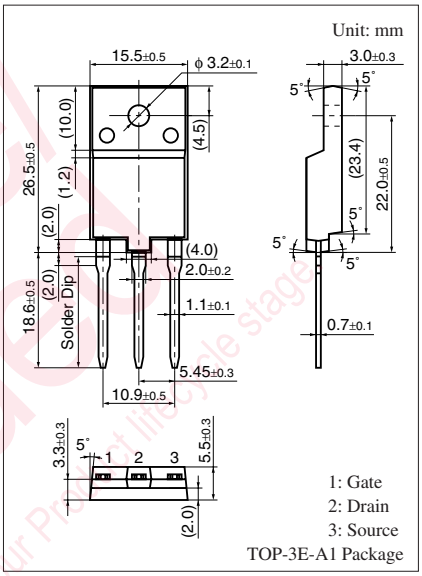
N-channel enhancement mode MOSFET

■ Features

- Low on-resistance, low Q_g
- High avalanche resistance

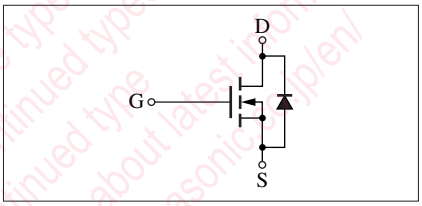
■ Applications

- For PDP
- For high-speed switching



Marking Symbol: K3652

Internal Connection



■ Absolute Maximum Ratings $T_C = 25°C$

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	V_{DSS}	230	V
Gate-source surrender voltage	V_{GSS}	±30	V
Drain current	I_D	50	A
Peak drain current	I_{DP}	200	A
Avalanche energy capability *	EAS	2 200	mJ
Power dissipation	P_D	100	W
$T_a = 25°C$		3	
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	–55 to +150	°C

Note) *: L = 1 mH, I_L = 50 A, V_{DD} = 100 V, 1 pulse, T_a = 25°C

■ Electrical Characteristics $T_C = 25°C \pm 3°C$

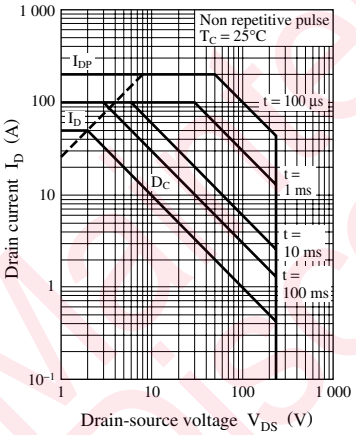
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	I_D = 1 mA, V_{GS} = 0	230			V
Gate threshold voltage	V_{th}	V_{DS} = 25 V, I_D = 10 mA	2		4	V
Drain-source cutoff current	I_{DSS}	V_{DS} = 184 V, V_{GS} = 0			100	µA
Gate-source cutoff current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0			±1	µA
Drain-source ON resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 25 A		29	40	mΩ
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = 25 V, I_D = 25 A	17	35		S
Short-circuit forward transfer capacitance (Common-source)	C_{iss}	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz		5 950		pF
Short-circuit output capacitance (Common-source)	C_{oss}			850		pF
Reverse transfer capacitance (Common-source)	C_{rss}			80		pF
Turn-on delay time	$t_{d(on)}$	V_{DD} = 100 V, I_D = 25 A		65		ns
Rise time	T_r	R_L = 4 Ω, V_{GS} = 10 V		140		ns
Turn-off delay time	$t_{d(off)}$			470		ns
Fall time	t_f			145		ns

■ Electrical Characteristics (continued) $T_C = 25°C \pm 3°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Diode foward voltage	V_{DSF}	I_{DR} = 50 A, V_{GS} = 0			−1.5	V
Reverse recovery time	t_{rr}	L = 230 µH, V_{DD} = 100 V		235		ns
Reverse recovery charge	Q_{rr}	I_{DR} = 25 A, di/dt = 100 A/µs		1 180		nC
Gate charge load	Q_g	V_{DD} = 100 V, I_D = 25 A		105		nC
Gate-source charge	Q_{gs}	V_{GS} = 10 V		40		nC
Gate-drain charge	Q_{gd}			14		nC
Thermal resistance (ch-c)	$R_{th(ch-c)}$				1.25	°C/W
Thermal resistance (ch-a)	$R_{th(ch-a)}$				41.6	°C/W

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

Safe operation area



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