

# MOS FIELD EFFECT TRANSISTOR 2SK3715

## SWITCHING N-CHANNEL POWER MOS FET

#### **DESCRIPTION**

The 2SK3715 is N-channel MOS Field Effect Transistor designed for high current switching applications.

#### **ORDERING INFORMATION**

PART NUMBER	PACKAGE
2SK3715	Isolated TO-220

#### **FEATURES**

Super low on-state resistance

 $R_{DS(on)1} = 6.0 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 10 \text{ V, Ip} = 38 \text{ A)}$ 

 $R_{DS(on)2} = 9.5 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 4 \text{ V, ID} = 38 \text{ A)}$ 

- Low Ciss: Ciss = 8400 pF TYP.
- Built-in gate protection diode

(Isolated TO-220)



#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	60	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	I <sub>D(DC)</sub>	±75	Α
Drain Current (pulse) Note1	D(pulse)	±300	Α
Total Power Dissipation (Tc = 25°C)	P <sub>T1</sub>	40	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Single Avalanche Current Note2	las	67	Α
Single Avalanche Energy Note2	Eas	450	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

2. Starting Tch = 25°C, Vdd = 30 V, Rg = 25  $\Omega$ , Vgs = 20  $\rightarrow$  0 V

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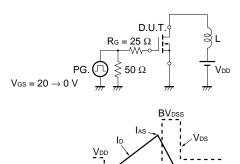


**ELECTRICAL CHARACTERISTICS (TA = 25°C)** 

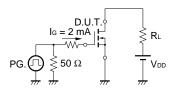
ww.DataSheeCHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	Vps = 60 V, Vgs = 0 V			10	μΑ
Gate Leakage Current	Igss	V <sub>G</sub> S = ±20 V, V <sub>D</sub> S = 0 V			±10	μΑ
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 38 A	33	65		S
Drain to Source On-state Resistance Note	R <sub>DS(on)1</sub>	Vgs = 10 V, Ip = 38 A		4.8	6.0	mΩ
	R <sub>DS(on)2</sub>	Vgs = 4 V, ID = 38 A		6.1	9.5	mΩ
Input Capacitance	Ciss	Vps = 10 V		8400		pF
Output Capacitance	Coss	V <sub>G</sub> S = 0 V		1200		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		530		pF
Turn-on Delay Time	td(on)	VDD = 30 V, ID = 38 A		24		ns
Rise Time	tr	Vgs = 10 V		15		ns
Turn-off Delay Time	td(off)	$R_G = 0 \Omega$		116		ns
Fall Time	tf			11		ns
Total Gate Charge	<b>Q</b> G	VDD = 48 V		145		nC
Gate to Source Charge	Qgs	V <sub>GS</sub> = 10 V		21		nC
Gate to Drain Charge	Q <sub>GD</sub>	ID = 75 A		39		nC
Body Diode Forward Voltage Note	V <sub>F</sub> (S-D)	I <sub>F</sub> = 75 A, V <sub>GS</sub> = 0 V		0.92	1.5	V
Reverse Recovery Time	trr	IF = 50 A, VGS = 0 V		59		ns
Reverse Recovery Charge	Qrr	di/dt = 50 A/μs		136		nC

#### **★ Note** Pulsed

#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

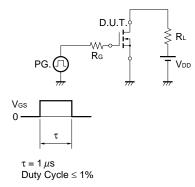


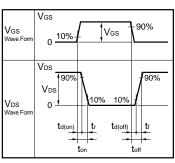




Starting Tch

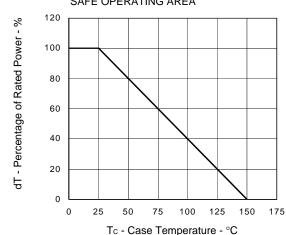
#### **TEST CIRCUIT 2 SWITCHING TIME**



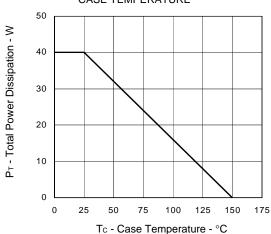


#### TYPICAL CHARACTERISTICS (TA = 25°C)

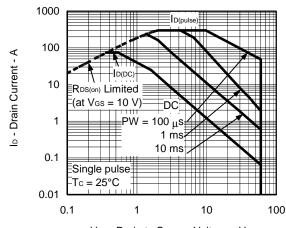
www.DataSheet DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



## TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

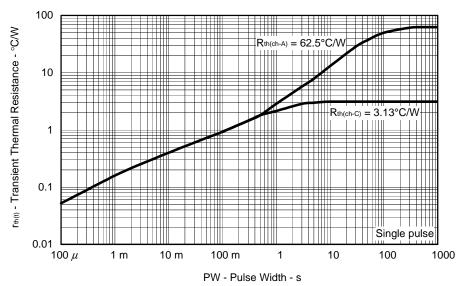


#### ★ FORWARD BIAS SAFE OPERATING AREA

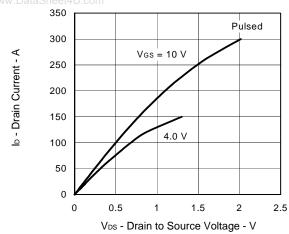


#### $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

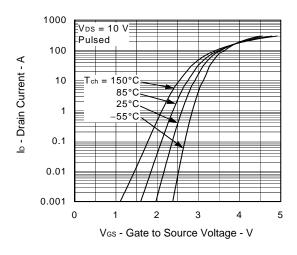
#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



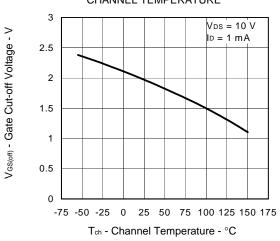
#### DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



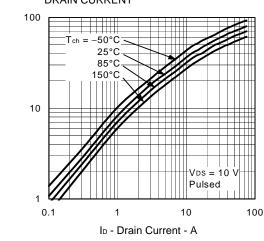
#### FORWARD TRANSFER CHARACTERISTICS



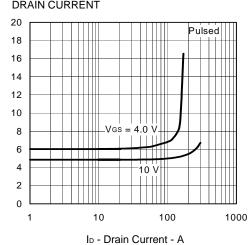
#### GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



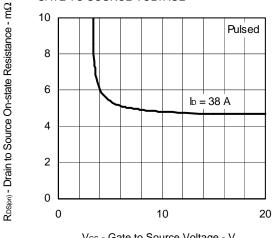
#### FORWARD TRANSFER ADMITTANCE vs. **DRAIN CURRENT**



#### DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**



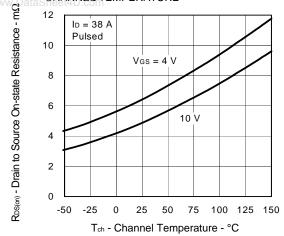
#### DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



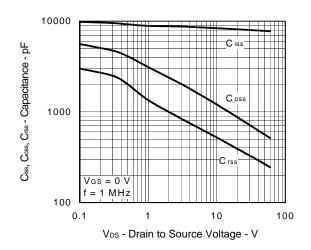
RDS(on) - Drain to Source On-state Resistance - mΩ

y<sub>fs</sub> | - Forward Transfer Admittance - S

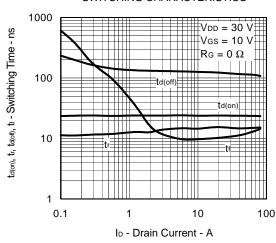
## DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



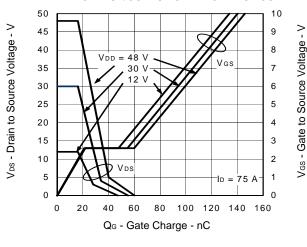
#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



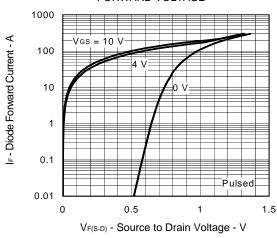
#### SWITCHING CHARACTERISTICS



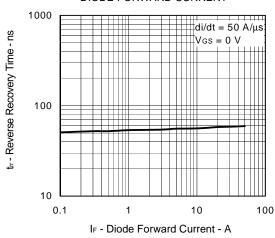
#### DYNAMIC INPUT/OUTPUT CHARACTERISTICS



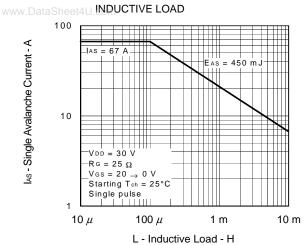
## SOURCE TO DRAIN DIODE FORWARD VOLTAGE



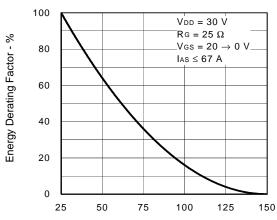
## REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



### SINGLE AVALANCHE CURRENT vs.



## SINGLE AVALANCHE ENERGY DERATING FACTOR

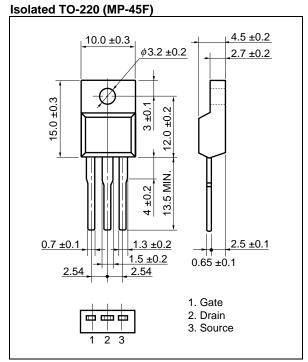


Starting Tch - Starting Channel Temperature - °C

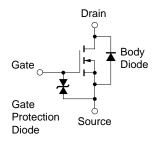


#### PACKAGE DRAWING (Unit: mm)

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#### **EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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