DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR
2SK3984

SWITCHING
N-CHANNEL POWER MOSFET

DESCRIPTION

The 2SK3984 is N-channel MOS Field Effect Transistor designed for high speed switching applications such as class-D amplifier.

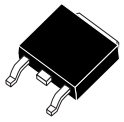
ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3984-ZK	TO-252 (MP-3ZK)

FEATURES

- Super low on-state resistance
  $R_{DS(on)}$ = 71 mΩ TYP. (V_{GS} = 10 V, I_D = 9 A)
  $R_{DS(on)}$ = 85 mΩ MAX. (V_{GS} = 10 V, I_D = 9 A)
- Low C_{iss}: C_{iss} = 750 pF TYP.

(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	100	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±18	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±45	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	30	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Single Avalanche Energy Note2	E_{AS}	10	mJ
Repetitive Avalanche Current Note3	I_{AR}	10	A
Repetitive Avalanche Energy Note3	E_{AR}	10	mJ

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	125	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	4.17	°C/W

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 50 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

3. $T_{ch(peak)}$ ≤ 150°C, R_G = 25 Ω

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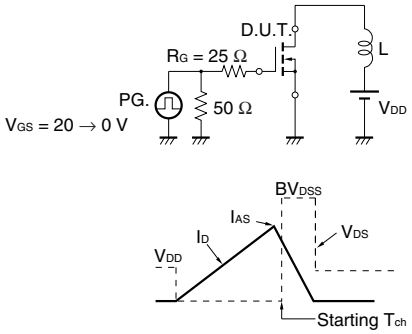
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

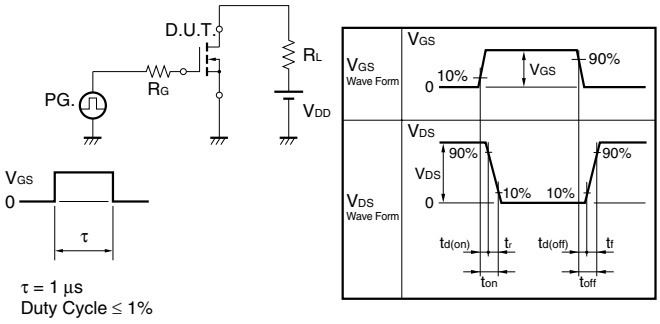
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	4.5	5.5	6.5	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 9 A	2.5	5.8		S
Drain to Source On-state Resistance Note	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 9 A		71	85	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		750		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		120		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		40		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 9 A		15		ns
Rise Time	t_r	V_{GS} = 10 V		6		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		17		ns
Fall Time	t_f			5		ns
Total Gate Charge	Q_G	V_{DD} = 50 V		13		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		5.5		nC
Gate to Drain Charge	Q_{GD}	I_D = 18 A		4		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 18 A, V_{GS} = 0 V		0.9	1.5	V
<R> Reverse Recovery Time	t_{rr}	I_F = 18 A, V_{GS} = 0 V		56		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		146		nC

Note Pulsed

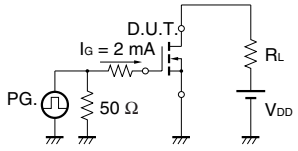
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

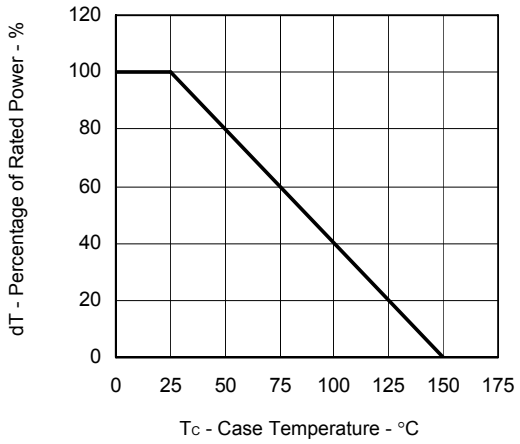


TEST CIRCUIT 3 GATE CHARGE

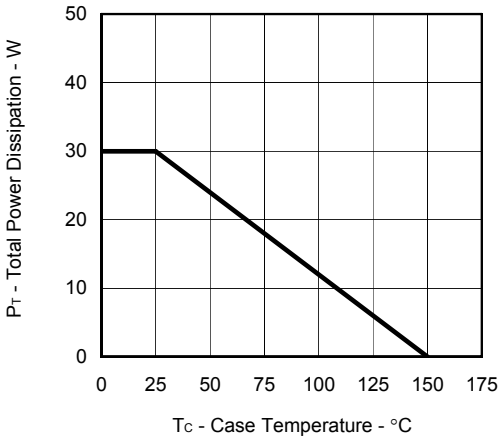


TYPICAL CHARACTERISTICS (T_A = 25°C)

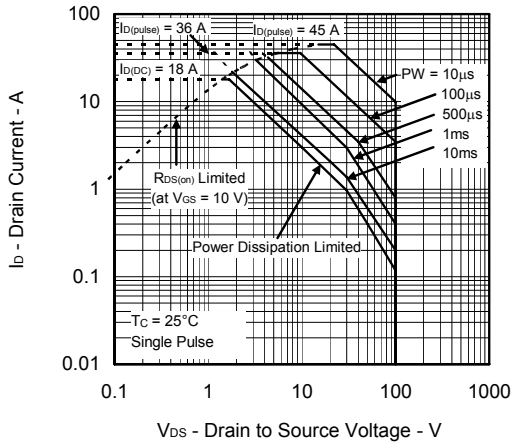
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



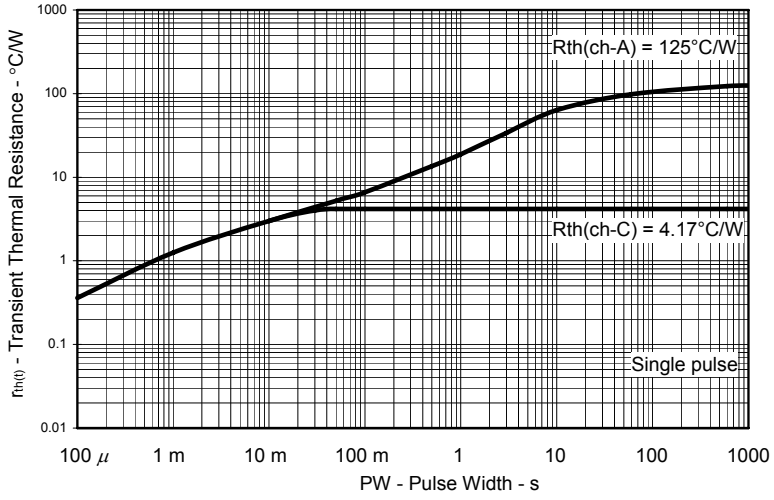
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



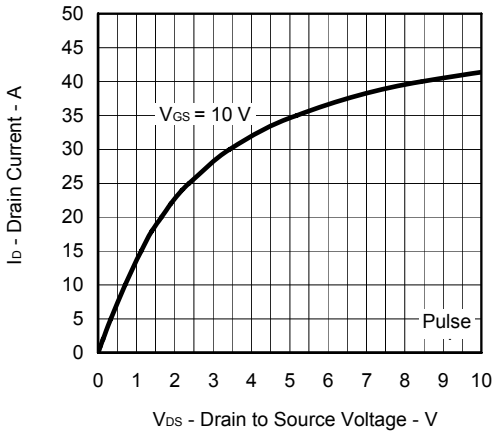
FORWARD BIAS SAFE OPERATING AREA



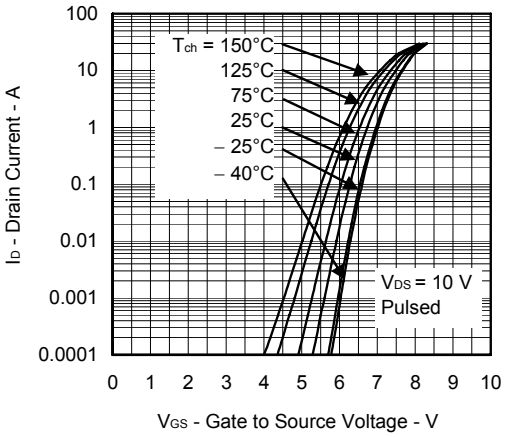
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



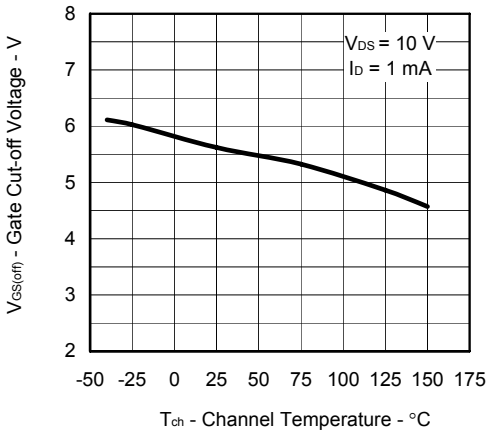
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



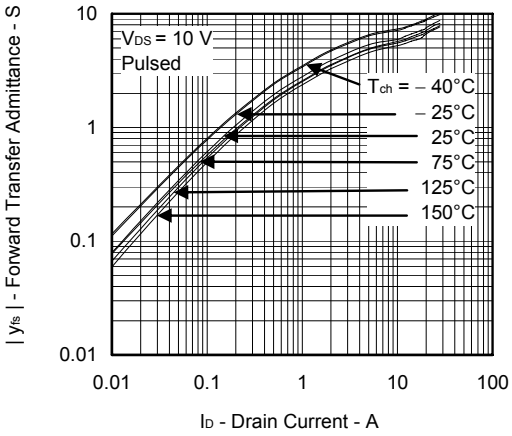
FORWARD TRANSFER CHARACTERISTICS



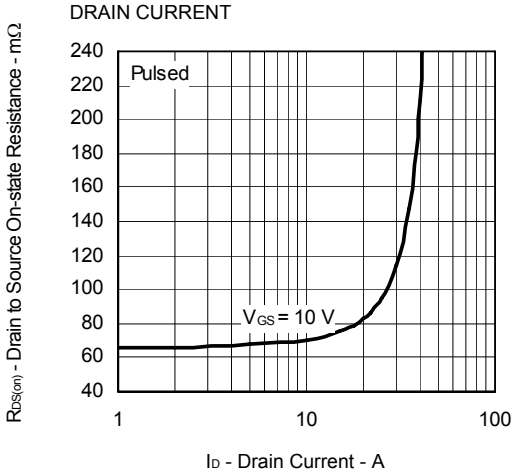
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



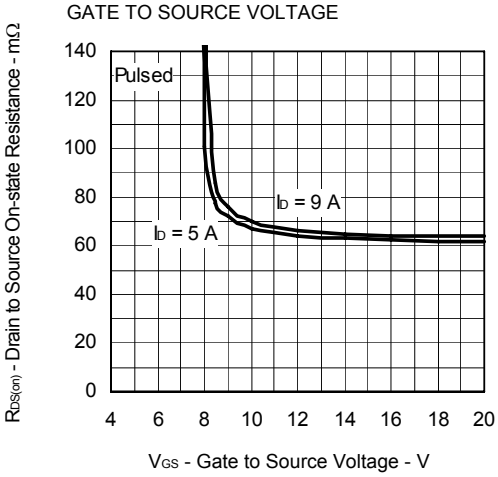
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



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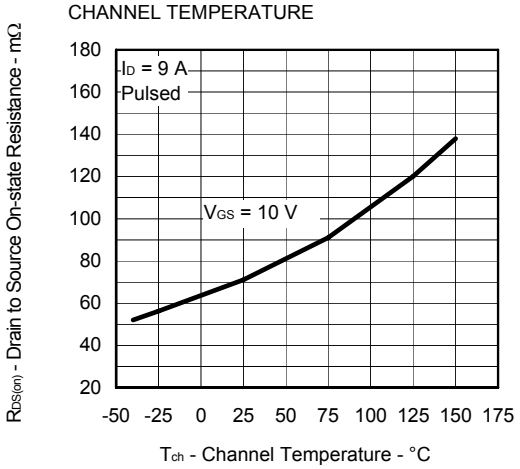
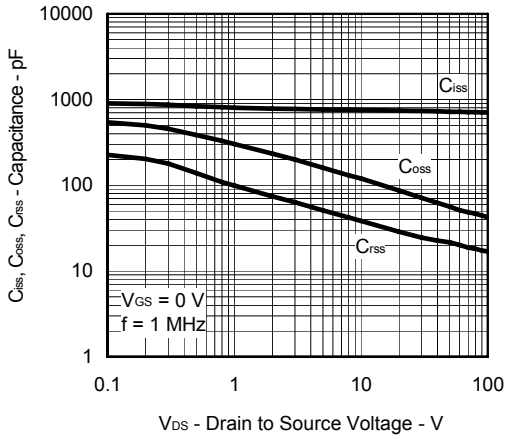
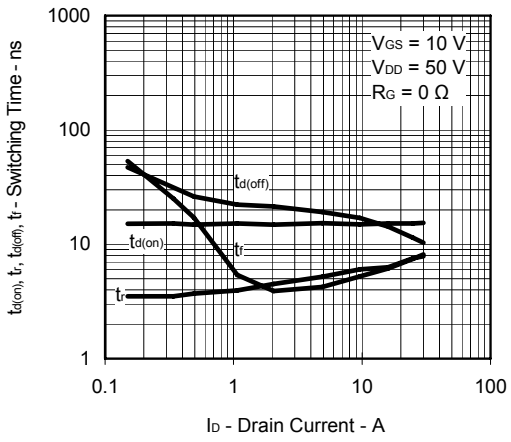
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



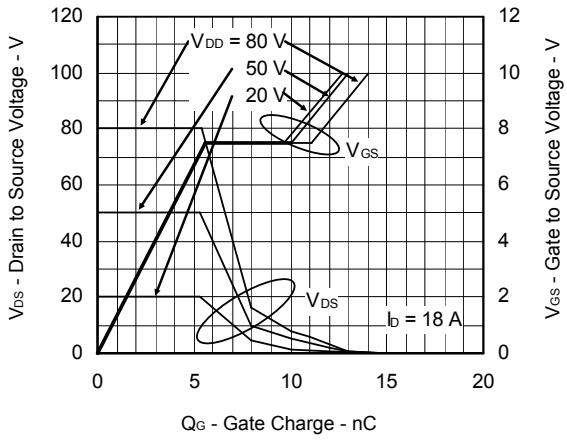
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



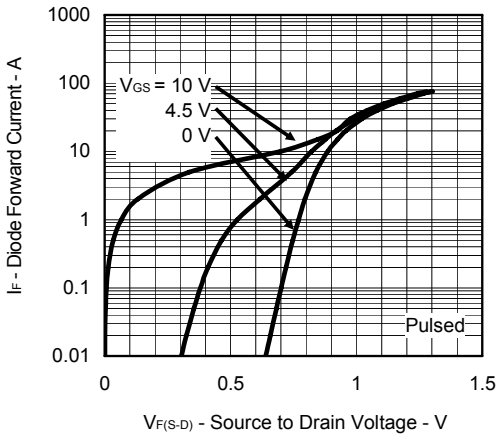
SWITCHING CHARACTERISTICS



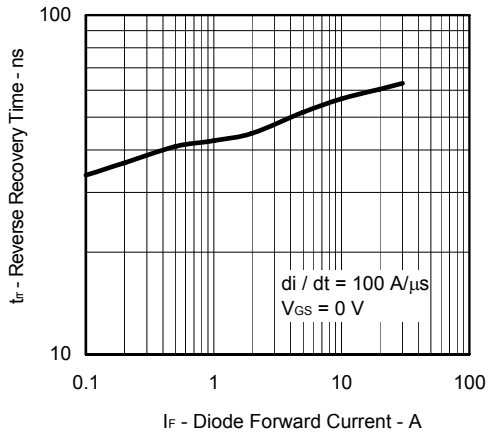
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



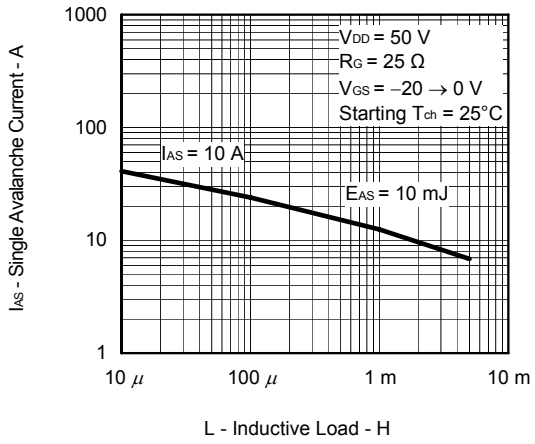
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

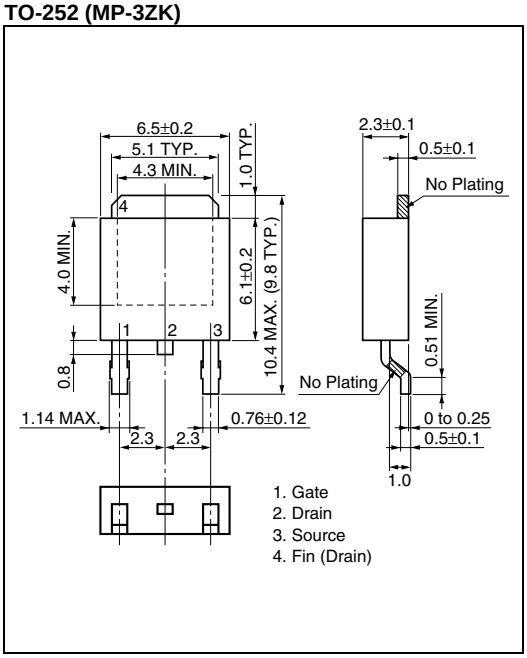


SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

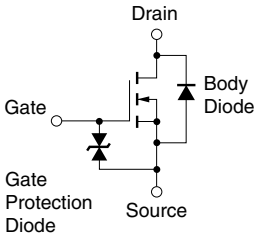


PACKAGE DRAWINGS (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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