DATA SHEET

MOS FIELD EFFECT TRANSISTOR
2SK4069

SWITCHING
N-CHANNEL POWER MOSFET

DESCRIPTION

The 2SK4069 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

FEATURES

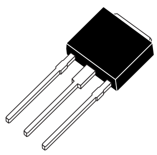
- Low on-state resistance
  $R_{DS(on)1}$ = 12 mΩ MAX. (V_{GS} = 10 V, I_D = 15 A)
- Low Q_{GD}: Q_{GD} = 3.2 nC TYP.
- 4.5 V drive available

ORDERING INFORMATION

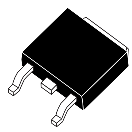
	PART NUMBER	PACKAGE
<R>	2SK4069(1)-S27-AY Note	TO-251 (MP-3-b)
	2SK4069-ZK-E1-AY Note	TO-252 (MP-3ZK)
	2SK4069-ZK-E2-AY Note	TO-252 (MP-3ZK)

Note Pb-free (This product does not contain Pb in external electrode.)

(TO-251)



(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	25	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±30	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±120	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	21	W
Total Power Dissipation	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	18	A
Single Avalanche Energy Note2	E_{AS}	32.4	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 12 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

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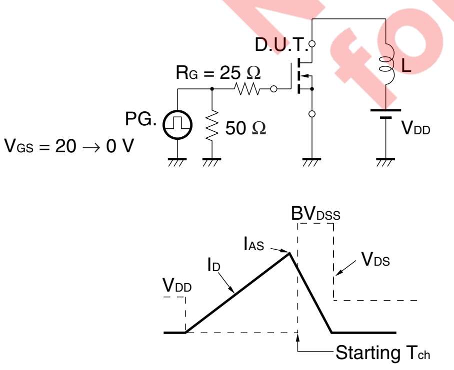
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

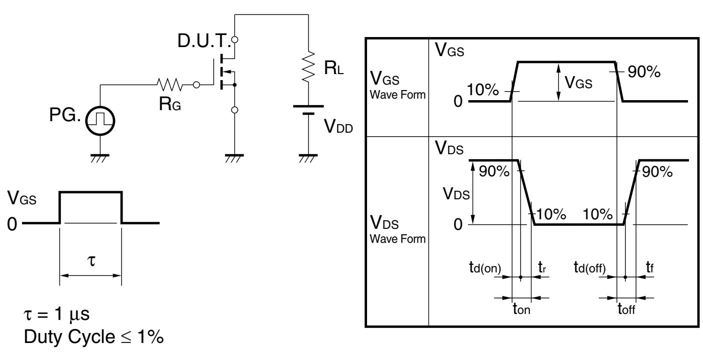
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	| y_{fs} |	V_{DS} = 10 V, I_D = 7.5 A	5	10		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 15 A		9.4	12	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 15 A		15	21	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		860		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		255		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		90		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 12 V, I_D = 30 A		14/7.5		ns
Rise Time	t_r	V_{GS} = 4.5 V/12 V		13/4.2		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 3 Ω		1.9/24		ns
Fall Time	t_f			14/4.4		ns
Total Gate Charge	Q_{G1}	V_{DD} = 12 V ,V_{GS} = 12 V, I_D = 30 A		17		nC
Total Gate Charge	Q_{G2}	V_{DD} = 12 V ,V_{GS} = 4.5 V, I_D = 30 A		6.7		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 12 V , I_D = 30 A		2.4		nC
Gate to Drain Charge	Q_{GD}			3.2		nC
Gate Resistance	R_G			1.5		Ω
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 30 A, V_{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 30 A, V_{GS} = 0 V		29		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		20		nC

Note Pulsed

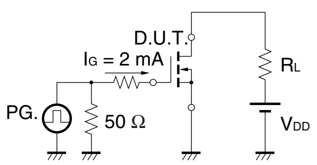
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

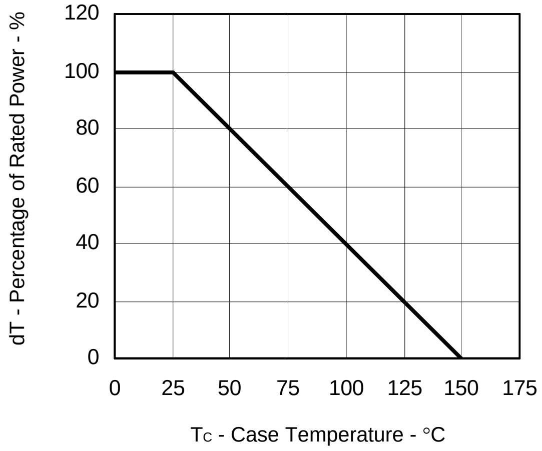


TEST CIRCUIT 3 GATE CHARGE

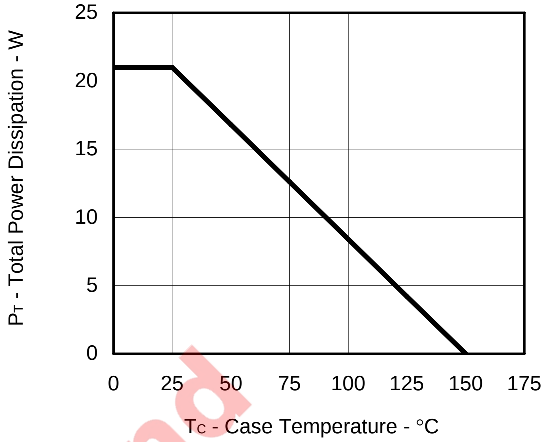


TYPICAL CHARACTERISTICS (T_A = 25°C)

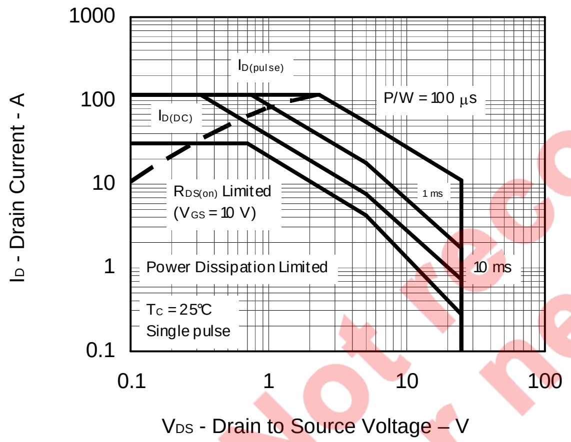
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



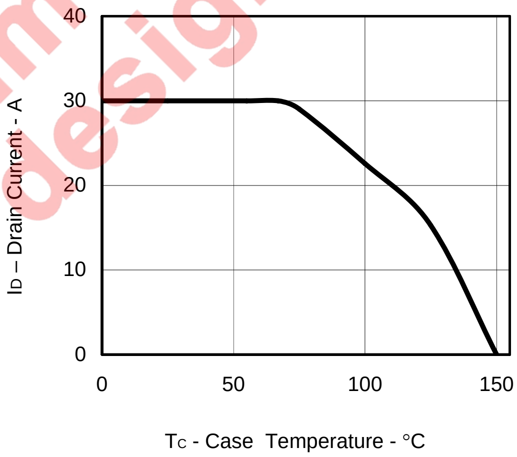
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



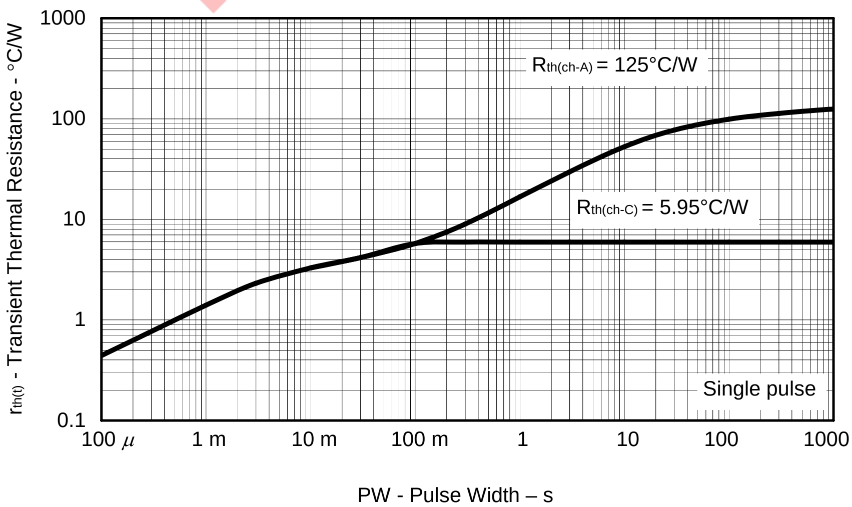
FORWARD BIAS SAFE OPERATING AREA



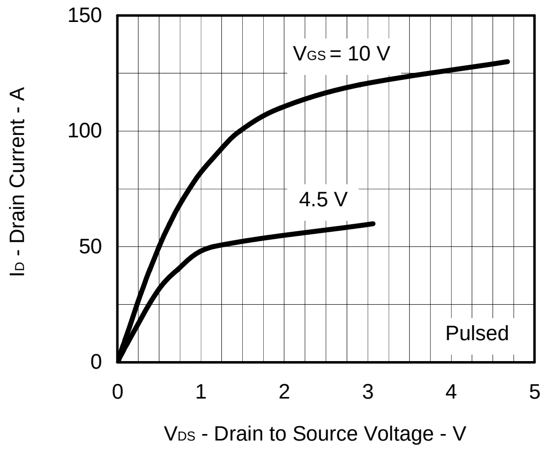
DRAIN CURRENT vs CASE TEMPERATURE



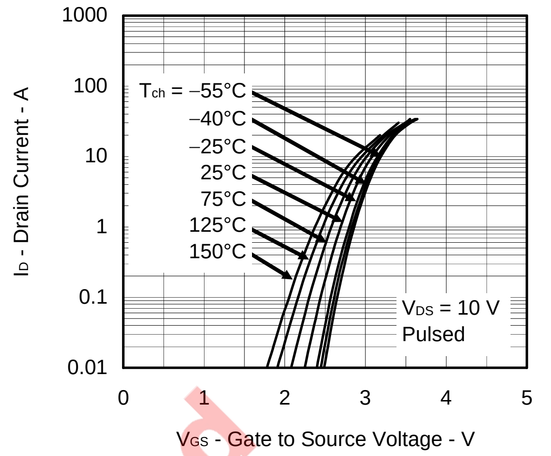
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



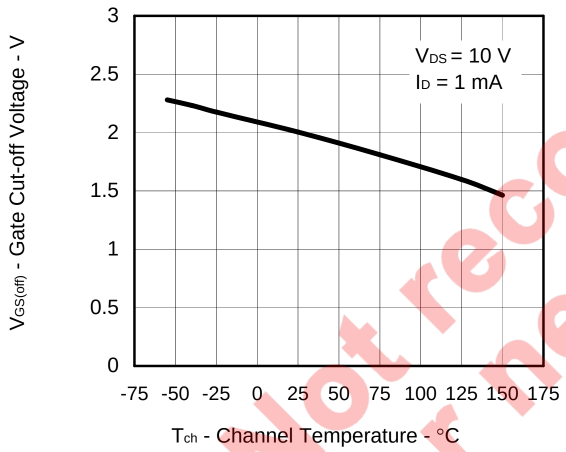
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



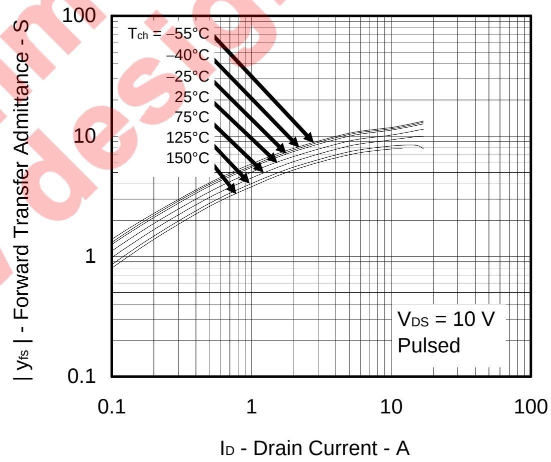
FORWARD TRANSFER CHARACTERISTICS



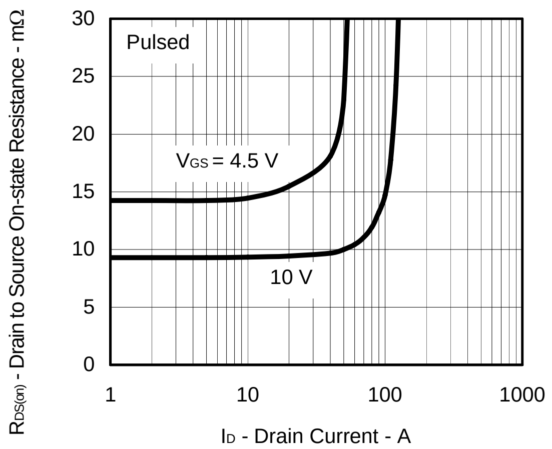
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



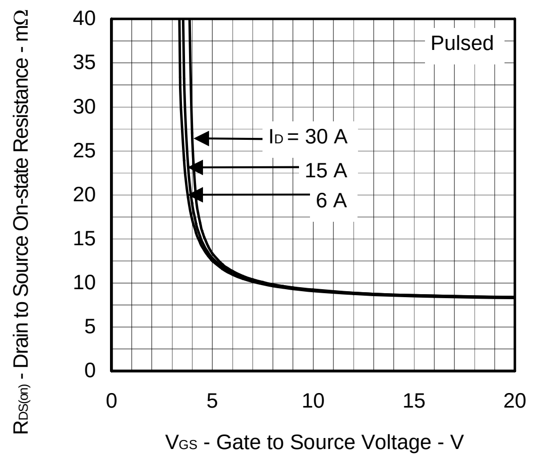
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



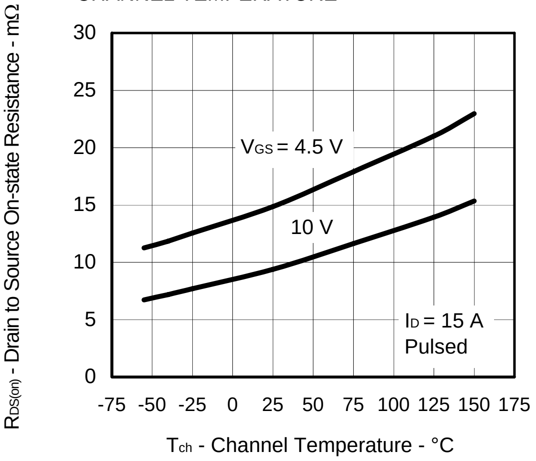
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



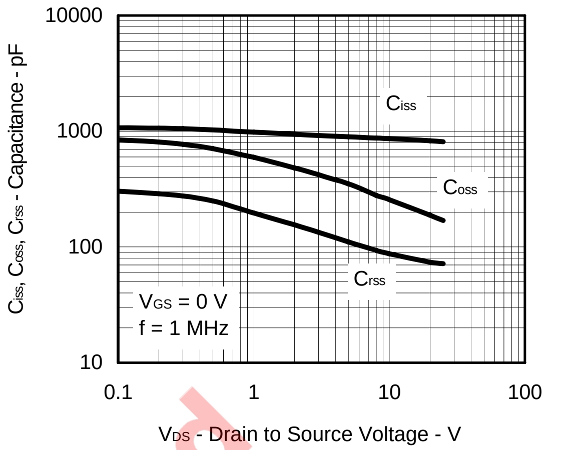
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



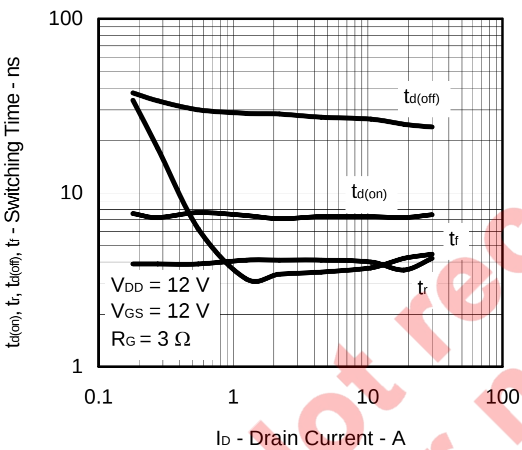
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



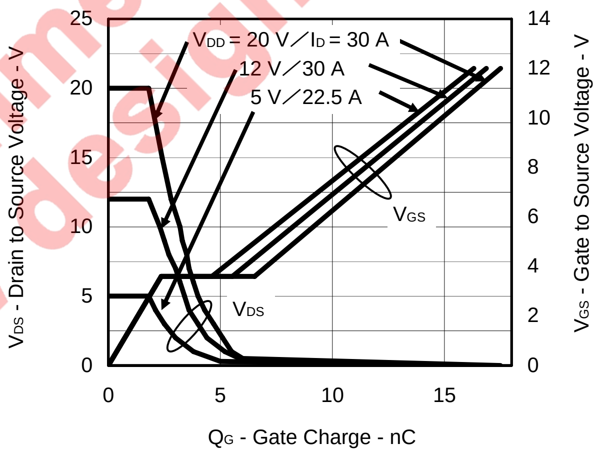
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



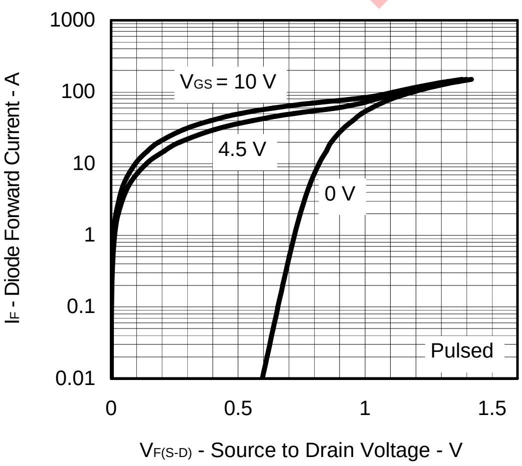
SWITCHING CHARACTERISTICS



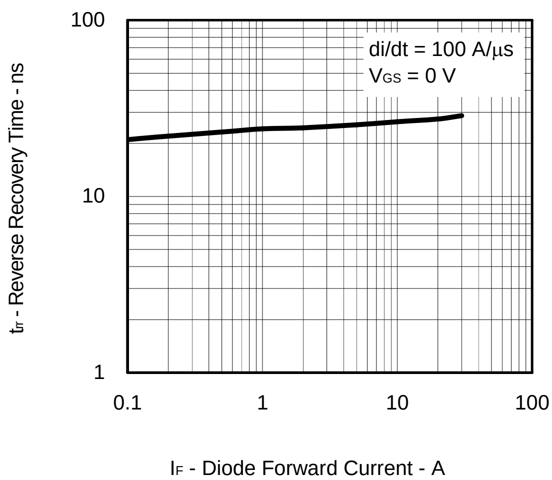
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



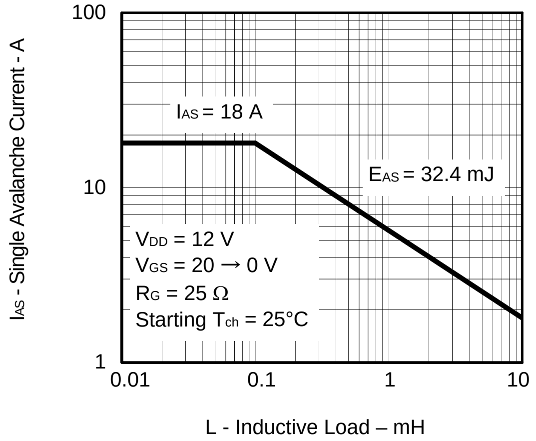
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



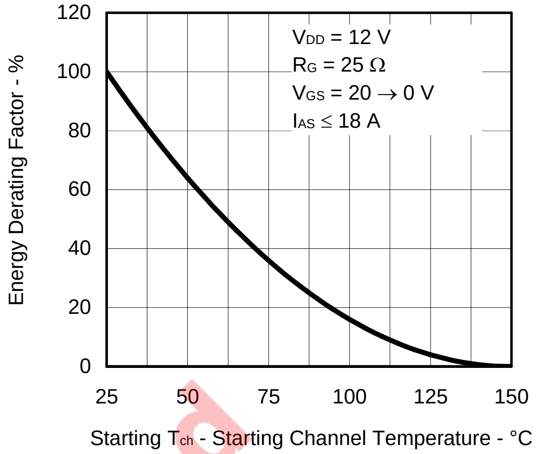
REVERSE RECOVERY TIME vs.
DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

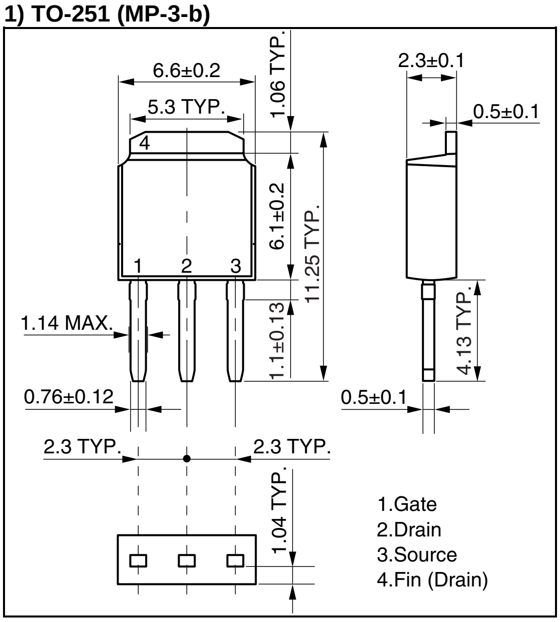


SINGLE AVALANCHE ENERGY
DERATING FACTOR

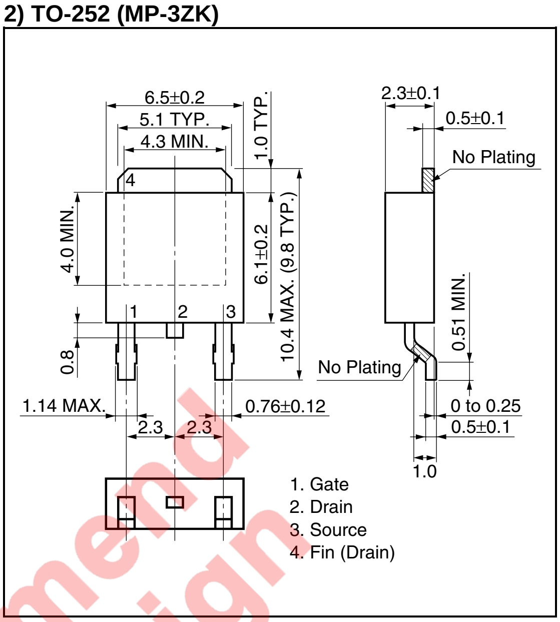


PACKAGE DRAWINGS (Unit: mm)

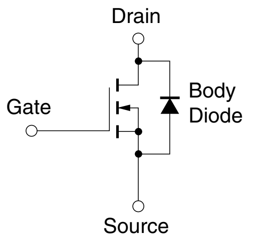
<R> **1) TO-251 (MP-3-b)**



2) TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.