

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

NEC

The 2SK4075 is N-channel MOS FET designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SK4075-ZK-E1-AY	Pure Sn (Tin)	Таре	TO-252 (MP-3ZK)
2SK4075-ZK-E2-AY		2500 p/reel	typ. 0.27 g

FEATURES

Low on-state resistance

- $\begin{aligned} R_{DS(on)1} &= 6.7 \text{ m}\Omega \text{ MAX. } (V_{GS} = 10 \text{ V}, \text{ I}_{D} = 30 \text{ A}) \\ R_{DS(on)2} &= 10 \text{ m}\Omega \text{ MAX. } (V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 15 \text{ A}) \end{aligned}$
- Low Ciss: Ciss = 2900 pF TYP.

Logic level drive type

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	40	V
Gate to Source Voltage (VDs = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	D(DC)	±60	А
Drain Current (pulse) ^{Note1}	D(pulse)	±180	А
Total Power Dissipation (Tc = 25° C)	P _{T1}	52	W
Total Power Dissipation (T _A = 25°C)	Pt2	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note2	las	28	А
Single Avalanche Energy Note2	Eas	78	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = 20 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H

THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	2.4	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	125	°C/W

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The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.





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ELECTRICAL CHARACTERISTICS (TA = 25°C)

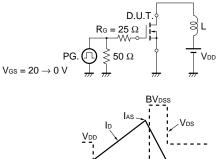
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 40 V, V _{GS} = 0 V			1	μA
Gate Leakage Current	lgss	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	v
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 15 A	9.3			S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10 V, I _D = 30 A		5.2	6.7	mΩ
	RDS(on)2	V _{GS} = 4.5 V, I _D = 15 A		7.2	10	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		2900		pF
Output Capacitance	Coss	V _{GS} = 0 V		450		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		293		pF
Turn-on Delay Time	td(on)	V _{DD} = 20 V		18		ns
Rise Time	tr	ID = 30 A		16		ns
Turn-off Delay Time	td(off)	V _{GS} = 10 V		54		ns
Fall Time	tr	R _G = 0 Ω		9		ns
Total Gate Charge	QG	V _{DD} = 32 V		54		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		11		nC
Gate to Drain Charge	Qgd	I⊳ = 60 A		15		nC
Body Diode Forward Voltage Note	VF(S-D)	IF = 60 A, VGS = 0 V		0.9	1.5	V
Reverse Recovery Time	trr	IF = 60 A, V _{GS} = 0 V		33		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ <i>µ</i> s		33		nC

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

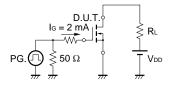
TEST CIRCUIT 2 SWITCHING TIME

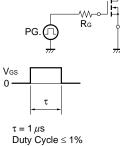
D.U.T.

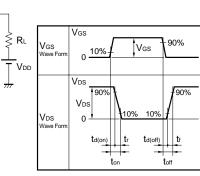


-Starting Tch

TEST CIRCUIT 3 GATE CHARGE





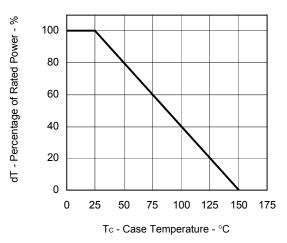


Data Sheet D18223EJ2V0DS

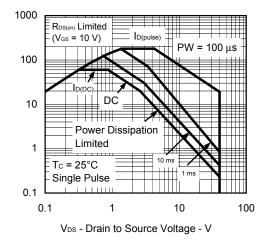
Ip - Drain Current - A

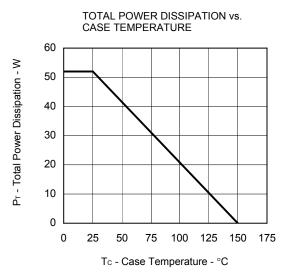
TYPICAL CHARACTERISTICS (TA = 25°C)

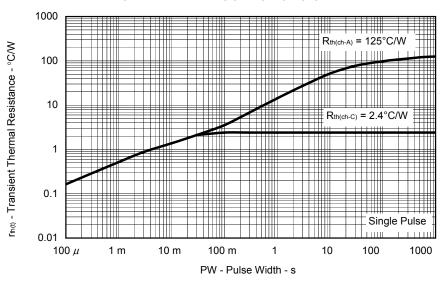
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA





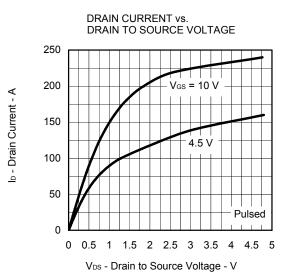






TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

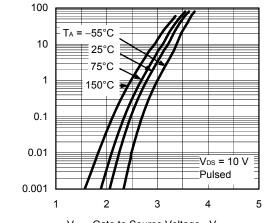
Data Sheet D18223EJ2V0DS



GATE CUT-OFF VOLTAGE vs.

CHANNEL TEMPERATURE

FORWARD TRANSFER CHARACTERISTICS

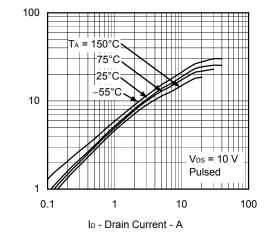


Ip - Drain Current - A

| yfs | - Forward Transfer Admittance - S

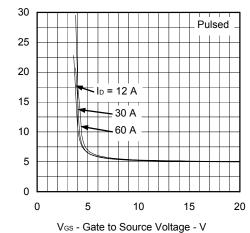
VGS - Gate to Source Voltage - V

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATERESISTANCE vs.

GATE TO SOURCE VOLTAGE



V_{GS(off)} - Gate Cut-off Voltage - V

2.5

2

1.5

1

0.5

0

-100



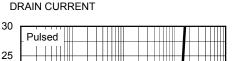
V_{DS} = 10 V

-50

0

I_D = 1 mA

 $R^{\mathrm{DS}(\sigma n)}$ - Drain to Source On-state Resistance - $m\Omega$

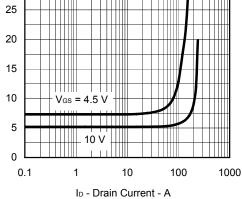


50

100

150

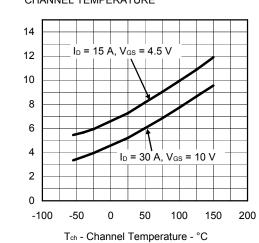
200



Data Sheet D18223EJ2V0DS

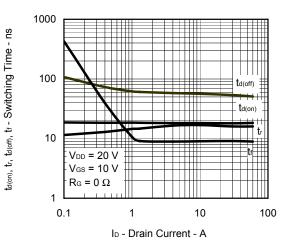
 $R_{DS(on)}$ - Drain to Source On-state Resistance - $m\Omega$

 $R_{DS(on)}$ - Drain to Source On-state Resistance - $m\Omega$

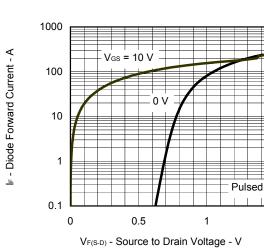


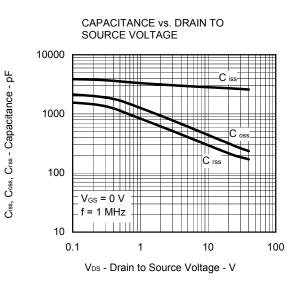
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



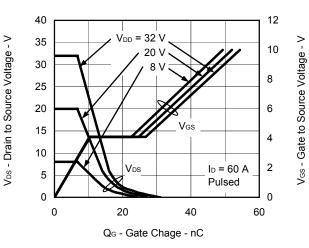


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

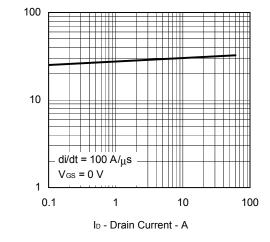




DYNAMIC INPUT/OUTPUT CHARACTERISTICS





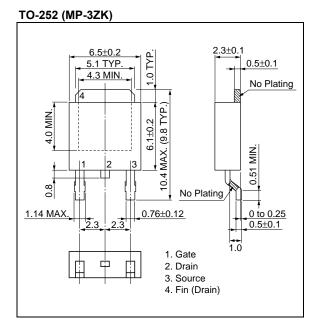


Data Sheet D18223EJ2V0DS

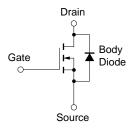
1.5

trr - Reverse Recovery Time - ns

PACKAGE DRAWING (Unit: mm)



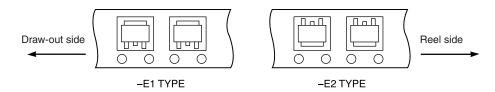
EQUIVALENT CIRCUIT



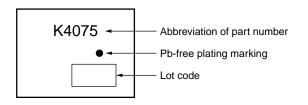
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The 2SK4075 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below	IR60-00-3
	Time at maximum temperature: 10 seconds or less	
	Time of temperature higher than 220°C: 60 seconds or less	
	Preheating time at 160 to 180°C: 60 to 120 seconds	
	Maximum number of reflow processes: 3 times	
	Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	
Partial heating	Maximum temperature (Pin temperature): 350°C or below	P350
	Time (per side of the device): 3 seconds or less	
	Maximum chlorine content of rosin flux: 0.2% (wt.) or less	

Caution Do not use different soldering methods together (except for partial heating).

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