

K4C89363AF

Network-DRAM-II Specification
Version 0.0

K4C89363AF

Revision History

Version 0.0 (Nov. 2002)

- First Release

K4C89363AF

2,097,152-WORDS x 4 BANKS x 36-BITS DOUBLE DATA RATE Network-DRAM

DESCRIPTION

K4C89363AF is a CMOS Double Data Rate Network-DRAM containing 301,989,888 memory cells. K4C89363AF is organized as 2,097,152-words x 4 banks x36 bits. K4C89363AF feature a fully synchronous operation referenced to clock edge whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. K4C89363AD can operate fast core cycle compared with regular DDR SDRAM.

K4C89363AF is suitable for Server, Network and other applications where large memory density and low power consumption are required. The Output Driver for Network-DRAM is capable of high quality fast data transfer under light loading condition.

FEATURES

Parameter		K4C89363AF		
		F6	FB	F5
t _{CK} Clock Cycle Time (min)	CL = 4	4.0 ns	4.5 ns	5.0 ns
	CL = 5	3.33 ns	3.75 ns	4.5 ns
	CL = 6	3.0ns	3.33 ns	4.0 ns
t _{RC} Random Read/Write Cycle Time (min)		20.0 ns	22.5 ns	25 ns
t _{RAC} Random Access Time (min)		20.0 ns	22.5 ns	25 ns
I _{DD1S} Operating Current (single bank) (max)		TBD	TBD	TBD
I _{DD2S} Power Down Current (max)		TBD	TBD	TBD
I _{DD3S} Self-Refresh Current (max)		TBD	TBD	TBD

- Fully Synchronous Operation
 - Double Data Rate (DDR)
 - Data input/output are synchronized with both edges of DS / QS.
 - Differential Clock (CLK and CLK) inputs
 - CS, FN and all address input signals are sampled on the positive edge of CLK.
 - Output data (DQs and QS) is aligned to the crossings of CLK and CLK.
- Fast clock cycle time of 3.0 ns minimum
 - Clock : 333 MHz maximum
 - Data : 666 Mbps/pin maximum
- Quad Independent Banks operation
- Fast cycle and Short Latency
- Selectable Data Strobe(Uni/Bi-directional data strobe)
- Distributed Auto-Refresh cycle in 3.9us
- Self-Refresh
- Power Down Mode
- Variable Write Length Control
- Write Latency = CAS Latency-1
- Programable CAS Latency and Burst Length
 - CAS Latency = 4, 5, 6
 - Burst Length = 2,4
- Organization : 2,097,152 words x 4 banks x 36 bits
- Power Supply Voltage V_{DD} : 2.5V ± 0.125V
 - V_{DDQ} : 1.8V ± 0.1V
- 1.8V CMOS I/O comply with SSTL - 1.8 (half strength driver)
- Package : 144Ball BGA, 1mm x 0.8mm Ball pitch
- JTAG(for x36)
- Notice : Network-DRAM is trademark of Samsung Electronics., Co LTD

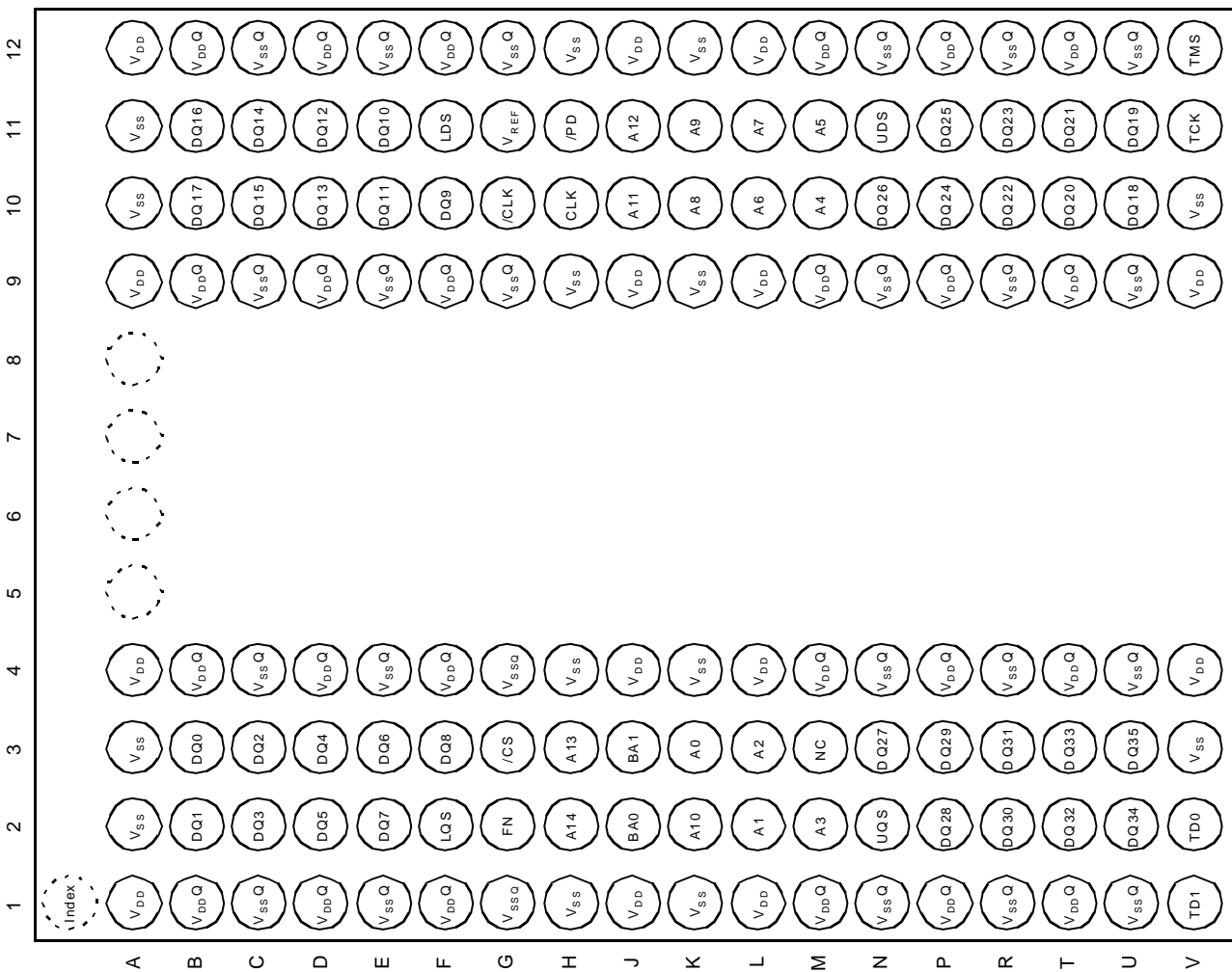
K4C89363AF

Pin Names

Pin	Name	Pin	Name
A0 ~ A14	Address Input	VDD	Power (+2.5V)
BA0, BA1	Bank Address	VSS	Ground
DQ0 ~ DQ35	Data Input/Output	VDDQ	Power (+1.8V)(for I/O buffer)
$\overline{\text{CS}}$	Chip Select	VSSQ	Ground(for I/O buffer)
FN	Function Control	VREF	Reference Voltage
$\overline{\text{PD}}$	Power Down Control	NC	No Connection
CLK, $\overline{\text{CLK}}$	Clock Input		

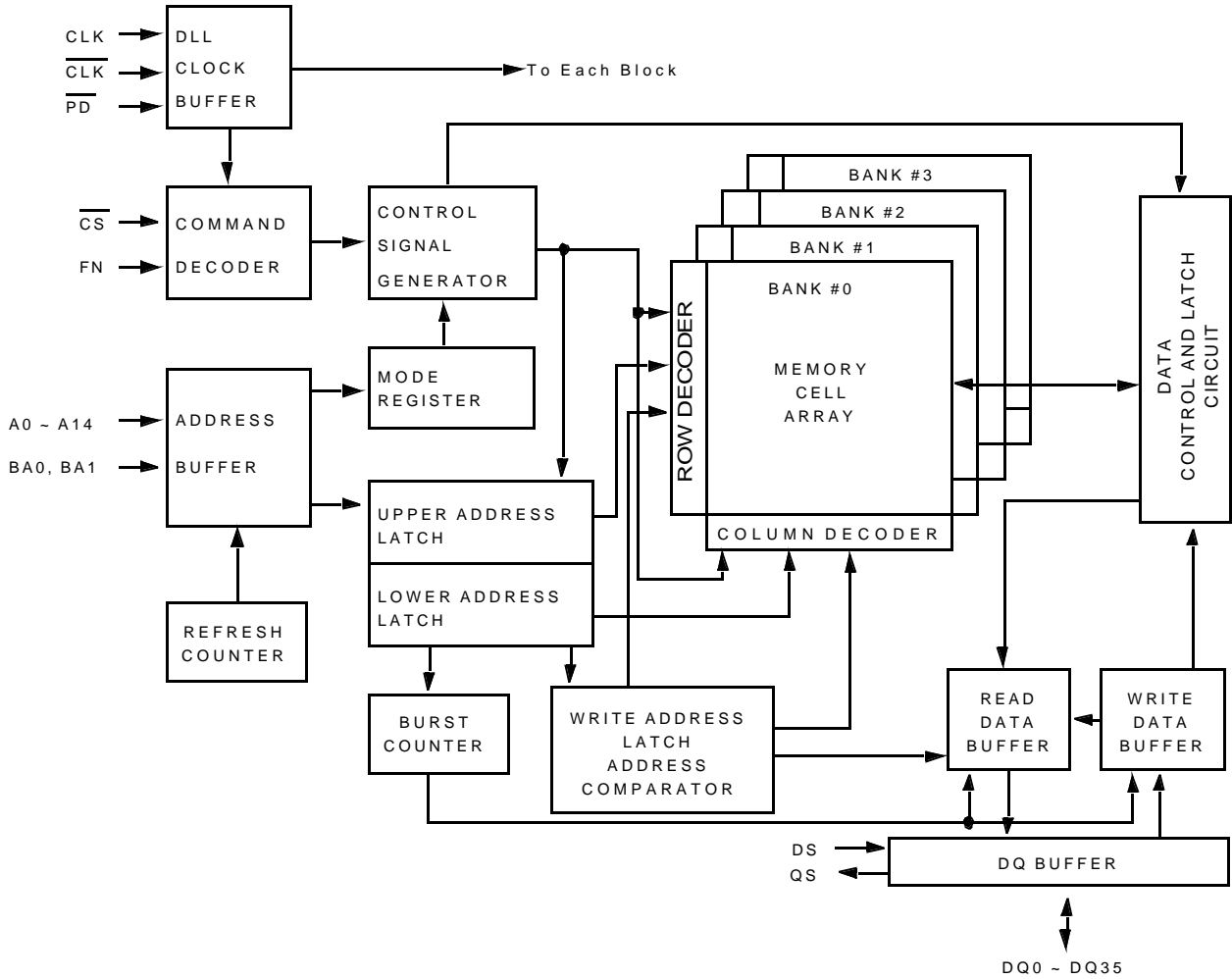
PIN ASSIGNMENT (TOP VIEW)

ball pitch=1.0 x 0.8mm



K4C89363AF

Block Diagram



Note : The K4C89363AD configuration is 4 Bank of 16384 x 128 x 36 of cell array with the DQ pins numbered DQ0~DQ35.

K4C89363AF

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V _{DD}	Power Supply Voltage	-0.3 ~ 3.3	V	
V _{DDQ}	Power Supply Voltage (for I/O buffer)	-0.3 ~ V _{DD} + 0.3	V	
V _{IN}	Input Voltage	-0.3 ~ V _{DD} + 0.3	V	
V _{OUT}	DQ pin Voltage	-0.3 ~ V _{DDQ} + 0.3	V	
V _{REF}	Input Reference Voltage	-0.3 ~ V _{DDQ} + 0.3	V	
T _{OPR}	Operating Temperature	0 ~ 70	°C	
T _{STG}	Storage Temperature	-55 ~ 150	°C	
T _{SOLDER}	Soldering Temperature(10s)	260	°C	
P _D	Power Dissipation	2	W	
I _{OUT}	Short Circuit Output Current	± 50	mA	

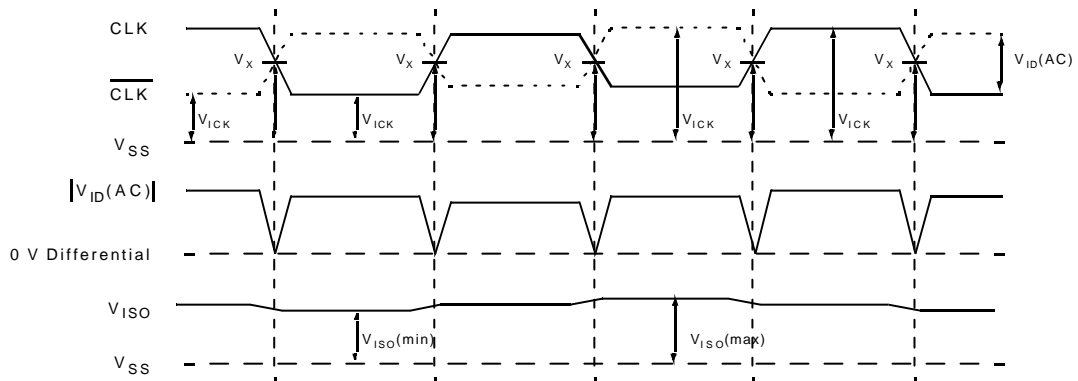
Caution : Conditions outside the limits listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may affect device reliability.

Recommended DC,AC Operating Conditions (Notes : 1) (T_a = 0 ~ 70 °C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V _{DD}	Power Supply Voltage	2.375	2.5	2.625	V	
V _{DDQ}	Power Supply Voltage (for I/O Buffer)	1.7	1.8	1.9	V	
V _{REF}	Input Reference Voltage	V _{DDQ} /2x96%	V _{DDQ} /2	V _{DDQ} /2x105%	V	2
V _{IH} (DC)	Input DC high Voltage	V _{REF} +0.125	-	V _{DDQ} +0.2	V	5
V _{IL} (DC)	Input DC Low Voltage	-0.1	-	V _{REF} -0.125	V	5
V _{ICK} (DC)	Differential Clock DC Input Voltage	-0.1	-	V _{DDQ} +0.1	V	10
V _{ID} (DC)	Input Differential Voltage. CLK and CLK Inputs (DC)	0.4	-	V _{DDQ} +0.2	V	7,10
V _{IH} (AC)	Input AC High Voltage	V _{REF} +0.2	-	V _{DDQ} +0.2	V	3,6
V _{IL} (AC)	Input AC Low Voltage	-0.1	-	V _{REF} -0.2	V	4,6
V _{ID} (AC)	Input Differential Voltage. CLK and CLK Inputs (AC)	0.55	-	V _{DDQ} +0.2	V	7,10
V _X (AC)	Differential AC Input Cross Point Voltage	V _{DDQ} /2-0.125	-	V _{DDQ} /2+0.125	V	8,10
V _{ISO} (AC)	Differential Clock AC Middle Level	V _{DDQ} /2-0.125	-	V _{DDQ} /2+0.125	V	9,10

K4C89363AF

- Notes:**
1. All voltages are referenced to V_{SS}, V_{SSQ}.
 2. V_{REF} is expected to track variations in V_{DDQ} DC level of the transmitting device.
Peak to peak AC noise on V_{REF} may not exceed ± 2% of V_{REF} (DC).
 3. Overshoot limit : V_{IH(max.)} = V_{DDQ} + 0.7V with a pulse width ≤ 5ns
 4. Undershoot limit : V_{IL(min.)} = -0.7V with a pulse width ≤ 5ns
 5. V_{IH(DC)} and V_{IL(DC)} are levels to maintain the current logic state.
 6. V_{IH(AC)} and V_{IL(AC)} are levels to change to the new logic state.
 7. V_{ID} is magnitude of the difference between CLK input level and $\overline{\text{CLK}}$ input level.
 8. The value of V_{x(AC)} is expected to equal V_{DDQ}/2 of the transmitting device.
 9. V_{ISO} means [V_{ICK(CLK)} + V_{ICK(CLK)}]/2
 10. Refer to the figure below.



11. In the case of external termination, VTT(Termination Voltage) should be gone in the range of V_{REF}(DC) ± 0.04V.

Pin Capacitance (V_{DD} = 2.5V, V_{DDQ} = 1.8V, f = 1 MHz, Ta = 25 °C)

Symbol	Parameter	Min	Max	Delts	Units
C _{IN}	Input Pin Capacitance	1.5	2.5	0.25	pF
C _{INC}	Clock Pin (CLK, $\overline{\text{CLK}}$) Capacitance	1.5	2.5	0.25	pF
C _{I/O}	DQ, DS, QS Capacitance	2.5	3.5	0.5	pF
C _{NC}	NC Pin Capacitance	-	1.5	-	pF

Note : These parameters are periodically sampled and not 100% tested.

K4C89363AF

DC Characteristics and Operating Conditions (V_{DD} = 2.5V ± 0.125V, V_{DDQ} = 1.8V ± 0.1V, T_a = 0~70 °C)

Parameter	Symbol	Max			Units	Notes
		F6	FB	F5		
Operating Current t _{CK} = min, I _{RC} = min Read/Write command cycling 0V <= V _{IN} <= V _{IL(AC)} (max.) V _{IH(AC)} (min.) <= V _{IN} <= V _{DDQ} 1 bank operation, Burst Length = 4 Address change up to 2 times during minimum I _{RC} .	I _{DD1S}	TBD	TBD	TBD	mA	1, 2
Standby Current t _{CK} = min, CS = V _{IH} , PD = V _{IH} . 0V <= V _{IN} <= V _{IL(AC)} (max.) V _{IH(AC)} (min.) <= V _{IH} <= V _{DDQ} All Banks : inactive state Other input signals are changed one time during 4*t _{CK}	I _{DD2N}	TBD	TBD	TBD		1
Standby (Power Down) Current t _{CK} = min, CS = V _{IH} , PD = V _{IL} (Power Down) 0V <= V _{IN} <= V _{DDQ} All Banks : inactive state	I _{DD2P}	TBD	TBD	TBD		1
Auto-Refresh Current t _{CK} = min, I _{REFC} = min, t _{REFI} = min Auto-Refresh command cycling 0V <= V _{IN} <= V _{IL(AC)} (max.), V _{IH(AC)} (min.) <= V _{IN} <= V _{DDQ} Address change up to 2 times during minimum I _{REFC} .	I _{DD5}	TBD	TBD	TBD		1
Self-Refresh Current Self-Refresh mode PD = 0.2V, 0V <= V _{IN} <= V _{DDQ}	I _{DD6}	TBD	TBD	TBD		

Parameter	Symbol	Min	Max	Unit	Notes	
Input Leakage Current (0V <= V _{IN} <= V _{DDQ} , All other pins not under test = 0V)	I _{LI}	-5	5	uA		
Output Leakage Current (Output disabled, 0V <= V _{OUT} <= V _{DDQ})	I _{LO}	-5	5	uA		
V _{REF} Current	I _{REF}	-5	5	uA		
Normal Output Driver	Output Source DC Current V _{DDQ} = 1.7V / V _{OH} = 1.420V	I _{OH} (DC)	-5.6	-	mA	3
	Output Sink DC Current V _{DDQ} = 1.7V / V _{OL} = 0.280V	I _{OL} (DC)	5.6	-		3
Strong Output Driver	Output Source DC Current V _{DDQ} = 1.7V / V _{OH} = 1.420V	I _{OH} (DC)	-9.8	-		3
	Output Sink DC Current V _{DDQ} = 1.7V / V _{OL} = 0.280V	I _{OL} (DC)	9.8	-		3
Weak Output Driver	Output Source DC Current V _{DDQ} = 1.7V / V _{OH} = 1.420V	I _{OH} (DC)	-2.8	-		3
	Output Sink DC Current V _{DDQ} = 1.7V / V _{OL} = 0.280V	I _{OL} (DC)	2.8	-		3

- Notes : 1. These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK}, t_{RC} and I_{RC}.
 2. These parameters depend on the output loading. The specified values are obtained with the output open.
 3. Refer to output driver characteristics for the detail. Output Driver Strength is selected by Extended Mode Register.

K4C89363AF

AC Characteristics and Operating Conditions (Notes : 1, 2)

Symbol	Parameter	F6		FB		F5		Units	Notes	
		Min	Max	Min	Max	Min	Max			
t _R RC	Random Cycle Time	20.0	-	22.5	-	25	-	ns	3	
t _{CK}	Clock Cycle Time	C _L = 4	4.0	7.5	4.5	7.5	5.0		7.5	3
		C _L = 5	3.33	7.5	3.75	7.5	4.5		7.5	3
		C _L = 6	3.0	7.5	3.33	7.5	4.0		7.5	3
t _R AC	Random Access Time	-	20.0	-	22.5	-	25		3	
t _{CH}	Clock High Time	0.45*t _{CK}	-	0.45*t _{CK}	-	0.45*t _{CK}	-		3	
t _{CL}	Clock Low Time	0.45*t _{CK}	-	0.45*t _{CK}	-	0.45*t _{CK}	-		3	
t _{CK} QS	QS Access Time from CLK	-0.45	0.45	-0.45	0.45	-0.5	0.5		3, 8	
t _Q SQ	Data Output Skew from QS	-	0.2	-	0.25	-	0.3		4	
t _{AC}	Data Access Time from CLK	-0.5	0.5	-0.5	0.5	-0.6	0.6		3, 8	
t _{OH}	Data Output Hold Time from CLK	-0.5	0.5	-0.5	0.5	-0.6	0.6		3, 8	
t _{HP}	CLK half period (minium of Actual t _{CH} , t _{CL})	min(t _{CH} , t _{CL})	-	min(t _{CH} , t _{CL})	-	min(t _{CH} , t _{CL})	-		3	
t _Q SP	QS(Read) Pulse Width	t _{HP} -t _Q HS	-	t _{HP} -t _Q HS	-	t _{HP} -t _Q HS	-		4, 8	
t _Q SQV	Data Output Valid Time from QS	t _{HP} -t _Q HS	-	t _{HP} -t _Q HS	-	t _{HP} -t _Q HS	-		4, 8	
t _Q HS	DQ, QS Hold skew factor	-	0.055x t _{CK} +0.17	-	0.055x t _{CK} +0.17	-	0.055x t _{CK} +0.17			
t _D QSS	DS(Write) Low to High Setup Time	0.8*t _{CK}	1.2*t _{CK}	0.8*t _{CK}	1.2*t _{CK}	0.8*t _{CK}	1.2*t _{CK}		3	
t _D SPRE	DS(Write) Preamble Pulse Width	0.4*t _{CK}	-	0.4*t _{CK}	-	0.4*t _{CK}	-		4	
t _D SPRES	DS First Input Setup Time	0	-	0	-	0	-		3	
t _D SPREH	DS First Low Input Hold Time	0.3*t _{CK}	-	0.3*t _{CK}	-	0.3*t _{CK}	-		3	
t _D SP	DS High or Low Input Pulse Width	0.45*t _{CK}	0.55*t _{CK}	0.45*t _{CK}	0.55*t _{CK}	0.45*t _{CK}	0.55*t _{CK}		4	
t _D SS	DS Input Falling Edge to Clock Setup Time	C _L = 4	0.9	-	0.9	-	1.0		-	3, 4
		C _L = 5	0.9	-	0.9	-	1.0	-	3, 4	
		C _L = 6	0.9	-	0.9	-	1.0	-	3, 4	
t _D SPST	DS(Write) Postamble Pulse Width	0.45*t _{CK}	-	0.45*t _{CK}	-	0.45*t _{CK}	-	4		
t _D SPSTH	DS(Write) Postamble Hold Time	C _L = 4	0.9	-	0.9	-	1.0	-	3, 4	
		C _L = 5	0.9	-	0.9	-	1.0	-	3, 4	
		C _L = 6	0.9	-	0.9	-	1.0	-	3, 4	
t _D S	Data Input Setup Time from DS	0.3	-	0.35	-	0.4	-	4		
t _D H	Data Input Hold Time from DS	0.3	-	0.35	-	0.4	-	4		
t _I S	Command / Address Input Setup Time	0.6	-	0.6	-	0.7	-	3		
t _I H	Command / Address Input Hold Time	0.6	-	0.6	-	0.7	-	3		

K4C89363AF

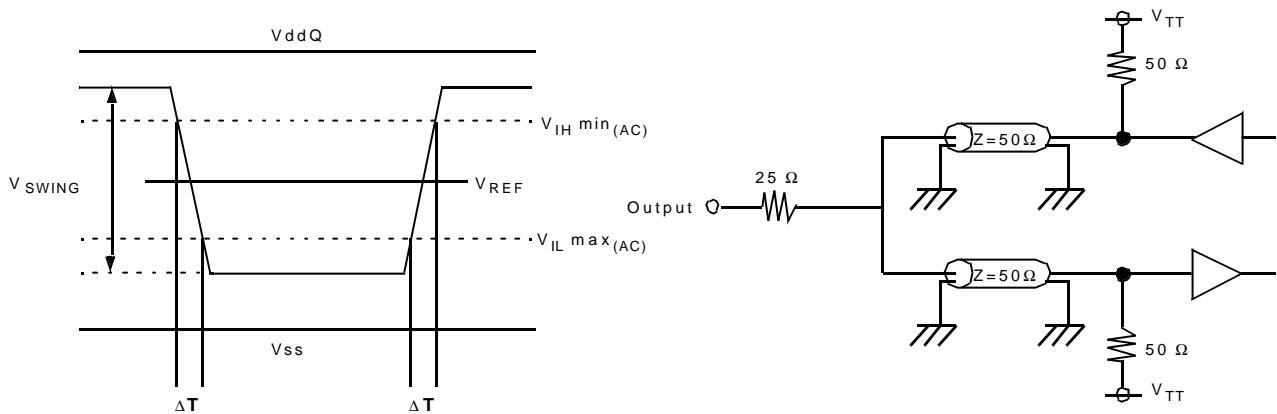
AC Characteristics and Operating Conditions (Notes : 1, 2) (Continued)

Symbol	Parameter	F6		FB		F5		Units	Notes
		Min	Max	Min	Max	Min	Max		
tLZ	Data-out Low Impedance Time from CLK	-0.5	-	-0.5	-	-0.6	-		3, 6, 8
tHZ	Data-out High Impedance Time from CLK	-	0.5	-	0.5	-	0.6		3, 7, 8
tQPDH	Last Output to PD High Hold Time	0	-	0	-	0	-		
tPDEX	Power Down Exit Time	0.6	-	0.6	-	0.7	-		3
tT	Input Transition Time	0.1	1	0.1	1	0.1	1		
tFPDL	PD Low Input Window for Self-Refresh Entry	$-0.5 \cdot t_{CK}$	5	$-0.5 \cdot t_{CK}$	5	$-0.5 \cdot t_{CK}$	5		3
tREFI	Auto-Refresh Average Interval	0.4	3.9	0.4	3.9	0.4	3.9	us	5
tPAUSE	Pause Time after Power-up	200	-	200	-	200	-		
tRC	Random Read/Write Cycle Time (Applicable to Same Bank)	C _L = 4	5	-	5	-	5	-	
		C _L = 5	6	-	6	-	6	-	
		C _L = 6	7	-	7	-	7	-	
tRCD	RDA/WRA to LAL Command Input Delay (Applicable to Same Bank)	1	1	1	1	1	1		
tRAS	LAL to RDA/WRA Command Input Delay (Applicable to Same Bank)	C _L = 4	4	-	4	-	4	-	
		C _L = 5	5	-	5	-	5	-	
		C _L = 6	6	-	6	-	6	-	
tRBD	Random Bank Access Delay (Applicable to Other Bank)	2	-	2	-	2	-		
tRWD	LAL following RDA to WRA Delay (Applicable to Other Bank)	BL = 2	2	-	2	-	2	-	
		BL = 4	3	-	3	-	3	-	
tWRD	LAL following WRA to RDA Delay (Applicable to Other Bank)	1	-	1	-	1	-		
tRSC	Mode Register Set Cycle Time	C _L = 4	7	-	7	-	7	-	Cycle
		C _L = 5	7	-	7	-	7	-	
		C _L = 6	7	-	7	-	7	-	
tPD	PD Low to Inactive State of Input Buffer	-	2	-	2	-	2		
tPDA	PD High to Active State of Input Buffer	1	-	1	-	1	-		
tPDV	Power down mode valid from REF command	C _L = 4	19	-	19	-	19	-	
		C _L = 5	23	-	23	-	23	-	
		C _L = 6	25	-	25	-	25	-	
tREFC	Auto-Refresh Cycle Time	C _L = 4	19	-	19	-	19	-	
		C _L = 5	23	-	23	-	23	-	
		C _L = 6	25	-	25	-	25	-	
tCKD	REF Command to Clock Input Disable at Self-Refresh Entry	t _{REFC}	-	t _{REFC}	-	t _{REFC}	-		
tLOCK	DLL Lock-on Time (Applicable to RDA command)	200	-	200	-	200	-		

K4C89363AF

AC Test Conditions

Symbol	Parameter	Value	Units	Notes
$V_{IH(min)}$	Input high voltage (minimum)	$V_{REF} + 0.2$	V	
$V_{IL(max)}$	Input low voltage (maximum)	$V_{REF} - 0.2$	V	
V_{REF}	Input reference voltage	$V_{ddQ}/2$	V	
V_{TT}	Termination voltage	V_{REF}	V	
V_{SWING}	Input signal peak to peak swing	0.7	V	
V_R	Differential clock input reference level	$V_{X(AC)}$	V	
$V_{ID(AC)}$	Input differential voltage	1.0	V	
SLEW	Input signal minimum slew rate	2.5	V/ns	
V_{OTR}	Output timing measurement reference voltage	$V_{ddQ}/2$	V	9



$$\text{Slew} = (V_{IH\ min(AC)} - V_{IL\ max(AC)}) / \Delta T$$

AC Test Load

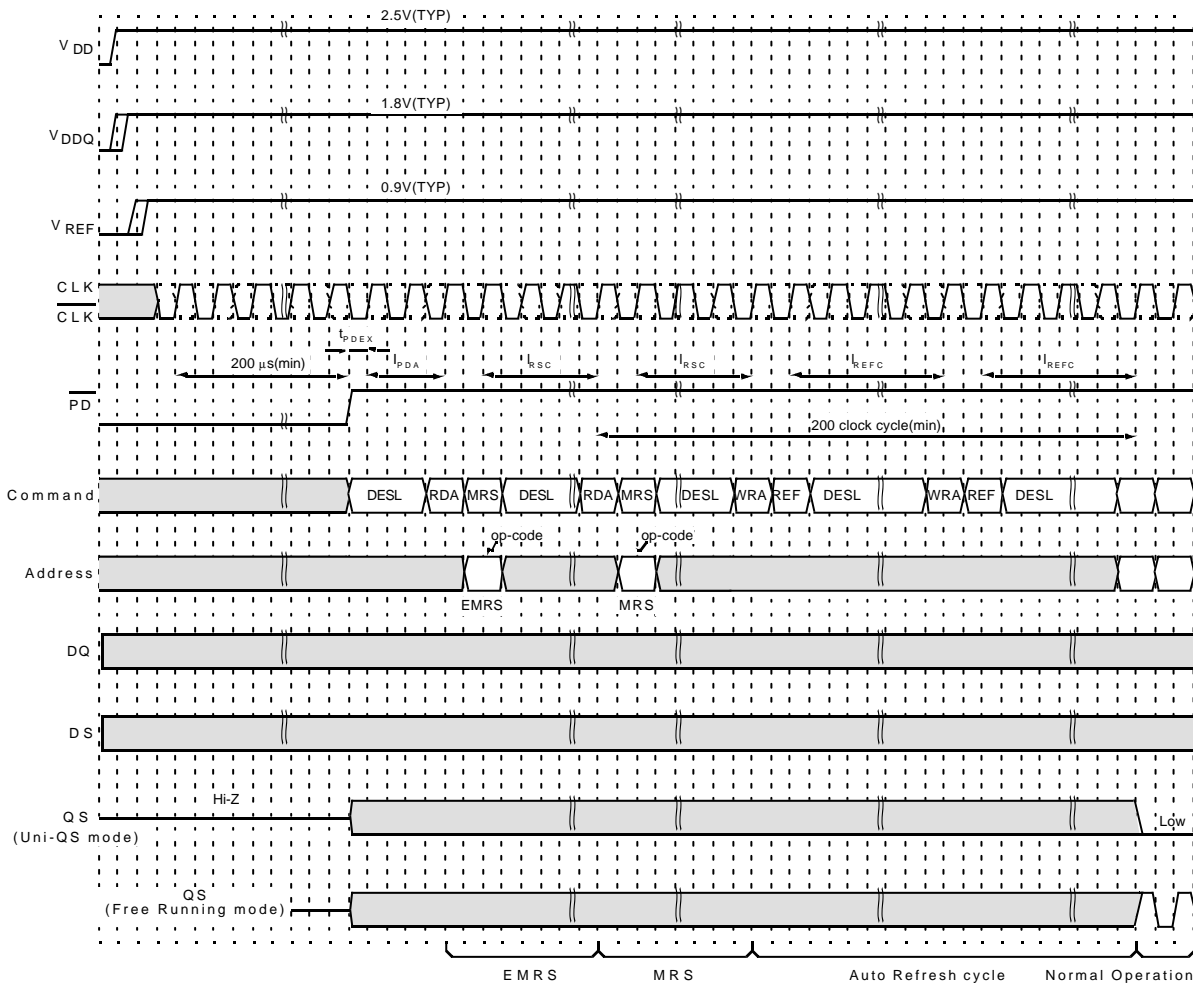
- Notes :**
- Transition times are measured between $V_{IH\ min(DC)}$ and $V_{IL\ max(DC)}$. Transition (rise and fall) of input signals have a fixed slope.
 - If the result of nominal calculation with regard to t_{CK} contains more than one decimal place, the result is rounded up to the nearest decimal place. (i.e., $t_{DQSS} = 0.8 * t_{CK}$, $t_{CK} = 3.3\text{ns}$, $0.8 * 3.3\text{ ns} = 2.64\text{ ns}$ is rounded up to 2.7 ns.)
 - These parameters are measured from the differential clock (CLK and CLK) AC cross point.
 - These parameters are measured from signal transition point of DS crossing V_{REF} level.
 - The $t_{REFI(MAX.)}$ applies to equally distributed refresh method.
The $t_{REFI(MIN.)}$ applies to both burst refresh method and distributed refresh method.
In such case, the average interval of eight consecutive Auto-Refresh commands has to be more than 400ns always. In other words, the number of Auto- Refresh cycles which can be performed within 3.2us (8X400ns) is to 8 times in the maximum.
 - Low Impedance State is specified at $V_{ddQ}/2 \pm 0.2\text{V}$ from steady state.
 - High Impedance State is specified where output buffer is no longer driven.
 - These parameters depend on the clock jitter. These parameters are measured at stable clock.
 - Output timing is measured by using Normal driver strength.

K4C89363AF

Power Up Sequence

1. As for \overline{PD} , being maintained by the low state ($\leq 0.2V$) is desirable before a power-supply injection.
2. Apply V_{DD} before or at the same time as V_{DDQ} .
3. Apply V_{DDQ} before or at the same time as V_{REF} .
4. Start clock (CLK, \overline{CLK}) and maintain stable condition for 200us (min.).
5. After stable power and clock, apply DESL and take $\overline{PD} = H$.
6. Issue EMRS to enable DLL and to define driver strength and data strobe type. (Note : 1)
7. Issue MRS for set CAS Latency (CL), Burst Type (BT), and Burst Length (BL). (Note : 1)
8. Issue two or more Auto-Refresh commands. (Note:1)
9. Ready for normal operation after 200 clocks from Extended Mode Register programming.

- Note :**
1. Sequence 6, 7 and 8 can be issued in random order.
 2. L=Logic Low, H = Logic High

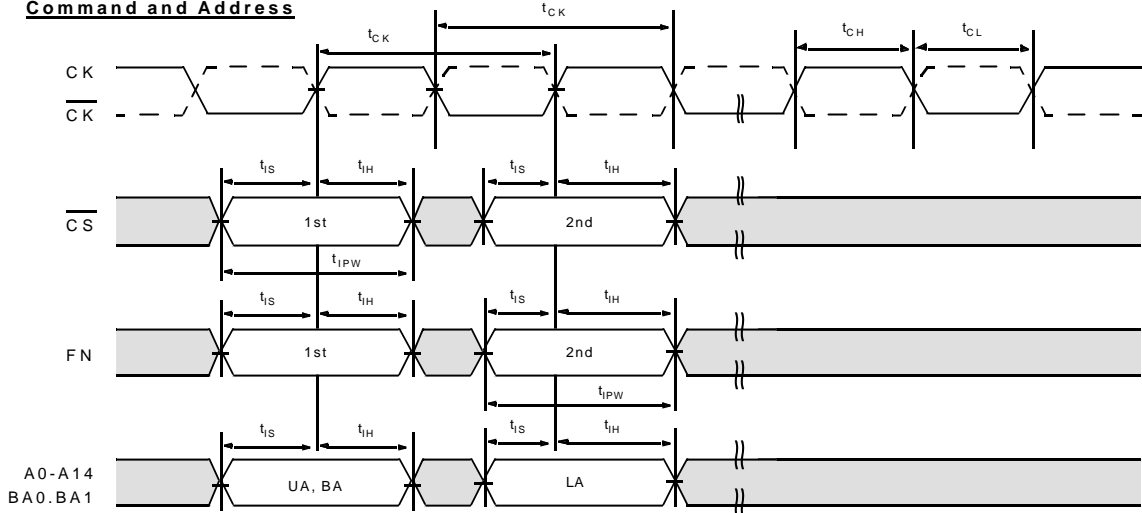


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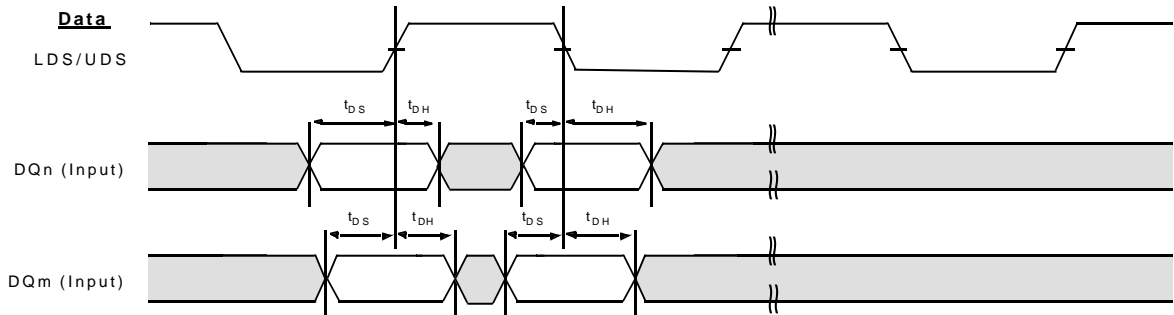
Basic Timing Diagrams

Input Timing

Command and Address

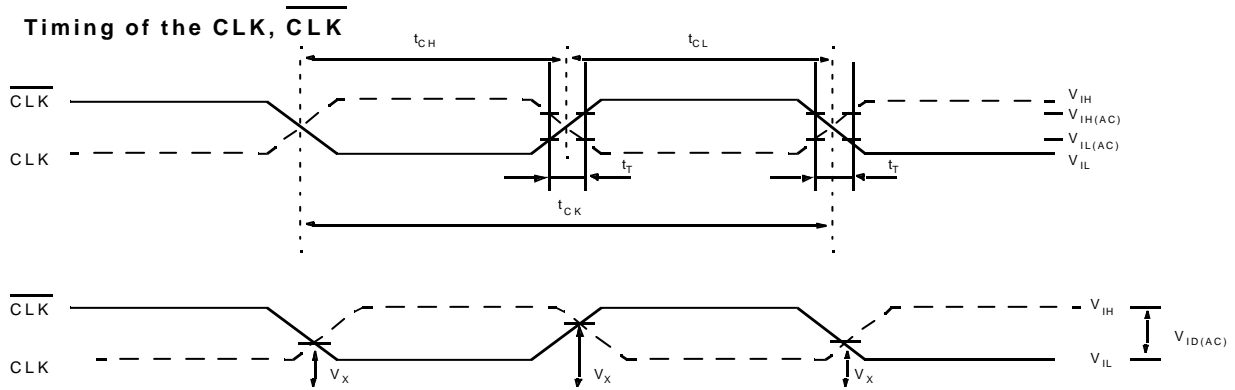


Data



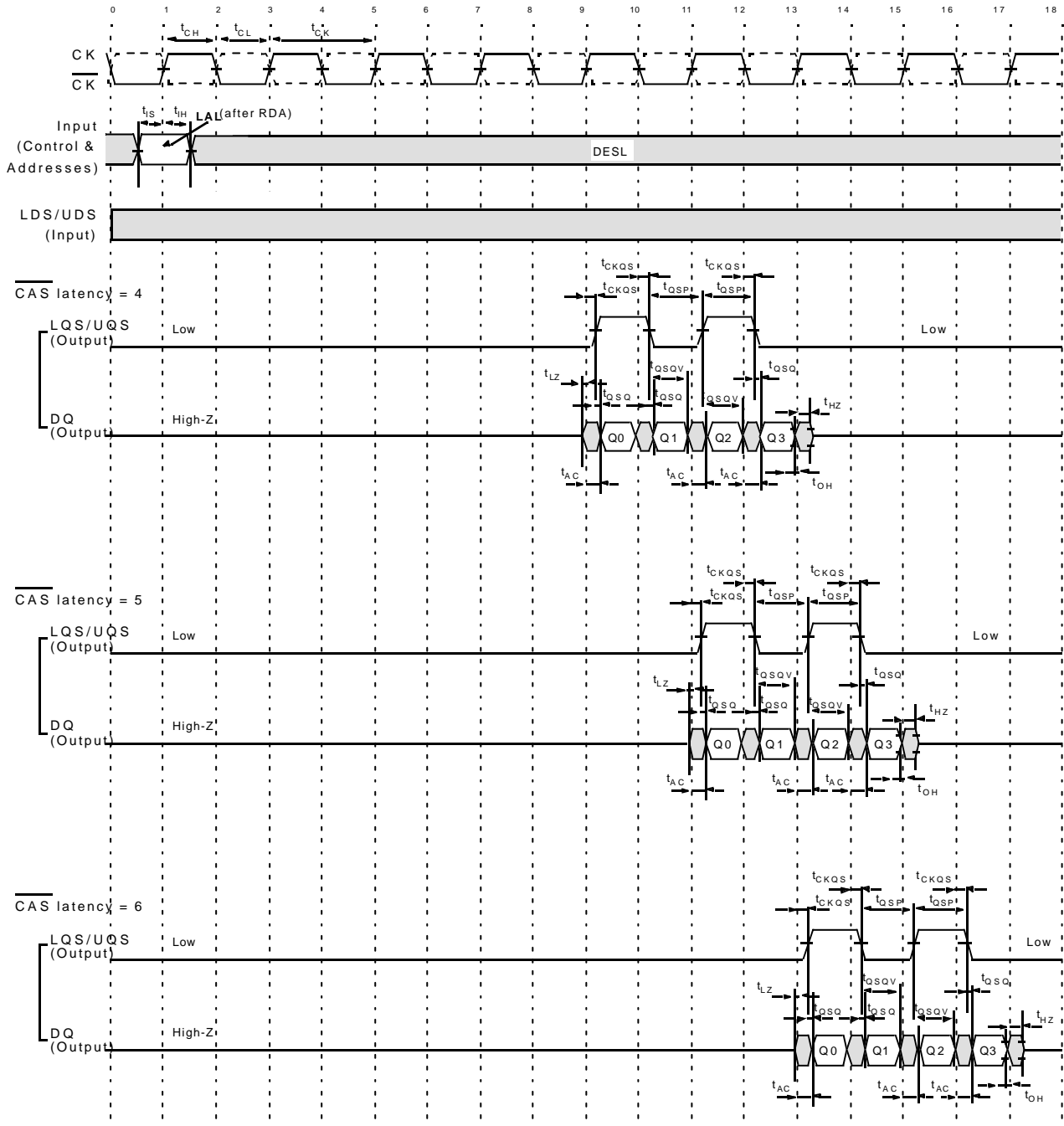
Refer to the Command Truth Table.

Timing of the CLK, \overline{CLK}



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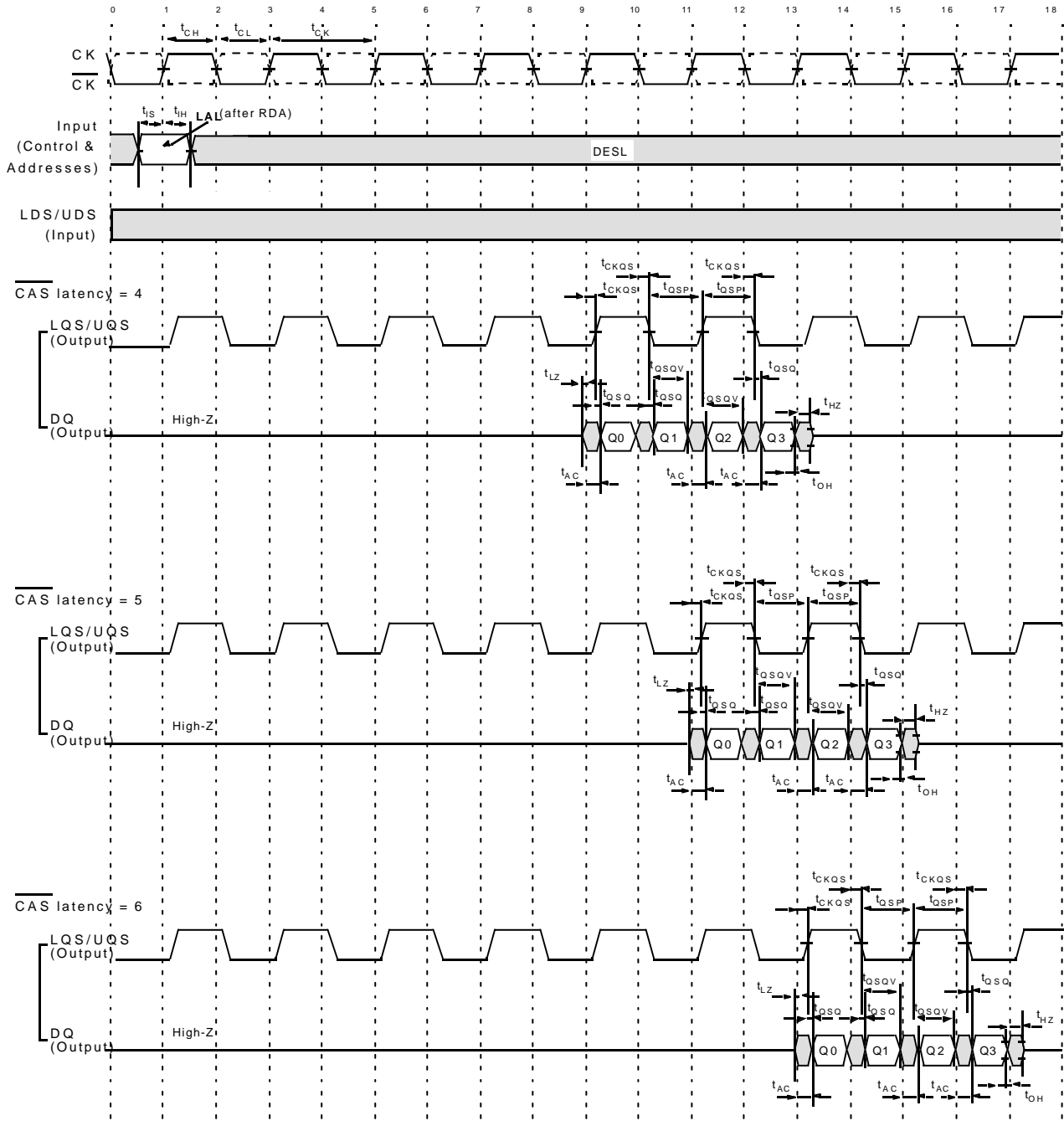
Read Timing (Burst Length = 4) Unidirectional DS/QS mode



Note : DQ0 to DQ17 are aligned with LQS.
DQ18 to DQ35 are aligned with UQS.

K4C89363AF

Read Timing (Burst Length = 4) Unidirectional DS/Free Running QS mode

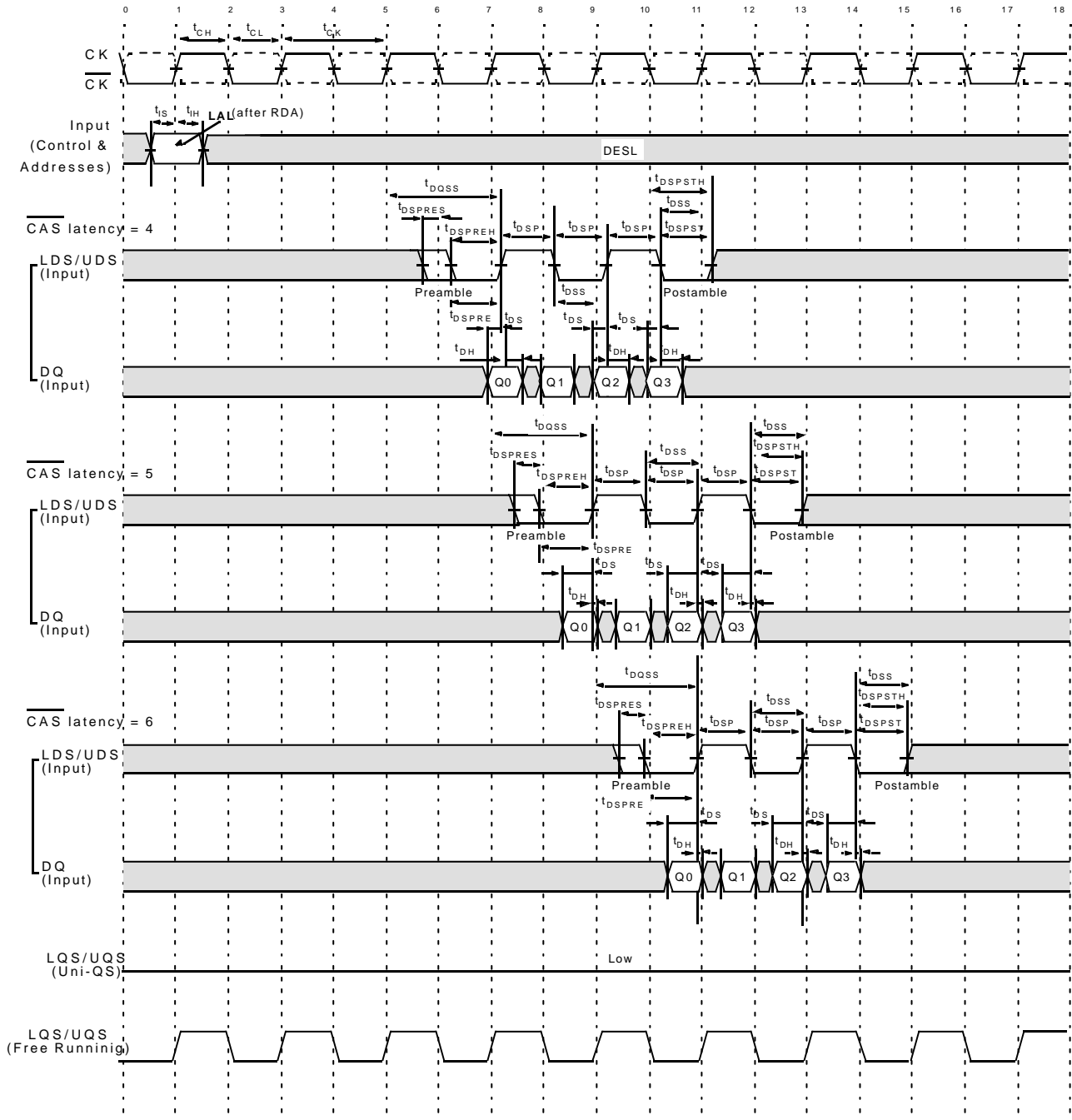


Note : DQ0 to DQ17 are aligned with LQS.
DQ18 to DQ35 are aligned with UQS.
LQS/UQS is always asserted in Free Running QS mode.

K4C89363AF

Write Timing (Burst Length = 4)

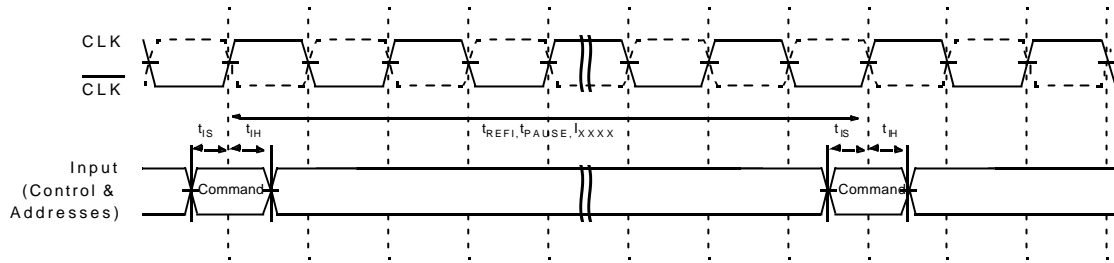
Unidirectional DS/QS mode, Unidirectional DS/Free Running QS mode



Note : DQ0 to DQ17 are sampled at both edges of LDS.
DQ18 to DQ35 are sampled at both edges of UDS.

K4C89363AF

t_{REFI} , t_{PAUSE} , t_{XXXX} Timing



Note. " t_{XXXX} " means " t_{RC} ", " t_{RCD} ", " t_{RAS} ", etc.

K4C89363AF

Function Truth Table (Notes : 1,2,3)

Command Truth Table (Notes : 4)

•The First Command

Symbol	Function	$\overline{\text{CS}}$	FN	BA1-BA0	A14-A9	A8	A7	A6-A0
DESL	Device Deselect	H	X	X	X	X	X	X
RDA	Read with Auto-close	L	H	BA	UA	UA	UA	UA
WRA	Write with Auto-close	L	L	BA	UA	UA	UA	UA

•The Second Command (The next clock of RDA or WRA command)

Symbol	Function	$\overline{\text{CS}}$	FN	BA1-BA0	A14-A13	A12-A11	A10-A9	A8	A7	A6-A0
LAL	Lower Address Latch	H	X	X	V	X	X	X	X	LA
REF	Auto-Refresh	L	X	X	X	X	X	X	X	X
MRS	Mode Register Set	L	X	V	L	L	L	L	V	V

Notes : 1. L = Logic Low, H = Logic High, X = either L or H, V = Valid (Specified Value), BA = Bank Address, UA = Upper Address, LA = Lower Address.

2. All commands are assumed to issue at a valid state.

3. All inputs for command (excluding SELFX and PDEX) are latched on the crossing point of differential clock input where CLK goes to High.

4. Operation mode is decided by the combination of 1st command and 2nd command refer to "STATE DIAGRAM" and the command table below.

Read Command Table

Command (Symbol)	$\overline{\text{CS}}$	FN	BA1-BA0	A14-A9	A8	A7	A6-A0	Notes
RDA (1st)	L	H	BA	UA	UA	UA	UA	
LAL (2nd)	H	X	X	X	X	X	LA	

Write Command Table

Command (Symbol)	$\overline{\text{CS}}$	FN	BA1-BA0	A14	A13	A12	A11	A10~A9	A8	A7	A6-A0
WRA (1st)	L	L	BA	UA	UA	UA	UA	UA	UA	UA	UA
LAL (2nd)	H	X	X	VW0	VW1	X	X	X	X	X	LA

Notes : 5. A14~A13 are used for Variable Write Length (VW) control at Write Operation.

VW Truth Table

	Function	VW0	VW1
BL = 2	Write All Words	L	X
	Write First One Word	H	X
BL = 4	Reserved	L	L
	Write All Words	H	L
	Write First Two Words	L	H
	Write First One Word	H	H

K4C89363AF

Function Truth Table (Continued)

Mode Register Set Command Truth Table

Command (Symbol)	$\overline{\text{CS}}$	FN	BA1-BA0	A14-A9	A8	A7	A6-A0	Notes
RDA (1st)	L	H	X	X	X	X	X	
MRS (2nd)	L	X	V	L	L	V	V	6

Note : 6. Refer to "Mode Register Table".

Auto-Refresh Command Table

Function	Command (Symbol)	Current State	$\overline{\text{PD}}$		$\overline{\text{CS}}$	FN	BA1-BA0	A14-A9	A8	A7	A6-A0	Notes
			n-1	n								
Active	WRA(1st)	Standby	H	H	L	L	X	X	X	X	X	
Auto-Refresh	REF(2nd)	Active	H	H	L	X	X	X	X	X	X	

Self-Refresh Command Table

Function	Command (Symbol)	Current State	$\overline{\text{PD}}$		$\overline{\text{CS}}$	FN	BA1-BA0	A14-A9	A8	A7	A6-A0	Notes
			n-1	n								
Active	WRA(1st)	Standby	H	H	L	L	X	X	X	X	X	
Self-Refresh Entry	REF(2nd)	Active	H	L	L	X	X	X	X	X	X	7, 8
Self-Refresh Continue	-	Self-Refresh	L	L	X	X	X	X	X	X	X	
Self-Refresh Exit	SELFEX	Self-Refresh	L	H	H	X	X	X	X	X	X	9

Power Down Table

Function	Command (Symbol)	Current State	$\overline{\text{PD}}$		$\overline{\text{CS}}$	FN	BA1-BA0	A14-A9	A8	A7	A6-A0	Notes
			n-1	n								
Power Down Entry	PDEN	Standby	H	L	H	X	X	X	X	X	X	8
Power Down Continue	-	Power Down	L	L	X	X	X	X	X	X	X	
Power Down Exit	PDEX	Power Down	L	H	H	X	X	X	X	X	X	9

Notes : 7. $\overline{\text{PD}}$ has to be brought to Low within t_{FDDL} from REF command.

8. $\overline{\text{PD}}$ should be brought to Low after DQ's state turned high impedance.

9. When $\overline{\text{PD}}$ is brought to High from Low, this function is executed asynchronously.

K4C89363AF

Function Truth Table (Continued)

Current State	PD		CS	FN	Address	Command	Action	Notes
	n-1	n						
Idle	H	H	H	X	X	DESL	NOP	
	H	H	L	H	BA, UA	RDA	Row activate for Read	
	H	H	L	L	BA, UA	WRA	Row activate for Write	
	H	L	H	X	X	PDEN	Power Down Entry	10
	H	L	L	X	X	-	Illegal	
	L	X	X	X	X	-	Refer to Power Down state	
Row Active for Read	H	H	H	X	LA	LAL	Begin read	
	H	H	L	X	Op-Code	MRS/EMRS	Access to Mode Register	
	H	L	H	X	X	PDEN	Illegal	
	H	L	L	X	X	MRS/EMRS	Illegal	
Row Active for Write	L	X	X	X	X	-	Invalid	
	H	H	H	X	LA	LAL	Begin Write	
	H	H	L	X	X	REF	Auto-Refresh	
	H	L	H	X	X	PDEN	Illegal	
Read	H	L	L	X	X	REF (Self)	Self-Refresh entry	
	L	X	X	X	X	-	Invalid	
	H	H	H	X	X	DESL	Continue burst read to end	
	H	H	L	H	BA, UA	RDA	Illegal	11
	H	H	L	L	BA, UA	WRA	Illegal	11
	H	L	H	X	X	PDEN	Illegal	
Write	H	L	L	X	X	-	Illegal	
	L	X	X	X	X	-	Invalid	
	H	H	H	X	X	DESL	Data write & continue burst write to end	
	H	H	L	H	BA, UA	RDA	Illegal	11
	H	H	L	L	BA, UA	WRA	Illegal	11
	H	L	H	X	X	PDEN	Illegal	
Auto-Refreshing	H	L	L	X	X	-	Illegal	
	L	X	X	X	X	-	Invalid	
	H	H	H	X	X	DESL	NOP-> Idle after t _{REFC}	
	H	H	L	H	BA, UA	RDA	Illegal	
	H	H	L	L	BA, UA	WRA	Illegal	
	H	L	H	X	X	PDEN	Self-Refresh entry	12
Mode Register Accessing	H	L	L	X	X	-	Illegal	
	L	X	X	X	X	-	Invalid	
	H	H	H	X	X	DESL	Nop-> Idle after t _{RSC}	
	H	H	L	H	BA, UA	RDA	Illegal	
	H	H	L	L	BA, UA	WRA	Illegal	
	H	L	H	X	X	PDEN	Illegal	
Power Down	H	L	L	X	X	-	Illegal	
	L	X	X	X	X	-	Invalid	
	L	L	X	X	X	-	Maintain Power Down Mode	
	L	H	H	X	X	RDEX	Exit Power Down Mode->Idle after t _{PDEX}	
Self-Refreshing	L	H	L	X	X	-	Illegal	
	H	X	X	X	X	-	Invalid	
	L	L	X	X	X	-	Maintain Self-Refresh	
	L	H	H	X	X	SELFX	Exit Self-Refresh->Idle after t _{REFC}	
	L	H	L	X	X	-	Illegal	

Notes : 10. Illegal if any bank is not idle.

11. Illegal to bank in specified states : Function may be Legal in the bank indicated by bank Address (BA).

12. Illegal if t_{FPDL} is not Satisfied.

K4C89363AF

Mode Register Table

Regular Mode Register (Notes : 1)

Address	BA1 ^{*1}	BA0 ^{*1}	A14-A8	A7 ^{*3}	A6-A4	A3	A2-A0
Register	0	0	0	TM	CL	BT	BL

A7	Test Mode (TM)
0	Regular (Default)
1	Test Mode Entry

A3	Burst Type (BT)
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency (CL)
0	0	X	Reserved ^{*2}
0	1	0	Reserved ^{*2}
0	1	1	Reserved ^{*2}
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved ^{*2}

A2	A1	A0	Burst Length (BL)
0	0	0	Reserved ^{*2}
0	0	1	2
0	1	0	4
0	1	1	Reserved ^{*2}
1	X	X	

Extended Mode Register (Notes : 4)

Address	BA1 ^{*4}	BA0 ^{*4}	A14-A7	A6-A5	A4-A3	A2-A1	A0 ^{*5}
Register	0	1	0	SS	DIC(QS)	DIC(DQ)	DS

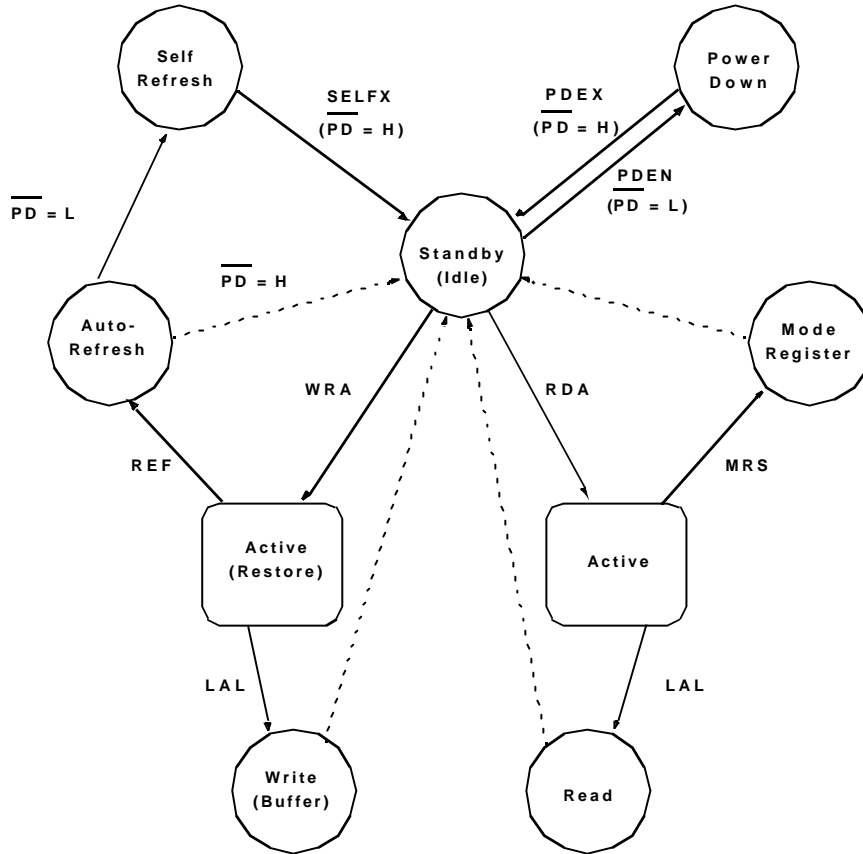
A6	A5	Strobe Select	QS		DQ		Output Driver Impedance Control (DIC)
			A4	A3	A2	A1	
0	0	Reserved ^{*2}					Normal Output Driver
0	1	Reserved ^{*2}					
1	0	Unidirectional DS/QS					Strong Output Driver
1	1	Unidirectional DS/Free Running QS					Weak Output Driver
			1	1	1	1	Reserved

- Note :**
1. Regular Mode Register Is Chosen Using the combination of BA0 = 0 and BA1 = 0.
 2. "Reserved" places in Regular Mode Register should not be set.
 3. A7 in Regular Mode Register must be set to "0"(Low state).
Because Test Mode is specific mode for supplier.
 4. Extended Mode Register is chosen using the Combination of BA0 = 1 and BA1 = 0.
 5. A0 in Extended Mode Register must be set to "0" to enable DLL for normal operation.

A0	DLL Switch (DS)
0	DLL Enable
1	DLL Disable

K4C89363AF

State Diagram



—————> Command Input

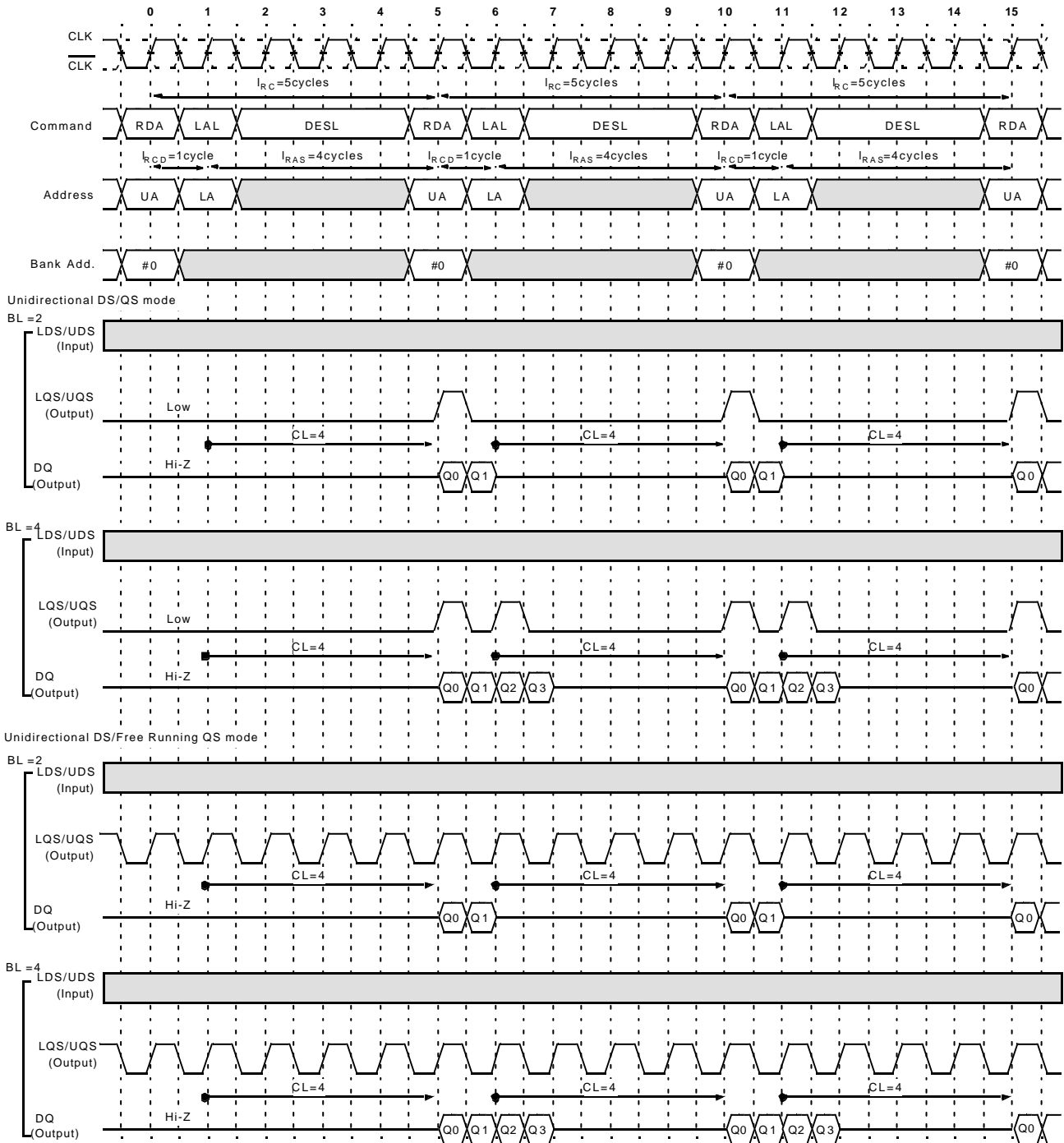
- - - - -> Automatic Return

The second command at Active state must be issued 1clock after RDA or WRA command input

K4C89363AF

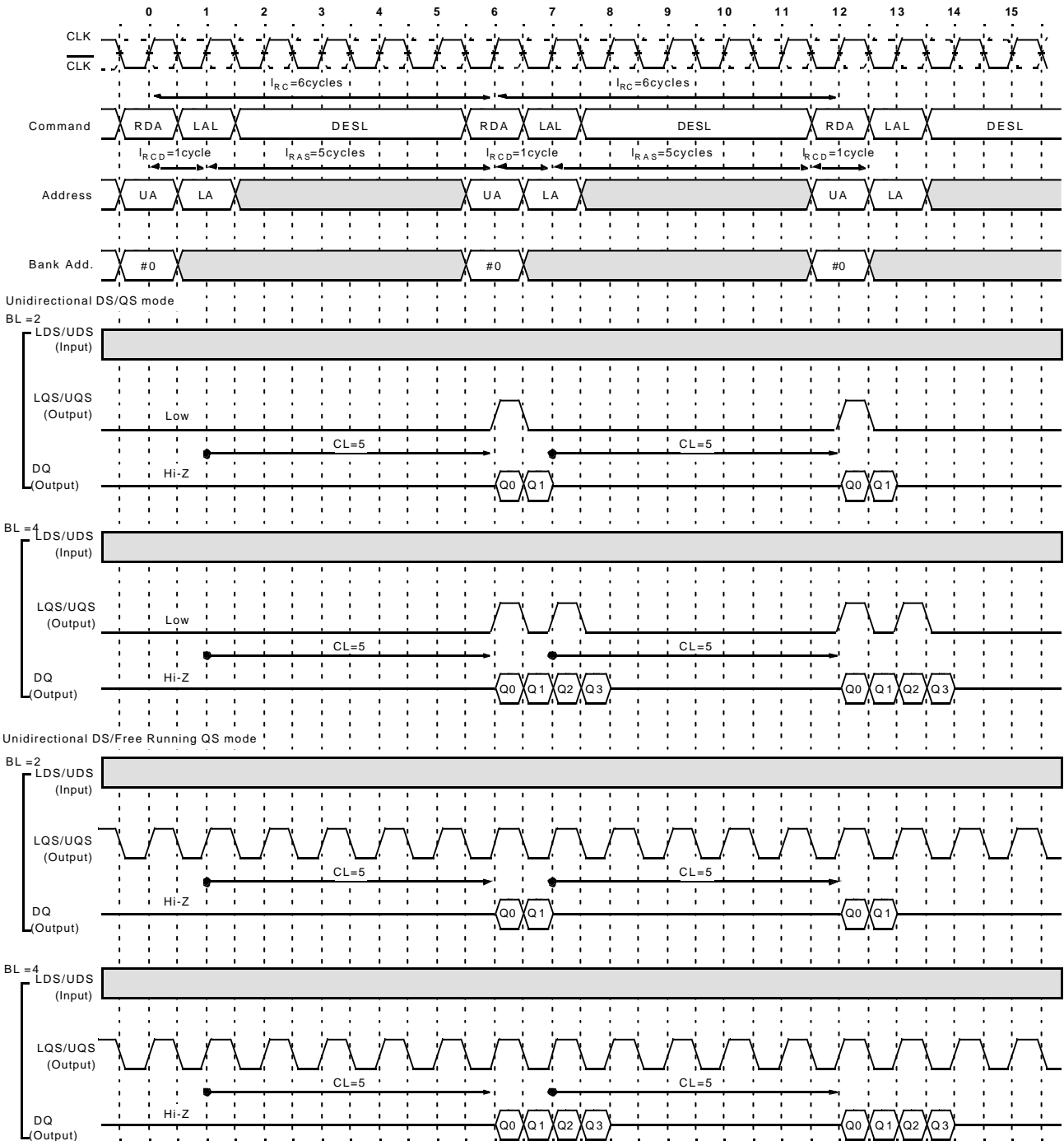
Timing Diagrams

Single Bank Read Timing (CL=4)



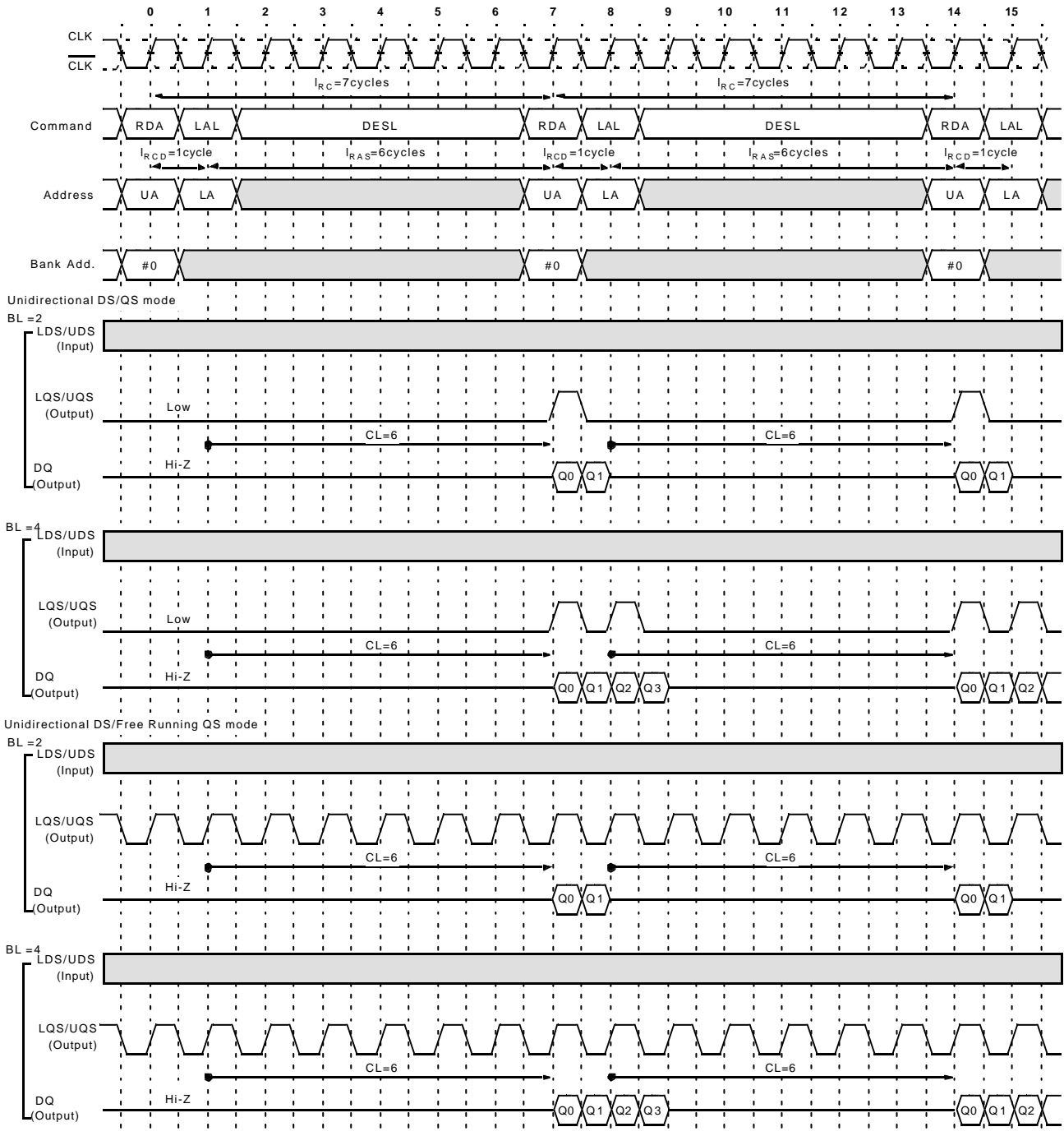
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Single Bank Read Timing (CL=5)



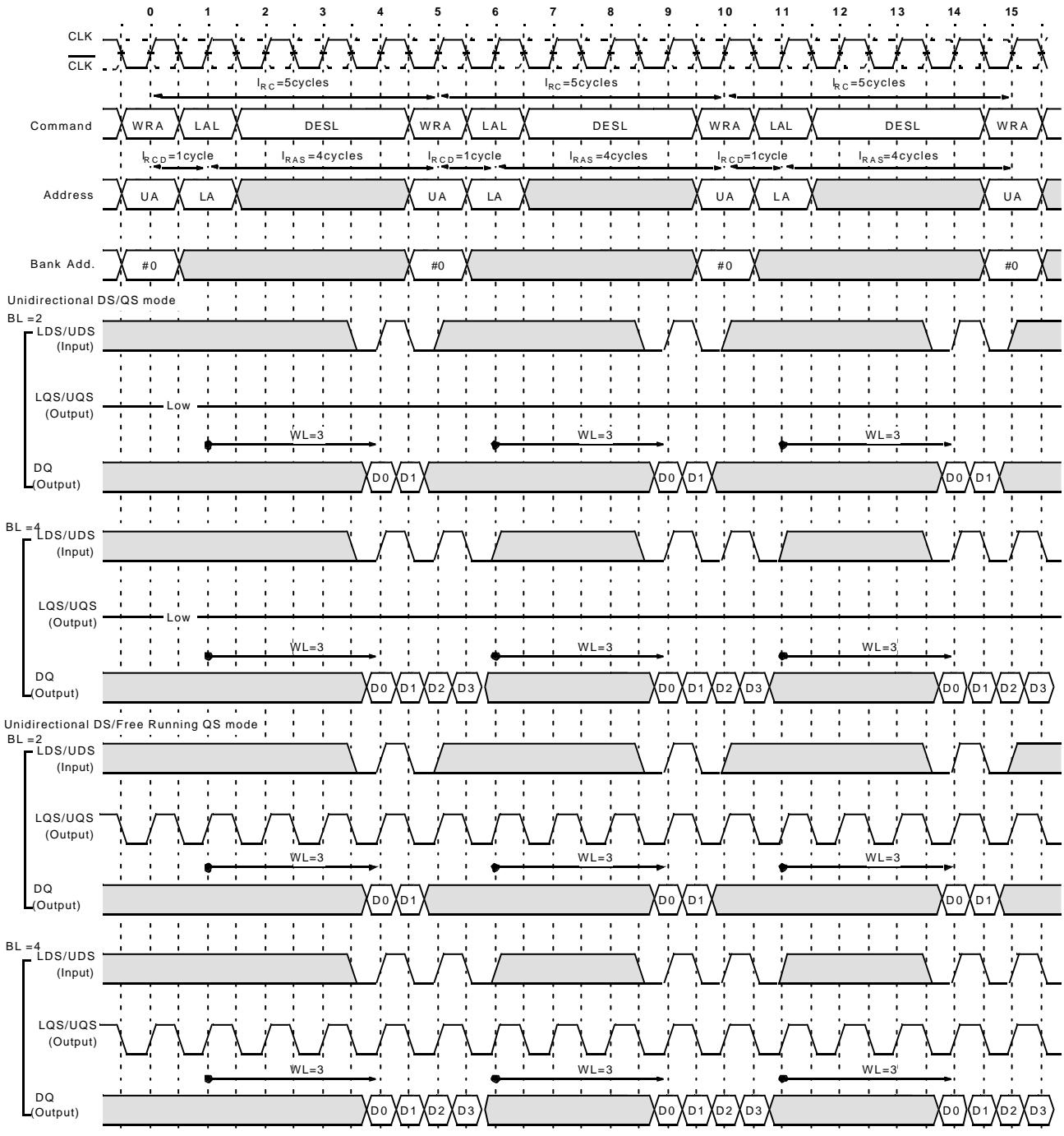
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Single Bank Read Timing (CL=6)



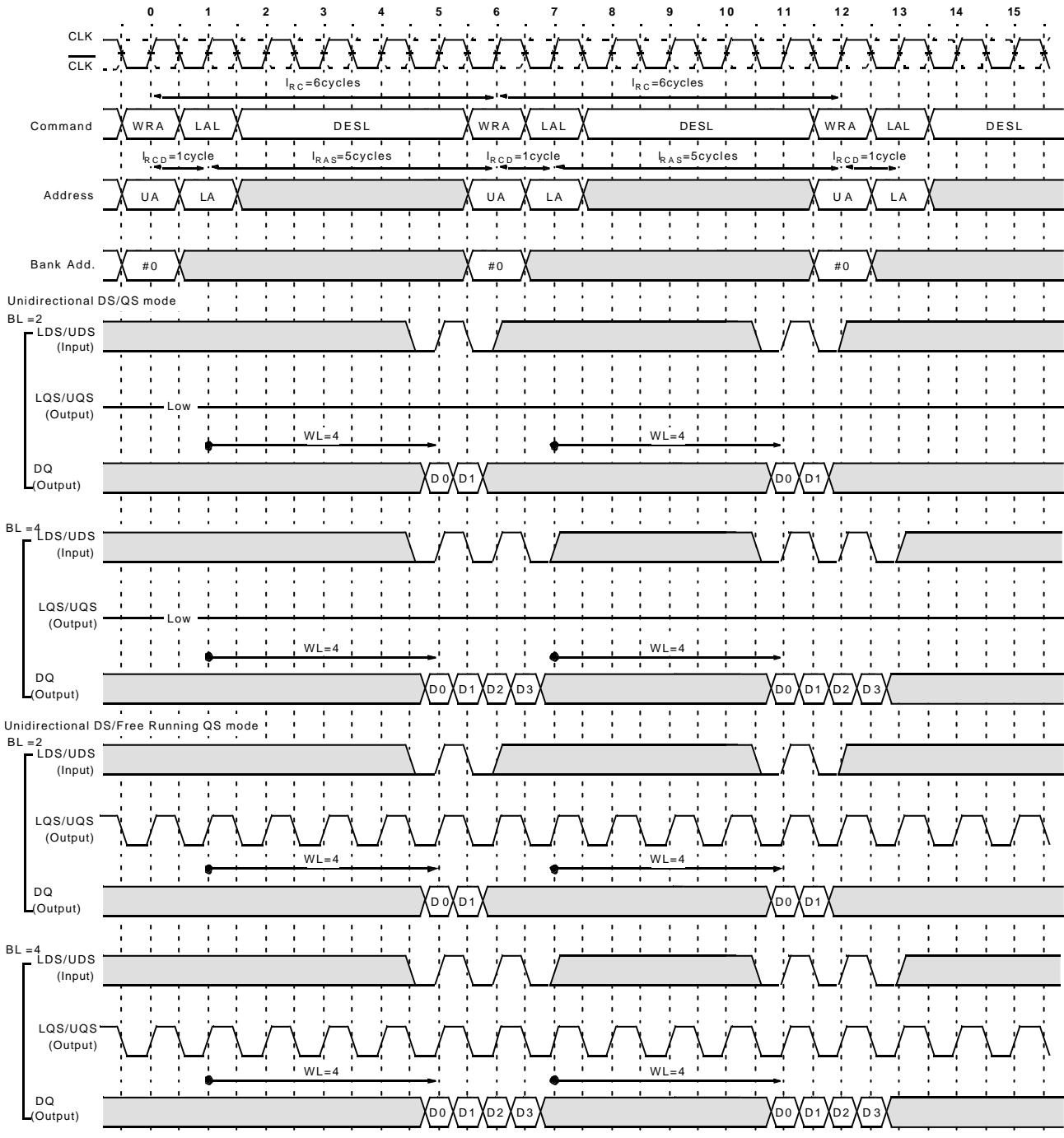
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Single Bank Write Timing (CL=4)



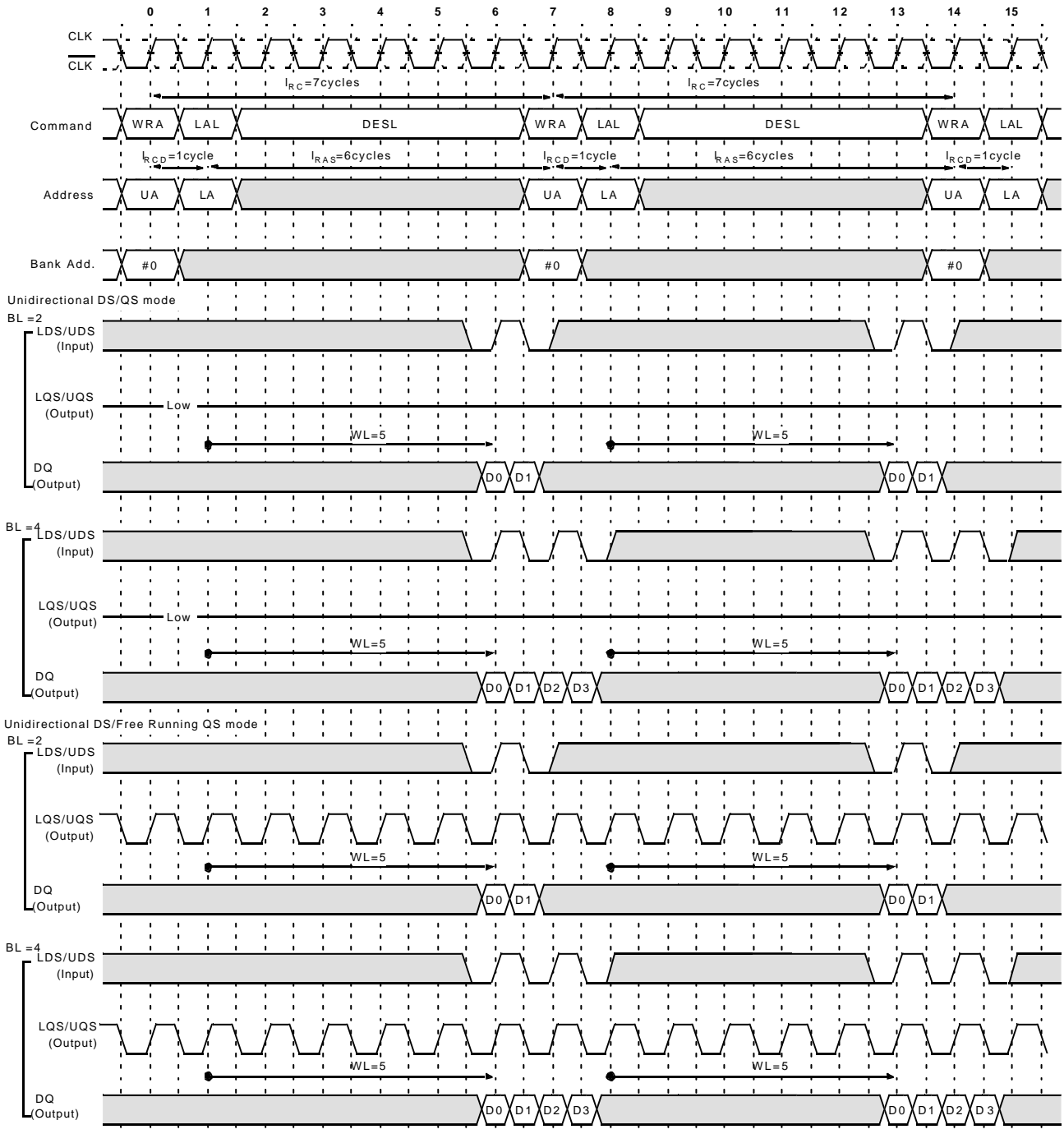
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Single Bank Write Timing (CL=5)



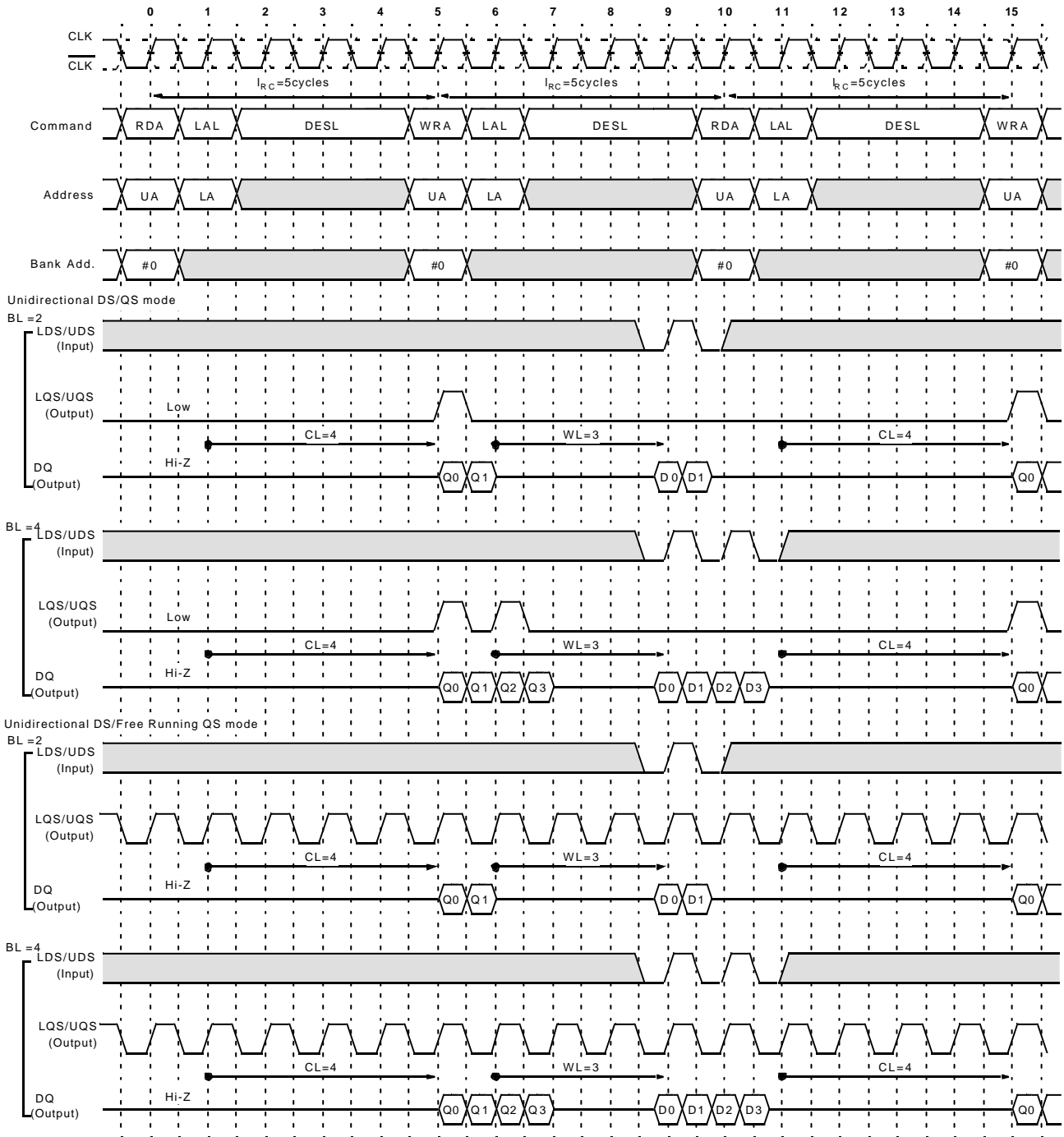
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Single Bank Write Timing (CL=6)



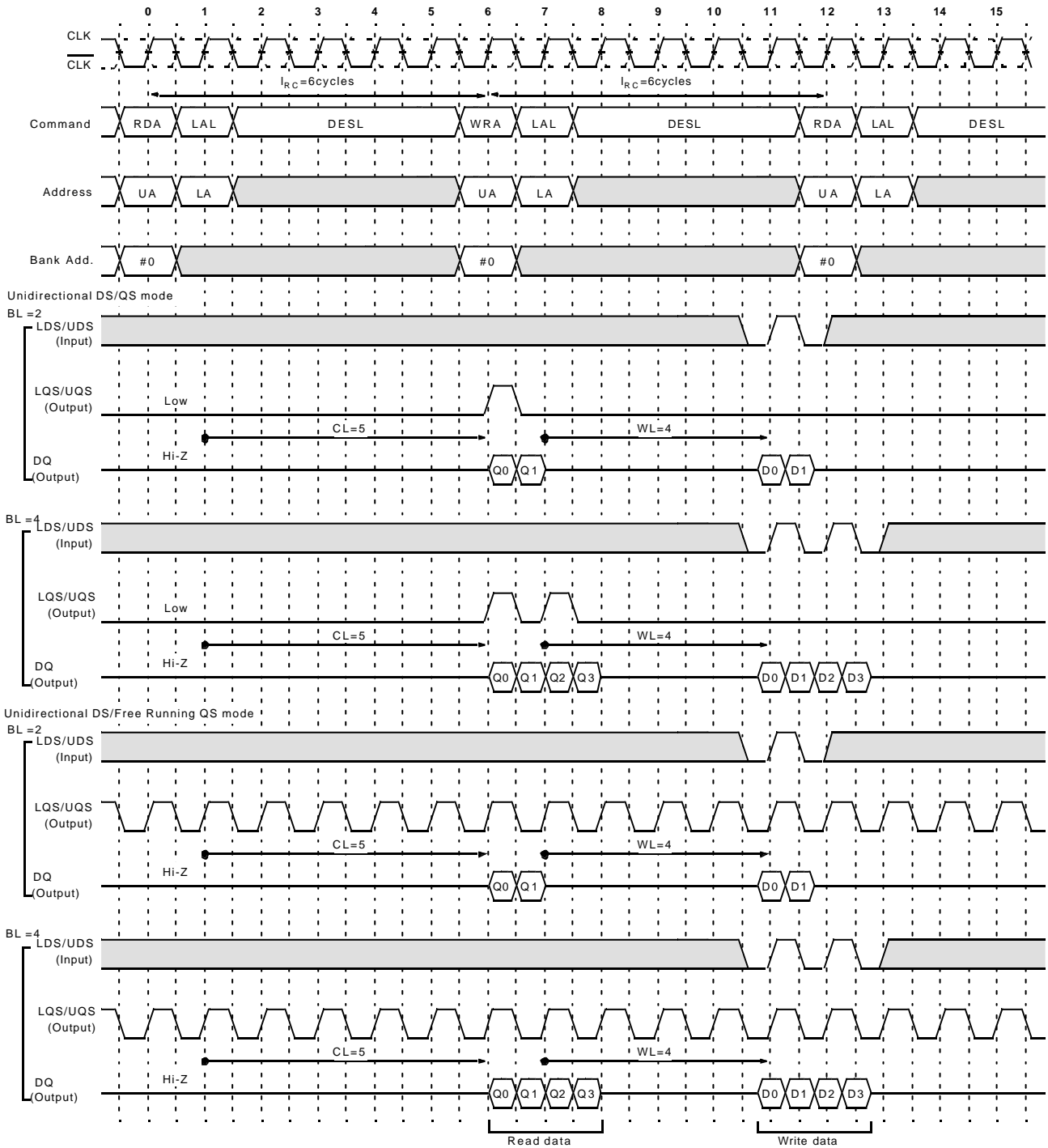
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Single Bank Read-Write Timing (CL=4)



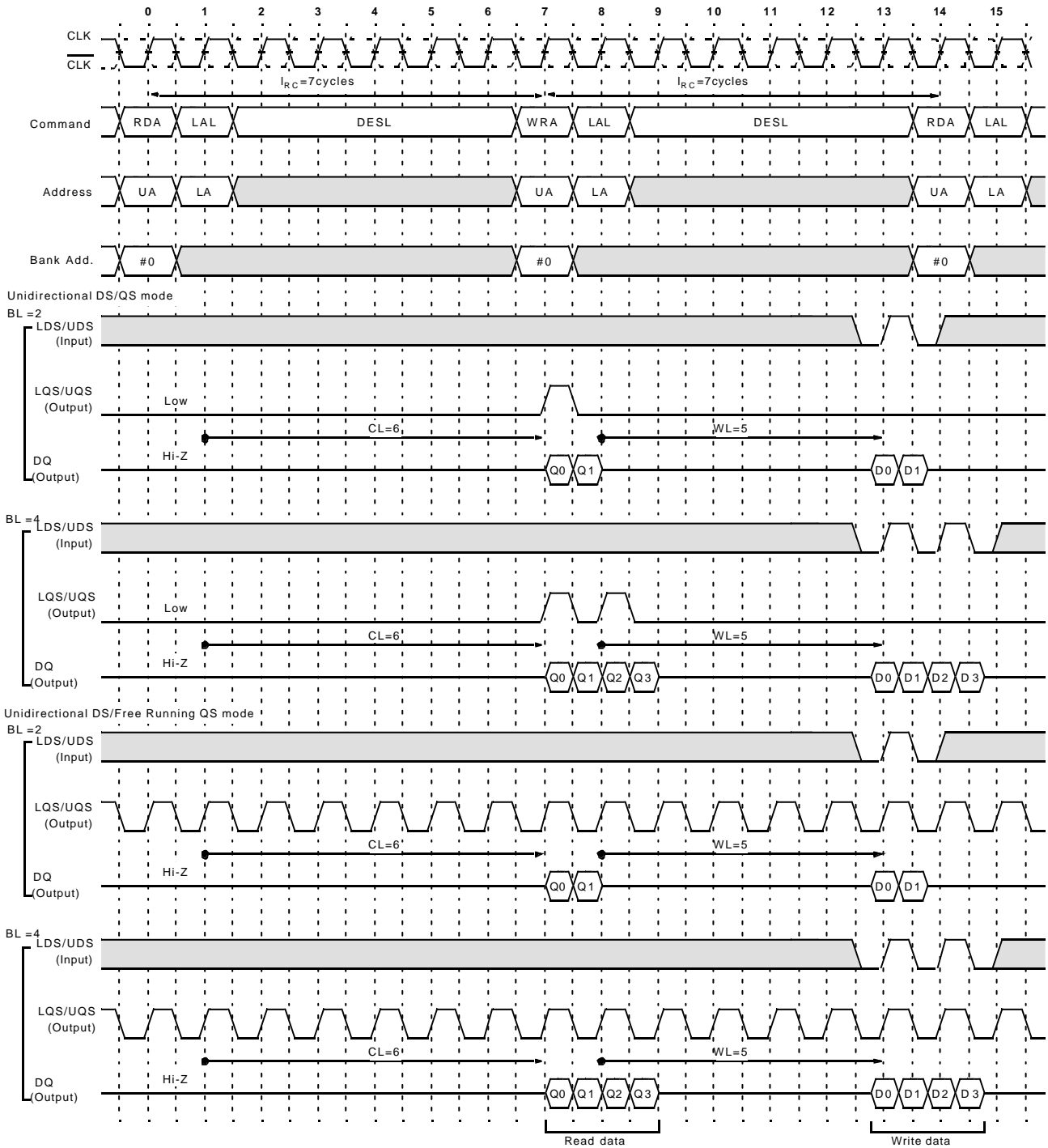
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Single Bank Read-Write Timing (CL=5)



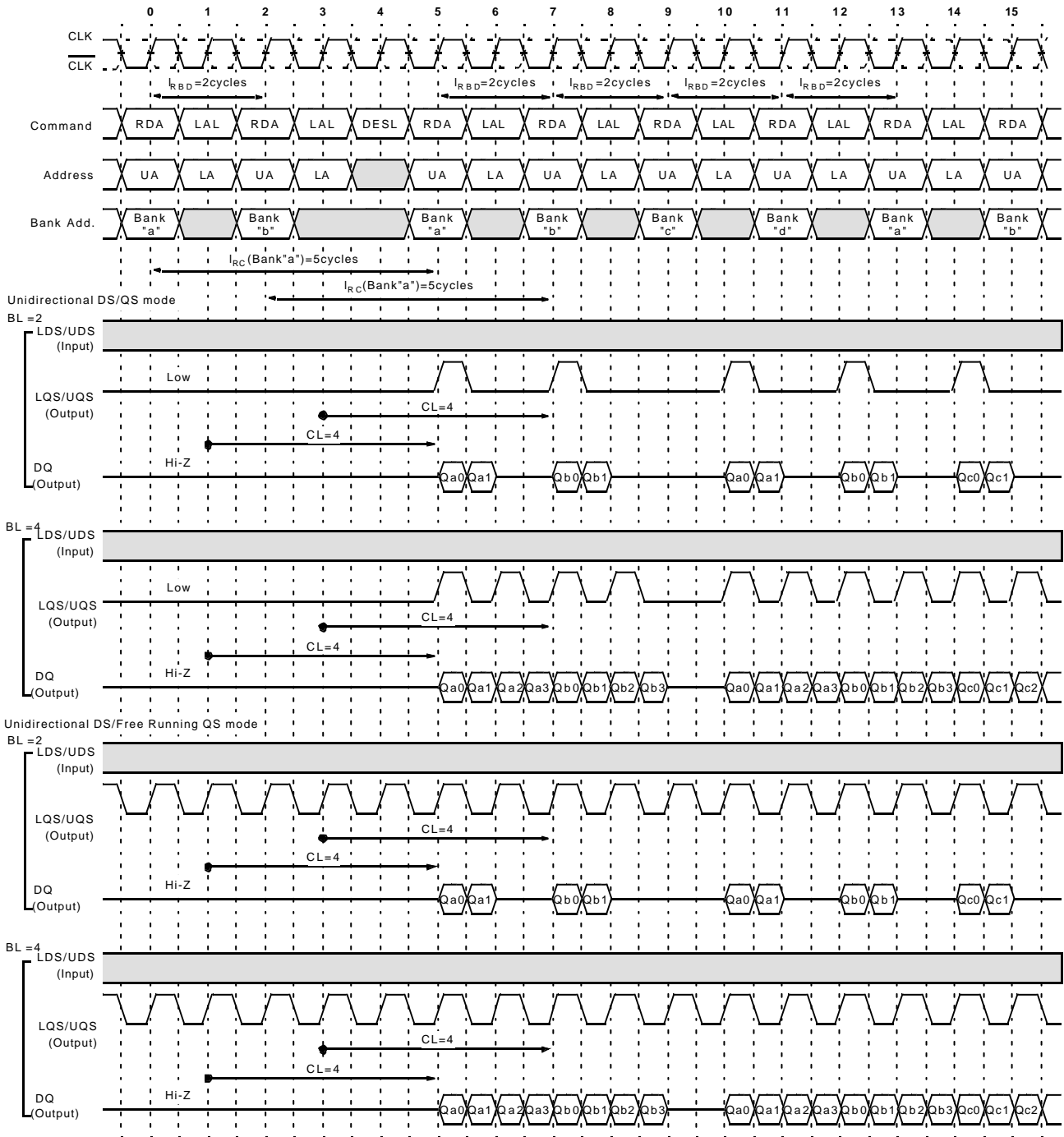
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Single Bank Read-Write Timing (CL=6)



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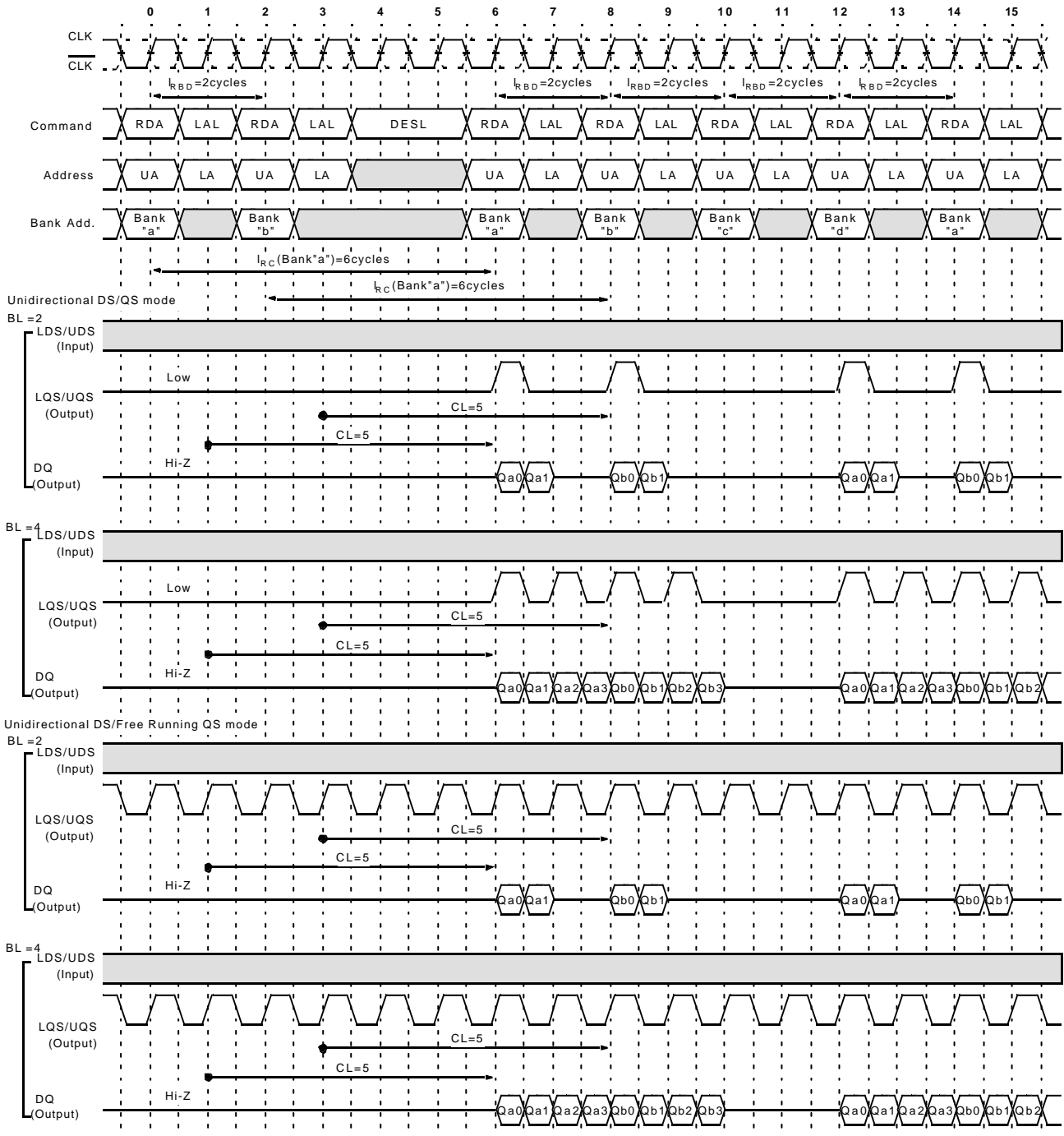
Multiple Bank Read Timing (CL=4)



Note: t_{RC} to the same bank must be satisfied

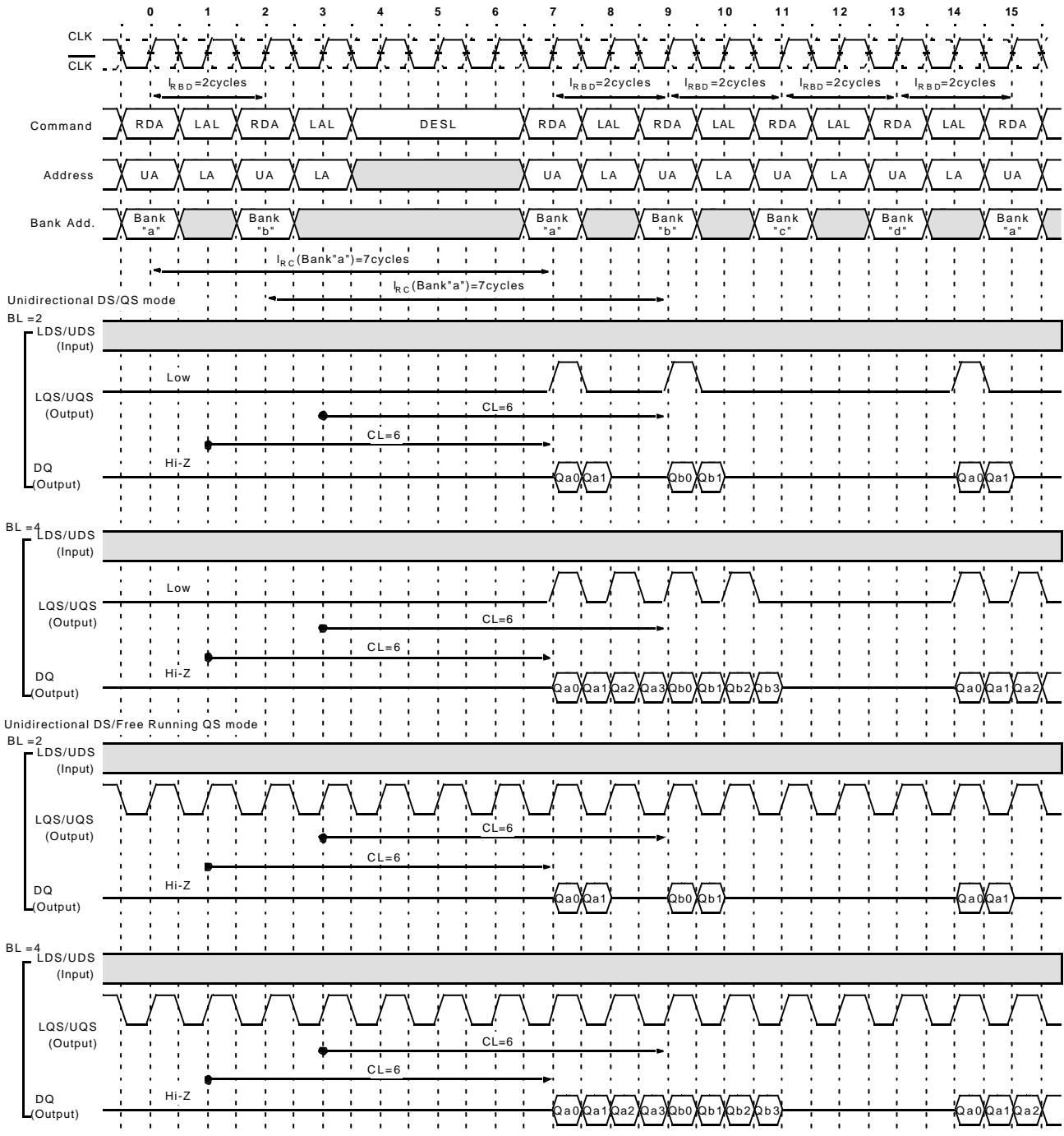
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Multiple Bank Read Timing (CL=5)



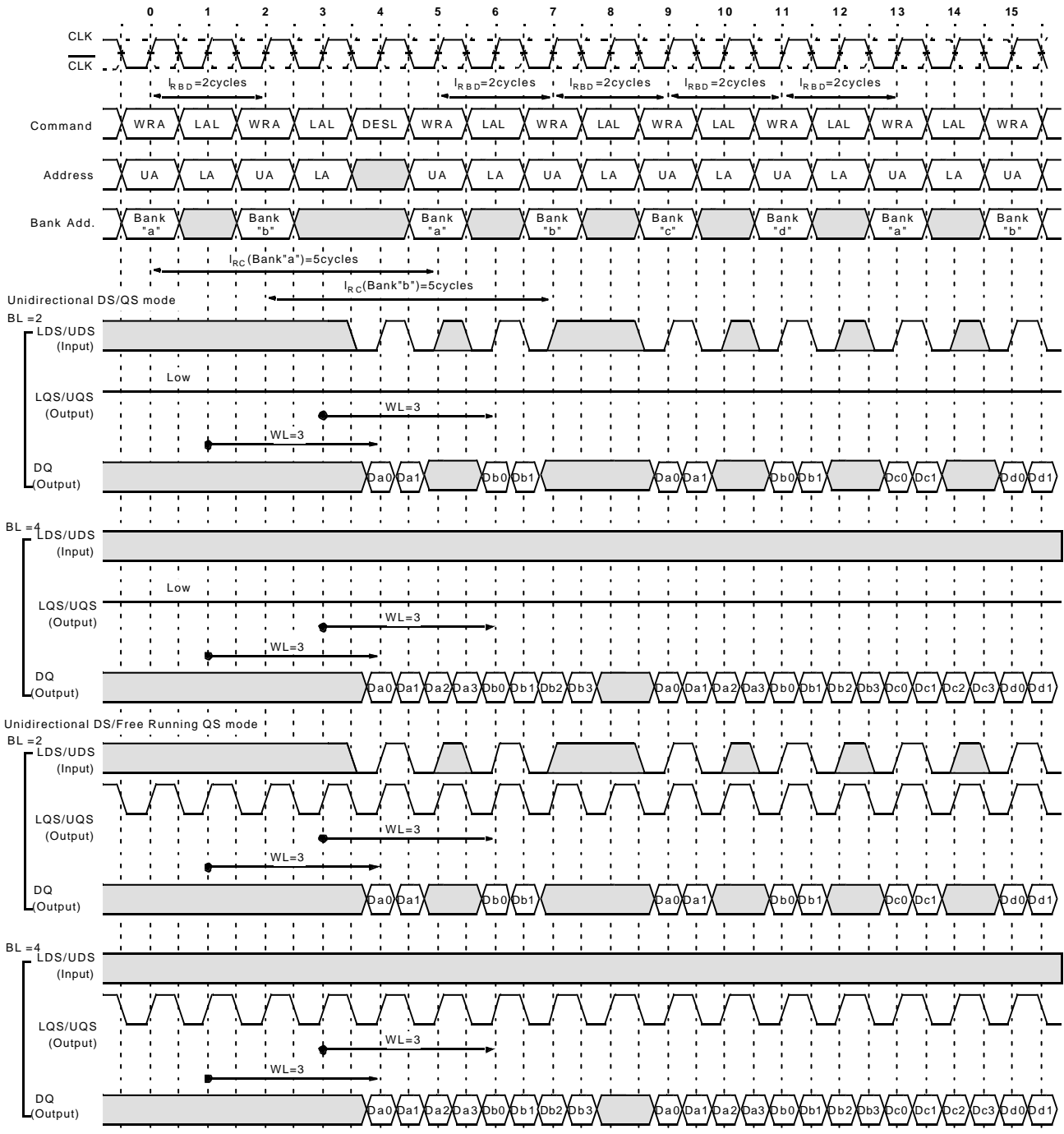
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Multiple Bank Read Timing (CL=6)



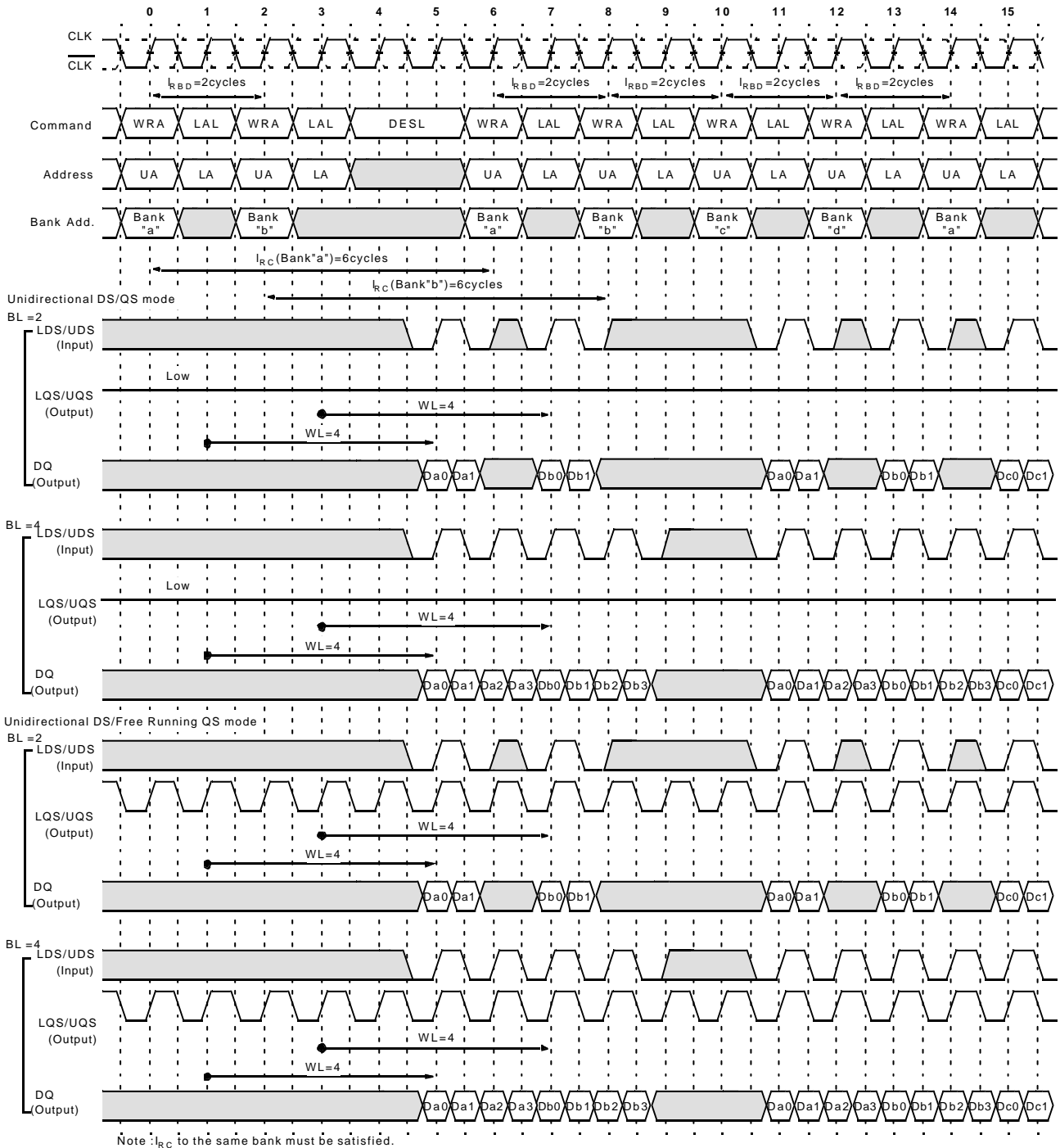
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Multiple Bank Write Timing (CL=4)



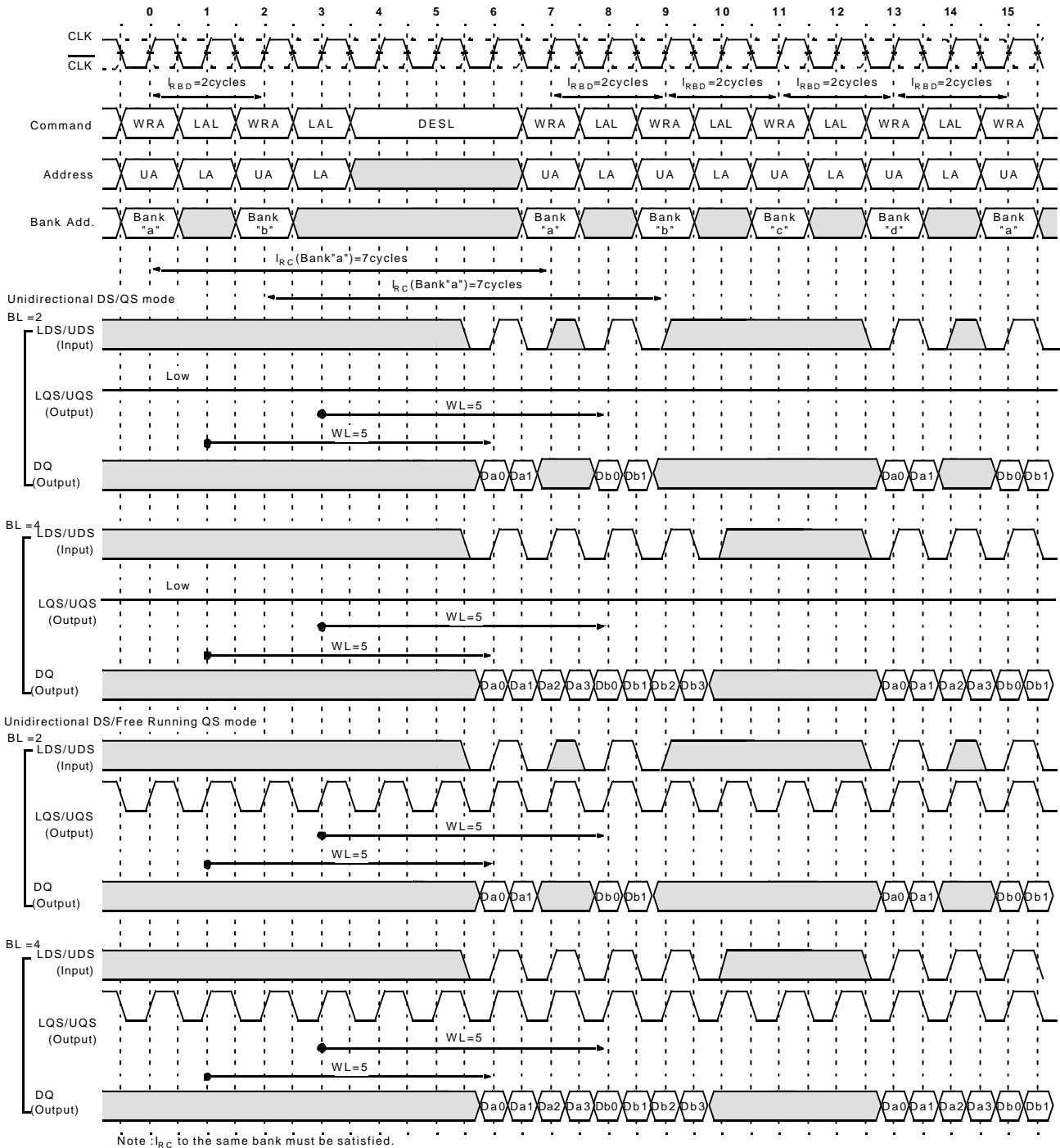
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Multiple Bank Write Timing (CL=5)



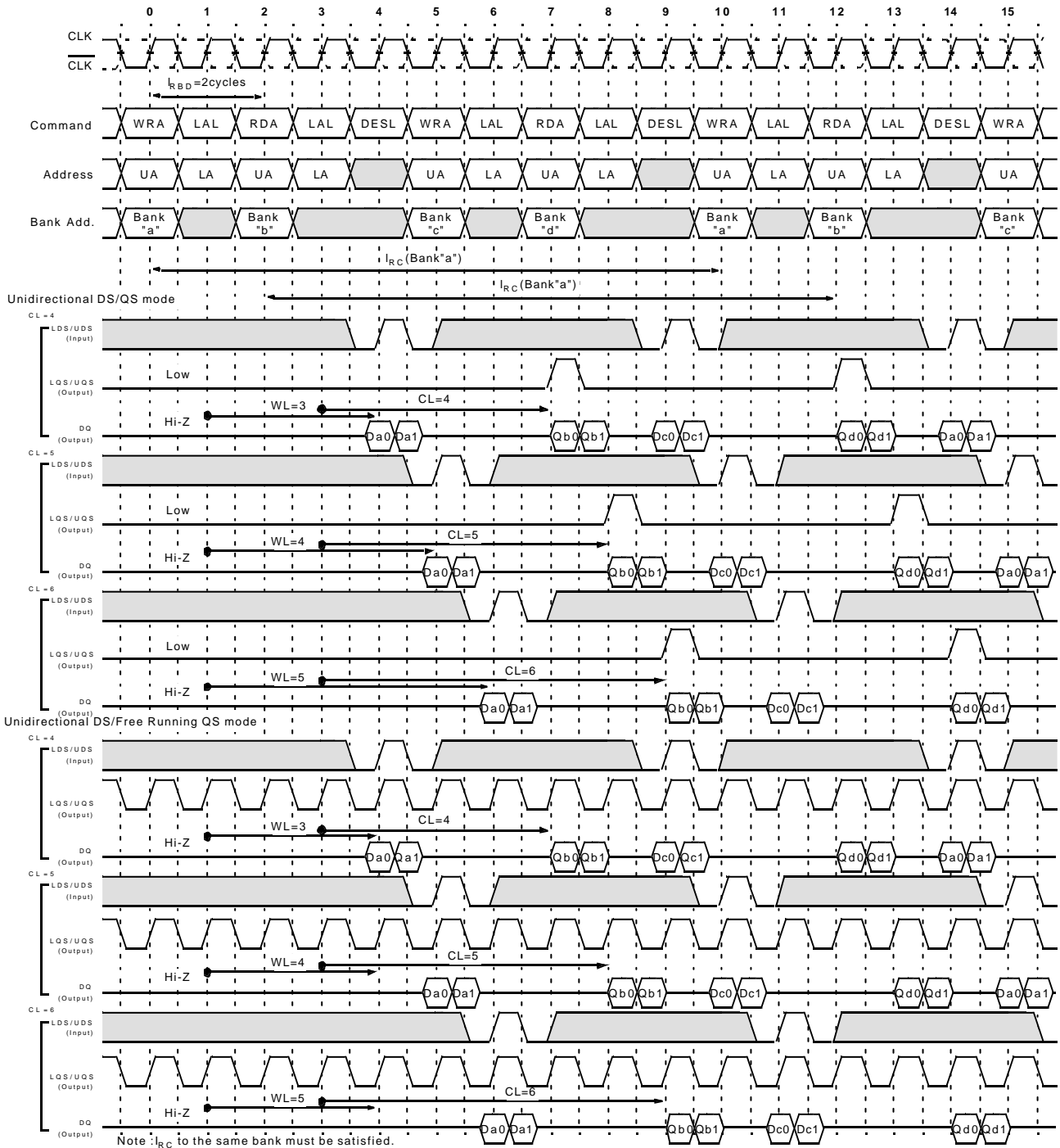
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Multiple Bank Write Timing (CL=6)



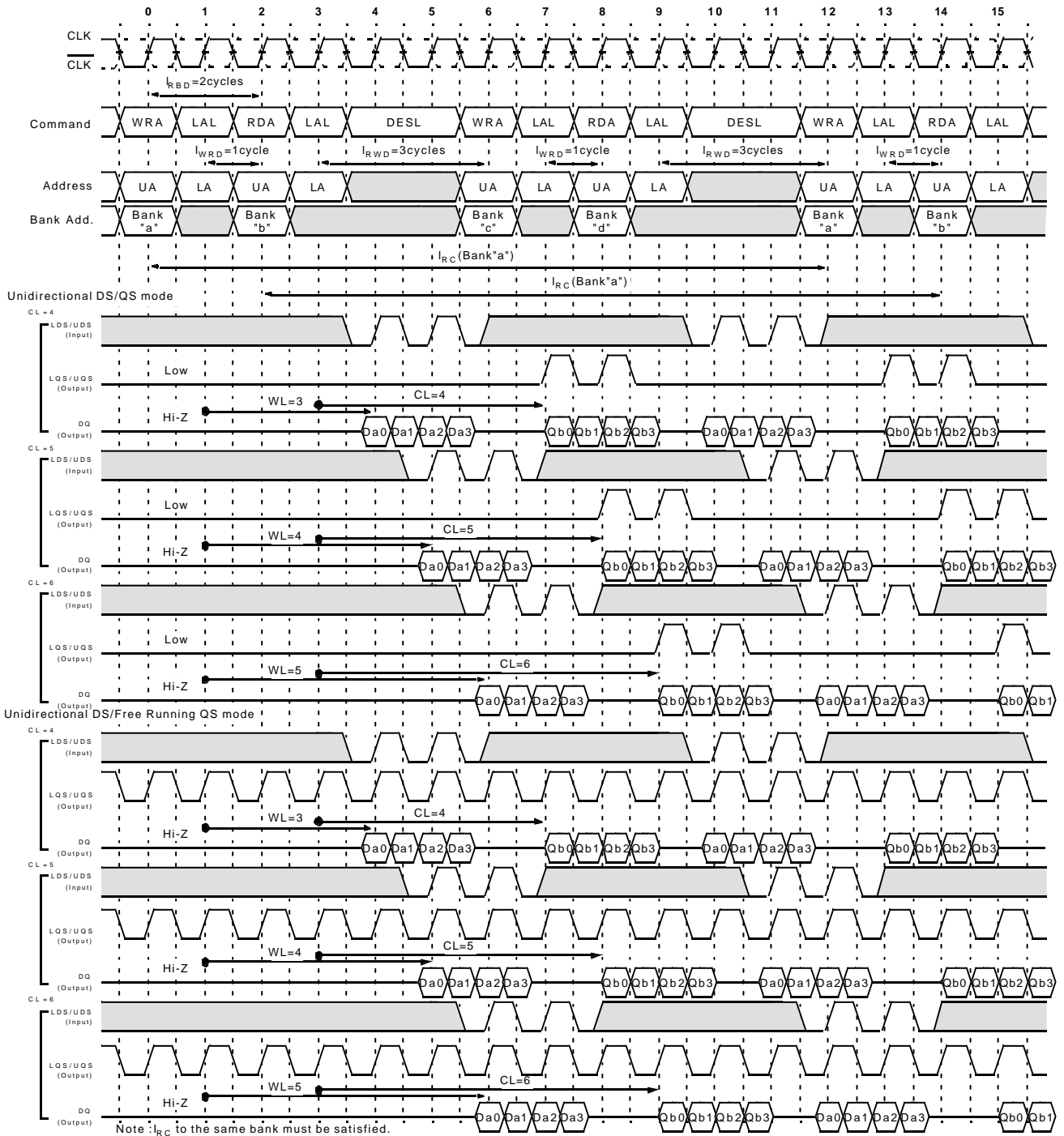
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Multiple Bank Read-Write Timing (BL=2)



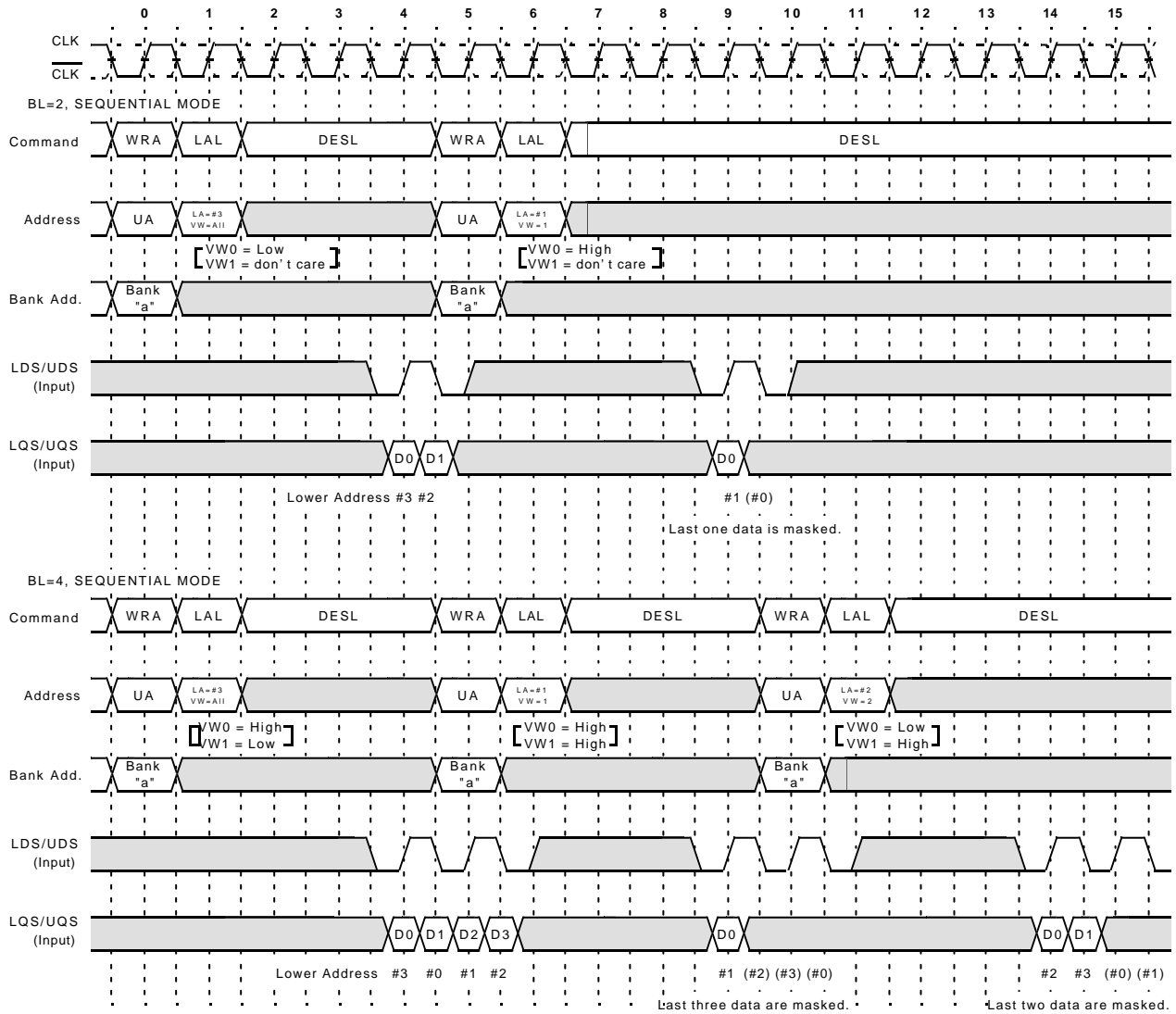
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Multiple Bank Read-Write Timing (BL=4)



K4C89363AF

Write with Variable Write Length (VW) Control(CL=4)

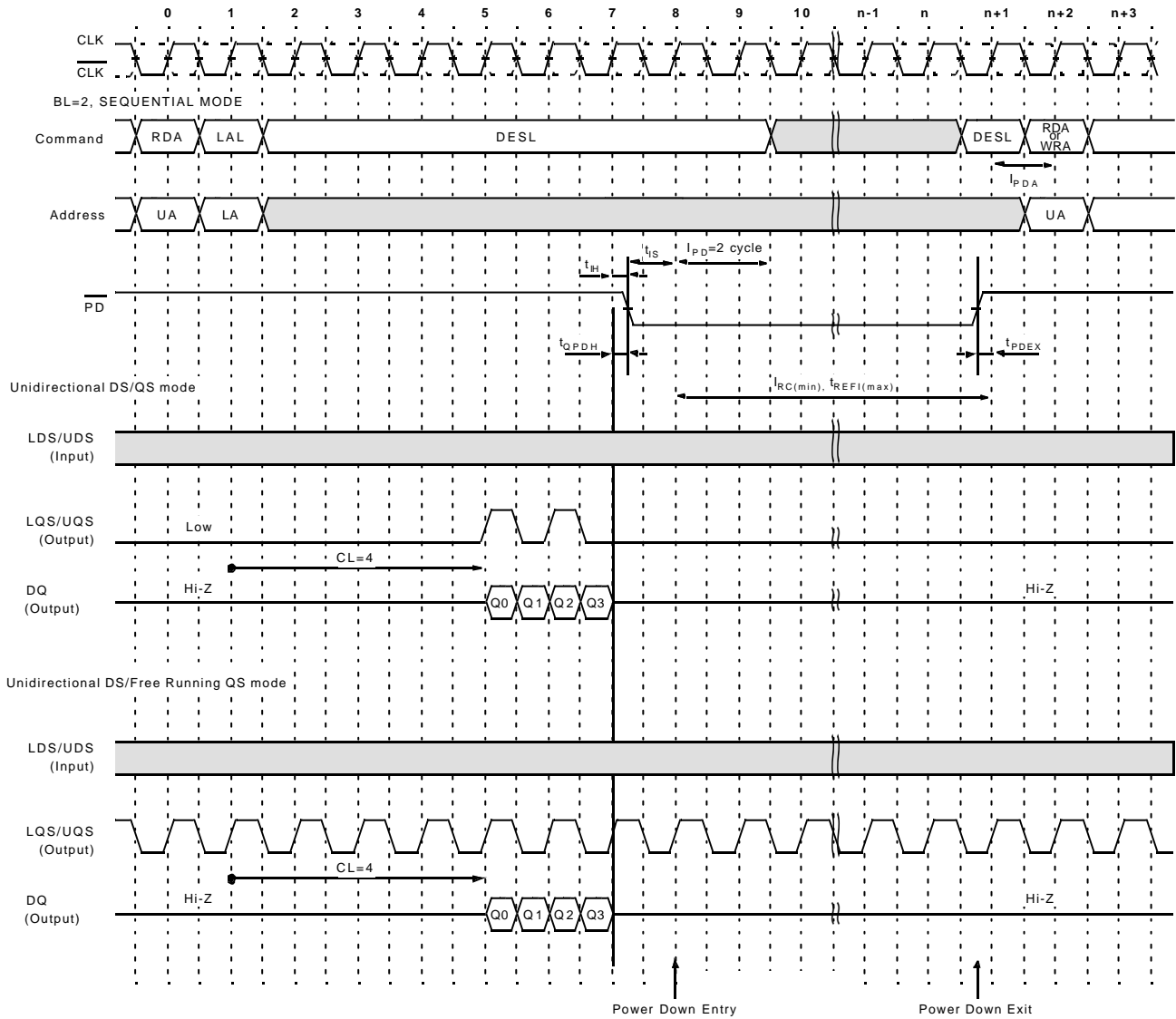


Note : DS input must be continued till end of burst count even if some of later data is masked.

K4C89363AF

Power Down Timing (CL=4, BL=4)

Read cycle to Power Down Mode

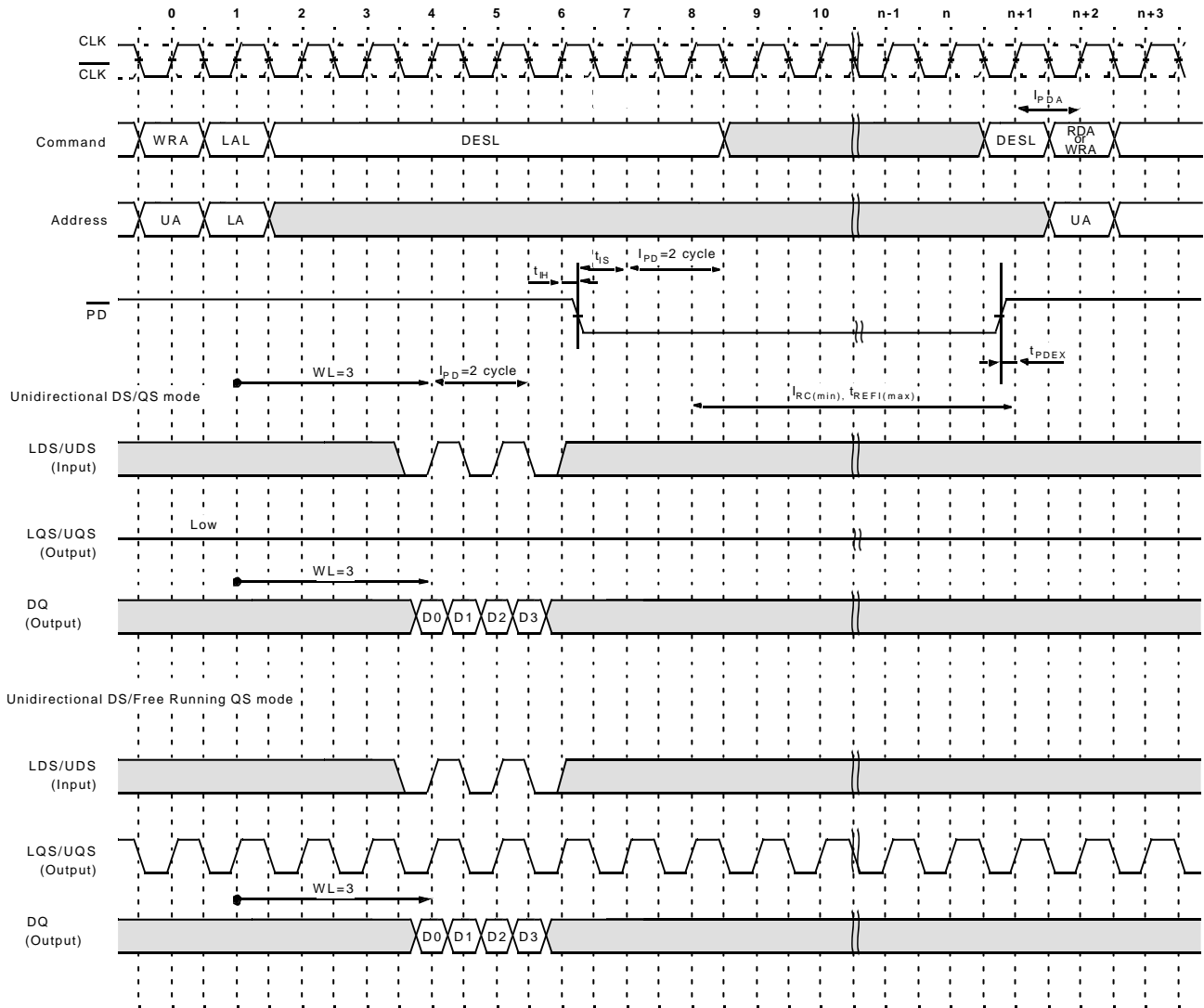


Note: \overline{PD} must be kept "High" level until end of Burst data output.
 \overline{PD} should be brought to "High" within $t_{REFI(max)}$ to maintain the data written into cell.
 In Power Down Mode, \overline{PD} "Low" and a stable clock signal must be maintained.
 When \overline{PD} is brought to "High", a valid executable command may be applied t_{PDA} cycles later.

K4C89363AF

Power Down Timing (CL=4, BL=4)

Write cycle to Power Down Mode

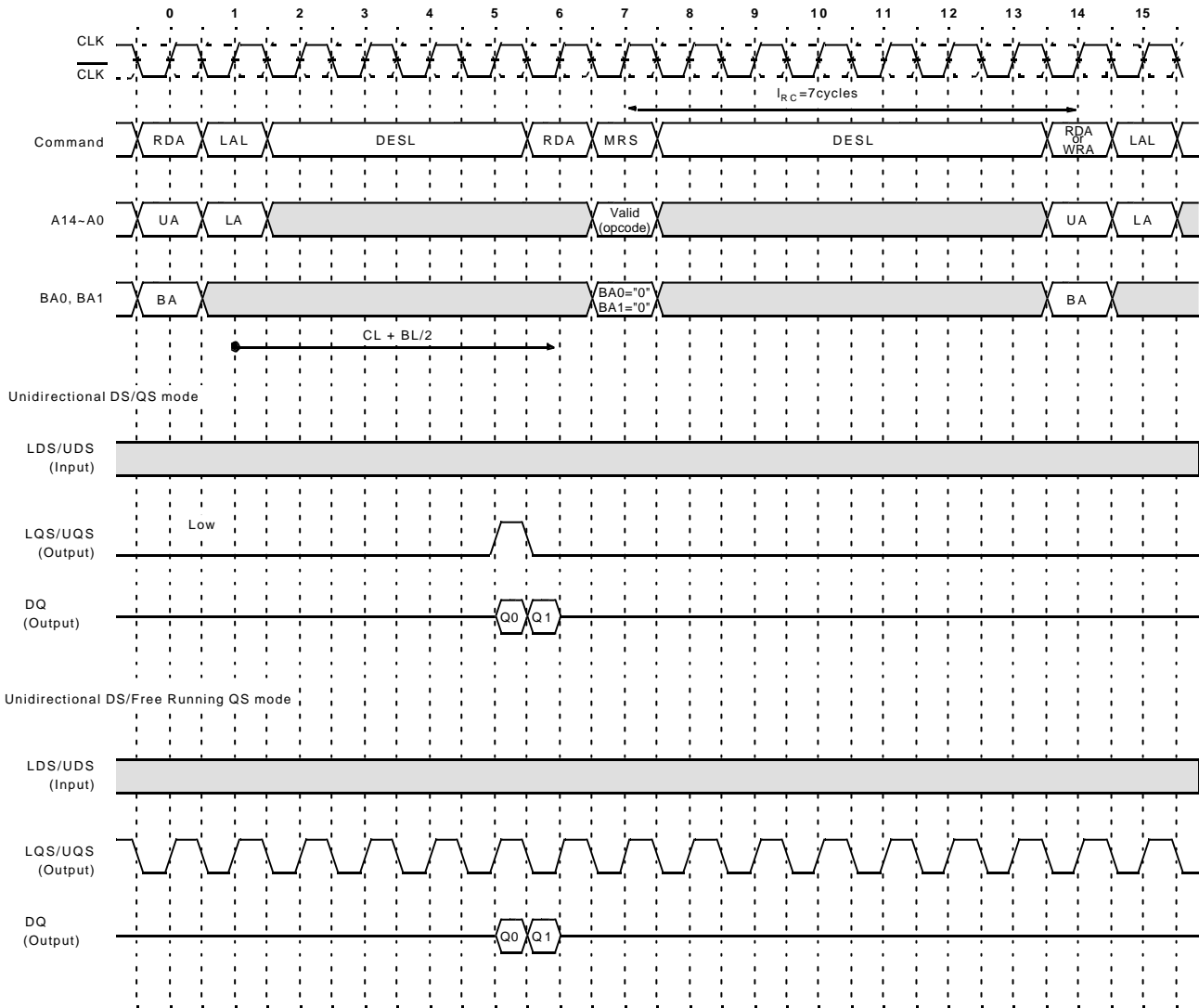


Note : \overline{PD} must be kept "High" level until end of Burst data output.
 \overline{PD} should be brought to "High" within $t_{REFI(max)}$ to maintain the data written into cell.
 In Power Down Mode, \overline{PD} "Low" and a stable clock signal must be maintained.
 When \overline{PD} is brought to "High", a valid executable command may be applied t_{PDA} cycles later.

K4C89363AF

Mode Register Set Timing (CL=4, BL=2)

From Read operation to Mode Register Set operation

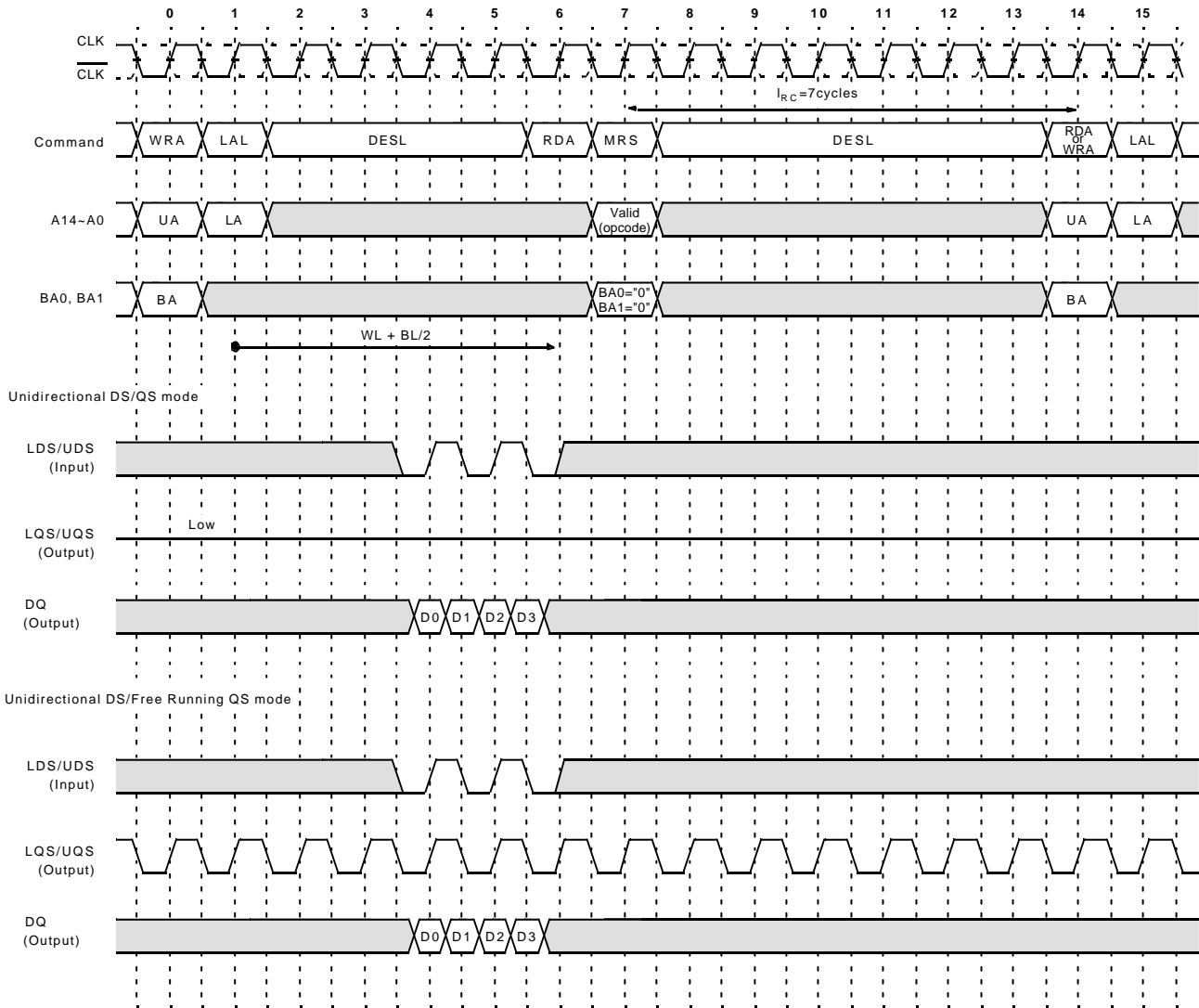


Note : Minimum delay from LAL following RDA to RDA of MRS operation is CL+BL/2.

K4C89363AF

Mode Register Set Timing (CL=4, BL=4)

From Write operation to Mode Register Set operation

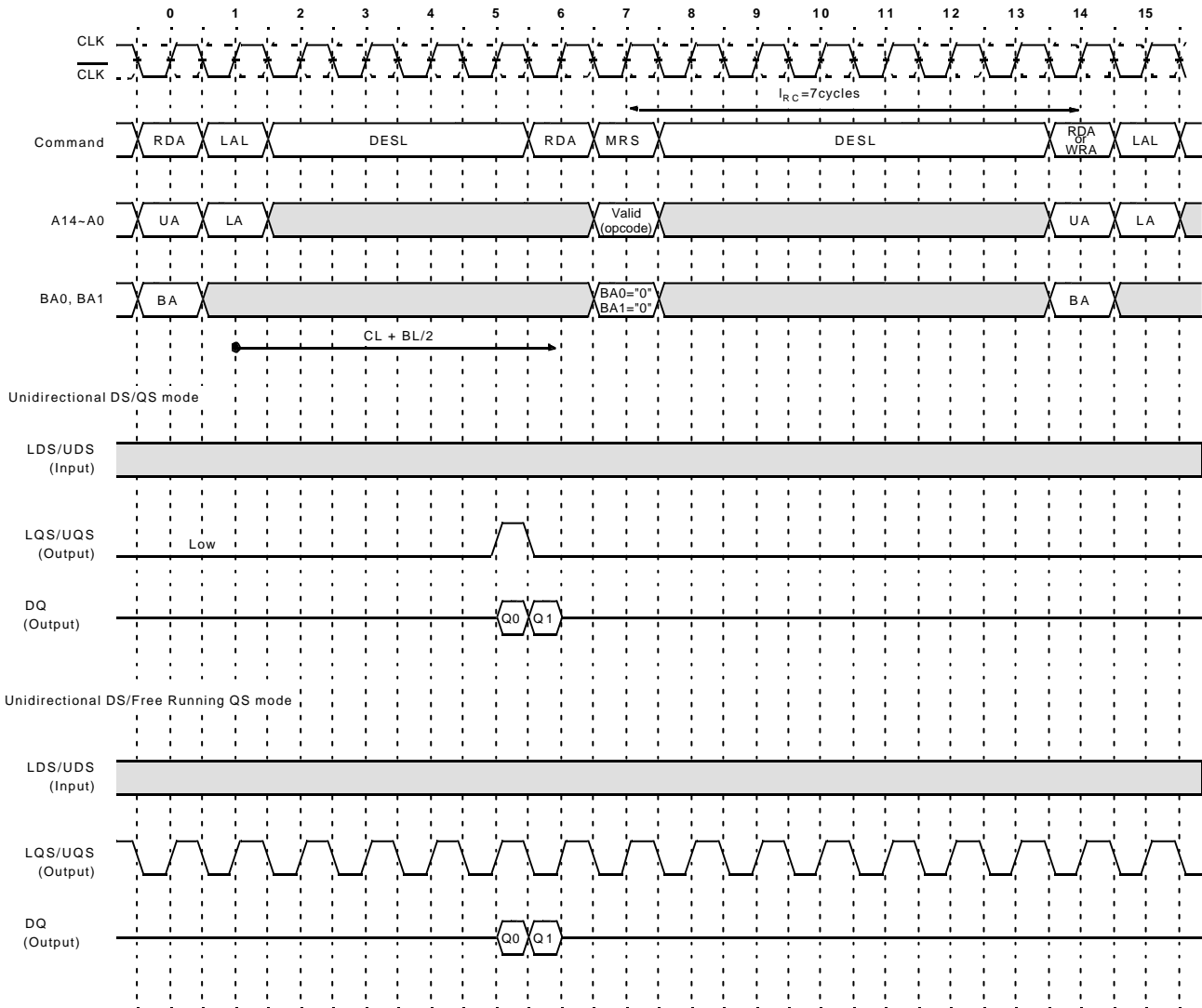


Note : Minimum delay from LAL following WRA to RDA of MRS operation is $WL+BL/2$.

K4C89363AF

Extended Mode Register Set Timing (CL=4, BL=2)

From Read operation to Extended Mode Register Set operation

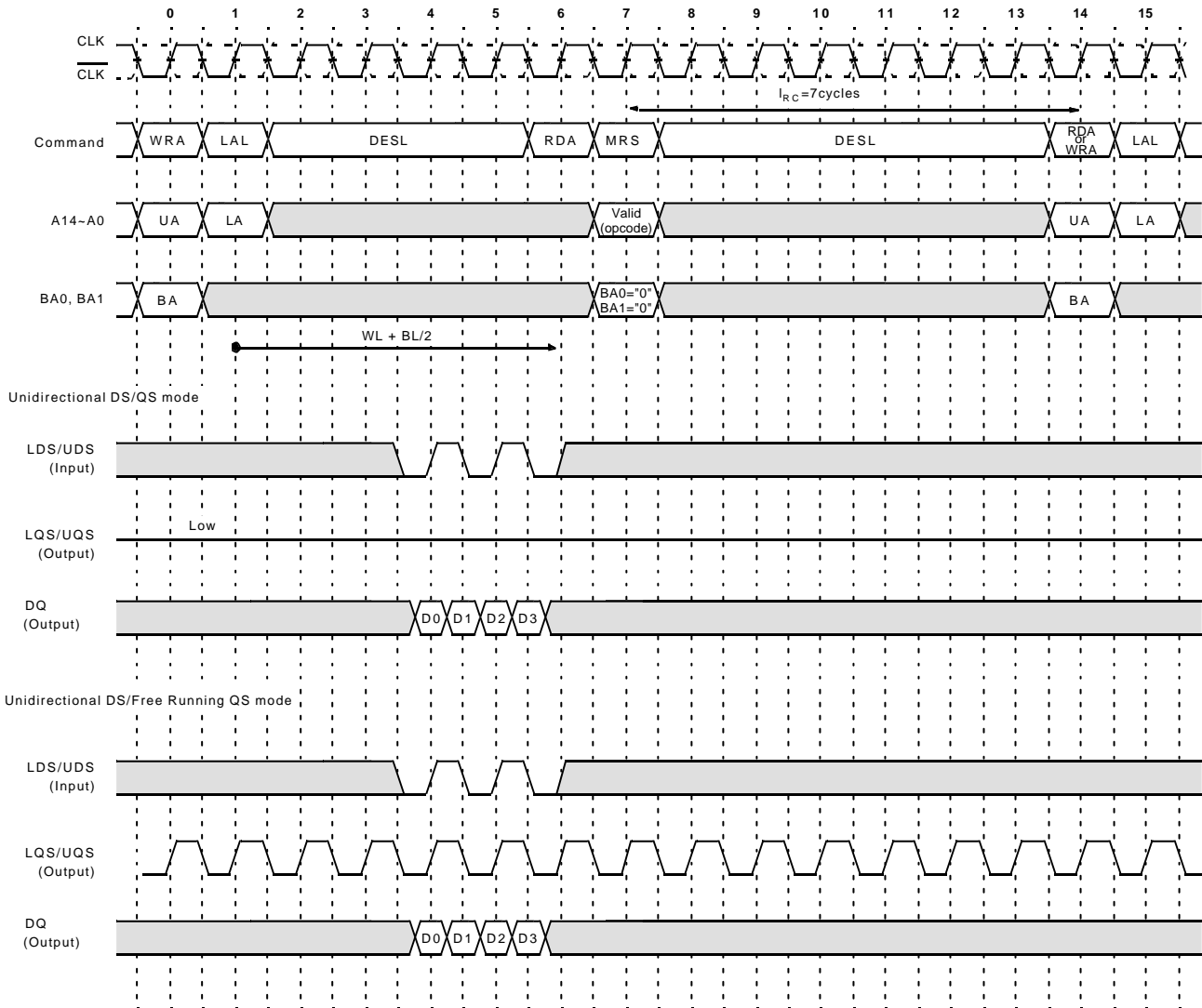


Note : Minimum delay from LAL following RDA to RDA of EMRS operation is $CL+BL/2$.
 When DQ strobe mode is changed by EMRS, QS output is invalid for I_{RSC} period.
 DLL switch in Extended Mode Register must be set to enable mode for normal operation.
 DLL lock-on time is needed after initial EMRS operation. See Power Up Sequence.

K4C89363AF

Extended Mode Register Set Timing (CL=4, BL=4)

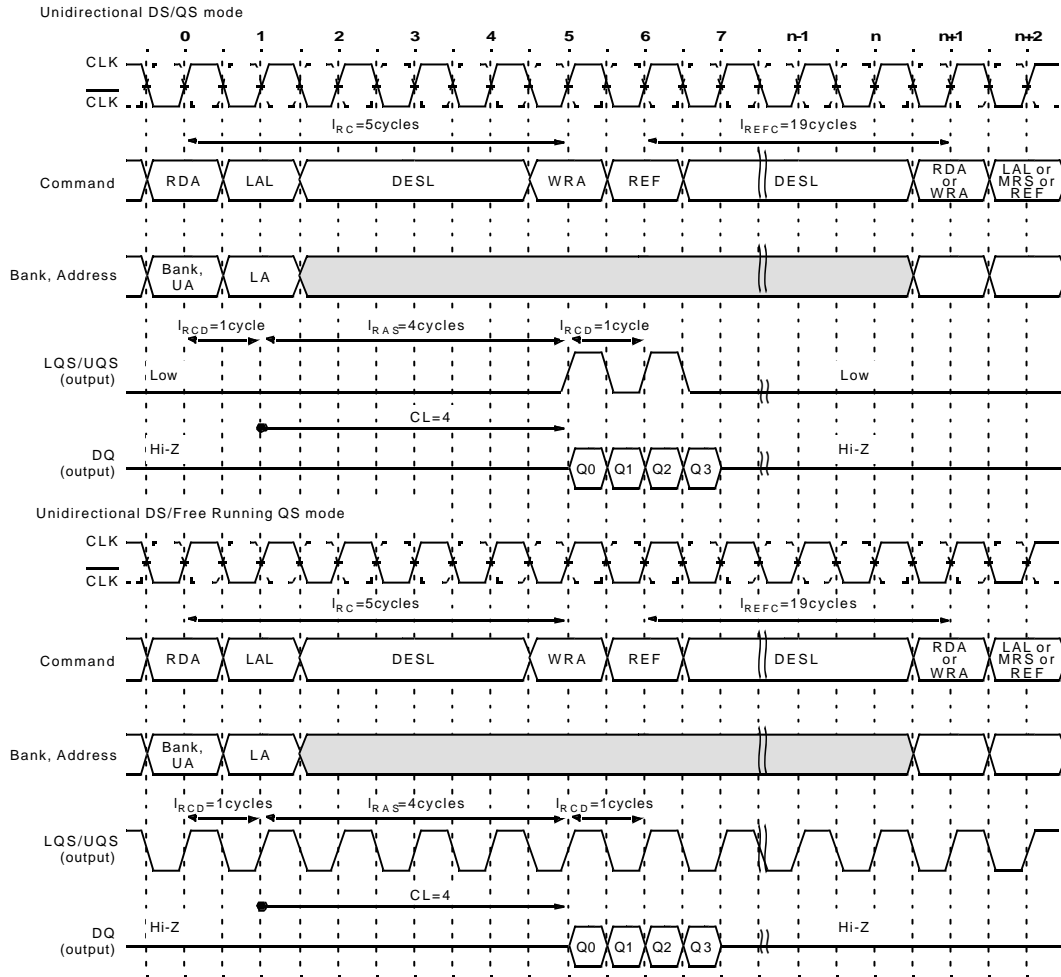
From Write operation to Extended Mode Register Set operation



Note : When DQ strobe mode is changed by EMRS, QS output is invalid for I_{RSC} period.
 DLL switch in Extended Mode Register must be set to enable mode for normal operation.
 DLL lock-on time is needed after initial EMRS operation. See Power Up Sequence.
 Minimum delay from LAL following WRA to RDA of EMRS operation is $WL+BL/2$.

K4C89363AF

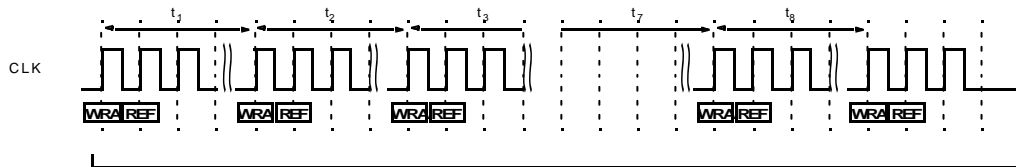
Auto-Refresh Timing (CL=4, BL=4)



Note : In case of CL=4, t_{REFC} must be meet 19 clock cycles.

When the Auto-Refresh operation is performed, the synthetic average interval of Auto-Refresh command specified by t_{REFI} must be satisfied.

t_{REFI} is average interval time in 8 Refresh cycles that is sampled randomly.



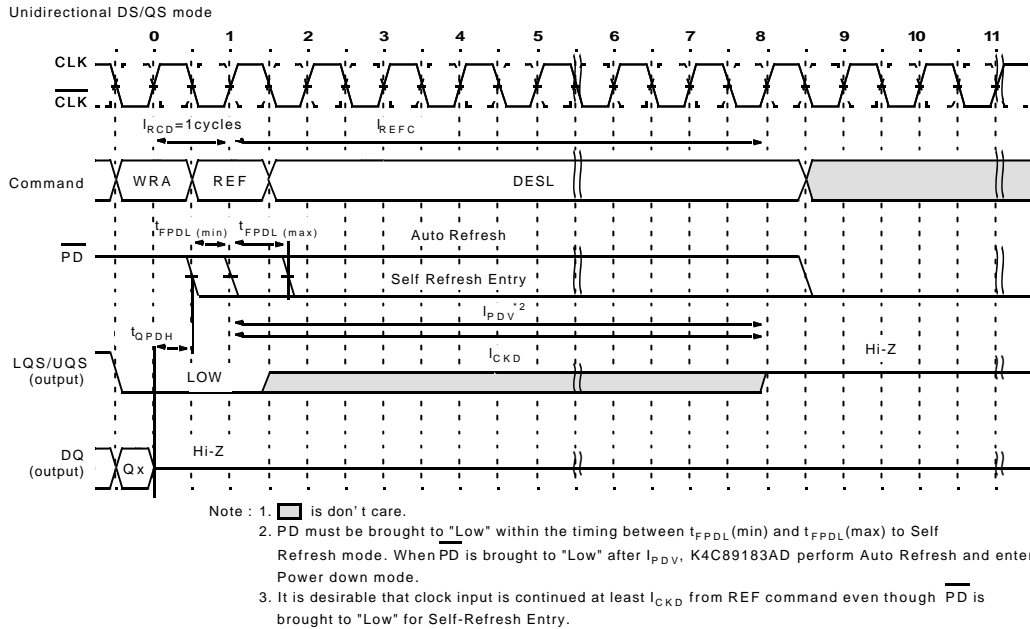
8 Refresh cycle

$$t_{REFI} = \frac{\text{Total time of 8 Refresh cycle}}{8} = \frac{t_1 + t_2 + t_3 + t_4 + t_5 + t_6 + t_7 + t_8}{8}$$

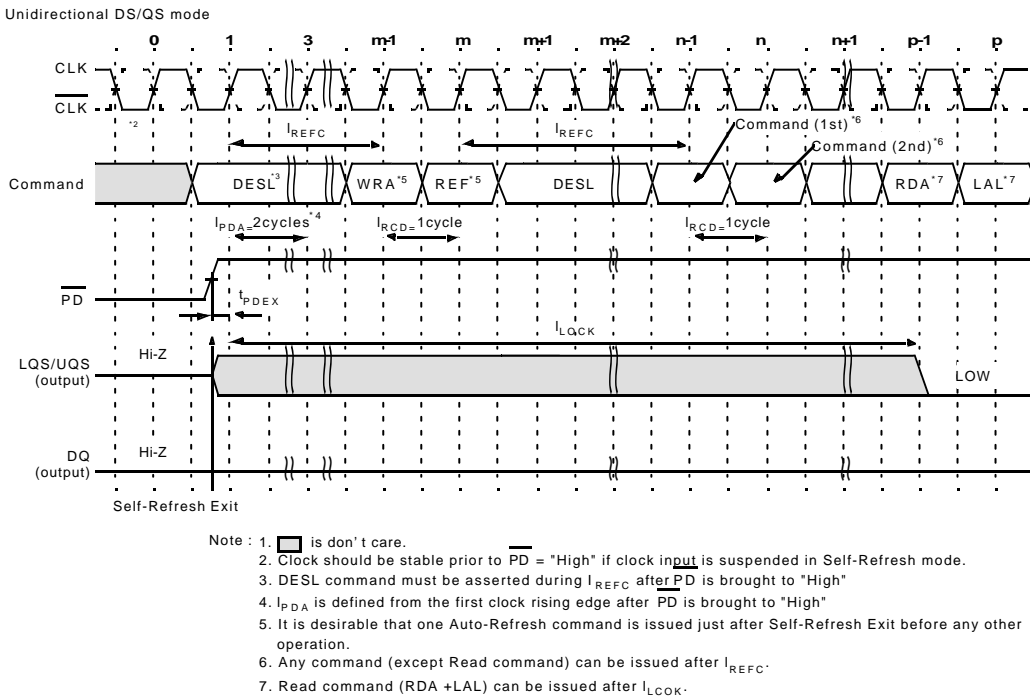
t_{REFI} is specified to avoid partly concentrated current of Refresh operation that is activated larger are than Read/Write operation.

K4C89363AF

Self-Refresh Entry Timing



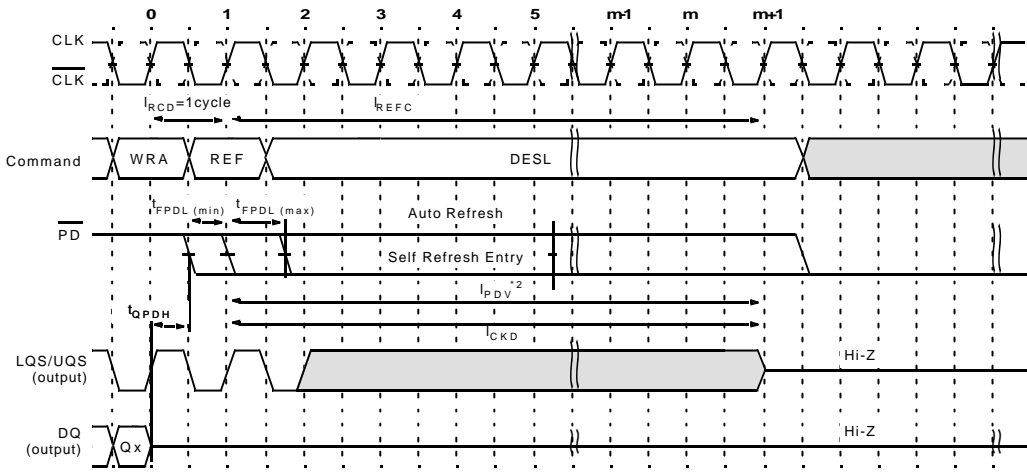
Self-Refresh Exit Timing



K4C89363AF

Self-Refresh Entry Timing

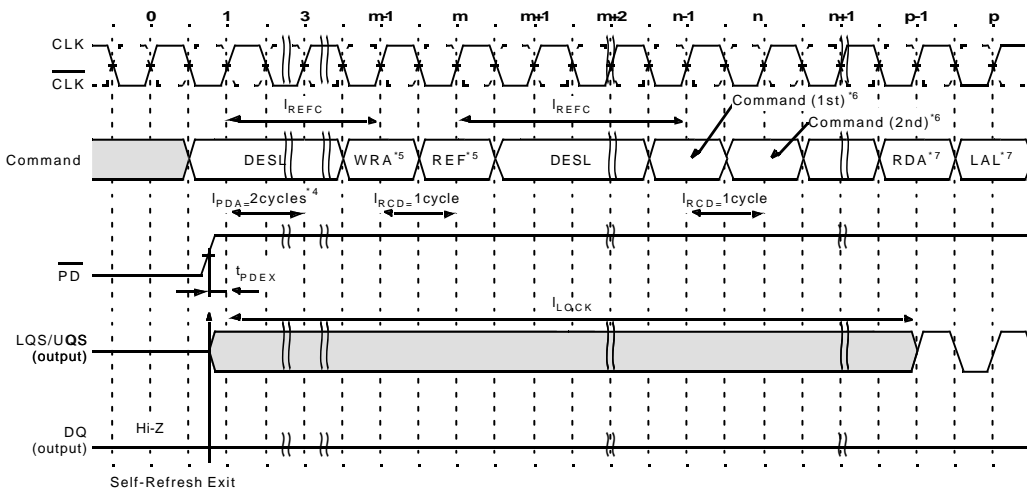
Unidirectional DS/Free Running QS mode



- Note: 1. is don't care.
 2. PD must be brought to "Low" within the timing between $t_{FPDL}(\min)$ and $t_{FPDL}(\max)$ to Self Refresh mode. When PD is brought to "Low" after I_{PDV} , K4C89183AD perform Auto Refresh and enter Power down mode.
 3. It is desirable that clock input is continued at least I_{CKD} from REF command even though PD is brought to "Low" for Self-Refresh Entry.

Self-Refresh Exit Timing

Unidirectional DS/Free Running QS mode



- Note: 1. is don't care.
 2. Clock should be stable prior to PD = "High" if clock input is suspended in Self-Refresh mode.
 3. DESL command must be asserted during I_{REFC} after PD is brought to "High"
 4. I_{PDA} is defined from the first clock rising edge after PD is brought to "High"
 5. It is desirable that one Auto-Refresh command is issued just after Self-Refresh Exit before any other operation.
 6. Any command (except Read command) can be issued after I_{REFC} .
 7. Read command (RDA + LAL) can be issued after I_{LOCK} .
 8. QS output is invalid until DLL lock from Self-Refresh exit.

K4C89363AF

Function Description

Network - DRAM

Network - DRAM is an acronym of Double Data Rate Network - DRAM.

Network - DRAM is competent to perform fast random core access, low latency and high-speed data transfer.

Pin Functions

Clock Inputs : $\overline{\text{CLK}}$ & $\overline{\text{CLK}}$

The $\overline{\text{CLK}}$ and $\overline{\text{CLK}}$ inputs are used as the reference for synchronous operation. $\overline{\text{CLK}}$ is master clock input. The $\overline{\text{CS}}$, FN and all address input signals are sampled on the crossing of the positive edge of $\overline{\text{CLK}}$ and the negative edge of $\overline{\text{CLK}}$. The QS and DQ output data are aligned to the crossing point of $\overline{\text{CLK}}$ and $\overline{\text{CLK}}$. The timing reference point for the differential clock is when the $\overline{\text{CLK}}$ and $\overline{\text{CLK}}$ signals cross during a transition.

Power Down : $\overline{\text{PD}}$

The $\overline{\text{PD}}$ input controls the entry to the Power Down or Self-Refresh modes. The $\overline{\text{PD}}$ input does not have a Clock Suspend function like a CKE input of a standard SDRAMs, therefore it is illegal to bring $\overline{\text{PD}}$ pin into low state if any Read or Write operation is being performed.

Chip Select & Function Control : $\overline{\text{CS}}$ & FN

The $\overline{\text{CS}}$ and FN inputs are a control signal for forming the operation commands on Network-DRAM. Each operation mode is decided by the combination of the two consecutive operation commands using the $\overline{\text{CS}}$ and FN inputs.

Bank Addresses : BA0 & BA1

The BA0 and BA1 inputs are latched at the time of assertion of the RDA or WRA command and are selected the bank to be used for the operation. BA0 and BA1 also define which mode register is loaded during the Mode Register Set command (MRS or EMRS).

	BA0	BA1
Bank #0	0	0
Bank #1	1	0
Bank #2	0	1
Bank #3	1	1

Address Inputs : A0 to A14

Address inputs are used to access the arbitrary address of the memory cell array within each bank. The Upper Addresses with Bank address are latched at the RDA or WRA command and the Lower Addresses are latched at the LAL command. The A0 to A14 inputs are also used for setting the data in the Regular or Extended Mode Register set cycle.

	Upper Address	Lower Address
K4C89363AF	A0 to A14	A0 to A6

K4C89363AF

Functional Description (Continued)

Data Input/Output : DQ0 ~ DQ35

The input data of DQ0 to DQ35 are taken in synchronizing with the both edges of LDS/UDS input signal.
The output data of DQ0 to DQ35 are outputted synchronizing with the both edges of LQS/UQS output signal.

Data Strobe : DS(LDS/UDS) or QS(LQS/UQS)

Method of data strobe is chosen by Extended mode register.

(1) Unidirectional DS/QS mode

DS is input signal and QS is output signal. Both edges of DS are used to sample all DQs at Write operation. Both edges of QS are used for trigger signal of all DQs at Read operation. During Write, Auto-Refresh and NOP cycle, QS assert always "Low" level. QS is Hi-Z in Self-Refresh mode.

(2) Unidirectional DS/Free running QS mode

DS is input signal and QS is output signal. Both edges of DS are used to sample all DQs at Write operation. Both edges of QS are used for trigger signal of all DQs at Read operation. QS assert always toggle signal except Self-Refresh mode. This strobe type is easy to use for pin to pin connect application.

Power Supply : V_{DD} , V_{DDQ} , V_{SS} , V_{SSQ}

V_{DD} and V_{SS} are supply pins for memory core and peripheral circuits.

V_{DDQ} and V_{SSQ} are power supply pins for the output buffer.

Reference Voltage : V_{REF}

V_{REF} is reference voltage for all input signals.

K4C89363AF

Command Functions and Operations

K4C89363AF is introduced the two consecutive command input method. Therefore, except for Power Down mode, each operation mode decided by the combination of the first command and the second command from stand-by states of the bank to be accessed.

Read Operation (1st command + 2nd command = RDA + LAL)

Issuing the RDA command with Bank Addresses and Upper Addresses to the idle bank puts the bank designated by Bank Address in a read mode. When the LAL command with Lower Addresses is issued at the next clock of the RDA command, the data is read out sequentially synchronizing with the both edges of QS output signal (Burst Read Operation). The initial valid read data appears after CAS latency, the burst length of read data and the burst type must be set in the Mode Register beforehand. The read operated bank goes back automatically to the idle state after I_{RC} .

Write Operation (1st command + 2nd command = WRA + LAL)

Issuing the WRA command with Bank Addresses and Upper Addresses to the idle bank puts the bank designated by Bank Address in a write mode. When the LAL command with Lower Addresses is issued at the next clock of the WRA command, the input data is latched sequentially synchronizing with the both edges of DS input signal (Burst Write Operation). The data and DS inputs have to be asserted in keeping with clock input after CAS latency-1 from the issuing of the LAL command. The DS have to be provided for a burst length. The CAS latency and the burst type must be set in the Mode Register beforehand. The write operated bank goes back automatically to the idle state after I_{RC} . Write Burst Length is controlled by VW0 and VW1 inputs with LAL command. See VW truth table.

Auto-Refresh Operation (1st command + 2nd command = WRA + REF)

K4C89363AF is required to refresh like a standard SDRAM. The Auto-Refresh operation is begun with the REF command following to the WRA command. The Auto-Refresh mode can be effective only when all banks are in the idle state and all DQ are in Hi-Z states. In a point to notice, the write mode started with the WRA command is canceled by the REF command having gone into the next clock of the WRA command instead of the LAL command. The minimum period between the Auto-Refresh command and the next command is specified by I_{REFC} . However, about a synthetic average interval of Auto-Refresh command, it must be careful. In case of equally distributed refresh, Auto-Refresh command has to be issued within once for every 3.9 us by the maximum. In case of burst refresh or random distributed refresh, the average interval of eight consecutive Auto-Refresh command has to be more than 400ns always. In other words, the number of Auto-Refresh cycles which can be performed within 3.2 us (8x400ns) is to 8 times in the maximum.

Self-Refresh Operation (1st command + 2nd command = WRA + REF with $\overline{PD} = "L"$)

It is the function of Self-Refresh operation that refresh operation can be performed automatically by using an internal timer. When all banks are in the idle state and all outputs are in Hi-z states, the K4C89363AF become Self-Refresh mode by issuing the Self-Refresh command. \overline{PD} has to be brought to "Low" within t_{FPDL} from the REF command following to the WRA command for a Self-Refresh mode entry. In order to satisfy the refresh period, the Self-Refresh entry command should be asserted within 3.9us after the latest Auto-Refresh command. Once the device enters Self-Refresh mode, the DESL command must be continued for I_{REFC} period. In addition, it is desirable that clock input is kept in I_{CKD} period. The device is in Self-Refresh mode as long as \overline{PD} held "Low". During Self-Refresh mode, all input and output buffers except for \overline{PD} are disabled, therefore the power dissipation lowers. Regarding a Self-Refresh mode exit, \overline{PD} has to be changed over from "Low" to "High" along with the DESL command, and the DESL command has to be continuously issued in the number of clocks specified by I_{REFC} . The Self-Refresh exit function is asynchronous operation. It is required that one Auto-Refresh command is issued to avoid the violence of the refresh period just after I_{REFC} from Self-Refresh exit.

K4C89363AF

Power Down Mode(\overline{PD} ="L")

When all banks are in the idle state and all DQ outputs are in Hi-Z states, the K4C89363AF become Power Down Mode by asserting \overline{PD} is "Low". When the device enters the Power Down Mode, all input and output buffers except for \overline{PD} , \overline{CLK} , \overline{CLK} and QS. Therefore, the power dissipation lowers. To exit the Power Down Mode, \overline{PD} has to be brought to "High" and the DESL command has to be issued for I_{PDA} cycle after \overline{PD} goes high. The Power Down exit function is asynchronous operation.

Mode Register Set (1st command + 2nd command = RDA + MRS)

When all banks are in the idle state, issuing the MRS command following to the RDA command can program the Mode Register. In a point to notice, the read mode started with the RDA command is canceled by the MRS command having gone into the next clock of the RDA command instead of the LAL command. The data to be set in the Mode Register is transferred using A0 to A14, BA0 and BA1 address inputs. The K4C89363AF have two mode registers. These are Regular and Extended Mode Register. The Regular or Extended Mode Register is chosen by BA0 and BA1 in the MRS command. The Regular Mode Register designates the operation mode for a read or write cycle. The Regular Mode Register has four function fields.

The four fields are as follows :

- (R-1) Burst Length field to set the length of burst data
- (R-2) \overline{Burst} Type field to designate the lower address access sequence in a burst cycle
- (R-3) CAS Latency field to set the access time in clock cycle
- (R-4) Test Mode field to use for supplier only.

The Extended Mode Register has two function fields.

The two fields are as follows:

- (E-1) DLL Switch field to choose either DLL enable or DLL disable
- (E-2) Output Driver Impedance Control field.
- (E-3) Data Strobe Select

Once these fields in the Mode Register are set up, the register contents are maintained until the Mode Register is set up again by another MRS command or power supply is lost. The initial value of the Regular or Extended Mode Register after power-up is undefined, therefore the Mode Register Set command must be issued before proper operation.

K4C89363AF

- Regular Mode Register/Extended Mode Register change bits (BA0, BA1)
These bits are used to choose either Regular MRS or Extended MRS

BA 1	BA 0	A 14 ~ A 0
0	0	Regular MRS cycle
0	1	Extended MRS cycle
1	X	Reserved

Regular Mode Register Fields

(R-1) Burst Length field (A2 to A0)

This field specifies the data length for column access using the A2 to A0 pins and sets the Burst Length to be 2 or 4 words.

A 2	A 1	A 0	Burst Length
0	0	0	Reserved
0	0	1	2 words
0	1	0	4 words
0	1	1	Reserved
1	X	X	Reserved

(R-2) Burst Type field (A3)

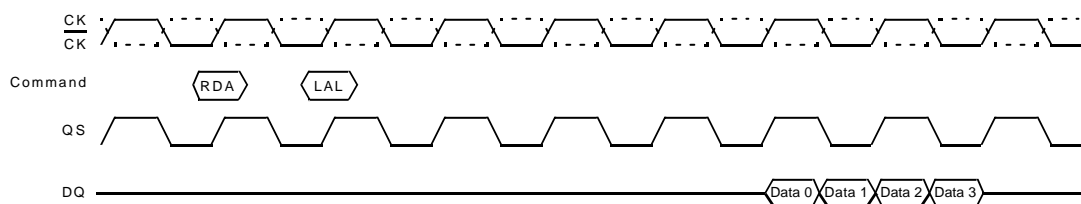
This Burst Type can be chosen Interleave mode or Sequential mode. When the A3 bit is "0", Sequential mode is selected. When the A3 bit is "1", Interleave mode is selected. Both burst types support burst length of 2 and 4 words.

A 3	Burst Type
0	Sequential
1	Interleave

- Addressing sequence of Sequential mode (A3)

A column access is started from the inputted lower address and is performed by incrementing the lower address input to the device.

CAS Latency = 4 (Free Running QS mode)



Addressing sequence for Sequential mode

Data	Access Address	Burst Length
Data 0	n	
Data 1	n + 1	
Data 2	n + 2	
Data 3	n + 3	

K4C89363AF

Functional Description (Continued)

- Addressing sequence of Inteleave mode

A column access is started from the inputted lower address and is performed by interleaving the address bits in the sequence shown as the following.

Addressing sequence for Interleave mode

Data	Access Address	Burst Length
Data 0	...A8 A7 A6 A5 A4 A3 A2 A1 A0	
Data 1	...A8 A7 A6 A5 A4 A3 A2 A1 A0	
Data 2	...A8 A7 A6 A5 A4 A3 A2 A1 A0	
Data 3	...A8 A7 A6 A5 A4 A3 A2 A1 A0	

(R-3) CAS Latency field (A6 to A4)

This field specifies the number of clock cycles from the assertion of the LAL command following the RDA command to the first data read. The minimum values of CAS Latency depends on the frequency of CLK. In a write mode, the place of clock which should input write data is CAS Latency cycles - 1.

Addressing sequence for Interleave mode

A 6	A 5	A 4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved

(R-4) Test Mode field (A7)

This bit is used to enter Test Mode for supplier only and must be set to "0" for normal operation.

(R-5) Reserved field in the Regular Mode Register

- Reserved bits (A8 to A14)

These bits are reserved for future operations. They must be set to "0" for normal operation.

K4C89363AF

Extended Mode Register Fields

(E-1) DLL Switch field (A0)

This bit is used to enable DLL. When the A0 bit is set "0", DLL is enabled.

(E-2) Output Driver Impedance Control field (A1 to A4)

This field is used to choose Output Driver Strength. Four types of Driver Strength are supported. QS and DQ Driver Strength can be chosen separately. A2-A1 specified the DQ Driver Strength. A4-A3 specified the QS Driver Strength.

QS		DQ		Output Driver Impedance Control
A4	A3	A2	A1	
0	0	0	0	Normal Output Driver
0	1	0	1	Strong Output Driver
1	0	1	0	Weaker Output Driver
1	1	1	1	Reserved

(E-3) Strobe Select (A6/A5)

Two types of strobe are supported. This field is used to choose the type of data strobe.

(1) Unidirectional DS/QS mode

Data strobe is separated DS for write strobe and QS for read strobe.

DS is used to sample write data at write operation. QS is aligned with read data at Read operation.

(2) Unidirectional DS/Free running QS mode

Data strobe is separated DS for write strobe and QS for read strobe.

DS is used to sample write data at write operation. QS is aligned with read data and always clocking

A6	A5	Strobe Select
0	0	Reserved
0	1	Reserved
1	0	Unidirectional DS/QS mode
1	1	Unidirectional DS/Free running QS mode

(E-4) Reserved field (A7 to A14)

These bits are reserved for future operations and must be set to "0" for normal operation.

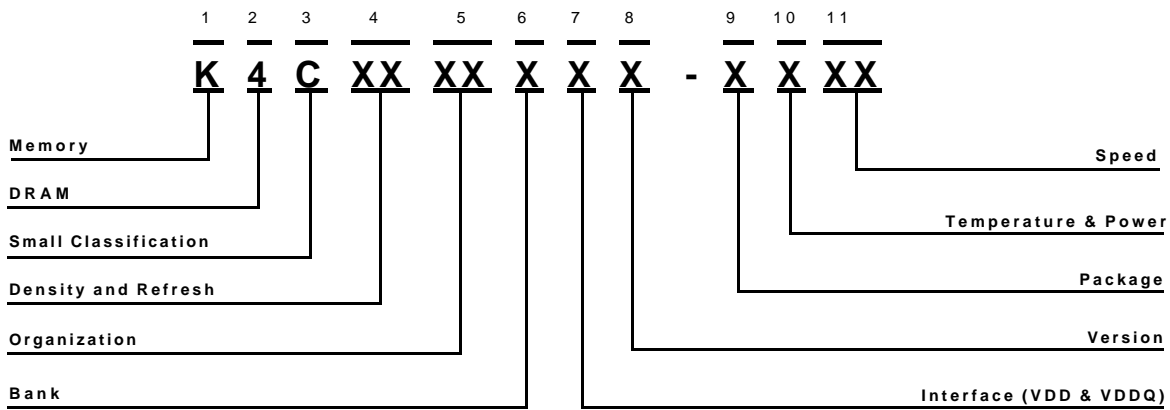
K4C89363AF

Package Outline Drawing (FBGA 144ball, 1.0 x 0.8 mm) - will be added

K4C89363AF

General Information

Organization	F6 (667Mbps)	FB (600Mbps)	F5 (500Mbps)
288M(x32)	K4C89323AF-GCF6	K4C89323AF-GCFB	K4C89323AF-GCF5
288M(x36)	K4C89363AF-GCF6	K4C89363AF-GCFB	K4C89363AF-GCF5



1. **SAMSUNG** Memory : K

2. **DRAM** : 4

3. **Small Classification**
C : Network-DRAM

4. **Density & Refresh**
89 : 288M 8K/32ms

5. **Organization**

32 : x32
36 : x36

6. **Bank**

3 : 4 Bank

7. **Interface (VDD & VDDQ)**

A: SSTL-2(2.5V, 1.8V)

8. **Version**

F : 7th Generation

9. **Package**

T : TSOP II (400mil x 875mil)
G : 144 FBGA

10. **Temperature & Power**

C : (Commercial, Normal)

11. **Speed**

F6 : 667Mbps/pin (333MHz, CL=6)
FB : 600Mbps/pin (300MHz, CL=6)
F5 : 500Mbps/pin (250MHz, CL=6)