

Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

4M x 16bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 4,194,304 x 16 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time (-45, -50 or -60), power consumption(Normal or Low power) are optional features of this family. All of this family have CAS-before-RAS refresh, RAS-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 4Mx16 EDO Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

• **Part Identification**

- K4E661612D-TI/P(3.3V, 8K Ref.)
- K4E641612D-TI/P(3.3V, 4K Ref.)

• **Active Power Dissipation**

Unit : mW

Speed	Refresh Cycle	
	8K	4K
-45	324	468
-50	288	432
-60	252	396

• **Refresh Cycles**

Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
K4E661612D*	8K	64 ms	128 ms
K4E641612D	4K		

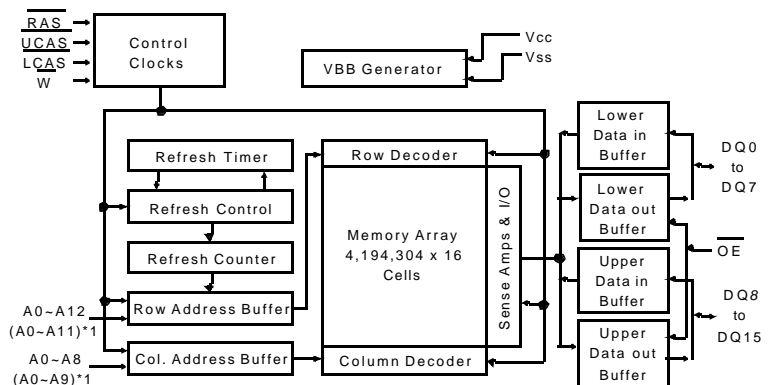
- * Access mode & RAS only refresh mode
 : 8K cycle/64ms(Normal), 8K cycle/128ms(L-ver.)
 CAS-before-RAS & Hidden refresh mode
 : 4K cycle/64ms(Normal), 4K cycle/128ms(L-ver.)

• **Performance Range**

Speed	t _{TRC}	t _{CAC}	t _{RC}	t _{HPC}
-45	45ns	12ns	74ns	17ns
-50	50ns	13ns	84ns	20ns
-60	60ns	15ns	104ns	25ns

- Extended Data Out Mode operation
- 2 CAS Byte/Word Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden refresh capability
- Fast parallel test mode capability
- Self-refresh capability (L-ver only)
- LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic TSOP(II) packages
- +3.3V ±0.3V power supply
- Industrial Temperature operating (-40~85°C)

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

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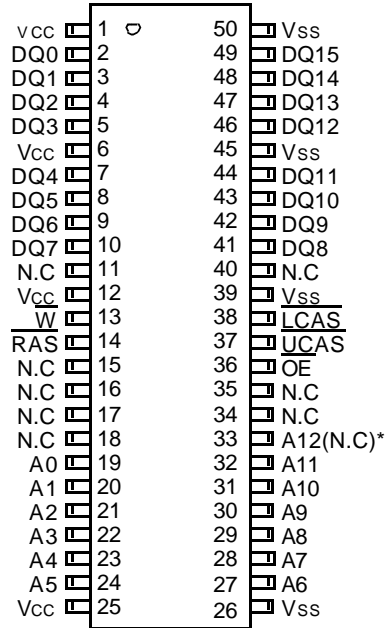
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PIN CONFIGURATION (Top Views)

- K4E661612D-T
- K4E641612D-T



(400mil TSOP(II))

*(N.C) : N.C for 4K Refresh Product

Pin Name	Pin function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 - 15	Data In/Out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS}}$	Upper Column Address Strobe
$\overline{\text{LCAS}}$	Lower Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+3.3V)
N.C	No Connection

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to +4.6	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.5 to +4.6	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{os} Address	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A= -40 to 85°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	V

*1 : V_{CC}+1.3V at pulse width ≤ 15ns which is measured at V_{CC}

*2 : -1.3 at pulse width ≤ 15ns which is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0 ≤ V _{IN} ≤ V _{CC} +0.3V, all other pins not under test=0 Volt)	I _{I(L)}	-5	5	μA
Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ V _{CC})	I _{O(L)}	-5	5	μA
Output High Voltage Level (I _{OH} =-2mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =2mA)	V _{OL}	-	0.4	V

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DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			K4E661612D	K4E641612D	
ICC1	Don't care	-45	90	130	m A
		-50	80	120	m A
		-60	70	110	m A
ICC2	Normal L	Don't care	1	1	m A
			1	1	m A
ICC3	Don't care	-45	90	130	m A
		-50	80	120	m A
		-60	70	110	m A
ICC4	Don't care	-45	100	100	m A
		-50	90	90	m A
		-60	80	80	m A
ICC5	Normal L	Don't care	0.5	0.5	m A
			200	200	uA
ICC6	Don't care	-45	130	130	m A
		-50	120	120	m A
		-60	110	110	m A
ICC7	L	Don't care	350	350	uA
ICCS	L	Don't care	350	350	uA

ICC1* : Operating Current (\overline{RAS} and \overline{UCAS} , \overline{LCAS} , Address cycling @ $t_{RC}=\min$.)

ICC2 : Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=\overline{VIH}$)

ICC3* : RAS-only Refresh Current ($\overline{UCAS}=\overline{LCAS}=\overline{VIH}$, \overline{RAS} , Address cycling @ $t_{RC}=\min$.)

ICC4* : Extended Data Out Mode Current ($\overline{RAS}=\overline{VIL}$, \overline{UCAS} or \overline{LCAS} , Address cycling @ $t_{HPC}=\min$.)

ICC5 : Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=\overline{VCC-0.2V}$)

ICC6* : CAS-Before-RAS Refresh Current (\overline{RAS} and \overline{UCAS} or \overline{LCAS} cycling @ $t_{RC}=\min$)

ICC7 : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(\overline{VIH})= $\overline{VCC-0.2V}$, Input low voltage(\overline{VIL})= $\overline{0.2V}$, \overline{UCAS} , $\overline{LCAS}=\overline{CAS-before-RAS}$ cycling or $\overline{0.2V}$

\overline{W} , $\overline{OE}=\overline{VIH}$, Address= $\overline{Don't\ care}$, $\overline{DQ}=\overline{Open}$, $\overline{TRC}=\overline{31.25us}$

ICCS : Self Refresh Current

$\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{0.2V}$, $\overline{W}=\overline{OE}=\overline{A0 \sim A12(A11)}=\overline{VCC-0.2V}$ or $\overline{0.2V}$, $\overline{DQ0 \sim DQ15}=\overline{VCC-0.2V}$, $\overline{0.2V}$ or \overline{Open}

*Note : ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1, ICC3 and ICC6, address can be changed maximum once while $\overline{RAS}=\overline{VIL}$. In ICC4, address can be changed maximum once within one EDO mode cycle time, t_{HPC} .

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CAPACITANCE (TA=25°C, VCC=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A12]	CIN1	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ15]	CDQ	-	7	pF

AC CHARACTERISTICS (-40°C ≤ TA ≤ 85°C, See note 2)

Test condition : VCC=3.3V±0.3V, Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	74		84		104		ns	
Read-modify-write cycle time	tRWC	101		113		138		ns	
Access time from $\overline{\text{RAS}}$	tRAC		45		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		12		13		15	ns	3,4,5
Access time from column address	tAA		23		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	tCEZ	3	13	3	13	3	13	ns	6,20
$\overline{\text{OE}}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Transition time (rise and fall)	tT	1	50	1	50	1	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	25		30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	45	10K	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	8		8		10		ns	
$\overline{\text{CAS}}$ hold time	tCSH	35		38		40		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	7	5K	8	10K	10	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	11	33	11	37	14	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	9	22	9	25	12	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	7		7		10		ns	
Column address set-up time	tASC	0		0		0		ns	13
Column address hold time	tCAH	7		7		10		ns	13
Column address to $\overline{\text{RAS}}$ lead time	tRAL	23		25		30		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	7		7		10		ns	
Write command pulse width	tWP	6		7		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	8		8		10		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	7		7		10		ns	16
Data set-up time	tDS	0		0		0		ns	9,19

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Data hold time	t _{DH}	7		7		10		ns	9, 19
Refresh period (Normal)	t _{REF}		64		64		64	ms	
Refresh period (L-ver)	t _{REF}		128		128		128	ms	
Write command set-up time	t _{WCS}	0		0		0		ns	7
CAS to W delay time	t _{CWD}	24		27		32		ns	7, 15
RAS to W delay time	t _{RWD}	57		64		77		ns	7
Column address to W delay time	t _{AWD}	35		39		47		ns	7
CAS set-up time (CAS -before-RAS refresh)	t _{CSR}	5		5		5		ns	17
CAS hold time (CAS -before-RAS refresh)	t _{CHR}	10		10		10		ns	18
RAS to CAS precharge time	t _{RPC}	5		5		5		ns	
Access time from CAS precharge	t _{CPA}		24		28		35	ns	3
Hyper Page cycle time	t _{HPC}	17		20		25		ns	21
Hyper Page read-modify-write cycle time	t _{HPRWC}	47		47		56		ns	21
CAS precharge time (Hyper page cycle)	t _{CP}	6.5		7		10		ns	14
RAS pulse width (Hyper page cycle)	t _{RASP}	45	200K	50	200K	60	200K	ns	
RAS hold time from CAS precharge	t _{RHCP}	24		30		35		ns	
OE access time	t _{OE A}		12		13		15	ns	3
OE to data delay	t _{OE D}	8		10		13		ns	
CAS precharge to W delay time	t _{CPWD}	36		41		52		ns	
Output buffer turn off delay time from OE	t _{OE Z}	3	11	3	13	3	13	ns	6
OE command hold time	t _{OE H}	5		5		5		ns	
Write command set-up time (Test mode in)	t _{WTS}	10		10		10		ns	11
Write command hold time (Test mode in)	t _{WTH}	10		10		10		ns	11
W to RAS precharge time (C-B-R refresh)	t _{WRP}	10		10		10		ns	
W to RAS hold time (C-B-R refresh)	t _{WRH}	10		10		10		ns	
Output data hold time	t _{DOH}	4		5		5		ns	
Output buffer turn off delay from RAS	t _{REZ}	3	13	3	13	3	13	ns	6, 20
Output buffer turn off delay from W	t _{WEZ}	3	13	3	13	3	13	ns	6
W to data delay	t _{WED}	8		15		15		ns	
OE to CAS hold time	t _{OE CH}	5		5		5		ns	
CAS hold time to OE	t _{OE CH}	5		5		5		ns	
OE precharge time	t _{OE P}	5		5		5		ns	
W pulse width (Hyper Page Cycle)	t _{WPE}	5		5		5		ns	
RAS pulse width (C-B-R self refresh)	t _{RASS}	100		100		100		us	22, 23, 24
RAS precharge time (C-B-R self refresh)	t _{RPS}	74		90		110		ns	22, 23, 24
CAS hold time (C-B-R self refresh)	t _{CHS}	-50		-50		-50		ns	22, 23, 24

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TEST MODE CYCLE

(Note 11)

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	79		89		109		ns	
Read-modify-write cycle time	tRWC	110		121		145		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		55		65	ns	3,4,10,12
Access time from $\overline{\text{CAS}}$	tCAC		17		18		20	ns	3,4,5,12
Access time from column address	tAA		28		30		35	ns	3,10,12
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	55	10K	65	10K	ns	
$\overline{\text{CAS}}$ pulse width	tCAS	12	10K	13	10K	15	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	18		18		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	39		43		50		ns	
Column Address to $\overline{\text{RAS}}$ lead time	tRAL	28		30		35		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	29		35		39		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	62		72		84		ns	7
Column Address to $\overline{\text{W}}$ delay time	tAWD	40		47		54		ns	7
Hyper Page cycle time	tHPC	22		25		30		ns	21
Hyper Page read-modify-write cycle time	tHPRWC	52		53		61		ns	21
$\overline{\text{RAS}}$ pulse width (Hyper page cycle)	tRASP	50	200K	55	200K	65	200K	ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		29		33		40	ns	3
$\overline{\text{OE}}$ access time	tOEA		17		18		20	ns	3
$\overline{\text{OE}}$ to data delay	tOED	13		18		20		ns	
$\overline{\text{OE}}$ command hold time	tOEH	13		18		20		ns	

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NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{IH}/V_{IL} . $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. This parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ falling edge in OE controlled write cycle and read-modify-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
14. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
15. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.

K4E64(6)1612D Truth Table

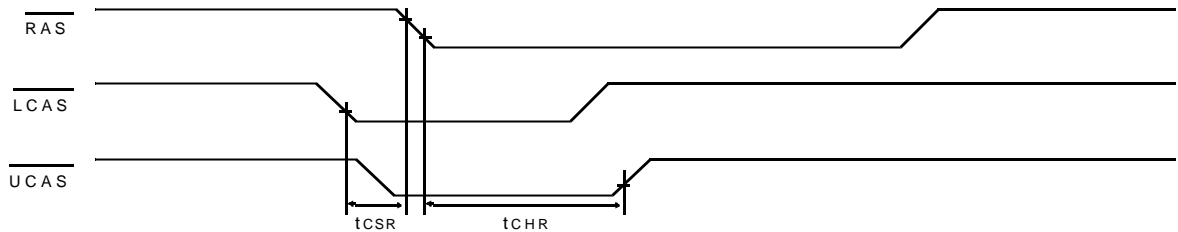
$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	DQ0 - DQ7	DQ8-DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

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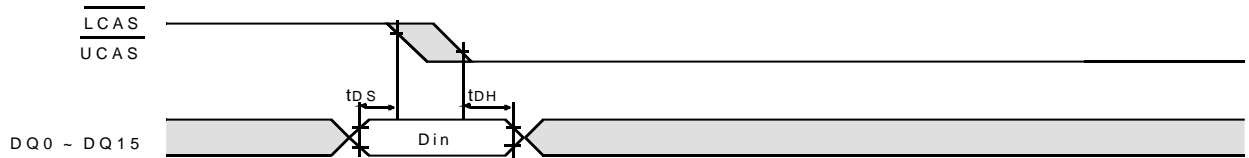
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- 16. t_{CWL} is specified from \overline{W} falling edge to the earlier \overline{CAS} rising edge.
- 17. t_{CSR} is referenced to earlier \overline{CAS} falling before \overline{RAS} transition low.
- 18. t_{CHR} is referenced to the later \overline{CAS} rising high after \overline{RAS} transition low.



- 19. t_{DS} is specified for the earlier \overline{CAS} falling edge and t_{DH} is specified by the later \overline{CAS} falling edge in early write cycle.



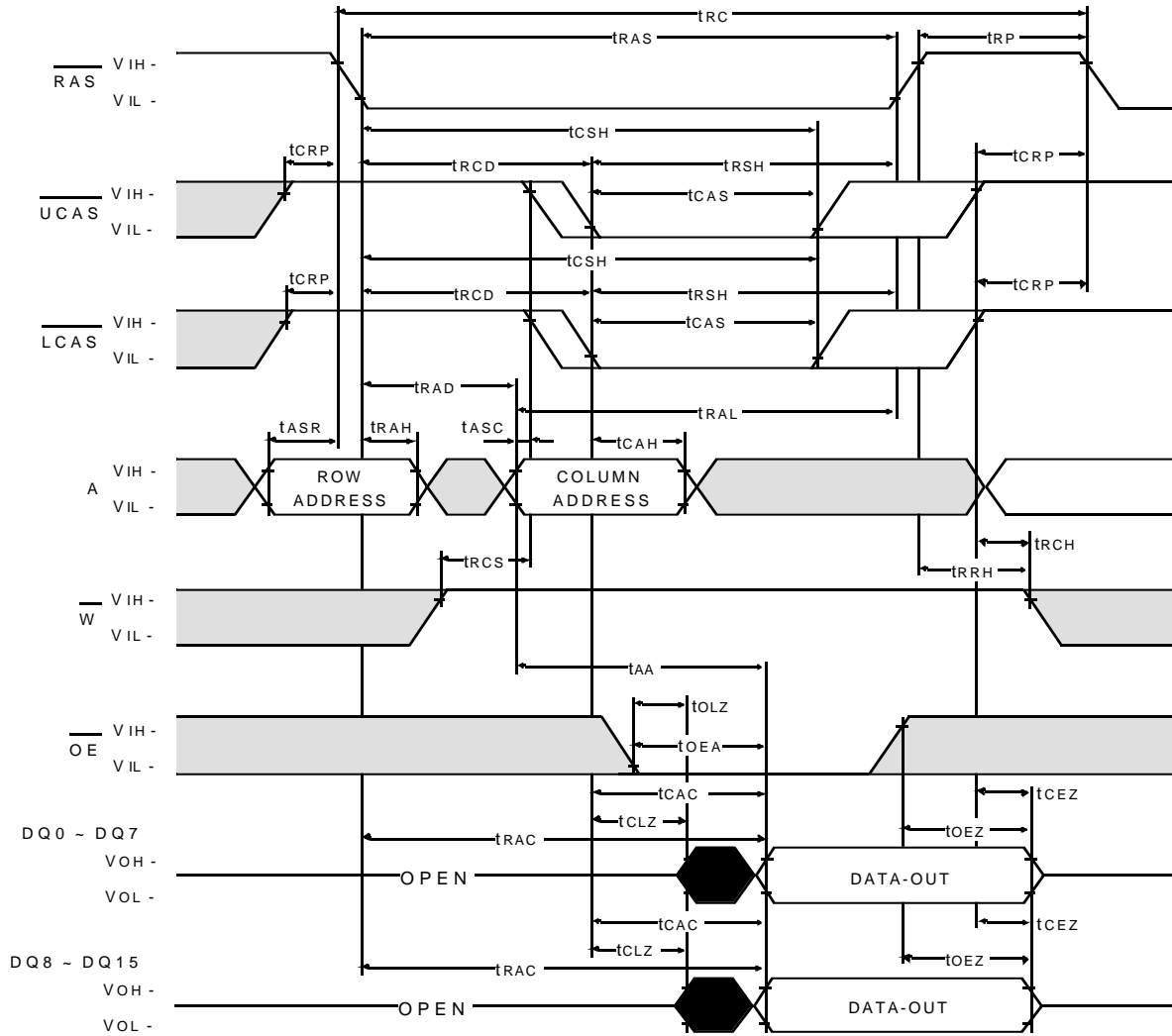
- 20. If \overline{RAS} goes high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going.
- 21. $t_{ASC} \geq 6ns$, Assume $t_T = 2.0ns$, if $t_{ASC} \leq 6ns$, then $t_{HPC}(\min)$ and $t_{CAS}(\min)$ must be increased by the value of " $6ns - t_{ASC}$ ".
- 22. If $t_{RASS} \geq 100\mu s$, then \overline{RAS} precharge time must use t_{RPS} instead of t_{RP} .
- 23. For \overline{RAS} -only-Refresh and Burst \overline{CAS} -before- \overline{RAS} refresh mode, 4096 cycles(4K/8K) of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
- 24. For distributed \overline{CAS} -before- \overline{RAS} with 15.6 μs interval, CBR refresh should be executed with in 15.6 μs immediately before and after self refresh in order to meet refresh specification.

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WORD READ CYCLE



Don't care
Undefined

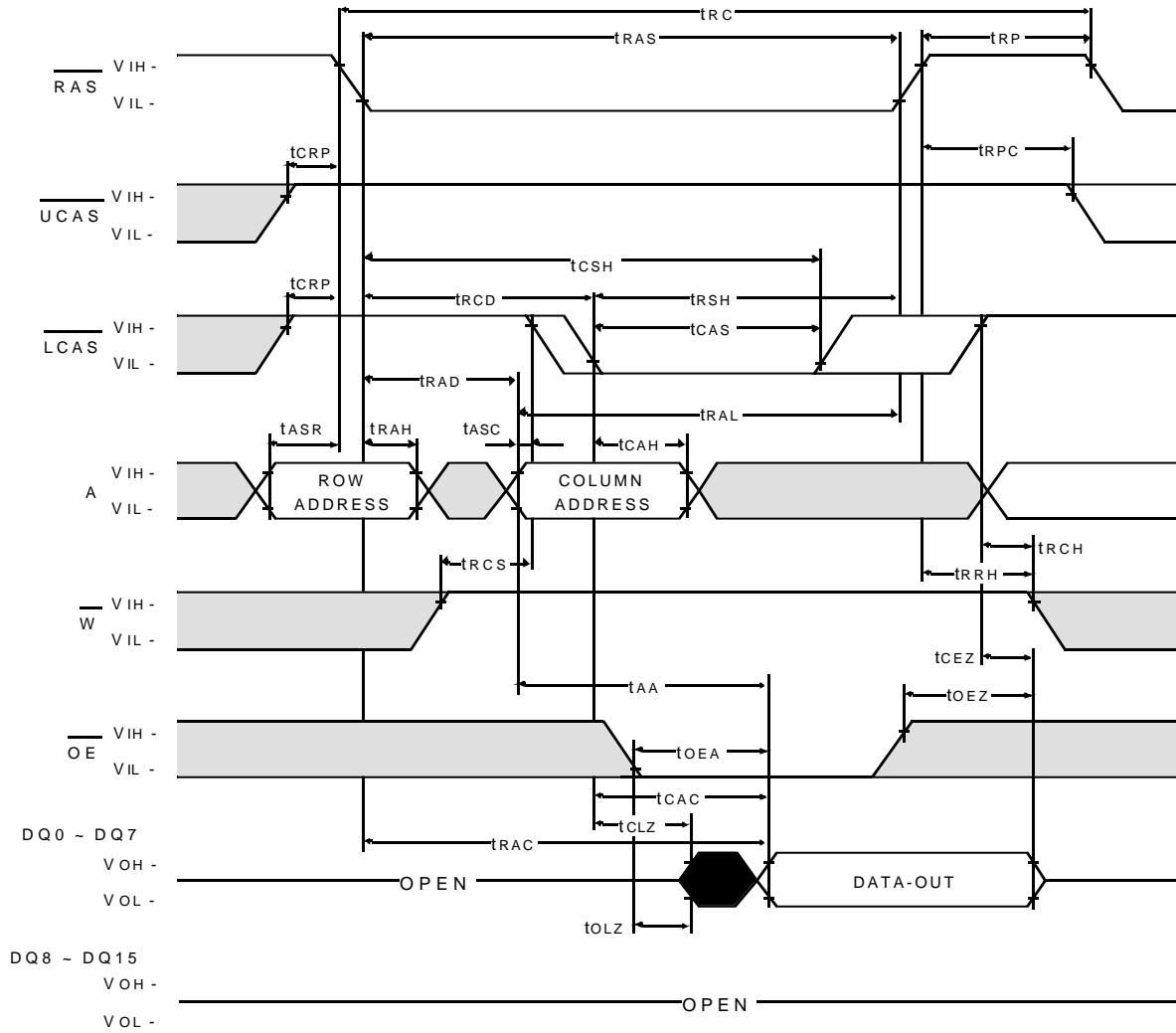
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LOWER BYTE READ CYCLE

NOTE : D IN = OPEN



□ Don't care
■ Undefined

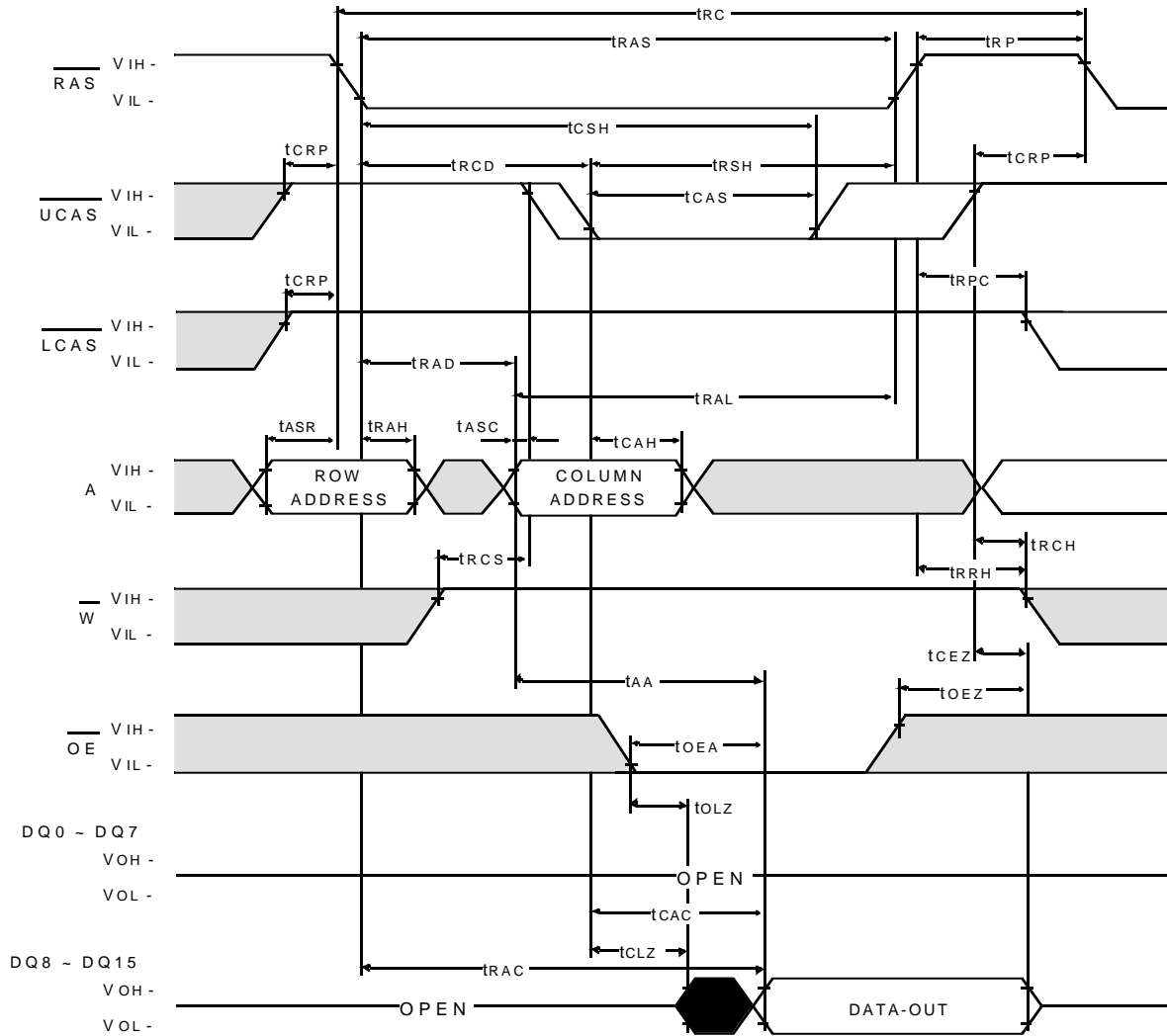
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UPPER BYTE READ CYCLE

NOTE : D IN = OPEN



□ Don't care
■ Undefined

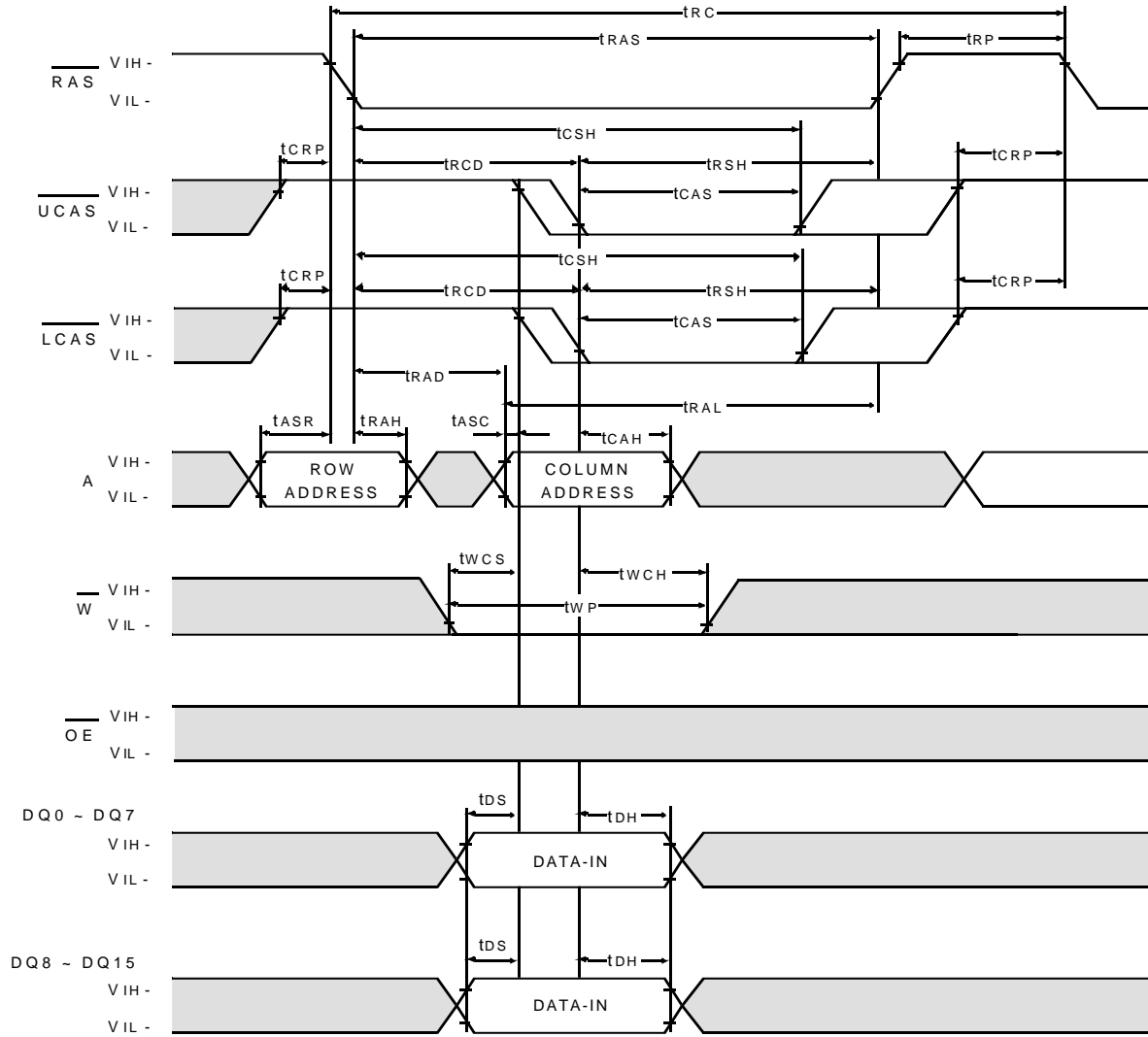
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WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



□ Don't care
■ Undefined

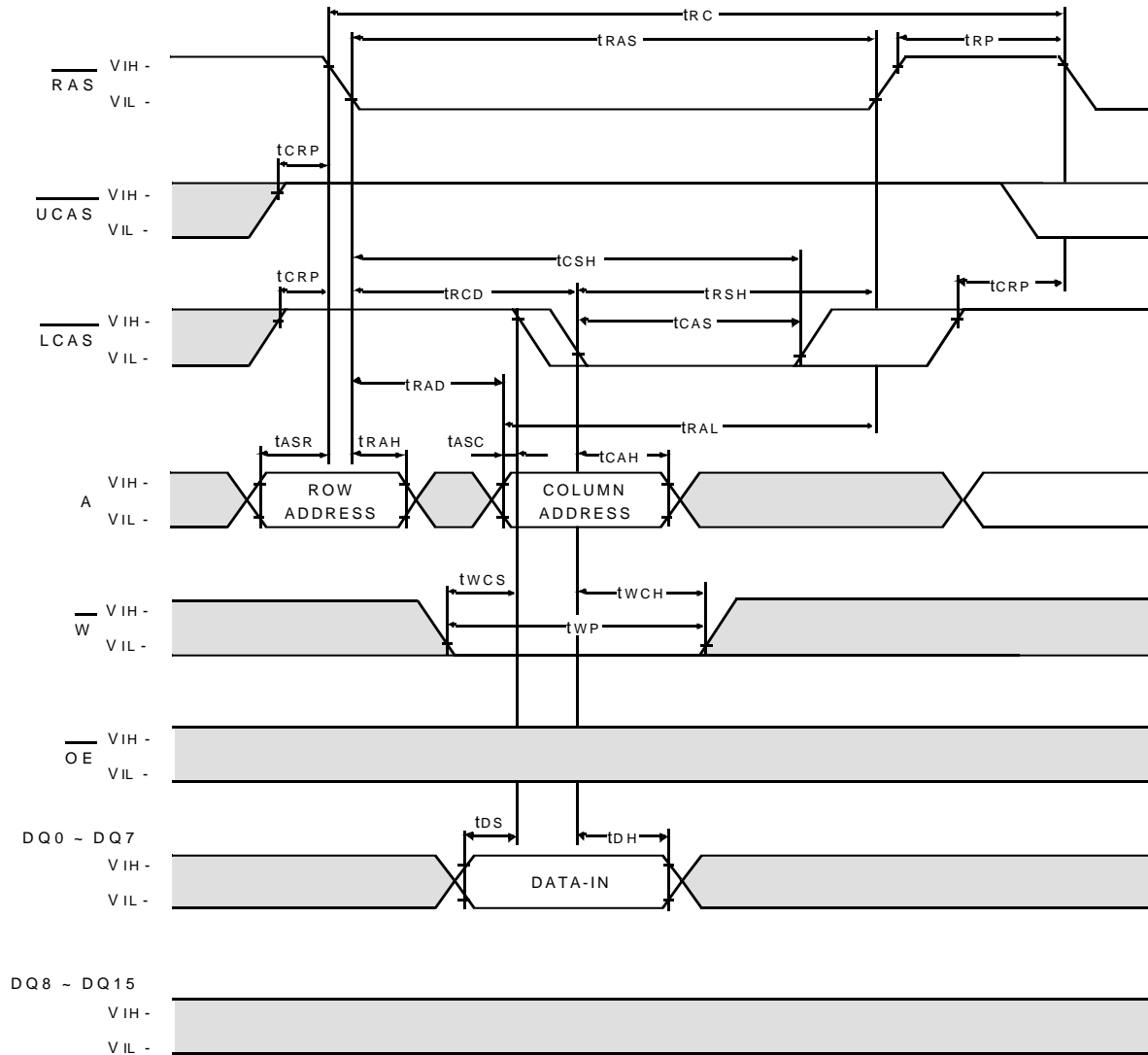
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LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



□ Don't care
■ Undefined

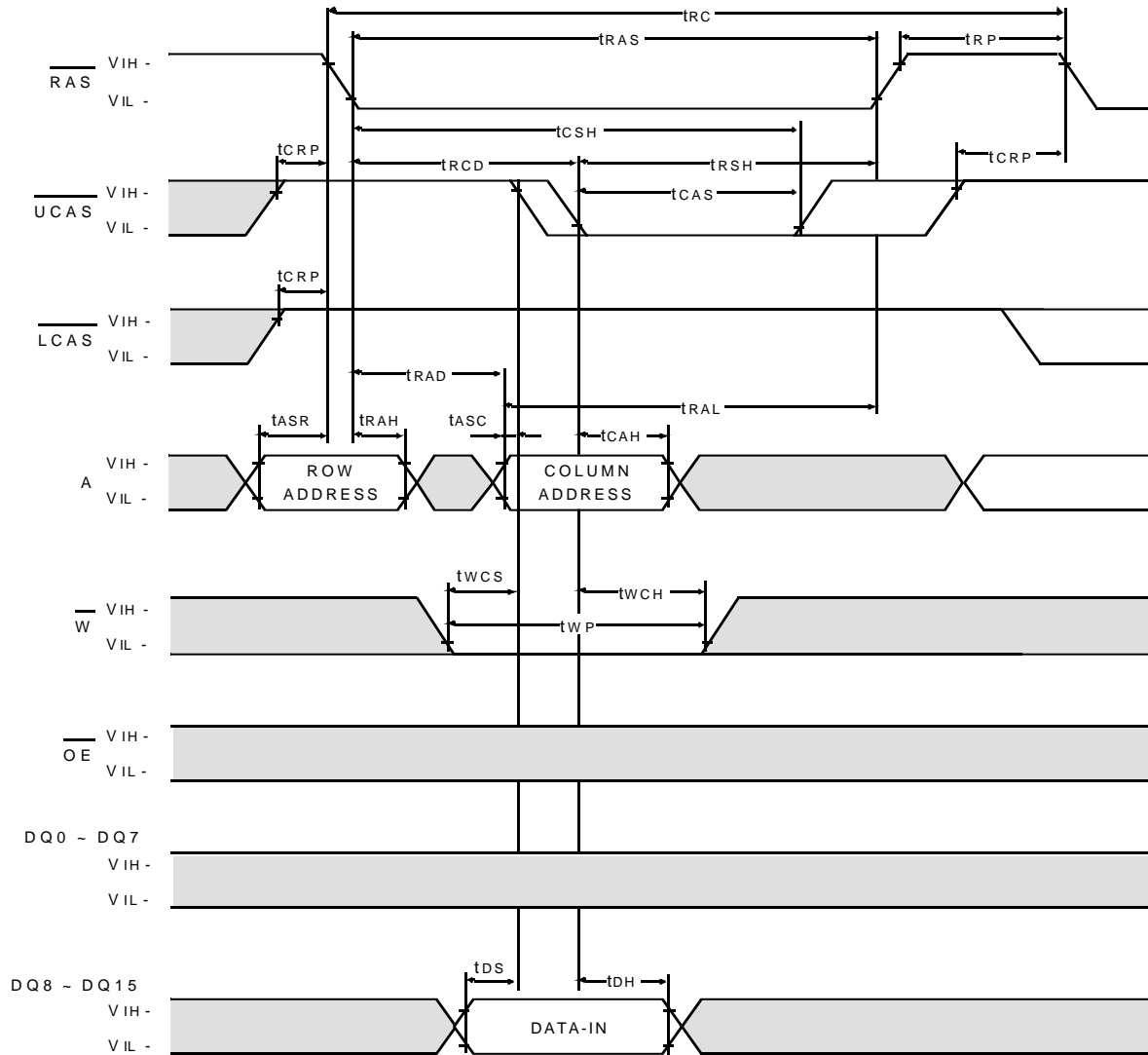
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K4E661612D, K4E641612D

CMOS DRAM

UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



□ Don't care

■ Undefined

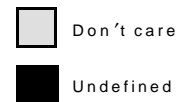
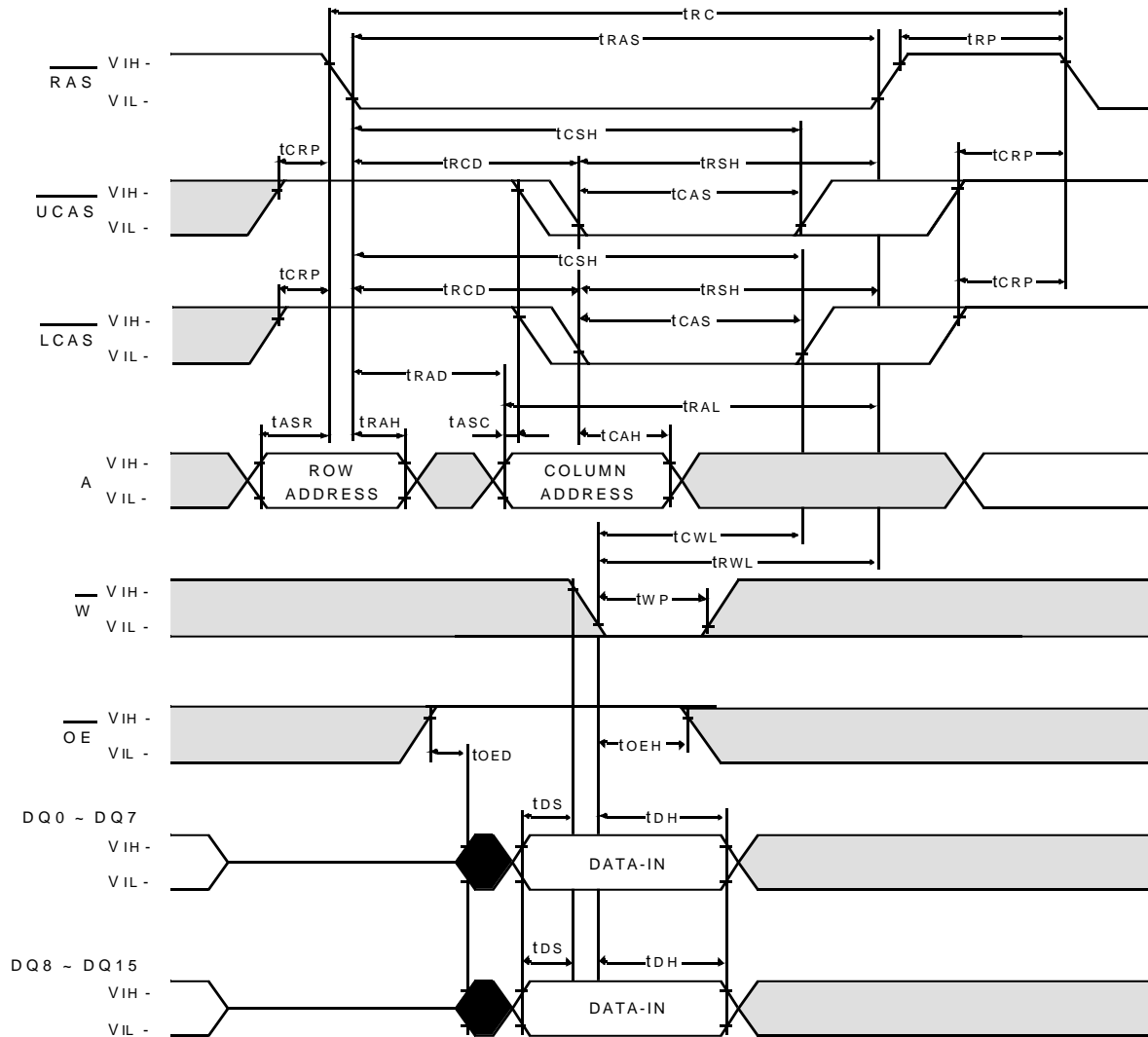
Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

WORD WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT = OPEN



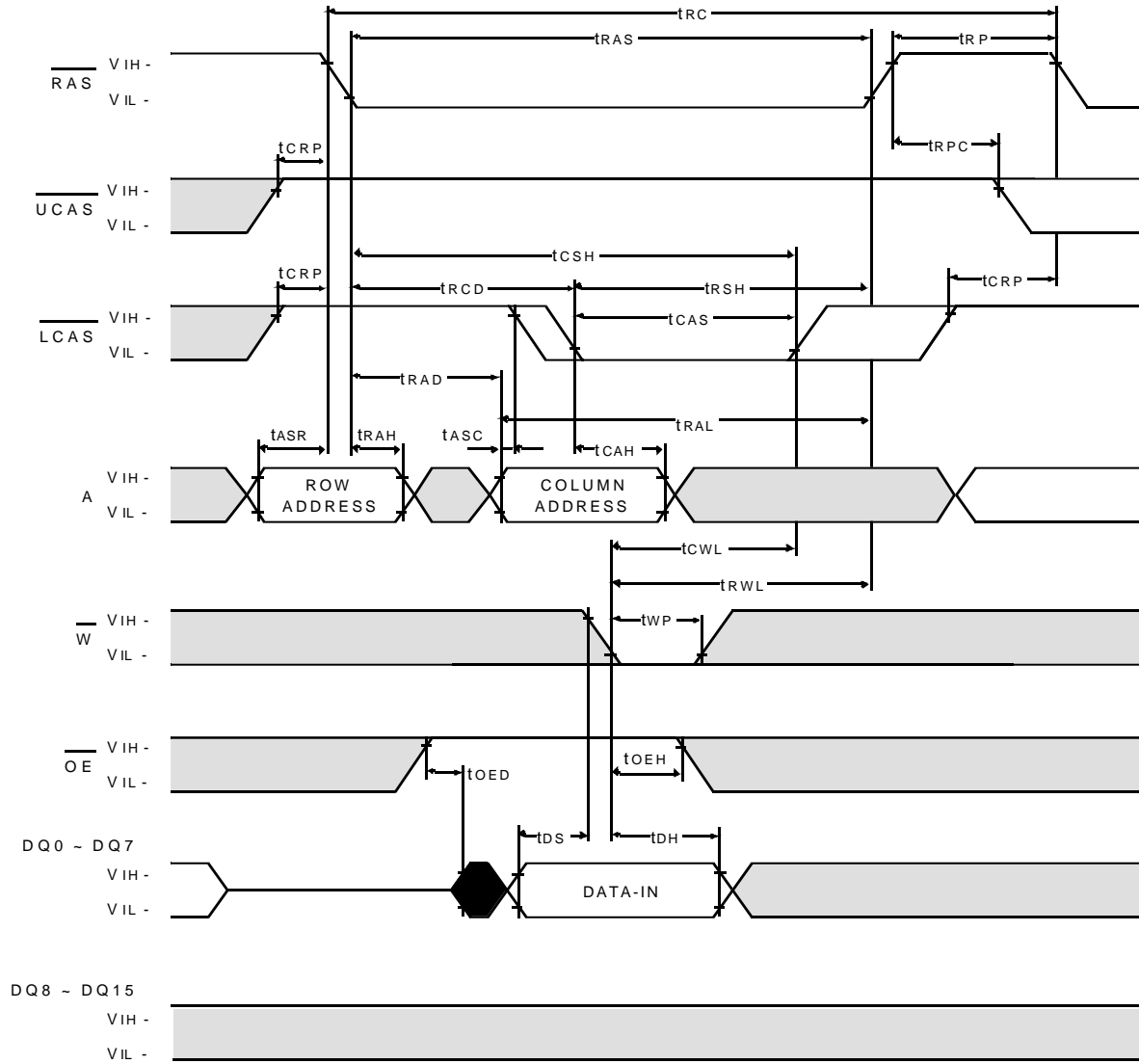
Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT = OPEN



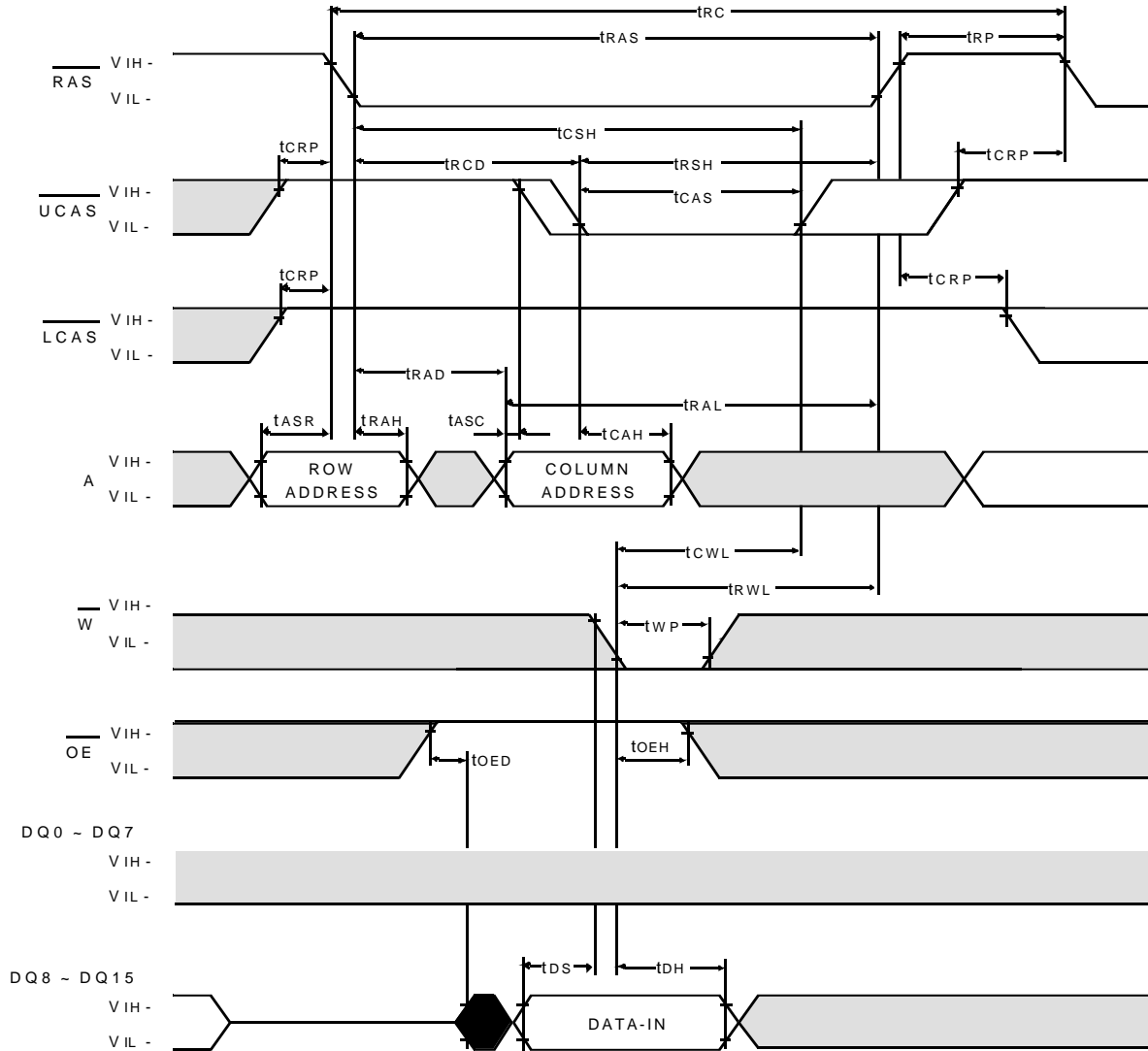
Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

UPPER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT = OPEN



Don't care

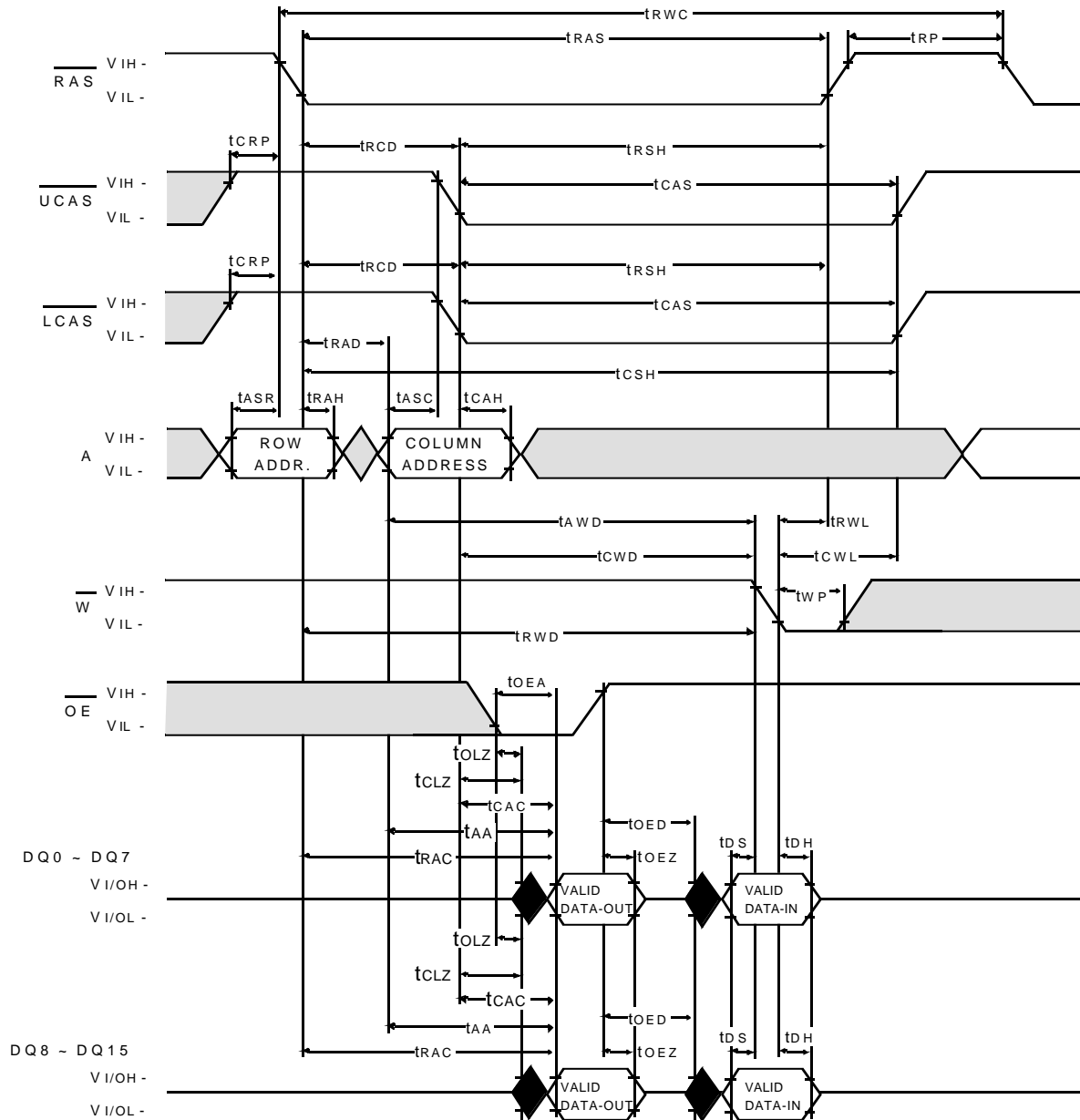
Undefined

Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

WORD READ - MODIFY - WRITE CYCLE



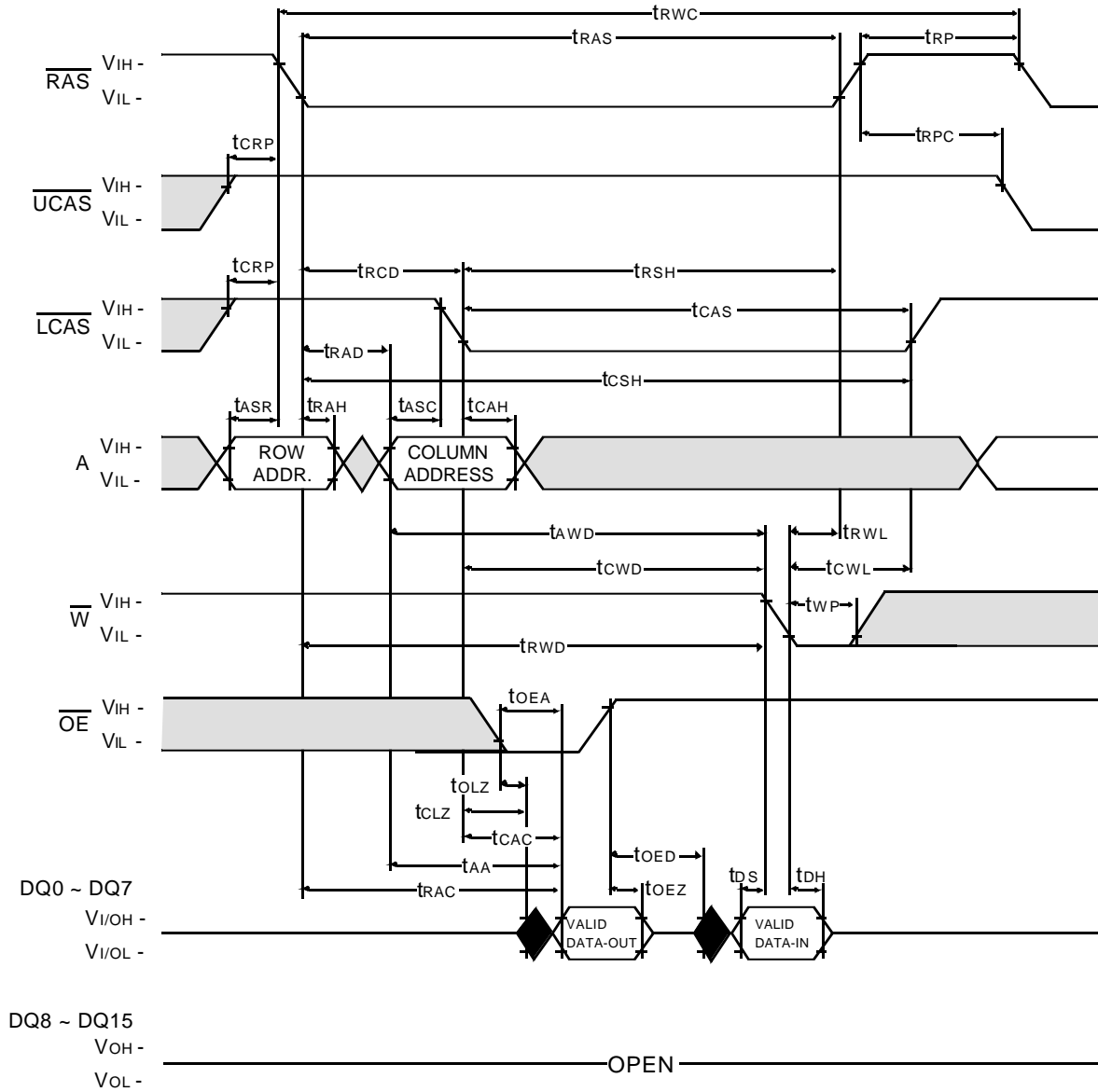
Don't care
Undefined

Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

LOWER-BYTE READ - MODIFY - WRITE CYCLE



□ Don't care

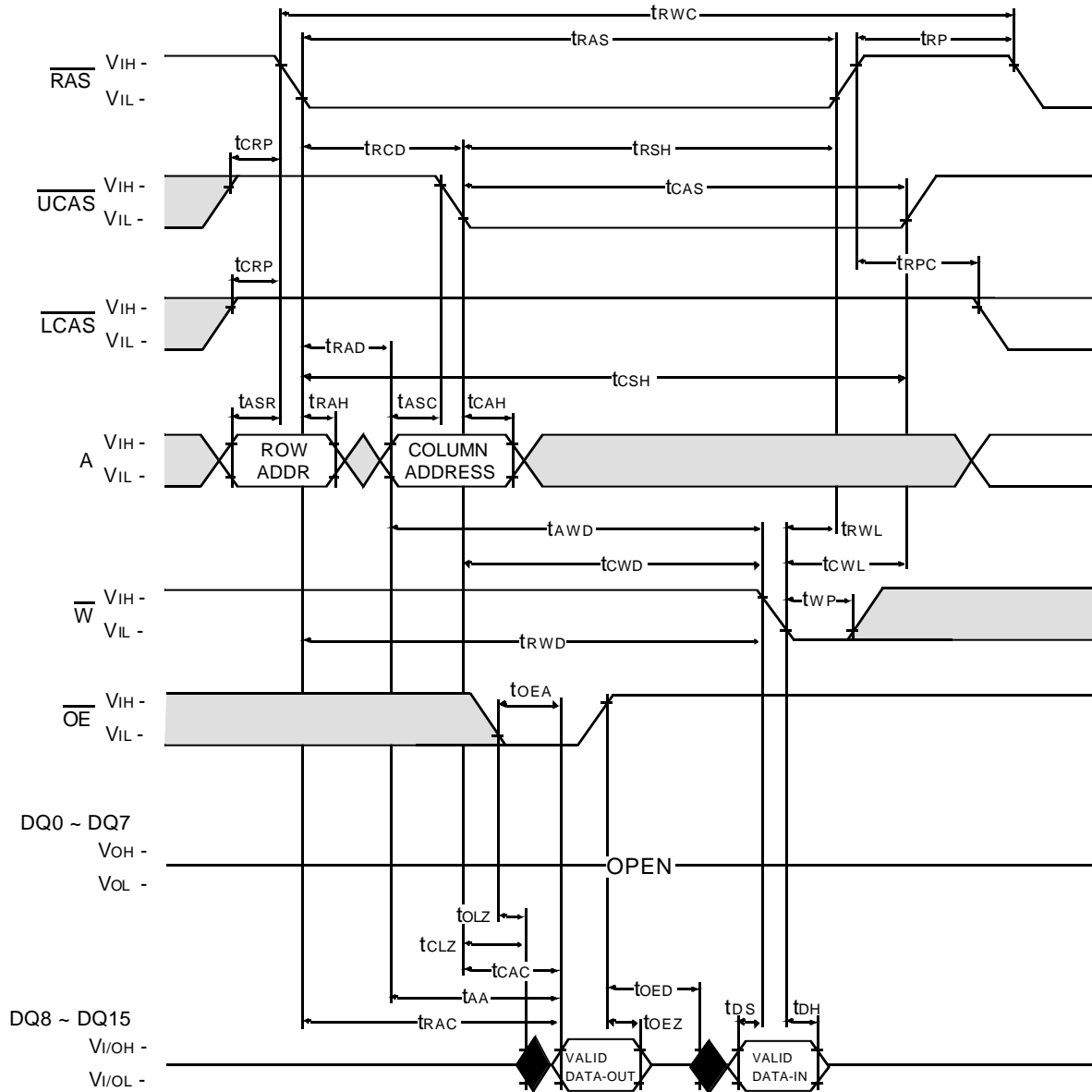
■ Undefined

Industrial Temperature

K4E661612D, K4E641612D

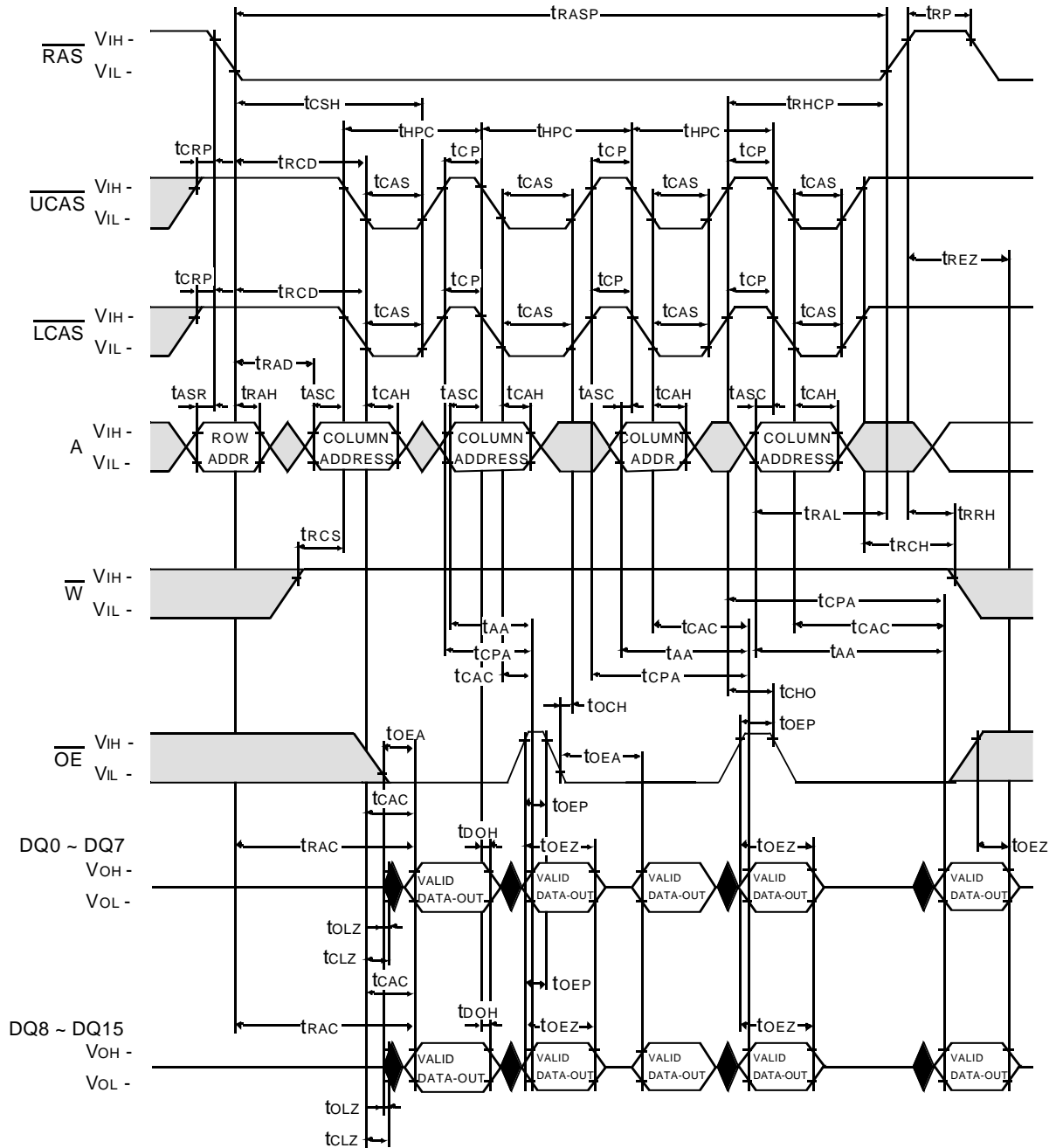
CMOS DRAM

UPPER-BYTE READ - MODIFY - WRITE CYCLE



□ Don't care
■ Undefined

HYPER PAGE MODE WORD READ CYCLE



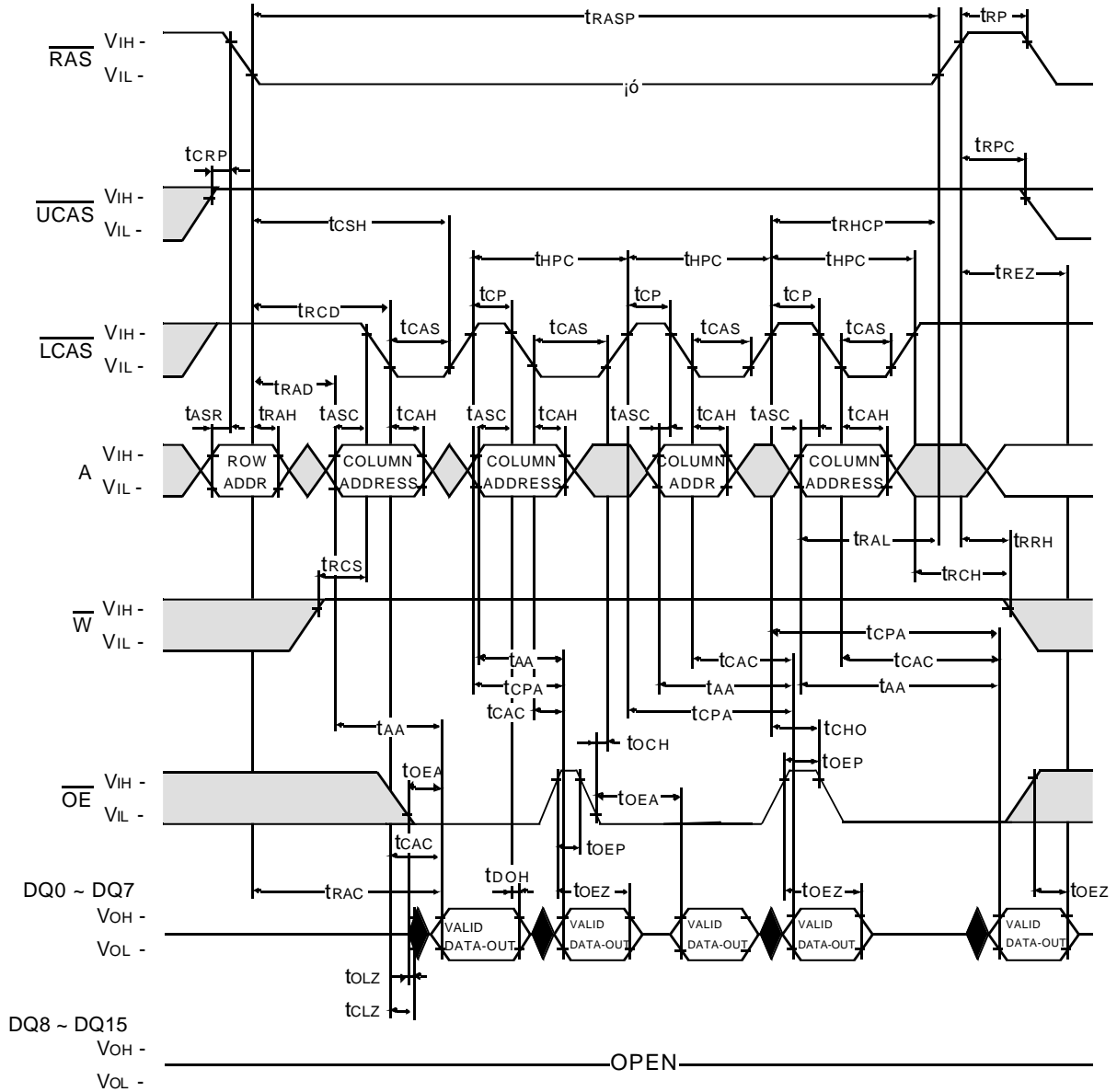
Don't care
Undefined

Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

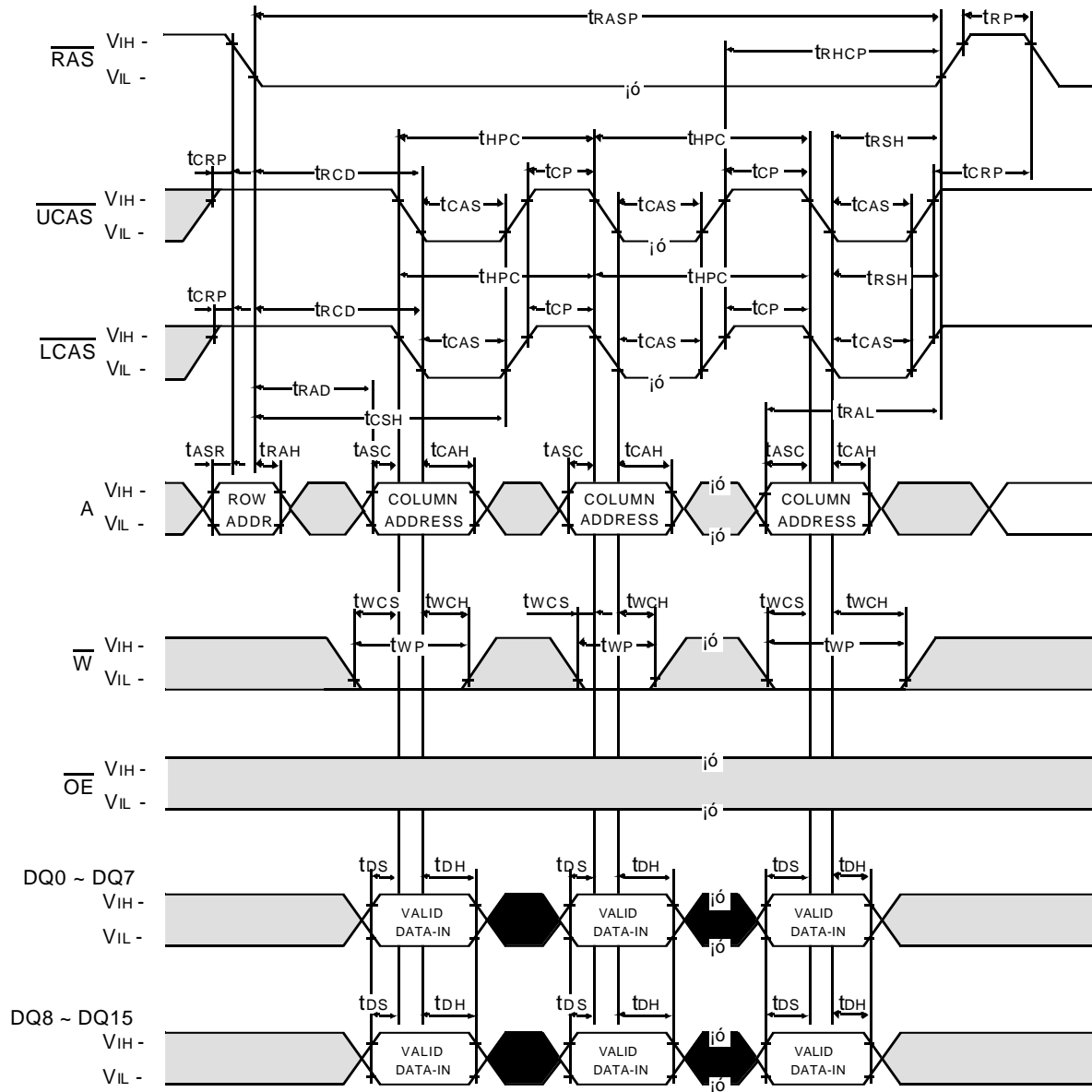
HYPER PAGE MODE LOWER BYTE READ CYCLE



Don't care
Undefined

HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



Don't care
 Undefined

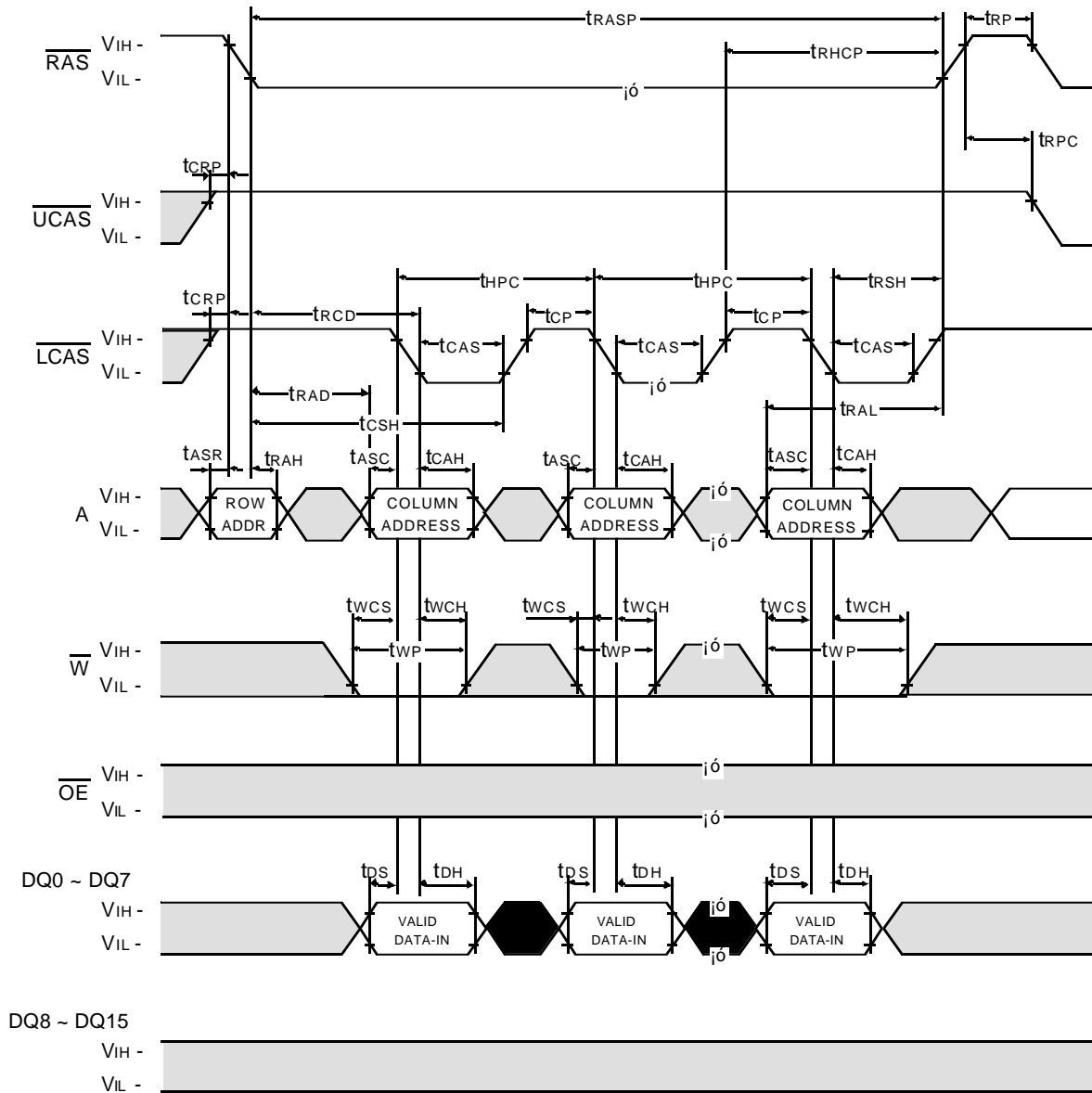
Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



Don't care
 Undefined

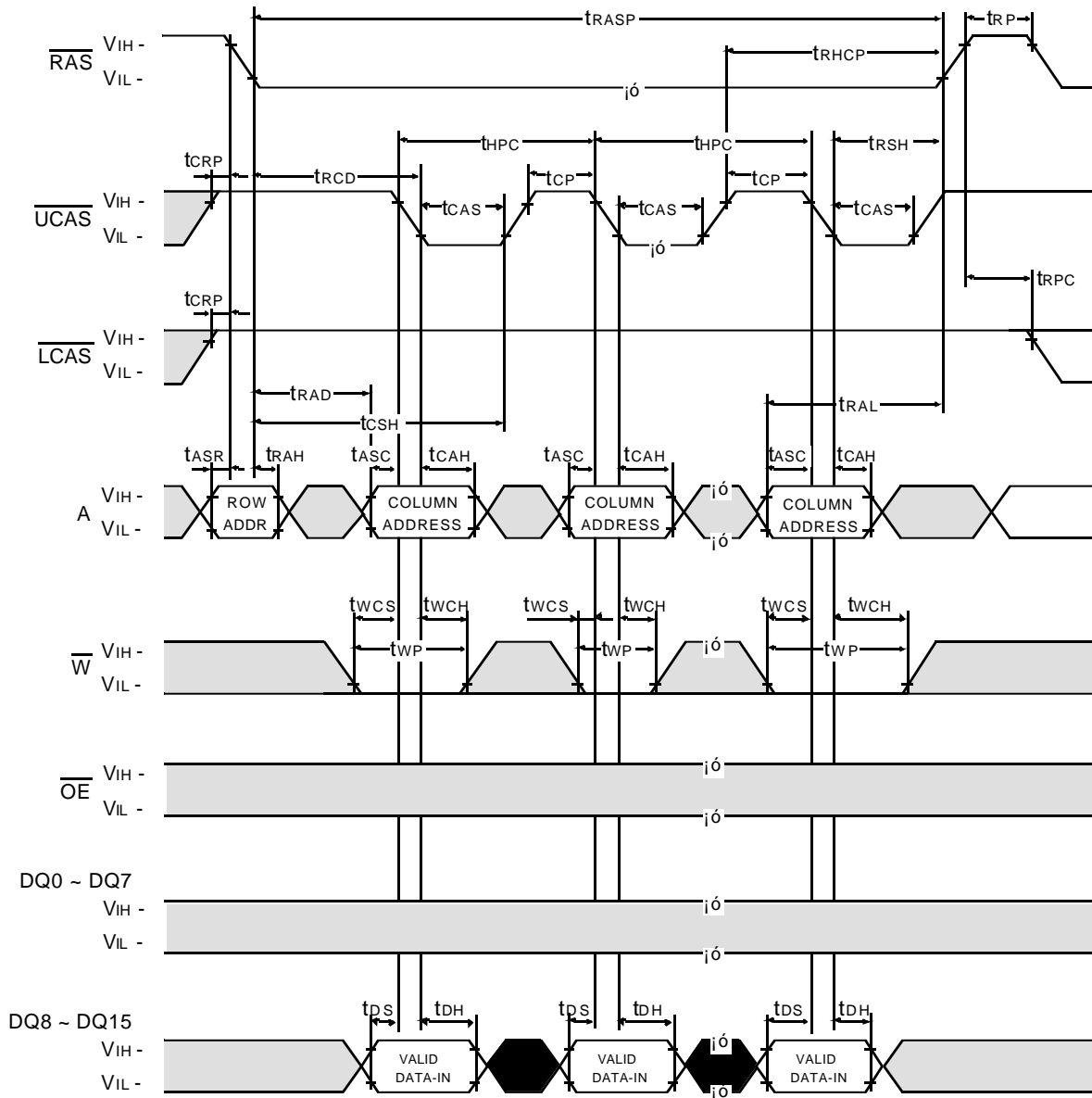
Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



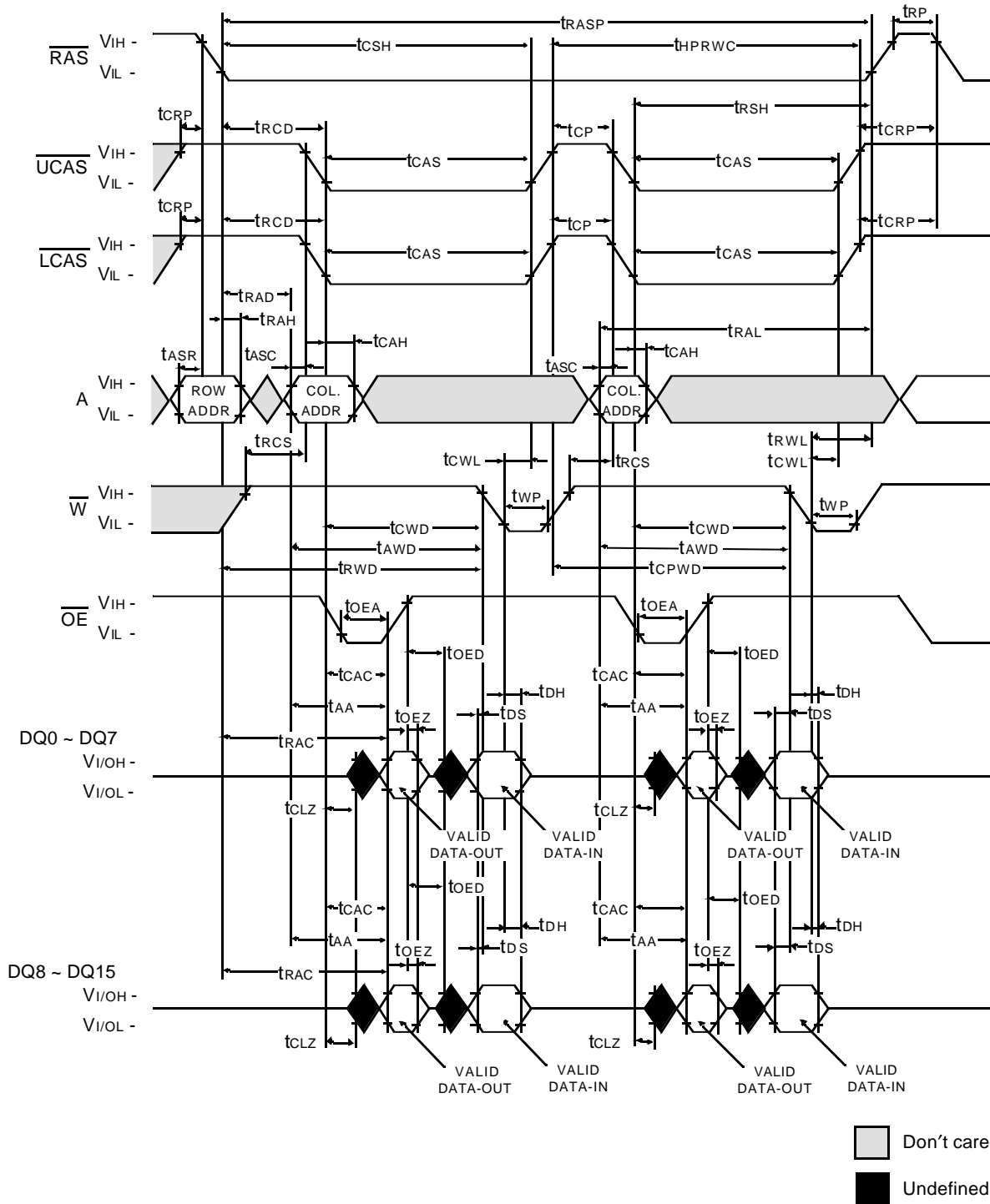
Don't care
 Undefined

Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

HYPER PAGE MODE WORD READ - MODIFY - WRITE CYCLE

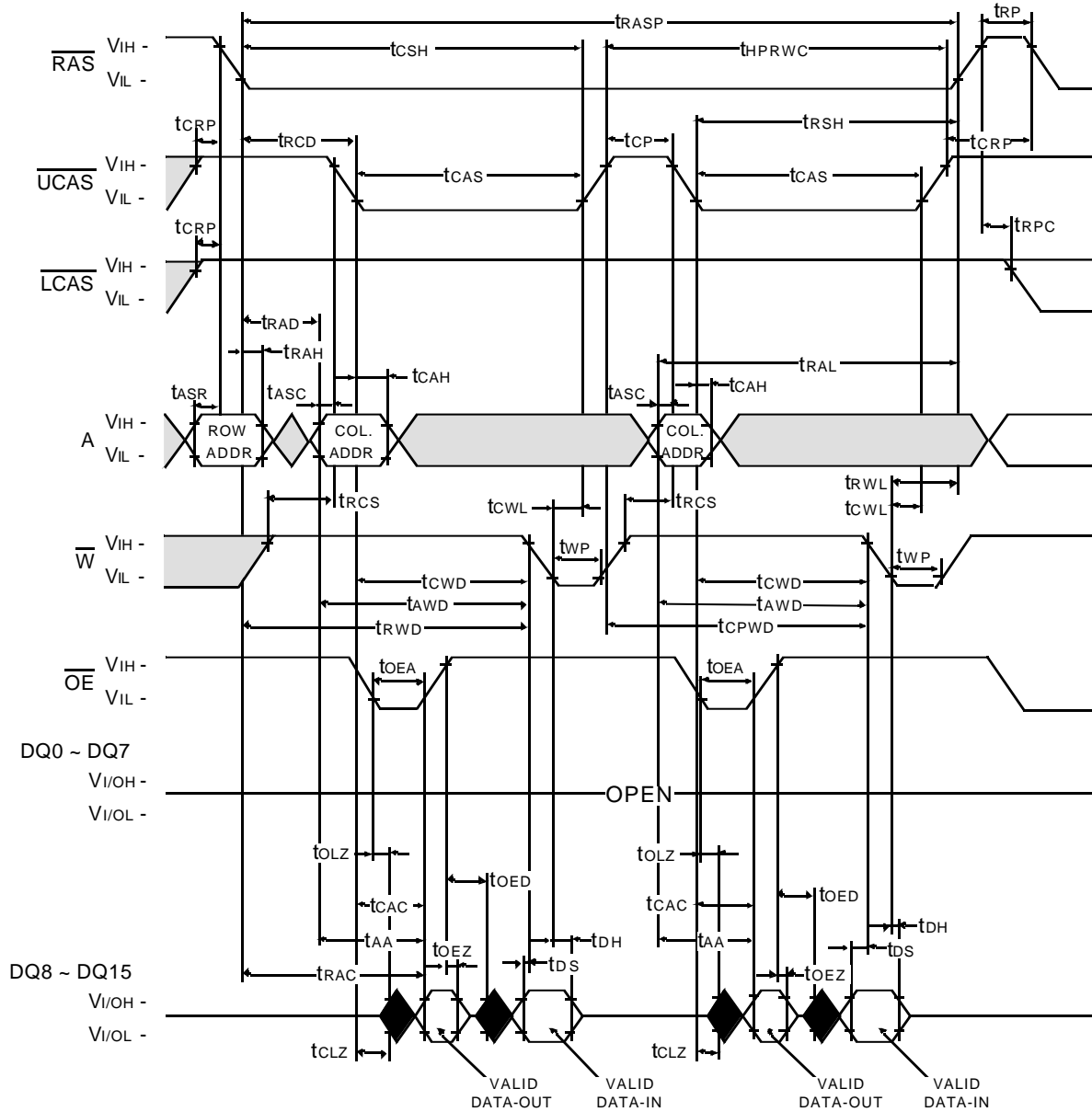


Industrial Temperature

K4E661612D, K4E641612D

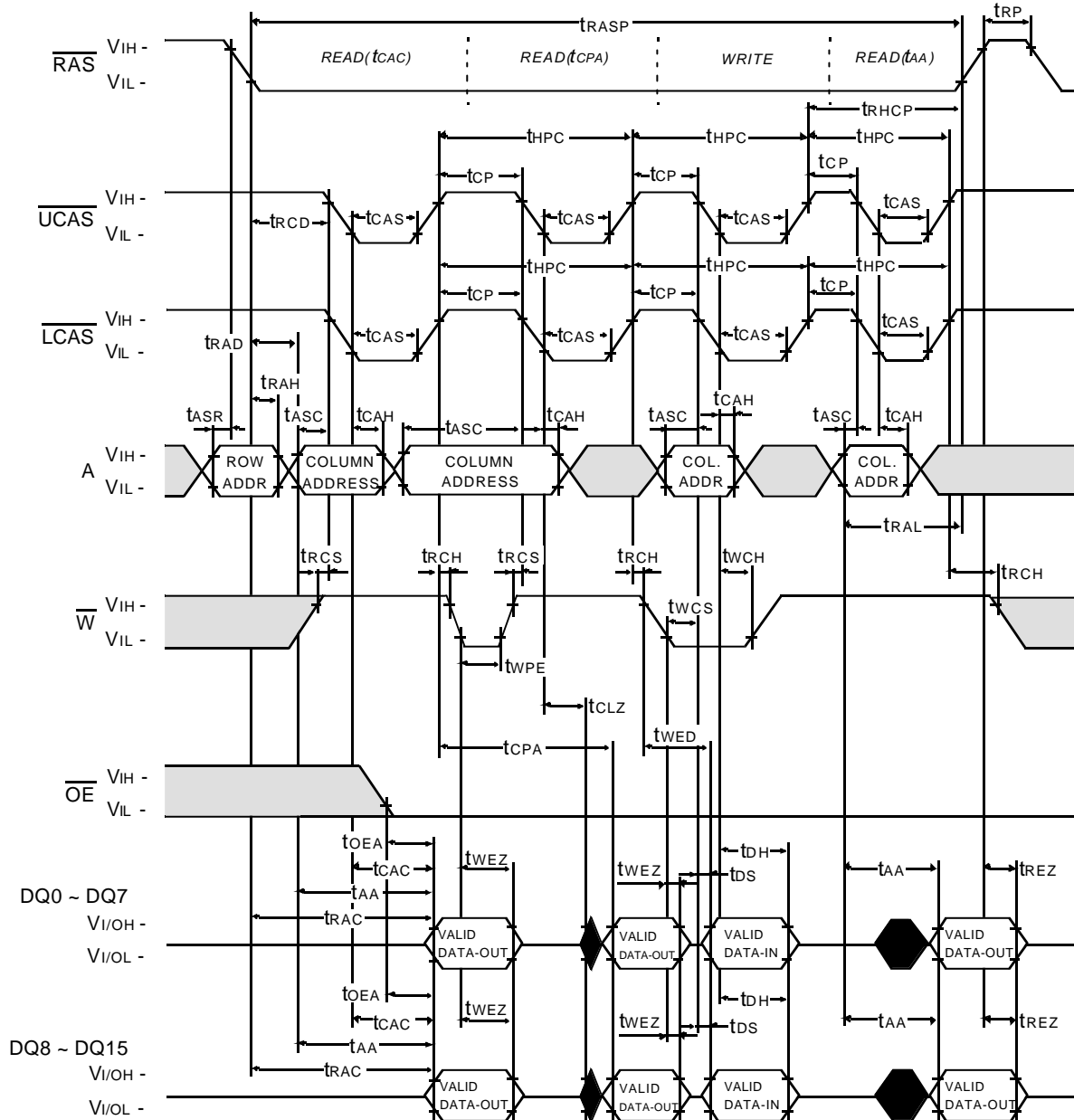
CMOS DRAM

HYPER PAGE MODE UPPER BYTE READ - MODIFY - WRITE CYCLE



Don't care
 Undefined

HYPER PAGE READ AND WRITE MIXED CYCLE



Don't care
 Undefined

Industrial Temperature

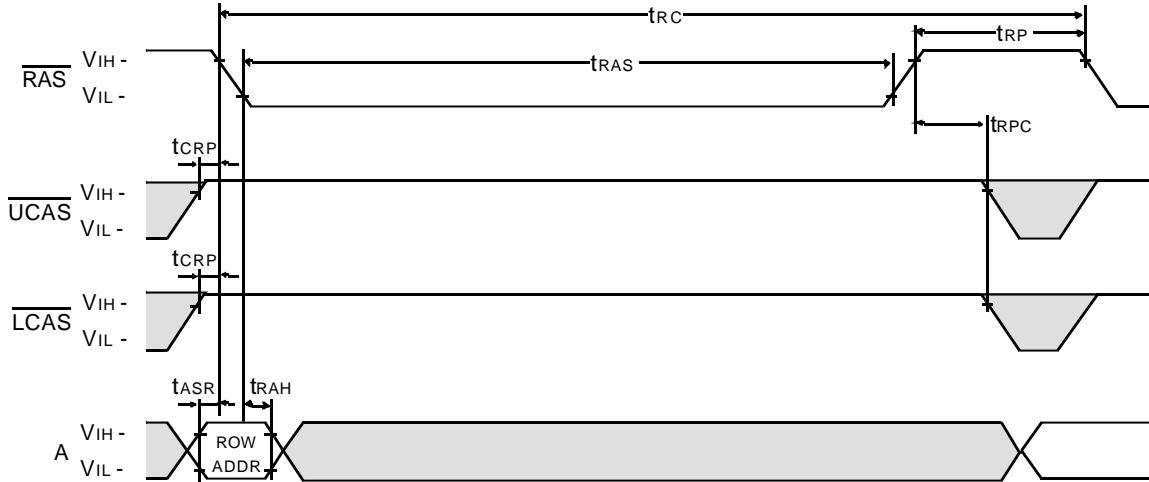
K4E661612D, K4E641612D

CMOS DRAM

RAS - ONLY REFRESH CYCLE

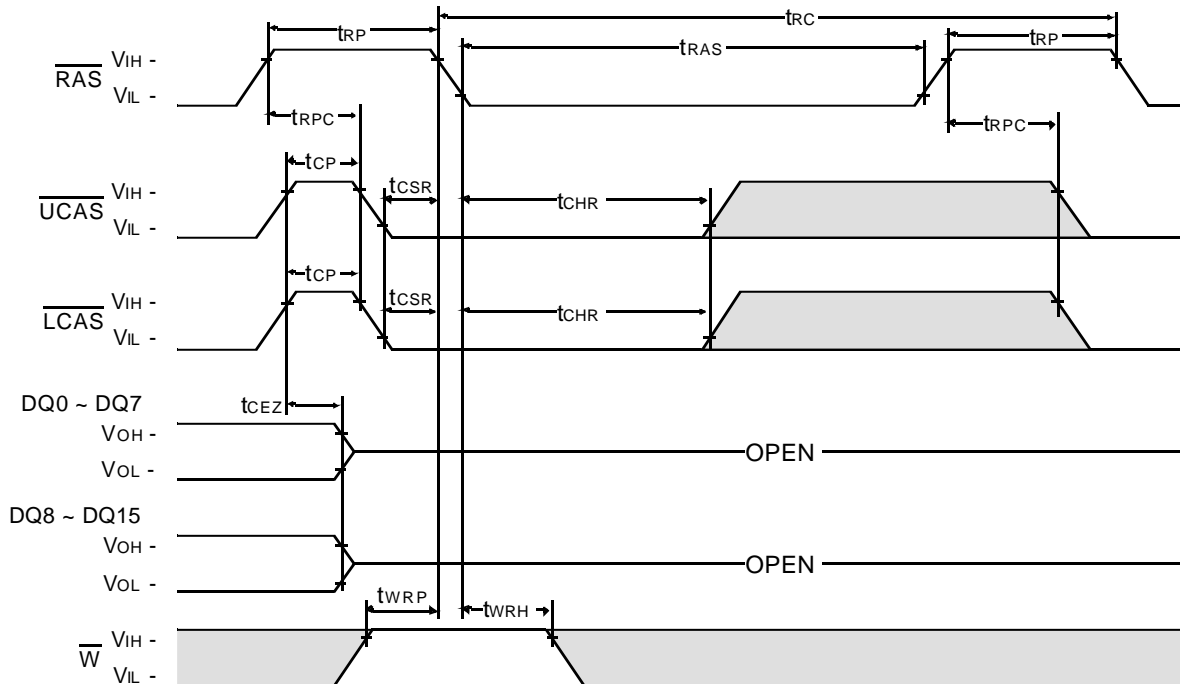
NOTE : \overline{W} , \overline{OE} , DIN = Don't care

DOUT = OPEN



CAS - BEFORE - RAS REFRESH CYCLE

NOTE : \overline{OE} , A = Don't care



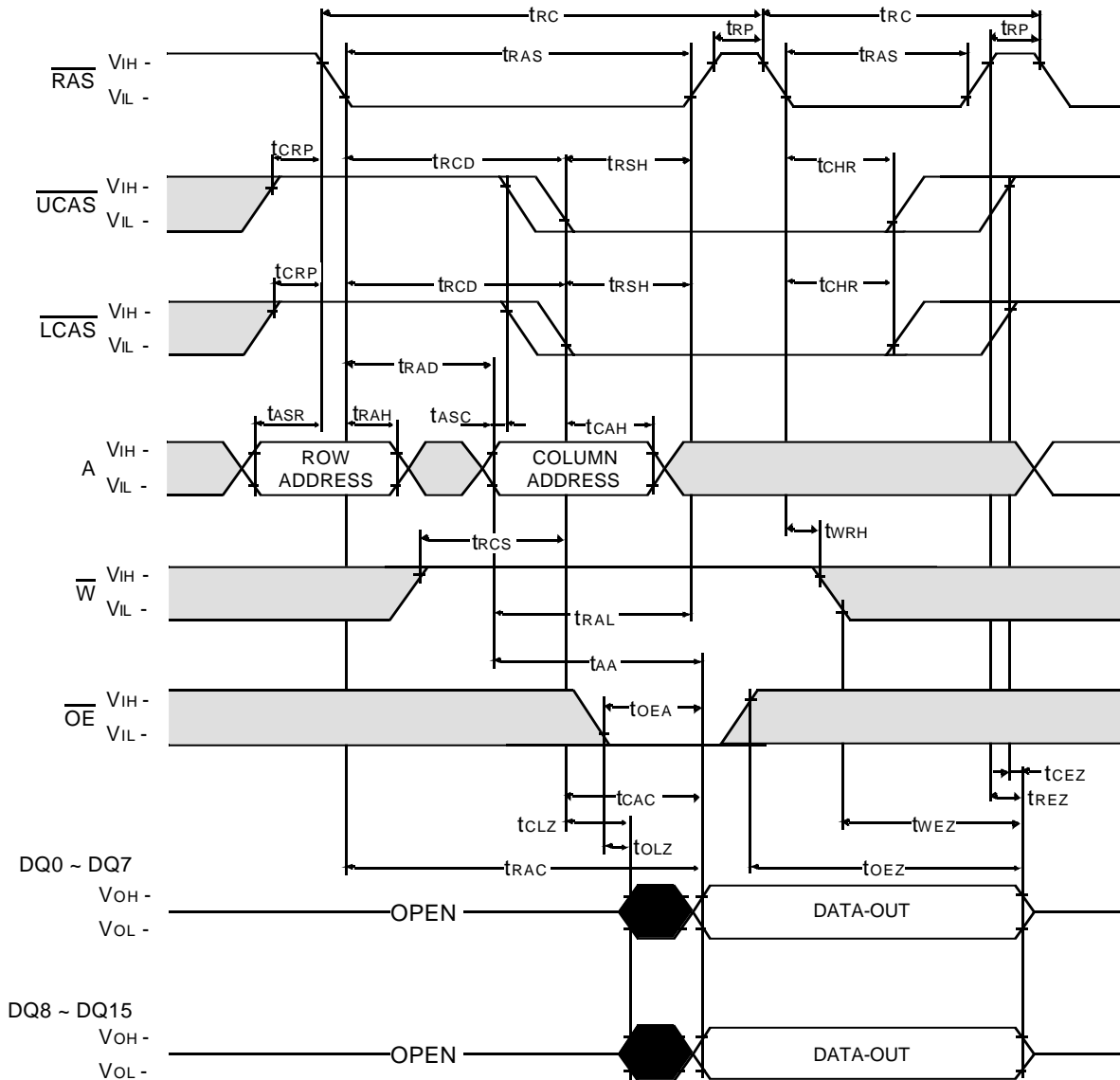
Don't care
 Undefined

Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

HIDDEN REFRESH CYCLE (READ)



Don't care
 Undefined

* In Hidden refresh cycle of 64Mb A-die & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

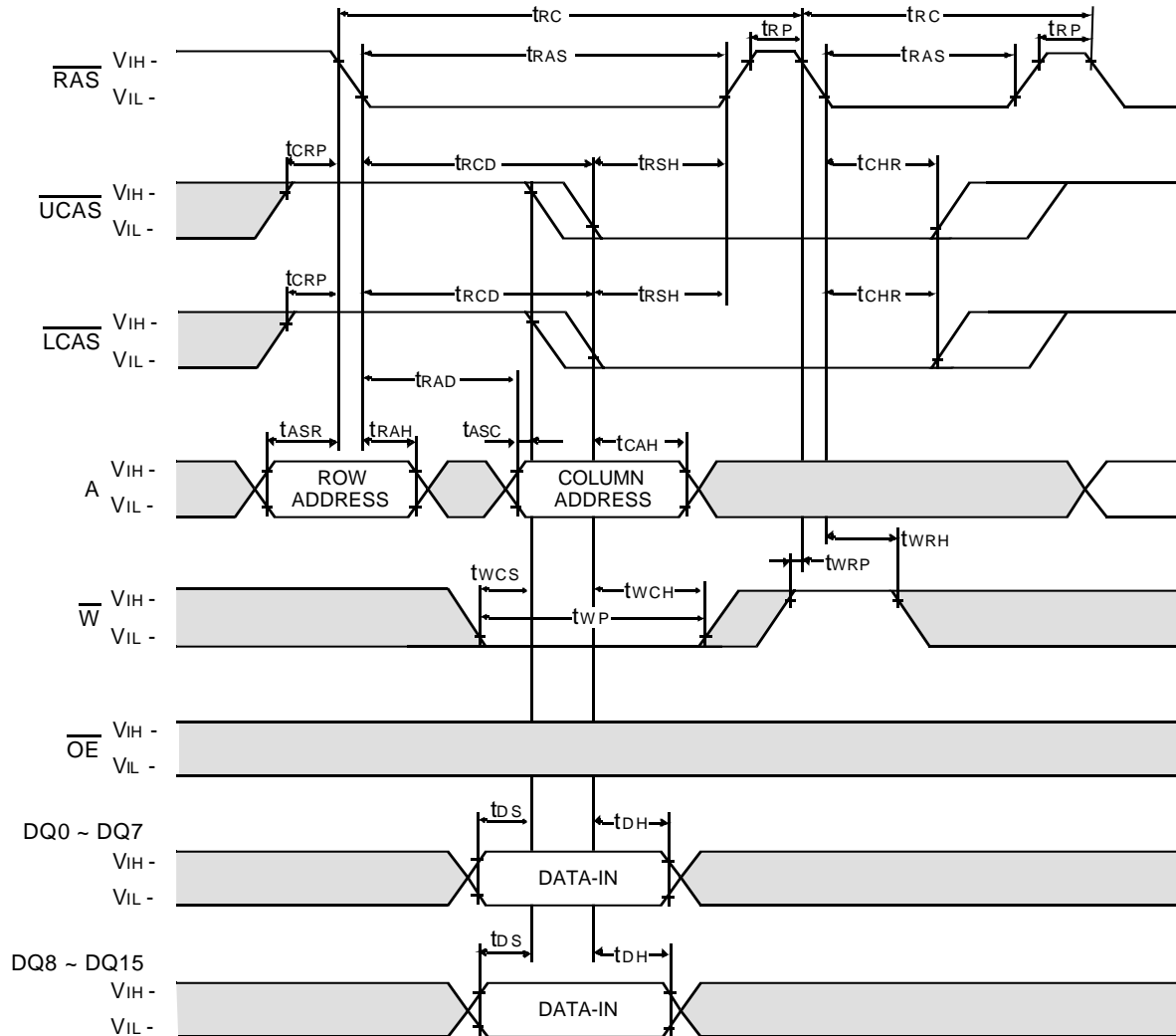
Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



□ Don't care
■ Undefined

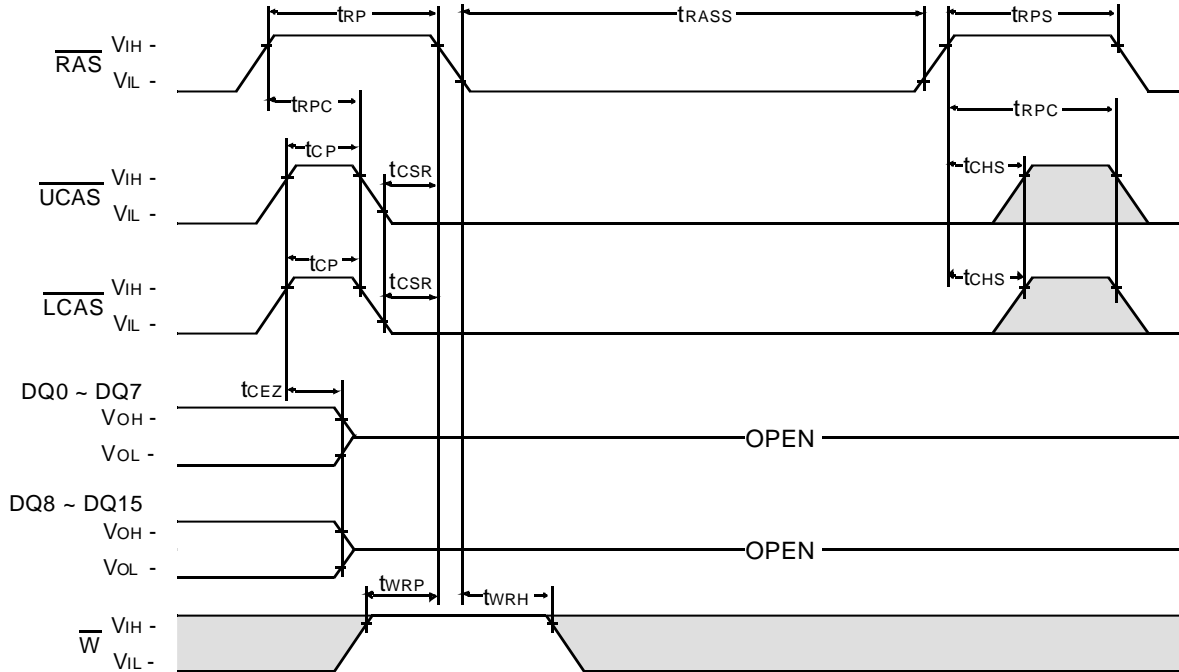
Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

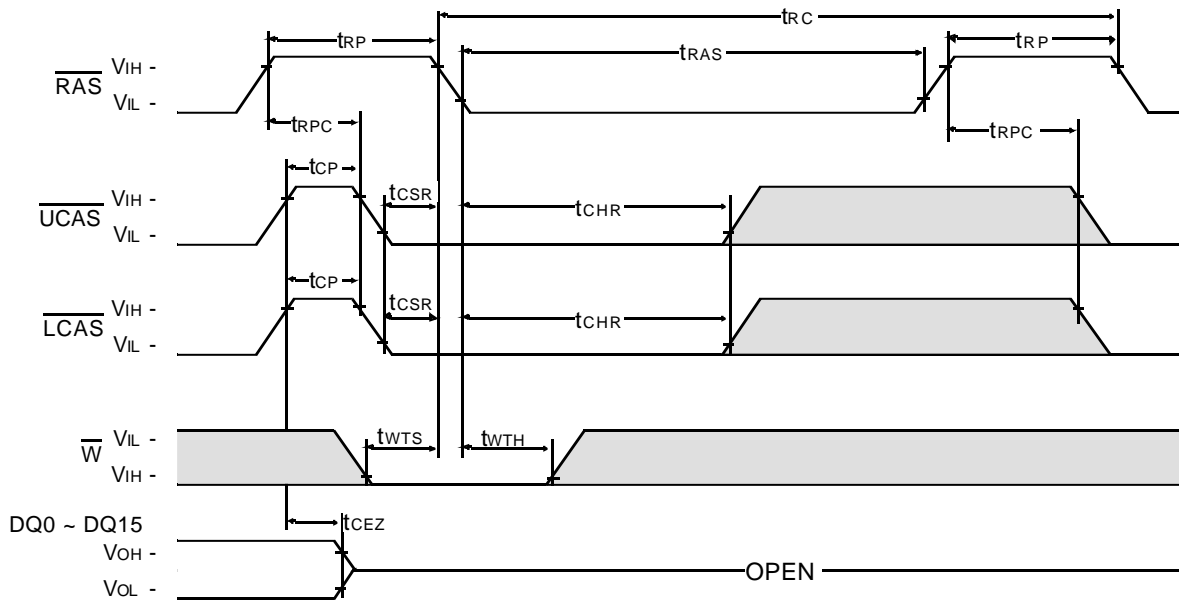
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : \overline{OE} , A = Don't care



TEST MODE IN CYCLE

NOTE : \overline{OE} , A = Don't care



Don't care
 Undefined

Industrial Temperature

K4E661612D, K4E641612D

CMOS DRAM

PACKAGE DIMENSION

