Preliminary

4Gb DDP LPDDR2-S4 SDRAM

134FBGA, 11x11.5, 2/CS, 2CKE
64M x32 + 64M x32

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	- First version for target specification. - K4P2G16(32)4C(E)C-AG_Ver 1.0	Sep. 13, 2010	Target	J.Y.Bae
0.1	- Corrected errata. - Revised Package ballout 1. Deleted ZQ1	Sep. 15, 2010	Target	J.Y.Bae
0.5	- Preliminary datasheet. - Corrected typo. - Revised DC characteristics.	Sep. 30, 2010	Preliminary	J.Y.Bae

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4Gb DDP LPDDR2-S4 SDRAM

LPDDR2-S4 SDRAM SPECIFICATION

4G = 64M x 32 + 64M x 32 (8M x 32 x 8 banks + 8M x 32 x 8 banks) 2/CS, 2CKE

1.0 KEY FEATURE

- Double-data rate architecture; two data transfers per clock cycle
- Bidirectional data strobes (DQS, $\overline{DQS}$), These are transmitted/received with data to be used in capturing data at the receiver
- Differential clock inputs (CK and $\overline{CK}$)
- Differential data strobes (DQS and $\overline{DQS}$)
- Commands & addresses entered on both positive and negative CK edges; data and data mask referenced to both edges of DQS
- 8 internal banks for concurrent operation
- Data mask (DM) for write data
- Burst Length: 4 (default), 8 or 16
- Burst Type: Sequential or Interleave
- Read & Write latency : Refer to Table 47 LPDDR2 AC Timing Table
- Auto Precharge option for each burst access
- Configurable Drive Strength
- Auto Refresh and Self Refresh Modes
- Partial Array Self Refresh and Temperature Compensated Self Refresh
- Deep Power Down Mode
- HSUL_12 compatible inputs
- VDD1/VDD2/VDDQ/VDDCA
  : 1.8V/1.2V/1.2V/1.2V
- No DLL : CK to DQS is not synchronized
- Edge aligned data output, center aligned data input
- Auto refresh duty cycle : 3.9us
- 2/CS, 2CKE

2.0 ORDERING INFORMATION

Part No.	Org.	Package	Temperature	Max Frequency	Interface
K4P4G304EC-FGC1	x32	11x11.5 134FBGA (Lead Free, Halogen Free)	Tc=-25~85'C	800Mbps (tCK=2.50ns)	HSUL_12

NOTE :
1) K4P4G304**E**C-% : VDD1=1.8V, VDD2=1.2V, VDDQ=1.2V, VDDCA=1.2V

3.0 LPDDR2 SDRAM ADDRESSING

[Table 1] LPDDR2 SDRAM Addressing

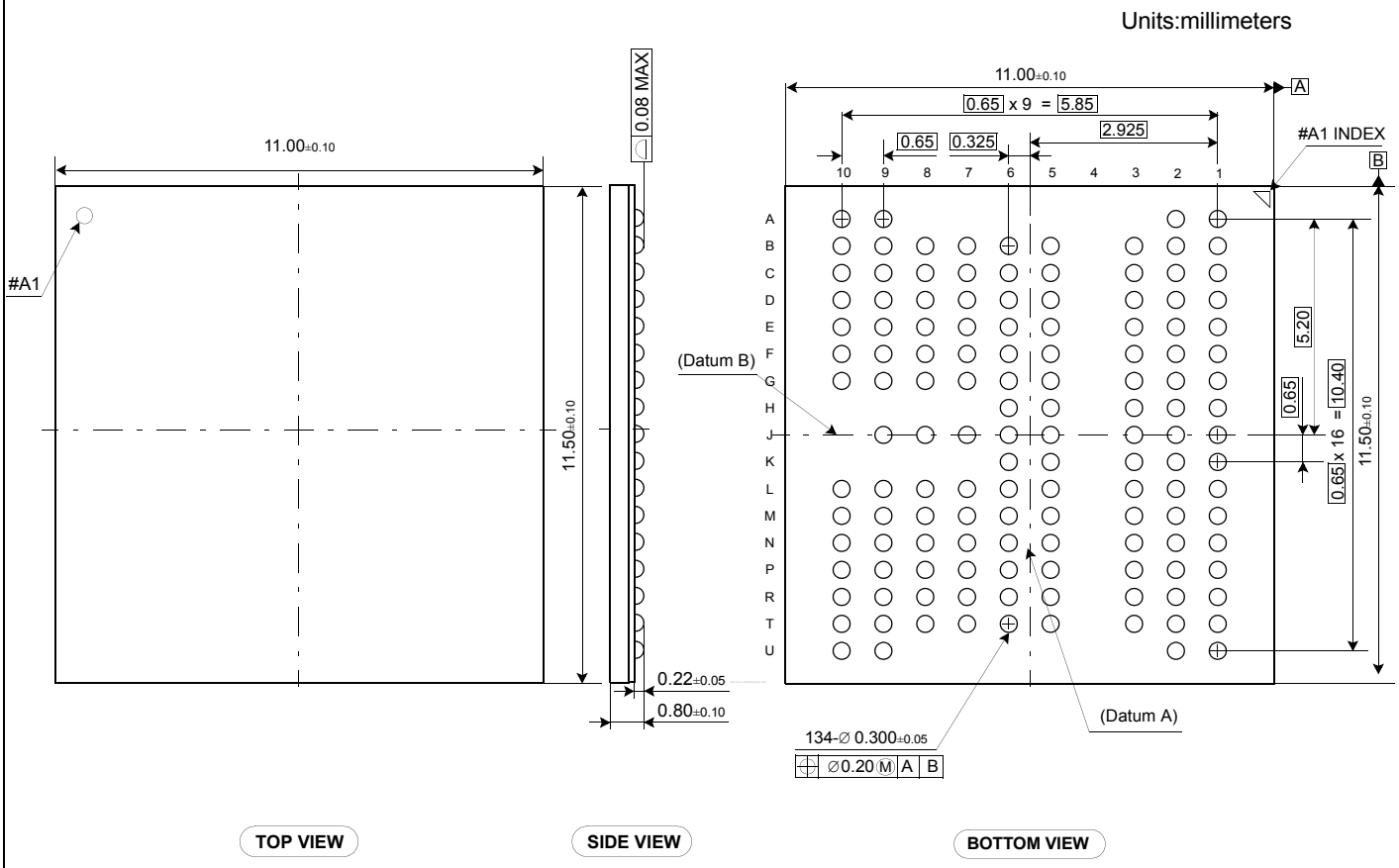
Items		2Gb
Device Type		**S4**
Number of Banks		8
Bank Addresses		BA0-BA2
t_{REFI}(us)*2		3.9
x16	Row Addresses	R0-R13
	Column Addresses*1	C0-C9
x32	Row Addresses	R0-R13
	Column Addresses*1	C0-C8

NOTE :
1) The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
2) t_{REFI} values for all bank refresh is Tc = -25~85°C, Tc means Operating Case Temperature
3) Row and Column Address values on the CA bus that are not used are “don’t care.”

4.0 PACKAGE DIMENSION & PIN DESCRIPTION

4.1 LPDDR2 SDRAM Package Dimension

134-Ball Fine pitch Ball Grid Array Package (measured in millimeters)



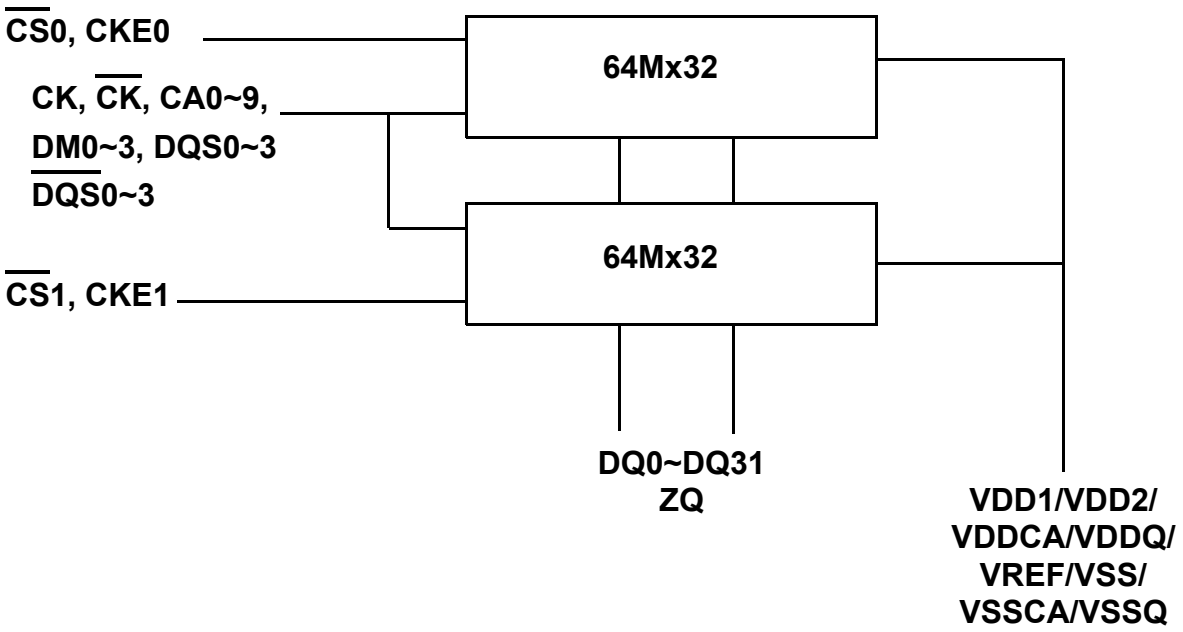
4.2 LPDDR2 SDRAM Package Ballout

134Ball FBGA										
	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU
B	DNU	NC	NC	NB	VDD2	VDD1	DQ31	DQ29	DQ26	DNU
C	VDD1	VSS	NC	NB	VSS	VSSQ	VDDQ	DQ25	VSSQ	VDDQ
D	VSS	VDD2	ZQ	NB	VDDQ	DQ30	DQ27	DQS3	$\overline{DQS3}$	VSSQ
E	VSSCA	CA9	CA8	NB	DQ28	DQ24	DM3	DQ15	VDDQ	VSSQ
F	VDDCA	CA6	CA7	NB	VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ
G	VDD2	CA5	Vref(CA)	NB	$\overline{DQS1}$	DQS1	DQ10	DQ9	DQ8	VSSQ
H	VDDCA	VSS	$\overline{CK}$	NB	DM1	VDDQ	NB	NB	NB	NB
J	VSSCA	NC	CK	NB	VSSQ	VDDQ	VDD2	VSS	Vref(DQ)	NB
K	CKE0	CKE1	NC	NB	DM0	VDDQ	NB	NB	NB	NB
L	$\overline{CS0}$	$\overline{CS1}$	NC	NB	$\overline{DQS0}$	DQS0	DQ5	DQ6	DQ7	VSSQ
M	CA4	CA3	CA2	NB	VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ
N	VSSCA	VDDCA	CA1	NB	DQ19	DQ23	DM2	DQ0	VDDQ	VSSQ
P	VSS	VDD2	CA0	NB	VDDQ	DQ17	DQ20	DQS2	$\overline{DQS2}$	VSSQ
R	VDD1	VSS	NC	NB	VSS	VSSQ	VDDQ	DQ22	VSSQ	VDDQ
T	DNU	NC	NC	NB	VDD2	VDD1	DQ16	DQ18	DQ21	DNU
U	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU

[Top View]

4.3 Input/output functional description

4.3.1 Functional Block Diagram



4.4 Input/output functional description

4.4.1 Pin Definition and Description

[Table 2] Pin Definition and Description

Name	Type	Description
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK. Single Data Rate (SDR) inputs, $\overline{CS}$ and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK and $\overline{CK}$. The positive Clock edge is defined by the crosspoint of a rising CK and a falling $\overline{CK}$. The negative Clock edge is defined by the crosspoint of a falling CK and a rising $\overline{CK}$.
CKE0, CKE1	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command truth table on page 23 for command code descriptions. CKE is sampled at the positive Clock edge.
$\overline{CS0}$, $\overline{CS1}$	Input	**Chip Select:** $\overline{CS}$ is considered part of the command code. See Command truth table on page 23 for command code descriptions. $\overline{CS}$ is sampled at the positive Clock edge.
CA0 - CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code. See Command truth table on page 23 for command code descriptions.
DQ0 - DQ31	I/O	**Data Inputs/Outputs:** Bi-directional data bus
DQS0 - DQS3 $\overline{DQS0}$ - $\overline{DQS3}$	I/O	**Data Strobes (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and Differential (DQS and $\overline{DQS}$). It is output with read data and input with write data. DQS is edge-aligned to read data and centered with write data. For x16, DQS0 and $\overline{DQS0}$ correspond to the data on DQ0 - DQ7, DQS1 and $\overline{DQS1}$ to the data on DQ8 - DQ15. For x32, DQS0 and $\overline{DQS0}$ correspond to the data on DQ0 - DQ7, DQS1 and $\overline{DQS1}$ to the data on DQ8 - DQ15, DQS2 and $\overline{DQS2}$ to the data on DQ16 - DQ23, DQS3 and $\overline{DQS3}$ to the data on DQ24 - DQ31.
DM0 - DM3	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM is for input only, the DM loading shall match the DQ and DQS (or $\overline{DQS}$). For x32 devices, DM0 is the input data mask signal for the data on DQ0-7, DM1 is the input data mask signal for the data on DQ8-15, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
V_{DD1}	Supply	**Core Power Supply 1:** Core power supply.
V_{DD2}	Supply	**Core Power Supply 2:** Core power supply.
V_{DDCA}	Supply	**Input Receiver Power Supply:** Power supply for CA0-9, CKE, CS, CK, and $\overline{CK}$ input buffers.
V_{DDQ}	Supply	**I/O Power Supply:** Power supply for Data input/output buffers.
V_{Ref} (CA)	Supply	**Reference Voltage for CA Input Receiver:** Reference voltage for all CA0-9, CKE, CS, CK, and $\overline{CK}$ input buffers.
V_{Ref} (DQ)	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all Data input buffers.
V_{SS}	Supply	**Ground**
V_{SSCA}	Supply	**Ground for Input Buffers (Receivers)**
V_{SSQ}	Supply	**I/O Ground**
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

NOTE :
1) Data includes DQ and DM.

5.0 FUNCTIONAL DESCRIPTION

This device contains the following number of bits:

4Gb has 2,147,483,648 bits + 2,147,483,648 bits

LPDDR2-S4 uses a double data rate archiecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

LPDDR2-S4 uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For LPDDR2-S4 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR2 must be initialized.

5.1 Simplified LPDDR2-S4 State Diagram

LPDDR2-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see datasheet of [Command Definition & Timing Diagram].

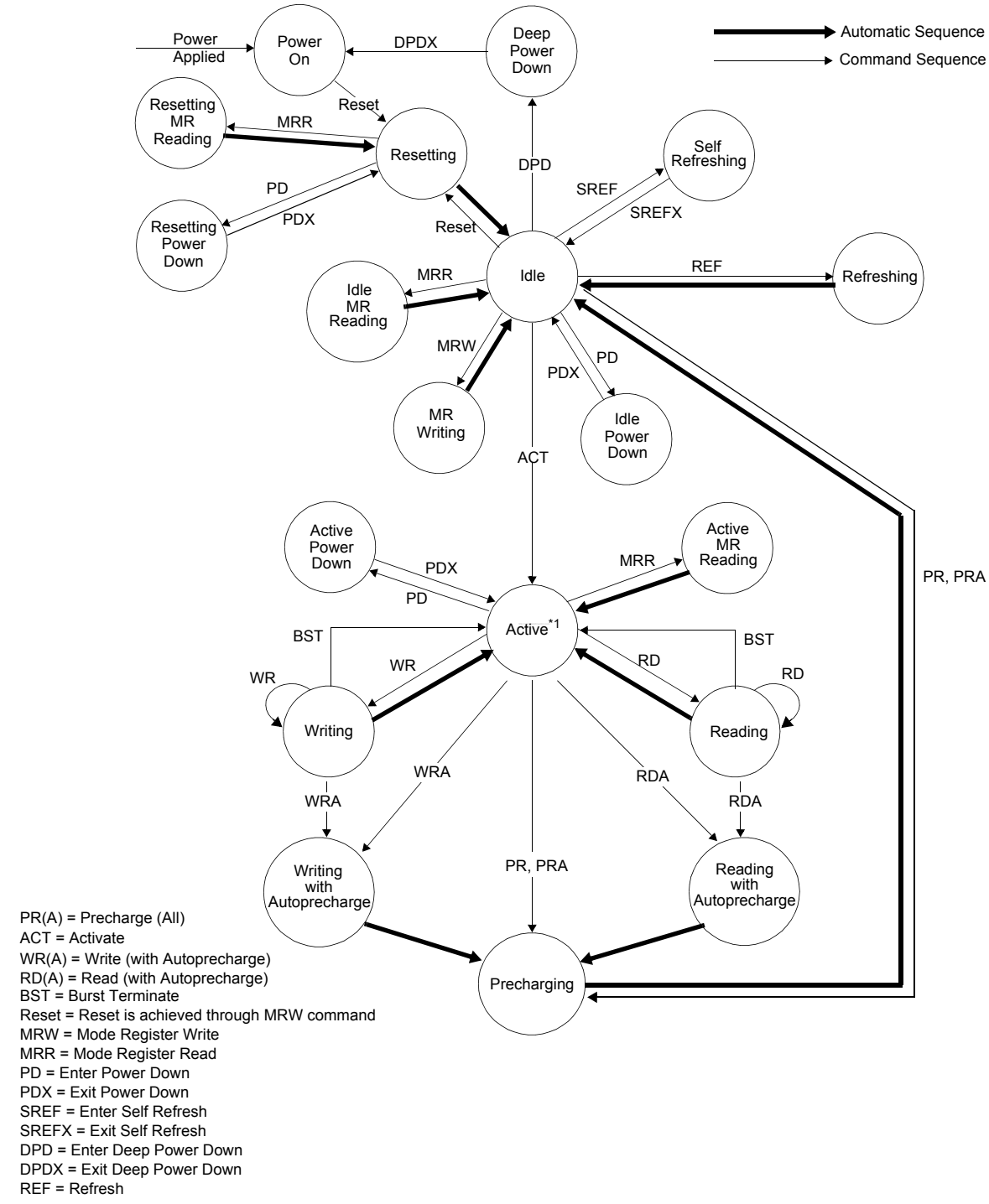


Figure 1. LPDDR2-S4: Simplified Bus Interface State Diagram

NOTE :
1) For LPDDR2-SDRAM in the Idle state, all banks are precharged.

5.2 Mode Register Definition

5.2.1 Mode Register Assignment and Definition in LPDDR2 SDRAM

Table 3 shows the 16 common mode registers for LPDDR2 SDRAM and NVM. Table 4 shows only LPDDR2 SDRAM mode registers and Table 5 shows only LPDDR2 NVM mode registers. Additionally Table 6 shows RFU mode registers and Reset Command.

Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written.

Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

[Table 3] Mode Register Assignment in LPDDR2 SDRAM(Common part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info.	R	(RFU)			RZQI		(RFU)	DI	DAI
1	01_H	Device Feature 1	W	nWR (for AP)			WC	BT	BL		
2	02_H	Device Feature 2	W	(RFU)					RL & WL		
3	03_H	I/O Config-1	W	(RFU)					DS		
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05_H	Basic Config-1	R	LPDDR2 Manufacturer ID							
6	06_H	Basic Config-2	R	Revision ID1							
7	07_H	Basic Config-3	R	Revision ID2							
8	08_H	Basic Config-4	R	I/O width		Density				Type	
9	09_H	Test Mode	W	Vendor-Specific Test Mode							
10	$0A_H$	IO Calibration	W	Calibration Code							
11:15	$0B_H$~$0F_H$	(reserved)		(RFU)							

[Table 4] Mode Register Assignment in LPDDR2 SDRAM (SDRAM part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
16	10_H	PASR_Bank	W	Bank Mask							
17	11_H	PASR_Seg	W	Segment Mask							
18-19	12_H-13_H	(Reserved)		(RFU)							

[Table 5] Mode Register Assignment in LPDDR2 SDRAM (NVM Part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
20:31	14_H~$1F_H$	(Do Not Use)									

[Table 6] Mode Register Assignment in LPDDR2 SDRAM (DQ Calibration and Reset Command)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
32	**20_H**	DQ Calibration Pattern A	R	See "DQ Calibration" on Operations & Timiing Diagram.							
33:39	**21_H~27_H**	(Do Not Use)									
40	**28_H**	DQ Calibration Pattern B	R	See "DQ Calibration" on Operations & Timiing Diagram.							
41:47	**29_H~$2F_H$**	(Do Not Use)									
48:62	**30_H~$3E_H$**	(Reserved)		(RFU)							
63	**$3F_H$**	Reset	W	X							
64:126	**40_H~$7E_H$**	(Reserved)		(RFU)							
127	**$7F_H$**	(Do Not Use)									
128:190	**80_H~BE_H**	(Reserved for Vendor Use)		(RFU)							
191	**BF_H**	(Do Not Use)									
192:254	**$C0_H$~FE_H**	(Reserved for Vendor Use)		(RFU)							
255	**FF_H**	(Do Not Use)									

The following notes apply to Table 3 Mode Register Assignment in LPDDR2 SDRAM(Common part), Table 4 Mode Register Assignment in LPDDR2 SDRAM (SDRAM part), Table 5 Mode Register Assignment in LPDDR2 SDRAM (NVM Part), and Table 6 Mode Register Assignment in LPDDR2 SDRAM (DQ Calibration and Reset Command):

NOTE :
1) RFU bits shall be set to '0' during Mode Register writes.
2) RFU bits shall be read as '0' during Mode Register reads.
3) All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS, $\overline{DQS}$ shall be toggled.
4) All Mode Registers that are specified as RFU shall not be written.
5) Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA<7:0> = 00_H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)			RZQI		(RFU)	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP<0>	0_B: DAI complete 1_B: DAI still in progress
DI (Device Information)	Read-only	OP<1>	0_B: S2 or S4 SDRAM 1_B: Do Not Use
RZQI (Built in Self Test for RZQ Information) 1)	Read-only	OP4:OP3	00_B: RZQ self test not supported 01_B: ZQ-pin may connect to VDDCA or float 10_B: ZQ-pin may short to GND 11_B: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)

NOTE :
1) RZQI will be set upon completion of the MRW ZQ Initialization Calibration command.
2) If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3] = 01 or OP[4:3] =10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3) In the case of possible assembly error (either OP[4:3]=01 per Note 4), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4) In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e 240-ohm +/- 1%).

MR1_Device Feature 1 (MA<7:0> = 01_H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write-only	OP<2:0>	010_B: BL4 (default) 011_B: BL8 100_B: BL16 **All others:** Reserved
BT 1)	Write-only	OP<3>	0_B: Sequential (default) 1_B: Interleaved
WC	Write-only	OP<4>	0_B: Wrap (default) 1_B: No wrap (allowed for SDRAM BL4 only)
nWR 2)	Write-only	OP<7:5>	001_B: nWR=3 (default) 010_B: nWR=4 011_B: nWR=5 100_B: nWR=6 101_B: nWR=7 110_B: nWR=8 **All others:** Reserved

NOTE :
1) BL 16, interleaved is not an official combination to be supported.
2) Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

[Table 7] Burst Sequence by BL, BT, and WC

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	0_B	0_B	wrap	any	4	0	1	2	3												
X	X	1_B	0_B				2	3	0	1												
X	X	X	0_B	nw	any		y	y+1	y+2	y+3												
X	0_B	0_B	0_B	wrap	seq	8	0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	4	5	6	7	0	1								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	0	1	2	3	4	5								
X	0_B	0_B	0_B		int		0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	0	1	6	7	4	5								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	4	5	2	3	0	1								
X	X	X	0_B	nw	any		**illegal (not allowed)**															
0_B	0_B	0_B	0_B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0_B	0_B	1_B	0_B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0_B	1_B	0_B	0_B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0_B	1_B	1_B	0_B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1_B	0_B	0_B	0_B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1_B	0_B	1_B	0_B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1_B	1_B	0_B	0_B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1_B	1_B	1_B	0_B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
X	X	X	0_B		int		**illegal (not allowed)**															
X	X	X	0_B	nw	any		**illegal (not allowed)**															

NOTE :
1) C0 input is not present on CA bus. It is implied zero.
2) For BL=4, the burst address represents C1 - C0.
3) For BL=8, the burst address represents C2 - C0.
4) For BL=16, the burst address represents C3 - C0.
5) For no-wrap (nw), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary. The variable y may start at any address with C0 equal to 0 and may not start at any address in Table 8 below for the respective density and bus width combinations.

[Table 8] LPDDR2-S4 Non Wrap Restrictions

2Gb	
Not across full page boundary	
x16	3FE, 3FF, 000, 001
x32	1FE, 1FF, 000, 001
Not across sub page boundary	
x16	1FE, 1FF, 200, 201
x32	None

NOTE :
1) Non-wrap BL=4 data-orders shown above are prohibited.

MR2_Device Feature 2 (MA<7:0> = 02_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

RL & WL	Write-only	OP<3:0>	**0001_B:** RL3 / WL1(default) **0010_B:** RL4 / WL2 **0011_B:** RL5 / WL2 **0100_B:** RL6 / WL3 **0101_B:** RL7 / WL4 **0110_B:** RL8 / WL4 **All others:** Reserved

MR3_I/O Configuration 1 (MA<7:0> = 03_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP<3:0>	**0000_B:** Reserved **0001_B:** 34.3-ohm typical **0010_B:** 40-ohm typical (default) **0011_B:** 48-ohm typical **0100_B:** 60-ohm typical **0101_B:** Reserved for 68.6-ohm typical **0110_B:** 80-ohm typical **0111_B:** 120-ohm typical **All others:** Reserved

MR4_Device Temperature (MA<7:0> = 04_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		

SDRAM Refresh Rate	Read-only	OP<2:0>	**000_B:** SDRAM Low temperature operating limit exceeded **001_B:** 4x t_{REFI}, 4x t_{REFIpb}, 4x t_{REFW} **010_B:** 2x t_{REFI}, 2x t_{REFIpb}, 2x t_{REFW} **011_B:** 1x t_{REFI}, 1x t_{REFIpb}, 1x t_{REFW} (<=85'C) **100_B:** Reserved **101_B:** 0.25x t_{REFI}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, do not de-rate SDRAM AC timing **110_B:** 0.25x t_{REFI}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, de-rate SDRAM AC timing **111_B:** SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	**0_B:** OP<2:0> value has not changed since last read of MR4. **1_B:** OP<2:0> value has changed since last read of MR4.

NOTE :
1) A Mode Register Read from MR4 will reset OP7 to '0'.
2) OP7 is reset to '0' at power-up. OP[2:0] bits are undefined after power-up.
3) If OP2 equals '1', the device temperature is greater than 85'C.
4) OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
5) LPDDR2 might not operate properly when OP[2:0] = 000_B or 111_B
6) For specified operating temperature range and maximum operating temperature refer to Table 17 Operating Temperature Range.
7) LPDDR2-S4 devices shall be de-rated by adding 1.875 ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in Table 47 LPDDR2 AC Timing Table. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
8) See "Temperature Sensor" on [Command Definition & Timing Diagram] for information on the recommended frequency of reading MR4.

MR5_Basic Configuration 1 (MA<7:0> = 05_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							

LPDDR2 Manufacturer ID	Read-only	OP<7:0>	**0000 0000_B :** Reserved **0000 0001_B :** Samsung **0000 0010_B :** Do Not Use **0000 0011_B :** Do Not Use **0000 0100_B :** Do Not Use **0000 0101_B :** Do Not Use **0000 0110_B :** Do Not Use **0000 0111_B :** Do Not Use **0000 1000_B :** Do Not Use **0000 1001_B :** Do Not Use **0000 1010_B :** Reserved **0000 1011_B :** Do Not Use **0000 1100_B :** Do Not Use **0000 1101_B :** Do Not Use **0000 1110_B :** Do Not Use **0000 1111_B :** Do Not Use **1111 1110_B :** Do Not Use **All others:** Reserved

MR6_Basic Configuration 2 (MA<7:0> = 06_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP<7:0>	**00000000_B:** A-version

NOTE :
1) MR6 is vendor specific.

MR7_Basic Configuration 3 (MA<7:0> = 07_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP<7:0>	**00000000_B:** A-version

NOTE :
1) MR7 is vendor specific.

MR8_Basic Configuration 4 (MA<7:0> = 08_H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP<1:0>	**00_B:** S4 SDRAM **01_B:** S2 SDRAM **10_B:** Do Not Use **11_B:** Reserved
Density	Read-only	OP<5:2>	**0000_B:** 64Mb **0001_B:** 128Mb **0010_B:** 256Mb **0011_B:** 512Mb **0100_B:** 1Gb **0101_B:** 2Gb **0110_B:** 4Gb **0111_B:** 8Gb **1000_B:** 16Gb **1001_B:** 32Gb **all others:** reserved
I/O width	Read-only	OP<7:6>	**00_B:** x32 **01_B:** x16 **10_B:** x8 **11_B:** Do Not Use

MR9_Test Mode (MA<7:0> = 09_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10_Calibration (MA<7:0> = $0A_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write-only	OP<7:0>	**0xFF:** Calibration command after initialization **0xAB:** Long calibration **0x56:** Short calibration **0xC3:** ZQ Reset **others:** Reserved

NOTE :
1) Host processor shall not write MR10 with “Reserved” values.
2) LPDDR2 devices shall ignore calibration command when a “Reserved” value is written into MR10.
3) See AC timing table for the calibration latency.
4) If ZQ is connected to V_{SSCA} through R_{ZQ}, either the ZQ calibration function (see "Mode Register Write ZQ Calibration Command" on [Command Definition & Timing Diagram]) or default calibration (through the ZQreset command) is supported. If ZQ is connected to V_{DDCA}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
5) LPDDR2 devices that do not support calibration shall ignore the ZQ Calibration command.
6) The MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR_11:15_(Reserved) (MA<7:0> = $0B_H$-$0F_H$):

MR_16_PASR_Bank Mask (MA<7:0> = 010_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask (4-Bank or 8-Bank)							

S4 SDRAM:

Bank <7:0> Mask [1]	Write-only	OP<7:0>	0_B: refresh enable to the bank (=unmasked, default) 1_B: refresh blocked (=masked)

NOTE :
1) For 4 bank S4 SDRAM, only OP<3:0> are used.

OP	Bank Mask	4 Bank	8 Bank
0	XXXXXXX1	Bank 0	Bank 0
1	XXXXXX1X	Bank 1	Bank 1
2	XXXXX1XX	Bank 2	Bank 2
3	XXXX1XXX	Bank 3	Bank 3
4	XXX1XXXX	-	Bank 4
5	XX1XXXXX	-	Bank 5
6	X1XXXXXX	-	Bank 6
7	1XXXXXXX	-	Bank 7

MR17_PASR_Segment Mask (MA<7:0> = 011_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment <7:0> Mask	Write-only	OP<7:0>	**0_B:** refresh enable to the segment (=unmasked, default) **1_B:** refresh blocked (=masked)

			1Gb	2Gb/4Gb	8Gb
Segment	**OP**	**Segment Mask**	**R12:10**	**R13:11**	**R14:12**
0	0	XXXXXXX1	**000_B**		
1	1	XXXXXX1X	**001_B**		
2	2	XXXXX1XX	**010_B**		
3	3	XXXX1XXX	**011_B**		
4	4	XXX1XXXX	**100_B**		
5	5	XX1XXXXX	**101_B**		
6	6	X1XXXXXX	**110_B**		
7	7	1XXXXXXX	**111_B**		

NOTE :
1) This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment.

MR18-19_(Reserved) (MA<7:0> = 012_H - 013_H):

MR20-31_(Do Not Use) (MA<7:0> = 14_H-$1F_H$):

MR32_DQ Calibration Pattern A (MA<7:0>=20_H):
Reads to MR32 return DQ Calibration Pattern "A". See "DQ Calibration" on Operations & Timiing Diagram.

MR33:39_(Do Not Use) (MA<7:0> = 21_H-27_H):

MR40_DQ Calibration Pattern B (MA<7:0>=28_H):
Reads to MR40 return DQ Calibration Pattern "B". See "DQ Calibration" on Operations & Timiing Diagram.

MR41:47_(Do Not Use) (MA<7:0> = 29_H-$2F_H$):

MR48:62_(Reserved) (MA<7:0> = 30_H-$3E_H$):

MR63_Reset (MA<7:0> = $3F_H$): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

NOTE :
1) For additional information on MRW RESET see "Mode Register Write Command" on [Command Definition & Timing Diagram].

MR64:126_(Reserved) (MA<7:0> = 40_H-$7E_H$):

MR127_(Do Not Use) (MA<7:0> = $7F_H$):

MR128:190_(Reserved for Vendor Use) (MA<7:0> = 80_H-BE_H):

MR191_(Do Not Use) (MA<7:0> = BF_H):

MR192:254_(Reserved for Vendor Use) (MA<7:0> = $C0_H$-FE_H):

MR255:(Do Not Use) (MA<7:0> = FF_H):

6.0 TRUTH TABLES

6.1 Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

6.1.1 Command truth table

[Table 9] Command truth table

SDRAM Command	SDR Command Pins			DDR CA pins (10)										CK EDGE
	CKE		$\overline{CS}$	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK(n-1)	CK(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	
			X	MA6	MA7	X								
Refresh (per bank)[10]	H	H	L	L	L	H	L	X						
			X	X										
Refresh (all bank)	H	H	L	L	L	H	H	X						
			X	X										
Enter Self Refresh	H	L	L	L	L	H	X							
	X		X	X										
Activate (bank)	H	H	L	L	H	R8/a15	R9/a16	R10/a17	R11/a18	R12/a19	BA0	BA1	BA2	
			X	R0/a5	R1/a6	R2/a7	R3/a8	R4/a9	R5/a10	R6/a11	R7/a12	R13/a13	R14/a14	
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	
			X	AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	
			X	AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	
Precharge (pre bank, all bank)	H	H	L	H	H	L	H	AB/a30	X/a31	X/a32	BA0	BA1	BA2	
			X	X/a20	X/a21	X/a22	X/a23	X/a24	X/a25	X/a26	X/a27	X/a28	X/a29	
BST	H	H	L	H	H	L	L	X						
			X	X										
Enter Deep Power Down	H	L	L	H	H	L	X							
	X		X	X										
NOP	H	H	L	H	H	H	X							
			X	X										
Maintain PD, SREF, DPD (NOP)	L	L	L	H	H	H	X							
			X	X										
NOP	H	H	H	X										
			X	X										
Maintain PD, SREF, DPD (NOP)	L	L	H	X										
			X	X										
Enter Power Down	H	L	H	X										
	X		X	X										
Exit PD, SREF, DPD	L	H	H	X										
	X		X	X										

NOTE:
1) All LPDDR2 commands are defined by states of $\overline{CS}$, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2) For LPDDR2 SDRAM, Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
3) AP “high” during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
4) “X” means “H or L (but a defined logic level)”
5) Self refresh exit and Deep Power Down exit are asynchronous.
6) V_{Ref} must be between 0 and VDDQ during Self Refresh and Deep Power Down operation.
7) CAxr refers to command/address bit “x” on the rising edge of clock.
8) $\underline{CA}$xf refers to command/address bit “x” on the falling edge of clock.
9) $\overline{CS}$ and CKE are sampled at the rising edge of clock.
10) Per Bank Refresh is only allowed in devices with 8 banks.
11) The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
12) AB "high" during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

6.2 LPDDR2-SDRAM Truth Tables

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the Banks.

[Table 10] LPDDR2-S4 : CKE Table

Device Current State*3	CKE_{n-1}*1	CKE_n*1	$\overline{CS}$*2	Command n*4	Operation n*4	Device Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6, 9
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6, 9
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6, 9, 12
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7, 10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	
	H	L	L	Enter Self-Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Deep Power Down	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
	H	H	Refer to the Command Truth Table				

NOTE :

1) "CKE_n" is the logic state of CKE at clock rising edge n; "CKE_{n-1}" was the state of CKE at the previous clock edge.
2) "$\overline{CS}$" is the logic state of $\overline{CS}$ at the clock rising edge n;
3) "Current state" is the state of the LPDDR2 device immediately prior to clock edge n.
4) "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".
5) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6) Power Down exit time (t_{XP}) should elapse before a command other than NOP is issued.
7) Self-Refresh exit time (t_{XSR}) should elapse before a command other than NOP is issued.
8) The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9) The clock must toggle at least once during the t_{XP} period.
10) The clock must toggle at least once during the t_{XSR} time.
11) 'X' means 'Don't care'.
12) Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.

[Table 11] Current State Bank n - Command to Bank n

Current State	Command	Operation	Next State	NOTES
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing(All Bank)	7
	MRW	Load value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	7, 8
	Precharge	Deactivate row in bank or banks	Precharging	9, 15
Row Active	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10, 11
	Write	Select column, and start write burst	Writing	10, 11, 12
	BST	Read burst terminate	Active	13
Writing	Write	Select column, and start new write burst	Writing	10, 11
	Read	Select column, and start read burst	Reading	10, 11, 14
	BST	Write burst terminate	Active	13
Power On	Reset	Begin Device Auto-Initialization	Resetting	7, 9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE :

1) The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Power Down.
2) All states and sequences not shown are illegal or reserved.
3) Current State Definitions:
- Idle: The bank or banks have been precharged, and tRP has been met.
- Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accesses are in progress.
- Reading: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
- Writing: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4) The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and Figure 11 Current State Bank n - Command to Bank n, and according to Figure 12 Current State Bank n - Command to Bank m.
- Precharging: starts with the registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
- Row Activating: starts with registration of an Activate command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'Active' state.
- Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
- Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

5) The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.
- Refreshing (Per Bank): starts with registration of an Refresh (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.
- Refreshing (All Bank): starts with registration of an Refresh (All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.
- Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
- Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
- Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
- MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
- Precharging All: starts with the registration of a Precharge-All command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

6) Bank-specific; requires that the bank is idle and no bursts are in progress.
7) Not bank-specific; requires that all banks are idle and no bursts are in progress.
8) Not bank-specific reset command is achieved through Mode Register Write command.
9) This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10) A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
11) The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
12) A Write command may be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.
13) Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank.
14) A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.
15) If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

[Table 12] Current State Bank n - Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	NOTES
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	7
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	10, 11, 13
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8, 14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8, 16
	Write	Select column, and start write burst to Bank m	Writing	8
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15
	Write	Select column, and start write burst to Bank m	Writing	8, 14, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15, 16
	Write	Select column, and start write burst to Bank m	Writing	8, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Power On	Reset	Begin Device Auto-Initialization	Resetting	12, 17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE :

1) The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2) All states and sequences not shown are illegal or reserved.
3) Current State Definitions:
- Idle: the bank has been precharged, and tRP has been met.
- Active: a row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
- Reading: a Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
- Writing: a Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4) Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.
5) A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.
6) The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
- Idle MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Idle state.
- Resetting MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Resetting state.
- Active MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Active state.
- MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Idle state.

7) t_{RRD} must be met between Activate command to Bank n and a subsequent Activate command to Bank m.
8) Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
9) This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10) MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when t_{RCD} is met.)
11) MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when t_{RP} is met.
12) Not bank-specific; requires that all banks are idle and no bursts are in progress.
13) The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon t_{RCD} and t_{RP} respectively.
14) A Write command may be applied after the completion of the Read burst, otherwise a BST must be issued to end the Read prior to asserting a Write command.
15) Read with Auto Precharge enabled and Write with Auto Precharge enabled may be followed by any valid command to other banks provided that the timing restrictions in Precharge & Auto Precharge clarification on Timing spec are followed.
16) A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.
17) Reset command is achieved through Mode Register Write command.
18) BST is allowed only if a Read or Write burst is ongoing.Data mask truth table.

6.3 Data mask truth table

Table 13 DM truth table provides the data mask truth table.

[Table 13] DM truth table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

NOTE :
1) Used to mask write data, provided coincident with the corresponding data.

7.0 ABSOLUTE MAXIMUM DC RATINGS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

[Table 14] Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	2
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.6	V	2
VDDCA supply voltage relative to VSSCA	VDDCA	-0.4	1.6	V	2,4
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	2,3
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	T_{STG}	-55	125	°C	5

NOTE :

1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

2) See “Power-Ramp” section in "Power-up, Initialization, and Power-Off" on [Command Definition & Timing Diagram] for relationships between power supplies.

3) $V_{RefDQ} \leq 0.6 \times VDDQ$; however, V_{RefDQ} may be $\geq$ VDDQ provided that $V_{RefDQ} \leq 300mV$.

4) $V_{RefCA} \leq 0.6 \times VDDCA$; however, V_{RefCA} may be $\geq$ VDDCA provided that $V_{RefCA} \leq 300mV$.

5) Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

8.0 AC & DC OPERATING CONDITIONS

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

8.1 Recommended DC Operating Conditions

[Table 15] Recommended LPDDR2-S4 DC Operating Conditions

Symbol	LPDDR2-S4B			DRAM	Unit
	Min	Typ	Max		
VDD1	1.70	1.80	1.95	Core Power1	V
VDD2	1.14	1.20	1.3	Core Power2	V
VDDCA	1.14	1.20	1.3	Input Buffer Power	V
VDDQ	1.14	1.20	1.3	I/O Buffer Power	V

NOTE :
1) VDD1 uses significantly less power than VDD2.

8.2 Input Leakage Current

[Table 16] Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current For CA, CKE, $\overline{CS}$, CK, $\overline{CK}$ Any input 0V ≤ VIN ≤ VDDCA (All other pins not under test = 0V)	I_L	-2	2	uA	2
V_{Ref} supply leakage current V_{RefDQ} = VDDQ/2 or V_{RefCA} = VDDCA/2 (All other pins not under test = 0V)	I_{VREF}	-1	1	uA	1

NOTE :
1) The minimum limit requirement is for testing purposes. The leakage current on V_{RefCA} and V_{RefDQ} pins should be minimal.
2) Although DM is for input only, the DM leakage shall match the DQ and DQS/$\overline{DQS}$ output leakage specification.

8.3 Operating Temperature Range

[Table 17] Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	T_{OPER}	-25	85	^oC

NOTE :
1) Operating Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.
2) Either the device case temperature rating or the temperature sensor (See "Temperature Sensor" on [Command Definition & Timing Diagram]) may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Extended Temperature Ranges. For example, TCASE may be above 85^{o}C when the temperature sensor indicates a temperature of less than 85^{o}C.

9.0 AC AND DC INPUT MEASUREMENT LEVELS

9.1 AC and DC Logic Input Levels for Single-Ended Signals

9.1.1 AC and DC Input Levels for Single-Ended CA and CS Signals

[Table 18] Single-Ended AC and DC Input Levels for CA and $\overline{CS}$ inputs

Symbol	Parameter	LPDDR2-800 to LPDDR2-667		Unit	Notes
		Min	Max		
V_{IHCA}(AC)	AC input logic high	Vref + 0.220	Note 2	V	1, 2
V_{ILCA}(AC)	AC input logic low	Note 2	Vref - 0.220	V	1, 2
V_{IHCA}(DC)	DC input logic high	Vref + 0.130	VDDCA	V	1
V_{ILCA}(DC)	DC input logic low	VSSCA	Vref - 0.130	V	1
V_{RefCA}(DC)	Reference Voltage for CA and $\overline{CS}$ inputs	0.49 * VDDCA	0.51 * VDDCA	V	3, 4

NOTE :
1) For CA and $\overline{CS}$ input only pins. $V_{Ref} = V_{RefCA}(DC)$.
2) See Overshoot and Undershoot Specifications on page 42.
3) The ac peak noise on V_{RefCA} may not allow V_{RefCA} to deviate from $V_{RefCA}(DC)$ by more than +/-1% VDDCA (for reference: approx. +/- 12 mV).
4) For reference: approx. VDDCA/2 +/- 12 mV.

9.2 AC and DC Input Levels for CKE

[Table 19] Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCKE}	CKE Input High Level	0.8 * VDDCA	Note 1	V	1
V_{ILCKE}	CKE Input Low Level	Note 1	0.2 * VDDCA	V	1

NOTE :
1) See Overshoot and Undershoot Specifications on page 42.

9.2.1 AC and DC Input Levels for Single-Ended Data Signals

[Table 20] Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	LPDDR2-800 to LPDDR2-667		Unit	Notes
		Min	Max		
V_{IHDQ}(AC)	AC input logic high	Vref + 0.220	Note 2	V	1, 2
V_{ILDQ}(AC)	AC input logic low	Note 2	Vref - 0.220	V	1, 2
V_{IHDQ}(DC)	DC input logic high	Vref + 0.130	VDDQ	V	1
V_{ILDQ}(DC)	DC input logic low	VSSQ	Vref - 0.130	V	1
V_{RefDQ}(DC)	Reference Voltage for DQ, DM inputs	0.49 * VDDQ	0.51 * VDDQ	V	3, 4

NOTE :
1)For DQ input only pins. Vref = V_{RefDQ}(DC).
2)See Overshoot and Undershoot Specifications on page 42.
3)The ac peak noise on V_{RefDQ} may not allow V_{RefDQ} to deviate from V_{RefDQ}(DC) by more than +/-1% VDDQ (for reference: approx. +/ - 12 mV).
4)For reference: approx. VDDQ/2 +/- 12 mV.

9.3 Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{RefCA} and V_{RefDQ} are illustrated in Figure 2. It shows a valid reference voltage $V_{Ref}(t)$ as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise). VDD stands for VDDCA for V_{RefCA} and VDDQ for V_{RefDQ}. $V_{Ref}(DC)$ is the linear average of $V_{Ref}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 18, Single-Ended AC and DC Input Levels for CA and CS inputs. Furthermore $V_{Ref}(t)$ may temporarily deviate from $V_{Ref}(DC)$ by no more than +/- 1% VDD. Vref(t) cannot track noise on VDDQ or VDDCA if this would send Vref outside these specifications.

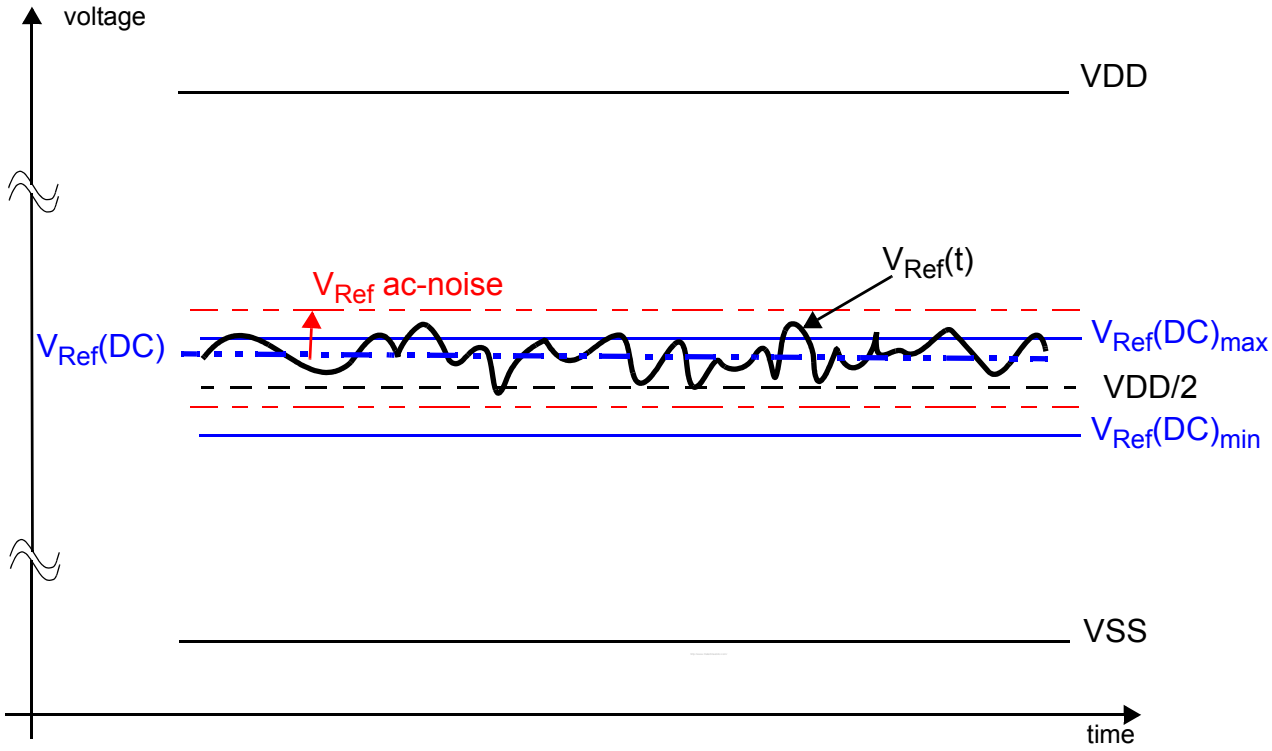


Figure 2. Illustration of $V_{Ref}(DC)$ tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on V_{Ref}.

"V_{Ref} " shall be understood as $V_{Ref}(DC)$, as defined in Figure 2.

This clarifies that dc-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. Devices will function correctly with appropriate timing deratings with V_{Ref} outside these specified levels so long as V_{Ref} is maintained between 0.44 x V_{DDQ} (or V_{DDCA}) and 0.56 x V_{DDQ} (or V_{DDCA}) and so long as the controller achieves the required single-ended AC and DC input levels from instantaneous V_{Ref} (see Table 18, Single-Ended AC and DC Input Levels for CA and CS inputs and Table 20, Single-Ended AC and DC Input Levels for DQ and DM) Therefore, System timing and voltage budgets need to account for V_{Ref} deviations outside if this range.

This also clarifies that the LPDDR2 setup/hold specification and derating values need to include time and voltage associated with V_{Ref} ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit (+/-1% of VDD) are included in LPDDR2 timings and their associated deratings.

9.4 Input Signal

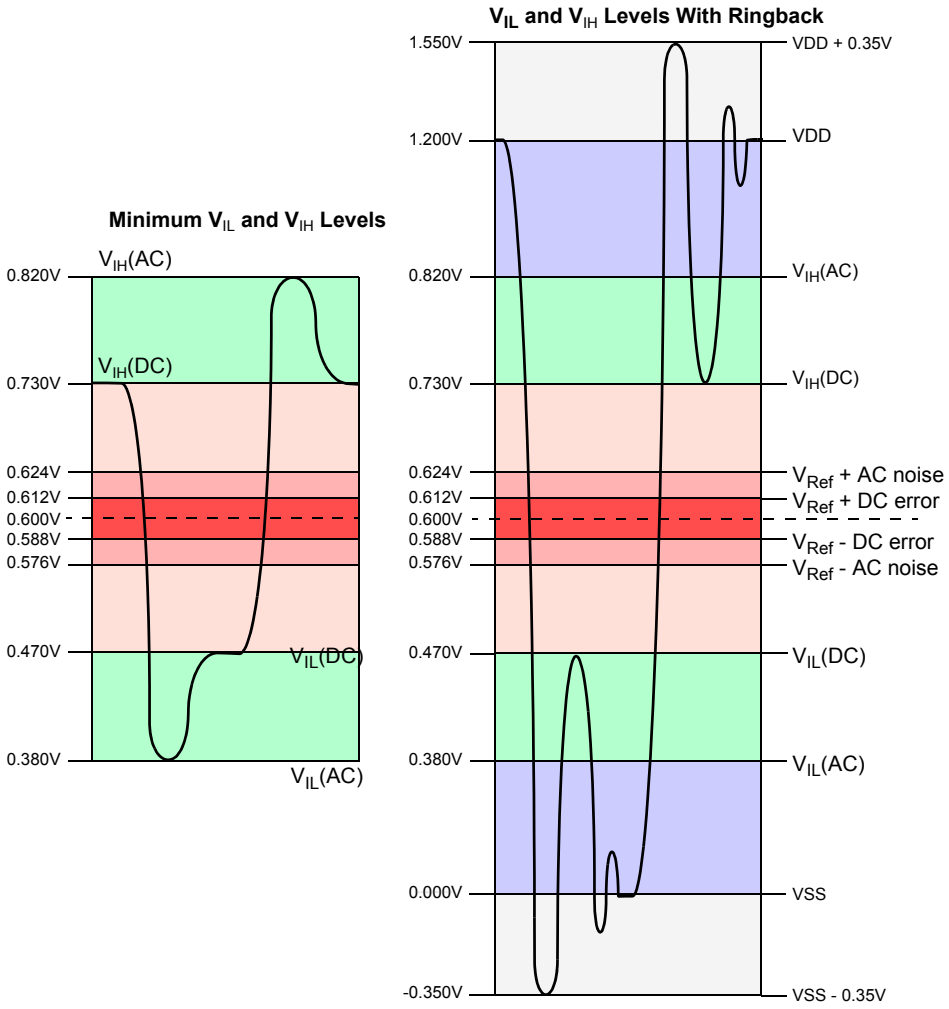


Figure 3. LPDDR2-667 to LPDDR2-800 Input Signal

NOTE :
1) Numbers reflect nominal values
2) For CA0-9, CK, $\overline{CK}$, and $\overline{CS}$, VDD stands for VDDCA. For DQ, DM, DQS, and $\overline{DQS}$, VDD stands for VDDQ.
3) For CA0-9, CK, $\overline{CK}$, and $\overline{CS}$, VSS stands for VSSCA. For DQ, DM, DQS, and $\overline{DQS}$, VSS stands for VSSQ

9.5 AC and DC Logic Input Levels for Differential Signals

9.5.1 Differential signal definition

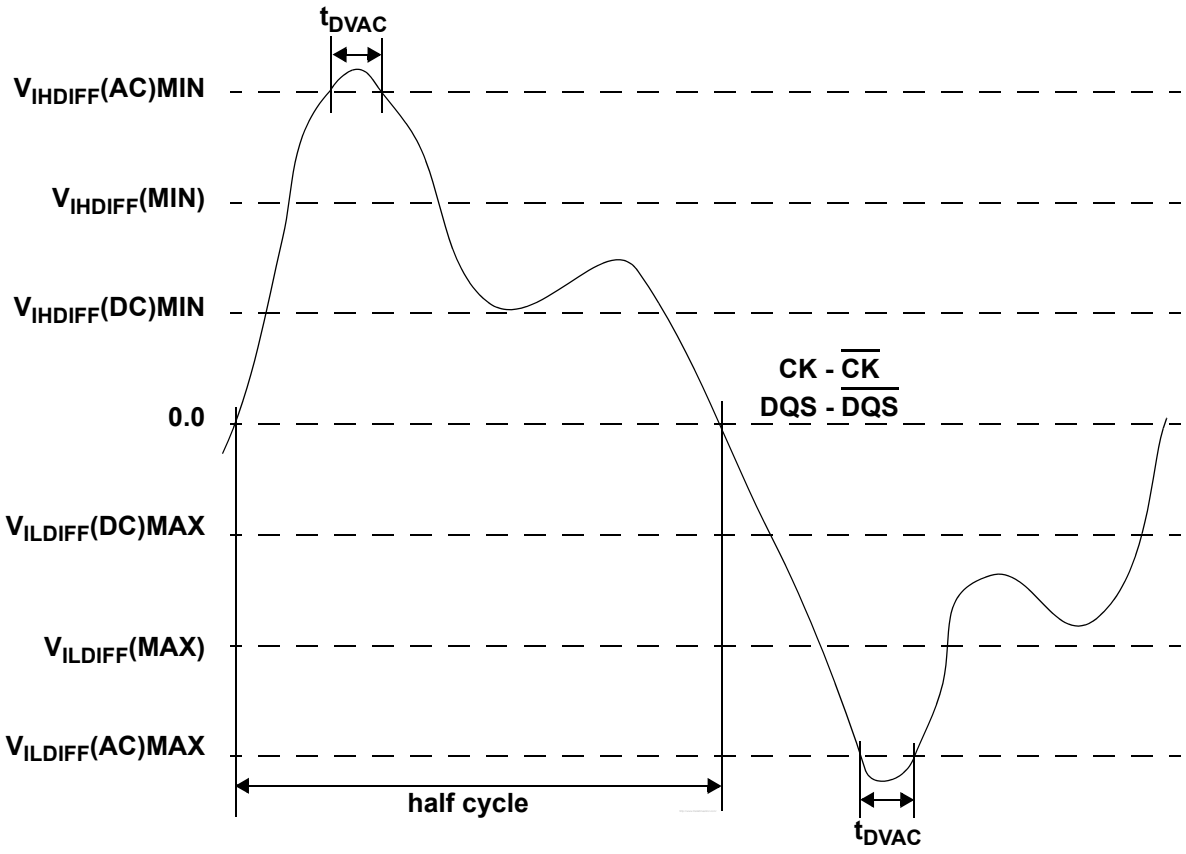


Figure 4. Definition of differential ac-swing and "time above ac-level" t_{DVAC}

9.5.2 Differential swing requirements for clock (CK - CK) and strobe (DQS - DQS)

[Table 21] Differential AC and DC Input Levels

Symbol	Parameter	LPDDR2-800 to LPDDR2-667		Unit	Notes
		Min	Max		
V_{IHdiff}(DC)	Differential input high	2 x (V_{IH}(dc) - Vref)	Note 3	V	1
V_{ILdiff}(DC)	Differential input low	Note 3	2 x (V_{IL}(dc) - Vref)	V	1
V_{IHdiff}(AC)	Differential input high ac	2 x (V_{IH}(ac) - Vref)	Note 3	V	2
V_{ILdiff}(AC)	Differential input low ac	Note 3	2 x (V_{IL}(ac) - Vref)	V	2

NOTE :
1)Used to define a differential signal slew-rate.
2)For CK - $\overline{CK}$ use V_{IH}/V_{IL}(AC) of CA and V_{RefCA}; for DQS - $\overline{DQS}$, use V_{IH}/V_{IL}(AC) of DQs and V_{RefDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3) These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, and $\overline{DQS}$ need to be within the respective limits (V_{IH}(DC) max, V_{IL}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Figure 10 Overshoot and Undershoot Definition.
4) For CK and $\overline{CK}$, Vref = V_{RefCA}(DC). For DQS and $\overline{DQS}$, Vref = V_{RefDQ}(DC).

[Table 22] Allowed time before ringback (tDVAC) for CK - $\overline{CK}$ and DQS - $\overline{DQS}$

Slew Rate [V/ns]	tDVAC [ps] @ $\|V_{IH}/Ldiff(AC)\|$ = 440mV	tDVAC [ps] @ $\|V_{IH}/Ldiff(AC)\|$ = 600mV
	min	min
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

9.5.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, $\overline{CK}$, or $\overline{DQS}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{CK}$ shall meet V_{SEL}(AC)min / V_{SEL}(AC)max in every half-cycle.

DQS, $\overline{DQS}$ shall meet V_{SEH}(AC)min / V_{SEH}(AC)max in every half-cycle preceeding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

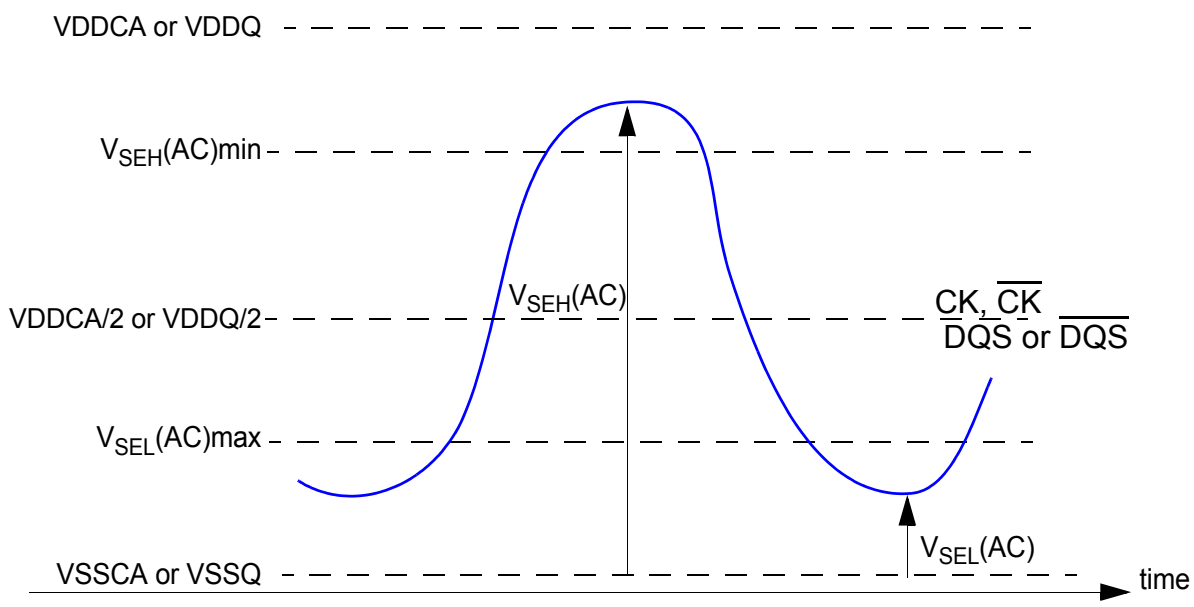


Figure 5. Single-ended requirement for differential signals.

Note that while CA and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS, $\overline{DQS}$ and VDDCA/2 for CK, $\overline{CK}$; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SEL}(AC)max, V_{SEH}(AC)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

The single ended requirements for CK, $\overline{CK}$, DQS and $\overline{DQS}$ are found in Table 18, Single-Ended AC and DC Input Levels for CA and CS inputs and Table 20, Single-Ended AC and DC Input Levels for DQ and DM, respectively.

[Table 23] Single-ended levels for CK, DQS, $\overline{CK}$, $\overline{DQS}$

Symbol	Parameter	LPDDR2-800 to LPDDR2-667		Unit	Notes
		Min	Max		
V_{SEH} (AC)	Single-ended highlevel for strobes	(VDDQ/2)+0.220	Note 3	V	1, 2
	Single-ended high-level for CK, $\overline{CK}$	(VDDCA/2)+0.220	Note 3	V	1, 2
V_{SEL} (AC)	Single-ended lowlevel for strobes	Note 3	(VDDQ/2)-0.220	V	1, 2
	Single-ended lowlevel for CK, $\overline{CK}$	Note 3	(VDDCA/2)-0.220	V	1, 2

NOTE :

1) For CK, $\overline{CK}$ use V_{SEH}/V_{SEL}(AC) of CA; for strobes (DQS0, $\overline{DQS0}$, DQS1, $\overline{DQS1}$, DQS2, $\overline{DQS2}$, DQS3, $\overline{DQS3}$) use V_{IH}/V_{IL}(AC) of DQs.

2) V_{IH}(AC)/V_{IL}(AC) for DQs is based on V_{RefDQ}; V_{SEH}(AC)/V_{SEL}(AC) for CA is based on V_{RefCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here

3) These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS0, $\overline{DQS0}$, DQS1, $\overline{DQS1}$, DQS2, $\overline{DQS2}$, DQS3, $\overline{DQS3}$ need to be within the respective limits (V_{IH}(DC) max, V_{IL}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

9.6 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in Table 23 Single-ended levels for CK, DQS, CK, DQS. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

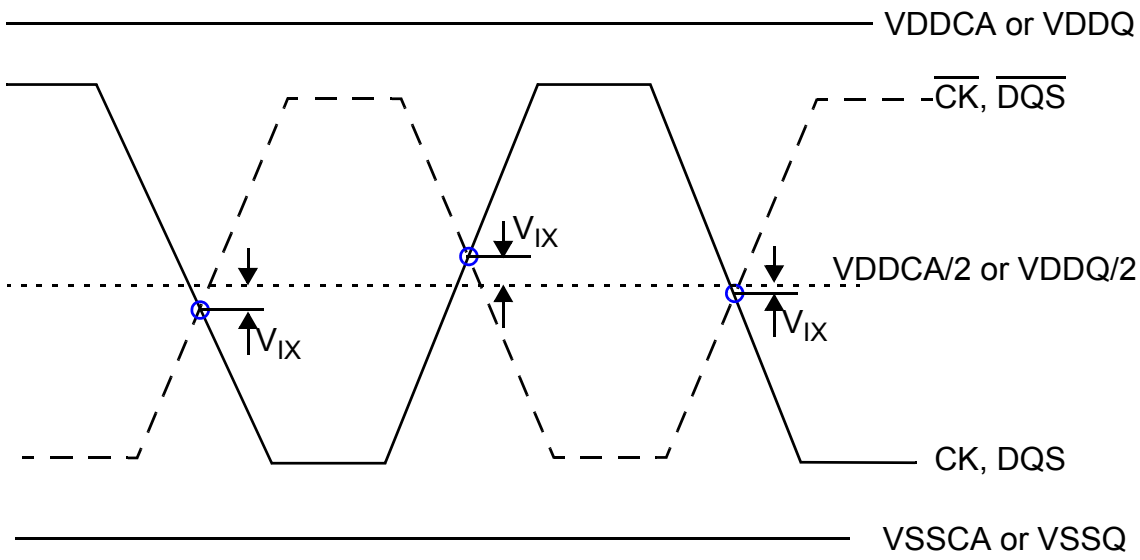


Figure 6. Vix Definition

[Table 24] Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	LPDDR2-800 to LPDDR2-667		Unit	Notes
		Min	Max		
V_{IXCA}	Differential Input Cross Point Voltage relative to VDDCA/2 for CK, $\overline{CK}$	- 120	120	mV	1,2
V_{IXDQ}	Differential Input Cross Point Voltage relative to VDDQ/2 for DQS, $\overline{DQS}$	- 120	120	mV	1,2

NOTE :
1)The typical value of VIX(AC) is expected to be about 0.5 × VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
2) For CK and $\overline{CK}$, Vref = V_{RefCA}(DC). For DQS and $\overline{DQS}$, Vref = V_{RefDQ}(DC).

9.7 Slew Rate Definitions for Single-Ended Input Signals

See CA and CS Setup, Hold and Derating on page 65. for single-ended slew rate definitions for address and command signals.
See Data Setup, Hold and Slew Rate Derating on page 71.for single-ended slew rate definitions for data signals.

9.8 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) are defined and measured as shown in Table 25 and Figure 7.

[Table 25] Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK - $\overline{CK}$ and DQS - $\overline{DQS}$).	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / DeltaTRdiff$
Differential input slew rate for falling edge (CK - $\overline{CK}$ and DQS - $\overline{DQS}$).	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / DeltaTFdiff$

NOTE :
1) The differential signal (i.e. CK - $\overline{CK}$ and DQS - $\overline{DQS}$) must be linear between these thresholds.

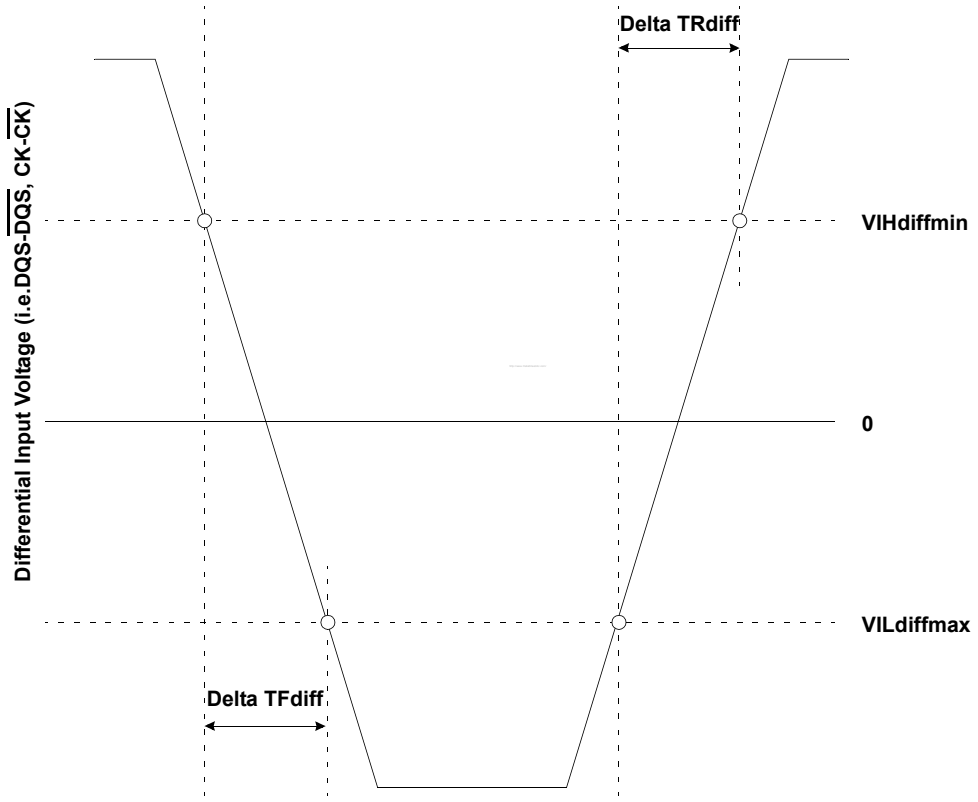


Figure 7. Differential Input Slew Rate Definition for DQS, $\overline{DQS}$ and CK, $\overline{CK}$

10.0 AC AND DC OUTPUT MEASUREMENT LEVELS

10.1 Single Ended AC and DC Output Levels

Table 26 shows the output levels used for measurements of single ended signals.

[Table 26] Single-ended AC and DC Output Levels

Symbol	Parameter		LPDDR2-800 to LPDDR2-667	Unit	Notes
$V_{OH}(DC)$	DC output high measurement level (for IV curve linearity)		0.9 x V_{DDQ}	V	1
$V_{OL}(DC)$	DC output low measurement level (for IV curve linearity)		0.1 x V_{DDQ}	V	2
$V_{OH}(AC)$	DC output high measurement level (for IV curve linearity)		V_{Ref} + 0.12	V	
$V_{OL}(AC)$	DC output low measurement level (for IV curve linearity)		V_{Ref} - 0.12	V	
I_{OZ}	Output Leakage current (DQ, DM, DQS, $\overline{DQS}$) (DQs are disabled; 0V ≤ VOUT ≤ VDDQ	Min	-5	uA	
		Max	5	uA	
MM_{PUPD}	Delta RON between pull-up and pull-down for DQ/DM	Min	-15	%	
		Max	15	%	

NOTE :
1) IOH = -0.1mA.
2) IOL = 0.1mA.

10.2 Differential AC and DC Output Levels

Table 27 shows the output levels used for measurements of differential signals (DQS, $\overline{DQS}$).

[Table 27] Differential AC and DC Output Levels

Symbol	Parameter	LPDDR2-800 to LPDDR2-667	Unit	Notes
$V_{OHdiff}(AC)$	AC differential output high measurement level (for output SR)	+ 0.20 x V_{DDQ}	V	
$V_{OLdiff}(AC)$	AC differential output low measurement level (for output SR)	- 0.20 x V_{DDQ}	V	

NOTE :
1) IOH = -0.1mA.
2) IOL = 0.1mA.

10.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL}(AC) and V_{OH}(AC) for single ended signals as shown in Table 28 and Figure 8.

[Table 28] Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	[V_{OH}(AC) - V_{OL}(AC)] / DeltaTRse
Single-ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	[V_{OH}(AC) - V_{OL}(AC)] / DeltaTFse

NOTE :
1) Output slew rate is verified by design and characterization, and may not be subject to production test.

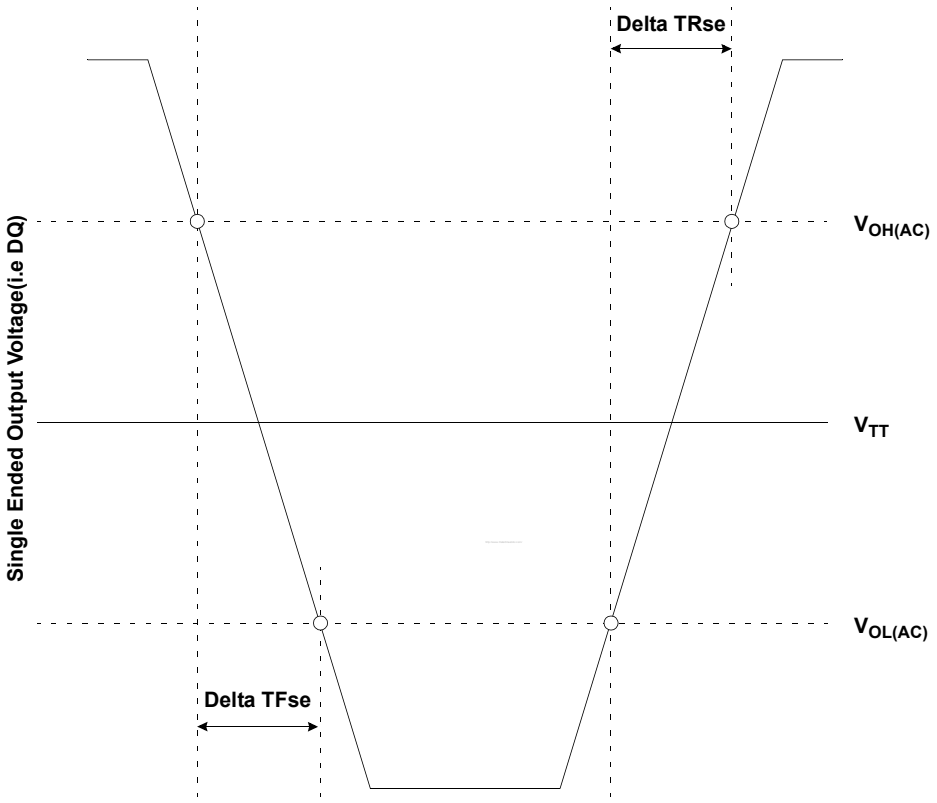


Figure 8. Single Ended Output Slew Rate Definition

[Table 29] Output Slew Rate (single-ended)

Parameter	Symbol	LPDDR2-800 to LPDDR2-667		Units
		Min	Max	
Single-ended Output Slew Rate (RON = 40Ω +/- 30%)	SRQse	1.5	3.5	V/ns
Single-ended Output Slew Rate (RON = 60Ω +/- 30%)	SRQse	1.0	2.5	V/ns
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4	
Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) se: Single-ended Signals				

NOTE :
1) Measured with output reference load.
2) The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pulldown drivers due to process variation.
3) The output slew rate for falling and rising edges is defined and measured between VOL(DC) and VOH(DC).
4) Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logichigh and 1/2 of DQ signals per data byte driving logic-low.

10.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOH-diff(AC) for differential signals as shown in Table 30 and Figure 9.

[Table 30] Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$[V_{OHdiff}(AC) - V_{OLdiff}(AC)]$ / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$[V_{OHdiff}(AC) - V_{OLdiff}(AC)]$ / DeltaTFdiff

NOTE :
1) Output slew rate is verified by design and characterization, and may not be subject to production test.

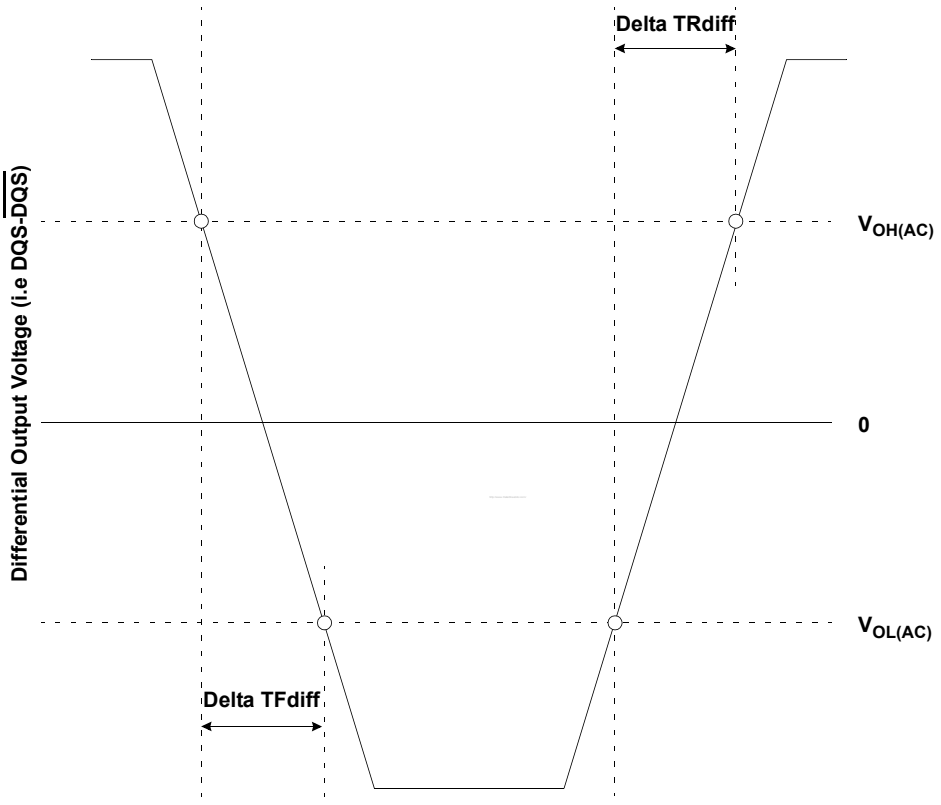


Figure 9. Differential Output Slew Rate Definition

[Table 31] Differential Output Slew Rate

Parameter	Symbol	LPDDR2-800 to LPDDR2-667		Units
		Min	Max	
Differential Output Slew Rate (RON = 40Ω +/- 30%)	SRQdiff	3.0	7.0	V/ns
Differential Output Slew Rate (RON = 60Ω +/- 30%)	SRQdiff	2.0	5.0	V/ns
Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) diff: Differential Signals				

NOTE :
1) Measured with output reference load.
2) The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
3) Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logichigh and 1/2 of DQ signals per data byte driving logic-low.

10.5 Overshoot and Undershoot Specifications

[Table 32] AC Overshoot/Undershoot Specification

Parameter		800	667	Units
Maximum peak amplitude allowed for overshoot area. (See Figure 10)	Max	0.35		V
Maximum peak amplitude allowed for undershoot area. (See Figure 10)	Max	0.35		V
Maximum area above VDD. (See Figure 10)	Max	0.20	0.24	V-ns
Maximum area below VSS. (See Figure 10)	Max	0.20	0.24	V-ns

NOTE :
1) For CA0-9, CK, $\overline{CK}$, $\overline{CS}$, and CKE, VDD stands for VDDCA. For DQ, DM, DQS, and $\overline{DQS}$, VDD stands for VDDQ.
2) For CA0-9, CK, $\overline{CK}$, $\overline{CS}$, and CKE, VSS stands for VSSCA. For DQ, DM, DQS, and $\overline{DQS}$, VSS stands for VSSQ.
3) Values are referenced from actual VDDQ, VDDCA, VSSQ, and VSSCA levels.

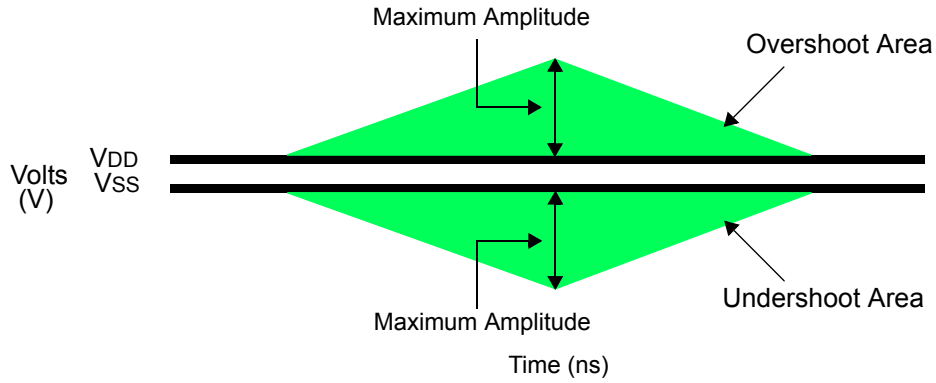


Figure 10. Overshoot and Undershoot Definition

NOTE :
1) For CA0-9, CK, $\overline{CK}$, $\overline{CS}$, and CKE, VDD stands for VDDCA. For DQ, DM, DQS, and $\overline{DQS}$, VDD stands for VDDQ.
2) For CA0-9, CK, $\overline{CK}$, $\overline{CS}$, and CKE, VSS stands for VSSCA. For DQ, DM, DQS, and $\overline{DQS}$, VSS stands for VSSQ.

11.0 OUTPUT BUFFER CHARACTERISTICS

11.1 HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

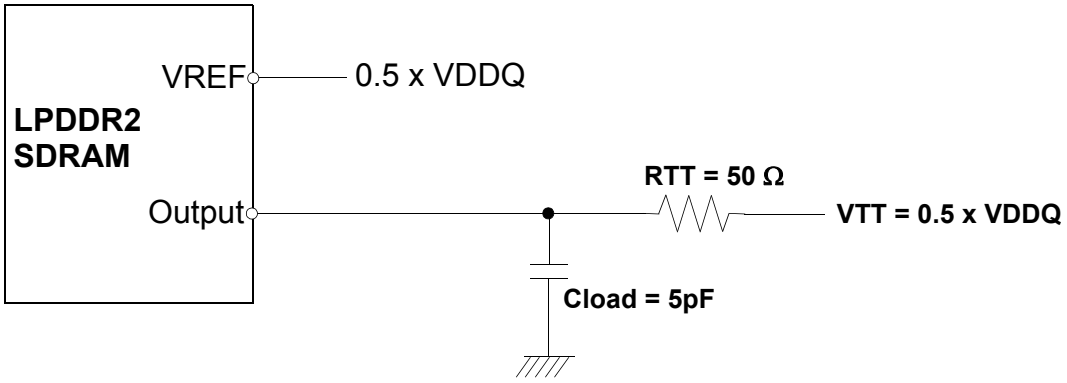


Figure 11. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

NOTE :

1) All output timing parameter values (like t_{DQSCK}, t_{DQSQ}, t_{QHS}, t_{HZ}, t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

12.0 RON_{PU} AND RON_{PD} RESISTOR DEFINITION

$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

NOTE :
1)This is under the condition that RON_{PD} is turned off.

$$RONPD = \frac{Vout}{ABS(Iout)}$$

NOTE :
1) This is under the condition that RON_{PU} is turned off.

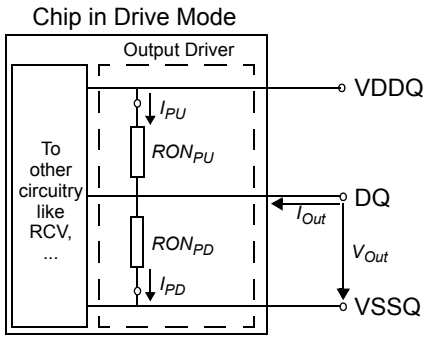


Figure 12. Output Driver: Definition of Voltages and Currents

12.1 RON_{PU} and RON_{PD} Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω

[Table 33] Output Driver DC Electrical Characteristics with ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
	RON34PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
40.0Ω	RON40PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
	RON40PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
48.0Ω	RON48PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
	RON48PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
60.0Ω	RON60PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
	RON60PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
80.0Ω	RON80PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
	RON80PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
120.0Ω	RON120PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1,2,3,4
	RON120PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1,2,3,4
Mismatch between pull-up and pull-down	MMPUPD		-15.00		+15.00	%	1,2,3,4,5

NOTE :
1) Across entire operating temperature range, after calibration.
2) RZQ = 240Ω.
3) The tolerance limits are specified after calibration with stable voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
4) Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ.
5) Mesaurement definition for mismatch between pull-up and pull-down,
MMPUPD: Measure RONPU and RONPD, both at 0.5 x VDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

For example, with MMPUPD(max) = 15% and RONPD = 0.85, RONPU must be less than 1.0

12.2 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

[Table 34] Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Notes
RONPD	0.5 x VDDQ	$85 - (dRONdT \times \Delta T) - (dRONdV \times \Delta V)$	$115 + (dRONdT \times \Delta T) - (dRONdV \times \Delta V)$	%	1,2
RONPU					

NOTE :

1) $\Delta T = T - T$ (@ calibration), $\Delta V = V - V$ (@ calibration)
2) dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

[Table 35] Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	MIn	Max	Unit	Notes
dRONdT	RON Temperature Sensitivity	0.00	0.75	% / C	
dRONdV	RON Voltage Sensitivity	0.00	0.20	% / mV	

12.3 RON_{PU} and RON_{PD} Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

[Table 36] Output Driver DC Electrical Characteristics without ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	24	34.3	44.6	Ω	1
	RON34PU	0.5 x VDDQ	24	34.3	44.6	Ω	1
40.0Ω	RON40PD	0.5 x VDDQ	28	40	52	Ω	1
	RON40PU	0.5 x VDDQ	28	40	52	Ω	1
48.0Ω	RON48PD	0.5 x VDDQ	33.6	48	62.4	Ω	1
	RON48PU	0.5 x VDDQ	33.6	48	62.4	Ω	1
60.0Ω	RON60PD	0.5 x VDDQ	42	60	78	Ω	1
	RON60PU	0.5 x VDDQ	42	60	78	Ω	1
80.0Ω	RON80PD	0.5 x VDDQ	56	80	104	Ω	1
	RON80PU	0.5 x VDDQ	56	80	104	Ω	1
120.0Ω	RON120PD	0.5 x VDDQ	84	120	156	Ω	1
	RON120PU	0.5 x VDDQ	84	120	156	Ω	1

NOTE:
1) Across entire operating temperature range, without calibration.

12.4 RZQ I-V Curve

[Table 37] RZQ I-V Curve

Voltage[V]	RON = 240Ω (RZQ)							
	Pull-Down				Pull-Up			
	Current [mA] / RON [Ohms]				Current [mA] / RON [Ohms]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	-0.19	-0.32	-0.21	-0.26
0.10	0.38	0.64	0.40	0.53	-0.38	-0.64	-0.40	-0.53
0.15	0.56	0.94	0.60	0.78	-0.56	-0.94	-0.60	-0.78
0.20	0.74	1.26	0.79	1.04	-0.74	-1.26	-0.79	-1.04
0.25	0.92	1.57	0.98	1.29	-0.92	-1.57	-0.98	-1.29
0.30	1.08	1.86	1.17	1.53	-1.08	-1.86	-1.17	-1.53
0.35	1.25	2.17	1.35	1.79	-1.25	-2.17	-1.35	-1.79
0.40	1.40	2.46	1.52	2.03	-1.40	-2.46	-1.52	-2.03
0.45	1.54	2.74	1.69	2.26	-1.54	-2.74	-1.69	-2.26
0.50	1.68	3.02	1.86	2.49	-1.68	-3.02	-1.86	-2.49
0.55	1.81	3.30	2.02	2.72	-1.81	-3.30	-2.02	-2.72
0.60	1.92	3.57	2.17	2.94	-1.92	-3.57	-2.17	-2.94
0.65	2.02	3.83	2.32	3.15	-2.02	-3.83	-2.32	-3.15
0.70	2.11	4.08	2.46	3.36	-2.11	-4.08	-2.46	-3.36
0.75	2.19	4.31	2.58	3.55	-2.19	-4.31	-2.58	-3.55
0.80	2.25	4.54	2.70	3.74	-2.25	-4.54	-2.70	-3.74
0.85	2.30	4.74	2.81	3.91	-2.30	-4.74	-2.81	-3.91
0.90	2.34	4.92	2.89	4.05	-2.34	-4.92	-2.89	-4.05
0.95	2.37	5.08	2.97	4.23	-2.37	-5.08	-2.97	-4.23
1.00	2.41	5.20	3.04	4.33	-2.41	-5.20	-3.04	-4.33
1.05	2.43	5.31	3.09	4.44	-2.43	-5.31	-3.09	-4.44
1.10	2.46	5.41	3.14	4.52	-2.46	-5.41	-3.14	-4.52
1.15	2.48	5.48	3.19	4.59	-2.48	-5.48	-3.19	-4.59
1.20	2.50	5.55	3.23	4.65	-2.50	-5.55	-3.23	-4.65

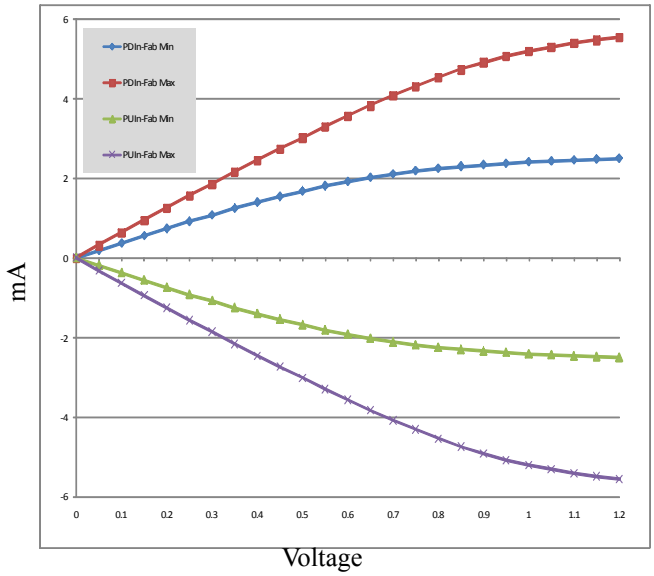


Figure 13. RON = 240 Ohms
IV Curve after ZQReset

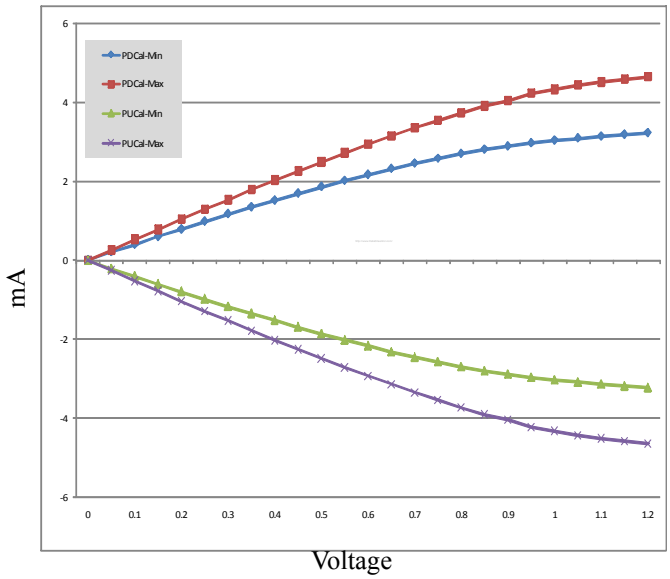


Figure 14. RON = 240 Ohms
IV Curve after Calibration

13.0 INPUT/OUTPUT CAPACITANCE

[Table 38] Input/output capacitance

Parameter	Symbol		LPDDR2 800-667	Units	Notes
Input capacitance, CK and $\overline{CK}$	CCK	Min	2.0	pF	1,2
		Max	5.0	pF	1,2
Input capacitance delta, CK and $\overline{CK}$	CDCK	Min	0.0	pF	1,2,3
		Max	0.40	pF	1,2,3
Cin, all other input-only pins except $\overline{CS}$ and CKE	CI1	Min	2.0	pF	1,2,4
		Max	5.0	pF	1,2,4
Cin, $\overline{CS}$0 / $\overline{CS}$1 and CKE0 / CKE1	CI2	Min	1.0	pF	1,2,4
		Max	3.0	pF	1,2,4
Cdelta, all other input-only pins except $\overline{CS}$ and CKE	CDI1	Min	-1.0	pF	1,2,5
		Max	1.0	pF	1,2,5
Cdelta, $\overline{CS}$0 / $\overline{CS}$1 and CKE0 / CKE1	CDI2	Min	-1.0	pF	1,2,5,10
		Max	1.0	pF	1,2,5,10
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	Min	2.5	pF	1,2,6,7
		Max	6	pF	1,2,6,7
Input/output capacitance delta, DQS, $\overline{DQS}$	CDDQS	Min	0.0	pF	1,2,7,8
		Max	0.50	pF	1,2,7,8
Input/output capacitance delta, DQ, DM	CDIO	Min	-1.0	pF	1,2,7,9
		Max	1.0	pF	1,2,7,9
Input/output capacitance ZQ Pin	CZQ	Min	0.0	pF	1,2
		Max	6.0	pF	1,2

(T_{OPER}; V_{DDQ} = 1.14-1.3V; V_{DDCA} = 1.14-1.3V; V_{DD1} = 1.7-1.95V,LPDDR2-S4B V_{DD2} = 1.14-1.3V)

NOTE :
1) This parameter applies to both die and package.
2) This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating.
3) Absolute value of CCK - $\overline{CCK}$.
4) CI applies to $\overline{CS}$, CKE, CA0-CA9.
5) CDI = CI - 0.5 * (CCK + $\overline{CCK}$)
6) DM loading matches DQ and DQS.
7) MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ohm typical)
8) Absolute value of CDQS and $\overline{CDQS}$.
9) CDIO = CIO - 0.5 * (CDQS + $\overline{CDQS}$) in byte-lane.
10) CDI2 = CI2 - 0.25 * (CCK_t + CCK_c)

14.0 IDD SPECIFICATION PARAMETERS AND TEST CONDITIONS

14.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:

LOW: $V_{IN} \leq V_{IL}$(DC) MAX

HIGH: $V_{IN} \geq V_{IH}$(DC) MIN

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See Table 39 and Table 40.

[Table 39] Definition of Switching for CA Input Signals

Switching for CA								
	CK (RISING) / $\overline{CK}$ (FALLING)	CK (FALLING) / $\overline{CK}$ (RISING)	CK (RISING) / $\overline{CK}$ (FALLING)	CK (FALLING) / $\overline{CK}$ (RISING)	CK (RISING) / $\overline{CK}$ (FALLING)	CK (FALLING) / $\overline{CK}$ (RISING)	CK (RISING) / $\overline{CK}$ (FALLING)	CK (FALLING) / $\overline{CK}$ (RISING)
Cycle	N		N+1		N+2		N+3	
$\overline{CS}$	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

NOTE :
1) $\overline{CS}$ must always be driven HIGH.
2) 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3) The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.

[Table 40] Definition of Switching for IDD4R

Clock	CKE	$\overline{CS}$	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Read_Rising	HLH	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Read_Falling	HHH	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

NOTE :
1) Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2) The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4R.

[Table 41] Definition of Switching for IDD4W

Clock	CKE	$\overline{CS}$	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Write_Rising	HLL	LHLHLHL	L
Falling	HIGH	LOW	N	Write_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Write_Rising	HLL	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Write_Falling	HHH	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

NOTE :
1) Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2) Data masking (DM) must always be driven LOW.
3) The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.

14.2 IDD Specifications

IDD values are for the entire operating voltage range and the standard and extended temperature ranges, unless otherwise noted.

[Table 42] LPDDR2 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Units	Notes
Operating one bank active-precharge current $t_{CK} = t_{CK(avg)min}$; $t_{RC} = t_{RCmin}$; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD0_1$	VDD1	mA	3,14
	$IDD0_2$	VDD2	mA	3,14
	$IDD0_{IN}$	VDDCA + VDDQ	mA	3,4,14
Idle power-down standby current: $t_{CK} = t_{CK(avg)min}$; CKE is LOW; $\overline{CS}$ is HIGH; All banks idle; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2P_1$	VDD1	mA	3,13
	$IDD2P_2$	VDD2	mA	3,13
	$IDD2P_{IN}$	VDDCA + VDDQ	mA	3,4,13
Idle power-down standby current with clock stop: CK =LOW, $\overline{CK}$ =HIGH; CKE is LOW; $\overline{CS}$ is HIGH; All banks idle; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2PS_1$	VDD1	mA	3,13
	$IDD2PS_2$	VDD2	mA	3,13
	$IDD2PS_{IN}$	VDDCA + VDDQ	mA	3,4,13
Idle non power-down standby current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH; $\overline{CS}$ is HIGH; All banks idle; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2N_1$	VDD1	mA	3,14
	$IDD2N_2$	VDD2	mA	3,14
	$IDD2N_{IN}$	VDDCA + VDDQ	mA	3,4,14
Idle non power-down standby current with clock stop: CK=LOW, $\overline{CK}$=HIGH; CKE is HIGH; $\overline{CS}$ is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2NS_1$	VDD1	mA	3,14
	$IDD2NS_2$	VDD2	mA	3,14
	$IDD2NS_{IN}$	VDDCA + VDDQ	mA	3,4,14

Parameter/Condition	Symbol	Power Supply	Units	Notes
Active power-down standby current: $t_{CK} = t_{CK(avg)min}$; $\overline{CKE}$ is LOW; $\overline{CS}$ is HIGH; One bank active; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3P_1$	VDD1	mA	3,14
	$IDD3P_2$	VDD2	mA	3,14
	$IDD3P_{IN}$	VDDCA + VDDQ	mA	3,4,14
Active power-down standby current with clock stop: CK=LOW, $\overline{CK}$=HIGH; $\overline{CKE}$ is LOW; $\overline{CS}$ is HIGH; One bank active; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3PS_1$	VDD1	mA	3,14
	$IDD3PS_2$	VDD2	mA	3,14
	$IDD3PS_{IN}$	VDDCA + VDDQ	mA	3,4,14
Active non power-down standby current: $t_{CK} = t_{CK(avg)min}$; $\overline{CKE}$ is HIGH; $\overline{CS}$ is HIGH; One bank active; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3N_1$	VDD1	mA	3,14
	$IDD3N_2$	VDD2	mA	3,14
	$IDD3N_{IN}$	VDDCA + VDDQ	mA	3,4,14
Active non power-down standby current with clock stop: CK=LOW, $\overline{CK}$=HIGH; $\overline{CKE}$ is HIGH; $\overline{CS}$ is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3NS_1$	VDD1	mA	3,14
	$IDD3NS_2$	VDD2	mA	3,14
	$IDD3NS_{IN}$	VDDCA + VDDQ	mA	3,4,14
Operating burst read current: $t_{CK} = t_{CK(avg)min}$; $\overline{CS}$ is HIGH between valid commands; One bank active; BL = 4; RL = RLmin; Address bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4R_1$	VDD1	mA	3,14
	$IDD4R_2$	VDD2	mA	3,14
	$IDD4R_{IN}$	VDDCA	mA	3,14
	$IDD4R_Q$	VDDQ	mA	3,6,14
Operating burst write current: $t_{CK} = t_{CK(avg)min}$; $\overline{CS}$ is HIGH between valid commands; One bank active; BL = 4; WL = WLmin; Address bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4W_1$	VDD1	mA	3,14
	$IDD4W_2$	VDD2	mA	3,14
	$IDD4W_{IN}$	VDDCA + VDDQ	mA	3,4,14
All Bank Refresh Burst current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH between valid commands; $t_{RC} = t_{RFCabmin}$; Burst refresh; Address bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5_1$	VDD1	mA	3,14
	$IDD5_2$	VDD2	mA	3,14
	$IDD5_{IN}$	VDDCA + VDDQ	mA	3,4,14
All Bank Refresh Average current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; Address bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5AB_1$	VDD1	mA	3,14
	$IDD5AB_2$	VDD2	mA	3,14
	$IDD5AB_{IN}$	VDDCA + VDDQ	mA	3,4,14
Per Bank Refresh Average current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}/8$; Address bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5PB_1$	VDD1	mA	1,3,14
	$IDD5PB_2$	VDD2	mA	1,3,14
	$IDD5PB_{IN}$	VDDCA + VDDQ	mA	1,3,4,14

Parameter/Condition	Symbol	Power Supply	Units	Notes
Self refresh current (Standard Temperature Range): CK=LOW, $\overline{CK}$=HIGH; CKE is LOW; Address bus inputs are STABLE; Data bus inputs are STABLE; Maximum 1x Self-Refresh Rate;	$IDD6_1$	VDD1	mA	2,3,8,9,10,13
	$IDD6_2$	VDD2	mA	2,3,8,9,10,13
	$IDD6_{IN}$	VDDCA + VDDQ	mA	2,3,4,8,9,10, 13
Deep Power-Down current: Address bus inputs are STABLE; Data bus inputs are STABLE;	$IDD8_1$	VDD1	uA	3,11, 12,13
	$IDD8_2$	VDD2	uA	3,11, 12,13
	$IDD8_{IN}$	VDDCA + VDDQ	uA	3,4,11, 12,13

NOTE :
1) Per Bank Refresh only applicable for LPDDR2-S4 devices of 1Gb or higher densities and LPDDR2-S2 devices of 4Gb and higher densities.
2) This is the general definition that applies to full array Self Refresh. Refer to Table 44, IDD6 Partial Array Self-Refresh Current for details of Partial Array Self Refresh IDD6 specification.
3) IDD values published are the maximum of the distribution of the arithmetic mean.
4) Measured currents are the summation of VDDQ and VDDCA.
5) To calculate total current consumption, the currents of all active operations must be considered.
6) Guaranteed by design with output load of 5pF and RON = 40Ohm.
7) IDD current specifications are tested after the device is properly initialized.
8) In addition, supplier data sheets may include additional Self Refresh IDD values for temperature subranges within the Standard or Extended Temperature Ranges.
9) 1x Self-Refresh Rate is the rate at which the LPDDR2-S4 device is refreshed internally during Self-Refresh in the Standard Temperature range.
10) IDD6 85°C is guaranteed, IDD6 45°C is typical values.
11) IDD8 85°C is guaranteed, IDD8 45°C is typical values.
12) DPD (Deep Power Down) function is an optional feature, and it will be enabled upon request.
Please contact Samsung for more information.
13) These specification values are under same condition of the both chips selected at the same time.
14) These specification values are under IDD2PS condition of the other unselected chip.

14.3 IDD Spec Table

[Table 43] IDD Specification for 4Gb DDP LPDDR2-S4B 2/CS, 2CKE

Symbol		Power Supply	VDD2=1.2V (S4B) 128M x32 (K4P4G304EC)		Units	Notes
			800Mbps	667Mbps		
IDD0	$IDD0_1$	VDD1	6.3	6.3	mA	3,14
	$IDD0_2$	VDD2	40.8	40.8	mA	3,14
	$IDD0_{IN}$	VDDCA + VDDQ	5.1	5.1	mA	3,4,14
IDD2P	$IDD2P_1$	VDD1	0.6	0.6	mA	3,13
	$IDD2P_2$	VDD2	1.6	1.6	mA	3,13
	$IDD2P_{IN}$	VDDCA + VDDQ	0.2	0.2	mA	3,4,13
IDD2PS	$IDD2PS_1$	VDD1	0.6	0.6	mA	3,13
	$IDD2PS_2$	VDD2	1.6	1.6	mA	3,13
	$IDD2PS_{IN}$	VDDCA + VDDQ	0.2	0.2	mA	3,4,13
IDD2N	$IDD2N_1$	VDD1	1.3	1.3	mA	3,14
	$IDD2N_2$	VDD2	8.8	8.3	mA	3,14
	$IDD2N_{IN}$	VDDCA + VDDQ	5.1	5.1	mA	3,4,14
IDD2NS	$IDD2NS_1$	VDD1	1.3	1.3	mA	3,14
	$IDD2NS_2$	VDD2	4.8	4.3	mA	3,14
	$IDD2NS_{IN}$	VDDCA + VDDQ	5.1	5.1	mA	3,4,14
IDD3P	$IDD3P_1$	VDD1	2.3	2.3	mA	3,14
	$IDD3P_2$	VDD2	3.8	3.8	mA	3,14
	$IDD3P_{IN}$	VDDCA + VDDQ	0.2	0.2	mA	3,4,14
IDD3PS	$IDD3PS_1$	VDD1	2.3	2.3	mA	3,14
	$IDD3PS_2$	VDD2	3.8	3.8	mA	3,14
	$IDD3PS_{IN}$	VDDCA + VDDQ	0.2	0.2	mA	3,4,14
IDD3N	$IDD3N_1$	VDD1	2.3	2.3	mA	3,14
	$IDD3N_2$	VDD2	12.8	12.3	mA	3,14
	$IDD3N_{IN}$	VDDCA + VDDQ	5.1	5.1	mA	3,4,14
IDD3NS	$IDD3NS_1$	VDD1	2.3	2.3	mA	3,14
	$IDD3NS_2$	VDD2	6.8	6.3	mA	3,14
	$IDD3NS_{IN}$	VDDCA + VDDQ	5.1	5.1	mA	3,4,14
IDD4R	$IDD4R_1$	VDD1	2.3	2.3	mA	3,14
	$IDD4R_2$	VDD2	130.8	120.8	mA	3,14
	$IDD4R_{IN}$	VDDCA	5.05	5.05	mA	3,14
	$IDD4R_Q$	VDDQ	110.05	100.05	mA	3,6,14
IDD4W	$IDD4W_1$	VDD1	2.3	2.3	mA	3,14
	$IDD4W_2$	VDD2	140.8	130.8	mA	3,14
	$IDD4W_{IN}$	VDDCA + VDDQ	13.1	13.1	mA	3,4,14

Symbol			Power Supply	VDD2=1.2V (S4B) 128M x32 (K4P4G304EC) 800Mbps	VDD2=1.2V (S4B) 128M x32 (K4P4G304EC) 667Mbps	Units	Notes
IDD5	$IDD5_1$		VDD1	10.3	10.3	mA	3,14
	$IDD5_2$		VDD2	100.8	100.8	mA	3,14
	$IDD5_{IN}$		VDDCA + VDDQ	5.1	5.1	mA	3,4,14
IDD5AB	$IDD5AB_1$		VDD1	2.3	2.3	mA	3,14
	$IDD5AB_2$		VDD2	10.8	10.8	mA	3,14
	$IDD5AB_{IN}$		VDDCA + VDDQ	5.1	5.1	mA	3,4,14
IDD5PB	$IDD5PB_1$		VDD1	2.3	2.3	mA	1,3,14
	$IDD5PB_2$		VDD2	20.8	20.8	mA	1,3,14
	$IDD5PB_{IN}$		VDDCA + VDDQ	5.1	5.1	mA	1,3,4,14
IDD6	$IDD6_1$	45°C	VDD1	0.24	0.24	mA	2,3,8,9,10,13
		85°C		1.0	1.0		
	$IDD6_2$	45°C	VDD2	0.9	0.9	mA	2,3,8,9,10,13
		85°C		3.4	3.4		
	$IDD6_{IN}$	45°C	VDDCA + VDDQ	0.1	0.1	mA	2,3,4,8,9,10,13
		85°C		0.2	0.2		
IDD8	$IDD8_1$	45°C	VDD1	10	10	uA	3,11,12,13
		85°C		40	40		
	$IDD8_2$	45°C	VDD2	20	20	uA	3,11,12,13
		85°C		100	100		
	$IDD8_{IN}$	45°C	VDDCA + VDDQ	10	10	uA	3,4,11,12,13
		85°C		60	60		

NOTE :
1) See Table 42, LPDDR2 IDD Specification Parameters and Operating Conditions for notes.

[Table 44] IDD6 Partial Array Self-Refresh Current

Parameter			4Gb DDP 2/CS, 2CKE LPDDR2-S4B 45°C	4Gb DDP 2/CS, 2CKE LPDDR2-S4B 85°C	Unit
IDD6 Partial Array Self-Refresh Current (max)	Full Array	VDD1	240	1000	uA
		VDD2	900	3400	
		VDDCA + VDDQ	100	200	
	1/2 Array	VDD1	200	700	uA
		VDD2	560	2000	
		VDDCA + VDDQ	100	200	
	1/4 Array	VDD1	180	600	uA
		VDD2	380	1400	
		VDDCA + VDDQ	100	200	
	1/8 Array	VDD1	160	500	uA
		VDD2	300	1200	
		VDDCA + VDDQ	100	200	

NOTE :
1) IDD6 85°C is the maximum and IDD6 45°C is typical of the distribution of the arithmetic mean.

15.0 ELECTRICAL CHARACTERISTICS AND AC TIMING

15.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR2 device.

15.1.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$

$$where \qquad N = 200$$

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

15.1.2 Definition for tCK(abs)

t_{CK}(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. t_{CK}(abs) is not subject to production test.

15.1.3 Definition for tCH(avg) and tCL(avg)

t_{CH}(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

t_{CL}(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

15.1.4 Definition for tJIT(per)

t_{JIT}(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).
t_{JIT}(per) = Min/max of {tCK_i - tCK(avg) where i = 1 to 200}.
t_{JIT}(per),act is the actual clock jitter for a given system.
t_{JIT}(per),allowed is the specified allowed clock period jitter.
t_{JIT}(per) is not subject to production test.

15.1.5 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

$\mathbf{t}_{JIT}(cc)$ = Max of $|\{tCK_{i+1} - tCK_i\}|$.

$\mathbf{t}_{JIT}(cc)$ defines the cycle to cycle jitter.

$\mathbf{t}_{JIT}(cc)$ is not subject to production test.

15.1.6 Definition for tERR(nper)

$\mathbf{t}_{ERR}(nper)$ is defined as the cumulative error across n multiple consecutive cycles from tCK(avg).

$\mathbf{t}_{ERR}(nper)$,act is the actual clock jitter over n cycles for a given system.

$\mathbf{t}_{ERR}(nper)$,allowed is the specified allowed clock period jitter over n cycles.

$\mathbf{t}_{ERR}(nper)$ is not subject to production test.

$$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

$\mathbf{t}_{ERR}(nper)$,min can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68LN(n)) \times tJIT(per), min$$

$\mathbf{t}_{ERR}(nper)$,max can be calculated by the formula shown below

$$tERR(nper), max = (1 + 0.68LN(n)) \times tJIT(per), max$$

Using these equations, $\mathbf{t}_{ERR}(nper)$ tables can be generated for each $\mathbf{t}_{JIT}(per)$,act value.

15.1.7 Definition for duty cycle jitter tJIT(duty)

$\mathbf{t}_{JIT}(duty)$ is defined with absolute and average specification of tCH / tCL.

$$tJIT(duty), min = MIN((tCH(abs), min - tCH(avg), min), (tCL(abs), min - tCL(avg), min)) \times tCK(avg)$$

$$tJIT(duty), max = MAX((tCH(abs), max - tCH(avg), max), (tCL(abs), max - tCL(avg), max)) \times tCK(avg)$$

15.1.8 Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times

[Table 45] Definition for tCK(abs), tCH(abs), and tCL(abs)

Paramter	Symbol	Min	Unit
Absolute Clock Period	tCK(abs)	tCK(avg).min + tJIT(per).min	ps
Absolute Clock HIGH Pulse Width	t_{CH}(abs)	tCH(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)
Absolute Clock LOW Pulse Width	t_{CL}(abs)	tCL(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)

NOTE :
1) tCK(avg),min is expressed as ps for this table.
2) tJIT(duty),min is a negative value.

15.2 Period Clock Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in Table 47, LPDDR2 AC Timing Table and how to determine cycle time de-rating and clock cycle de-rating.

15.2.1 Clock period jitter effects on core timing parameters

(tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR2 device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

NOTE :
1) tFAW is only applied in devices with 8 banks.

15.2.1.1 Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter (tCORE).

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

15.2.1.2 Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter (tCORE).

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

15.2.2 Clock jitter effects on Command/Address timing parameters

(tIS, tIH, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb)

These parameters are measured from a command/address signal (CKE, CS, CA0 - CA9) transition edge to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per)), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

15.2.3 Clock jitter effects on Read timing parameters

15.2.3.1 tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)} \right)$$

For example,

if the measured jitter into a LPDDR2-800 device has tCK(avg) = 2500 ps, tJIT(per),act,min = -172 ps and tJIT(per),act,max= + 193 ps, then

tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 0.9 - (193 - 100)/2500= .8628 tCK(avg)

15.2.3.2 tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per).

15.2.3.3 tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min. Therefore tQSH(abs)min and tQSL(abs)min can be specified with tCH(abs)min and tCL(abs)min.

tQSH(abs)min = tCH(abs)min – 0.05

tQSL(abs)min = tCL(abs)min – 0.05

These parameters determine absolute Data-Valid window at the LPDDR2 device pin.

Absolute min data-valid window @LPDDR2 device pin =

min { (tQSH(abs)min * tCK(avg)min – tDQSQmax – tQHSmax) , (tQSL(abs)min * tCK(avg)min – tDQSQmax – tQHSmax) }

This minimum data-valid window shall be met at the target frequency regardless of clock jitter.

15.2.3.4 tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.

tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

15.2.4 Clock jitter effects on Write timing parameters

15.2.4.1 tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn, $\overline{DQS}$n : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

15.2.4.2 tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx, $\overline{DQS}$x) crossing to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per)), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

15.2.4.3 tDQSS

This parameter is measured from a data strobe signal (DQSx, $\overline{DQSx}$) crossing to the subsequent clock signal (CK/$\overline{CK}$) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act,min - tJIT(per),allowed,min}{tCK(avg)}$$

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}$$

For example,

if the measured jitter into a LPDDR2-800 device has tCK(avg)= 2500 ps, tJIT(per),act,min = -172 ps and tJIT(per),act,max= + 193 ps, then

tDQSS,(min,derated) = 0.75 - (tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-172 + 100)/2500 = .7788 tCK(avg)

and

tDQSS,(max,derated) = 1.25 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (193 - 100)/2500 = 1.2128 tCK(avg)

15.3 LPDDR2-S4 Refresh Requirement per Device Density

[Table 46] LPDDR2-S4 Refresh Requirement Parameters (per density)

Parameter		Symbol	2 Gb	Unit
Number of Banks			8	
Refresh Window Tcase ≤ 85°C		t_{REFW}	32	ms
Required number of REFRESH commands (min)		R	8,192	
average time between REFRESH commands (for reference only) Tcase ≤ 85°C	REFab	t_{REFI}	3.9	us
	REFpb	t_{REFIpb}	0.4875	us
Refresh Cycle time		t_{RFCab}	130	ns
Per Bank Refresh Cycle time		t_{RFCpb}	60	ns
Burst Refresh Window = 4 x 8 x t_{RFCab}		t_{REFBW}	4.16	us

15.4 AC Timings

[Table 47] LPDDR2 AC Timing Table

Parameter	Symbol	min max	min t_{CK}	LPDDR2		Unit
				800	667	
Max. Frequency*4		~		400	333	MHz
Clock Timing						
Average Clock Period	$t_{CK}(avg)$	min		2.5	3	ns
		max		100		
Average high pulse width	$t_{CH}(avg)$	min		0.45		$t_{CK}(avg)$
		max		0.55		
Average low pulse width	$t_{CL}(avg)$	min		0.45		$t_{CK}(avg)$
		max		0.55		
Absolute Clock Period	$t_{CK}(abs)$	min		$t_{CK}(avg)$min -/+ $t_{JIT}(per)$min		ps
Absolute clock HIGH pulse width (with allowed jitter)	$t_{CH}(abs)$, allowed	min		0.43		$t_{CK}(avg)$
		max		0.57		
Absolute clock LOW pulse width (with allowed jitter)	$t_{CL}(abs)$, allowed	min		0.43		$t_{CK}(avg)$
		max		0.57		
Clock Period Jitter (with allowed jitter)	$t_{JIT}(per)$, allowed	min		-100	-110	ps
		max		100	110	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	$t_{JIT}(cc)$, allowed	max		200	220	ps
Duty cycle Jitter (with allowed jitter)	$t_{JIT}(duty)$, allowed	min		min(($t_{CH}(abs)$,min - $t_{CH}(avg)$,min), ($t_{CH}(abs)$,min - $t_{CH}(avg)$,min)) * $t_{CK}(avg)$		ps
		max		max(($t_{CH}(abs)$,max - $t_{CH}(avg)$,max), ($t_{CH}(abs)$,max - $t_{CH}(avg)$,max)) * $t_{CK}(avg)$		ps
Cumulative error across 2 cycles	$t_{ERR}(2per)$, allowed	min		-147	-162	ps
		max		147	162	
Cumulative error across 3 cycles	$t_{ERR}(3per)$, allowed	min		-175	-192	ps
		max		175	192	
Cumulative error across 4 cycles	$t_{ERR}(4per)$, allowed	min		-194	-214	ps
		max		194	214	
Cumulative error across 5 cycles	$t_{ERR}(5per)$, allowed	min		-209	-230	ps
		max		209	230	
Cumulative error across 6 cycles	$t_{ERR}(6per)$, allowed	min		-222	-244	ps
		max		222	244	
Cumulative error across 7 cycles	$t_{ERR}(7per)$, allowed	min		-232	-256	ps
		max		232	256	
Cumulative error across 8 cycles	$t_{ERR}(8per)$, allowed	min		-241	-256	ps
		max		241	256	
Cumulative error across 9 cycles	$t_{ERR}(9per)$, allowed	min		-249	-274	ps
		max		249	274	
Cumulative error across 10 cycles	$t_{ERR}(10per)$, allowed	min		-257	-282	ps
		max		257	282	
Cumulative error across 11 cycles	$t_{ERR}(11per)$, allowed	min		-263	-289	ps
		max		263	289	
Cumulative error across 12 cycles	$t_{ERR}(12per)$, allowed	min		-269	-296	ps
		max		269	296	

Parameter	Symbol	min max	min t_{CK}	LPDDR2		Unit
				800	667	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	t_{ERR}(nper), allowed	min		tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per), allowed, min		ps
		max		tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per), allowed, max		
ZQ Calibration Parameters						
Initialization Calibration Time*14	t_{ZQINIT}	min		1		us
Full Calibration Time*14	t_{ZQCL}	min	6	360		ns
Short Calibration Time*14	t_{ZQCS}	min	6	90		ns
Calibration Reset Time*14	$t_{ZQRESET}$	min	3	50		
Read Parameters*11						
DQS output access time from CK/CK#	t_{DQSCK}	min		2500		ps
		max		5500		
DQSCK Delta Short*15	$t_{DQSCKDS}$	max		450	540	ps
DQSCK Delta Medium*16	$t_{DQSCKDM}$	max		900	1050	ps
DQSCK Delta Long*17	$t_{DQSCKDL}$	max		1200	1400	ps
DQS - DQ skew	t_{DQSQ}	max		240	280	ps
Data hold skew factor	t_{QHS}	max		280	340	ps
DQS Output High Pulse Width	t_{QSH}	min		t_{CH}(avg) - 0.05		t_{CK}(avg)
DQS Output Low Pulse Width	t_{QSL}	min		t_{CL}(avg) - 0.05		t_{CK}(avg)
Data Half Period	t_{QHP}	min		min(t_{QSH}, t_{QSL})		t_{CK}(avg)
DQ / DQS output hold time from DQS	t_{QH}	min		t_{QHP} - t_{QHS}		ps
Read preamble*11,*12	t_{RPRE}	min		0.9		t_{CK}(avg)
Read postamble*11,*13	t_{RPST}	min		t_{CL} - 0.05		t_{CK}(avg)
DQS low-Z from clock*11	$t_{LZ(DQS)}$	min		$t_{DQSCK(MIN)}$ - 300		ps
DQ low-Z from clock*11	$t_{LZ(DQ)}$	min		$t_{DQSCK(MIN)}$ - (1.4 * $t_{QHS(MAX)}$)		ps
DQS high-Z from clock*11	$t_{HZ(DQS)}$	max		$t_{DQSCK(MAX)}$ - 100		ps
DQ high-Z from clock*11	$t_{HZ(DQ)}$	max		$t_{DQSCK(MAX)}$ + (1.4 * $t_{DQSQ(MAX)}$)		ps
Write Parameters*11						
DQ and DM input hold time (Vref based)	t_{DH}	min		270	350	ps
DQ and DM input setup time (Vref based)	t_{DS}	min		270	350	ps
DQ and DM input pulse width	t_{DIPW}	min		0.35		t_{CK}(avg)
Write command to 1st DQS latching transition	t_{DQSS}	min		0.75		t_{CK}(avg)
		max		1.25		
DQS input high-level width	t_{DQSH}	min		0.4		t_{CK}(avg)
DQS input low-level width	t_{DQSL}	min		0.4		t_{CK}(avg)
DQS falling edge to CK setup time	t_{DSS}	min		0.2		t_{CK}(avg)
DQS falling edge hold time from CK	t_{DSH}	min		0.2		t_{CK}(avg)
Write postamble	t_{WPST}	min		0.4		t_{CK}(avg)
Write preamble	t_{WPRE}	min		0.35		t_{CK}(avg)
CKE Input Parameters						
CKE min. pulse width (high and low pulse width)	t_{CKE}	min	3	3		t_{CK}(avg)
CKE input setup time	t_{ISCKE}*2	min		0.25		t_{CK}(avg)
CKE input hold time	t_{IHCKE}*3	min		0.25		t_{CK}(avg)
Command Address Input Parameters*11						

Parameter	Symbol	min max	min t_{CK}	LPDDR2		Unit
				800	667	
Address and control input setup time (Vref based)	t_{IS}*1	min		290	370	ps
Address and control input hold time (Vref based)	t_{IH}*1	min		290	370	ps
Address and control input pulse width	t_{IPW}	min		0.40		t_{CK}(avg)
Boot Parameters (10 MHz - 55 MHz)*5,7,8						
Clock Cycle Time	t_{CKb}	max	-	100		ns
		min		18		
CKE Input Setup Time	t_{ISCKEb}	min	-	2.5		ns
CKE Input Hold Time	t_{IHCKEb}	min	-	2.5		ps
Address & Control Input Setup Time	t_{ISb}	min	-	1150		ps
Address & Control Input Hold Time	t_{IHb}	min	-	1150		ns
DQS Output Data Access Time from CK/CK#	t_{DQSCKb}	min	-	2.0		ns
		max		10.0		
Data Strobe Edge to Ouput Data Edge t_{DQSQb} - 1.2	t_{DQSQb}	max	-	1.2		ns
Data Hold Skew Factor	t_{QHSb}	max	-	1.2		ns
Mode Register Parameters						
MODE REGISTER Write command period	t_{MRW}	min	5	5		t_{CK}(avg)
Mode Register Read command period	t_{MRR}	min	2	2		t_{CK}(avg)
LPDDR2 SDRAM Core Parameters*9						
Read Latency	RL	min	3	6	5	t_{CK}(avg)
Write Latency	WL	min	1	3	2	t_{CK}(avg)
ACTIVE to ACTIVE command period	t_{RC}	min		t_{RAS} + t_{RPab} (with all-bank Precharge) t_{RAS} + t_{RPpb} (with per-bank Precharge)		ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	t_{CKESR}	min	3	15		ns
Self refresh exit to next valid command delay	t_{XSR}	min	2	t_{RFCab} + 10		ns
Exit power down to next valid command delay	t_{XP}	min	2	7.5		ns
LPDDR2-S4 CAS to CAS delay	t_{CCD}	min	2	2		t_{CK}(avg)
Internal Read to Precharge command delay	t_{RTP}	min	2	7.5		ns
RAS to CAS Delay	t_{RCD}	min	3	18		ns
Row Precharge Time (single bank)	t_{RPpb}	min	3	18		ns
Row Precharge Time (all banks)	t_{RPab} 4-bank	min	3	18		ns
Row Precharge Time (all banks)	t_{RPab} 8-bank	min	3	21		ns
Row Active Time	t_{RAS}	min	3	42		ns
		max	-	70		us
Write Recovery Time	t_{WR}	min	3	15		ns
Internal Write to Read Command Delay	t_{WTR}	min	2	7.5		ns
Active bank A to Active bank B	t_{RRD}	min	2	10		ns
Four Bank Activate Window	t_{FAW}	min	8	50		ns
Minimum Deep Power Down Time	t_{DPD}	min		500		us
LPDDR2 Temperature De-Rating						
t_{DQSCK} De-Rating	t_{DQSCK} (Derated)	max		6000		ps

Parameter	Symbol	min max	min t_{CK}	LPDDR2		Unit
				800	667	
Core Timings Temperature De-Rating for SDRAM	t_{RCD} (Derated)	min		t_{RCD} + 1.875		ns
	t_{RC} (Derated)	min		t_{RC} + 1.875		ns
	t_{RAS} (Derated)	min		t_{RAS} + 1.875		ns
	t_{RP} (Derated)	min		t_{RP} + 1.875		ns
	t_{RRD} (Derated)	min		t_{RRD} + 1.875		ns

NOTE :
1) Input set-up/hold time for signal(CA0 ~ 9, $\overline{CS}$)
2) CKE input setup time is measured from CKE reaching high/low voltage level to CK/$\overline{CK}$ crossing.
3) CKE input hold time is measured from CK/$\overline{CK}$ crossing to CKE reaching high/low voltage level .
4) Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.
5) To guarantee device operation before the LPDDR2 device is configured a number of AC boot timing parameters are defined in the Table 47, LPDDR2 AC Timing Table . Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.
6) Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determeing devuce capabilities.
7) The SDRAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in Figure 5.2 Mode Register Definition.
8) The output skew parameters are measured with Ron default settings into the reference load.
9) The min tCK column applies only when tCK is greater than 6ns for LPDDR2-S4 devices. In this case, both min tCK values and analog timing (ns) shall be satisfied.
10) All AC timings assume an input slew rate of 1V/ns.
11) Read, Write, and Input Setup and Hold values are referenced to Vref.
12) For low-to-high and high-to-low transitions, the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure 15 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

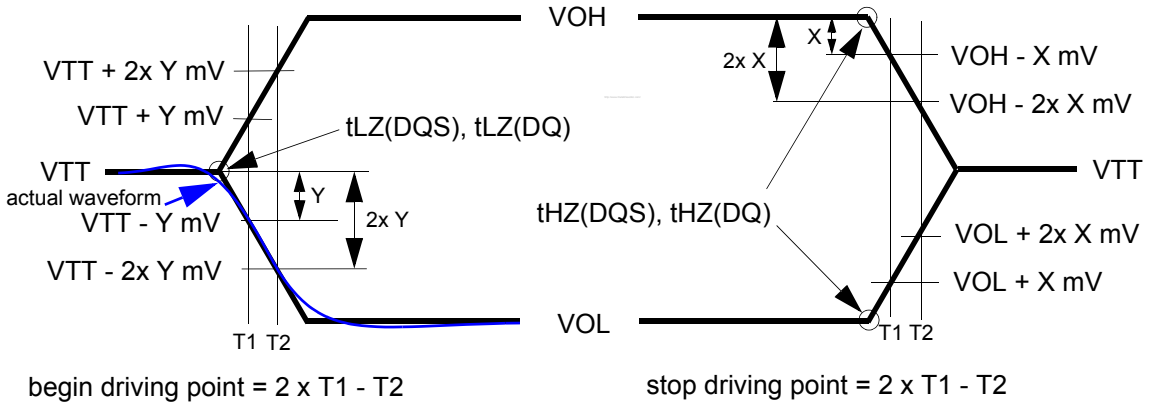


Figure 15. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS-$\overline{DQS}$.

13) Measured from the start driving of DQS - $\overline{DQS}$ to the start driving the first rising strobe edge.
14) Measured from the start driving the last falling strobe edge to the stop driving DQS - $\overline{DQS}$.
15) tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a contiguous sequence of bursts within a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.
16) tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 1.6us rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.
17) tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.
18) tFAW is only applied in devices with 8 banks.

15.5 CA and $\overline{CS}$ Setup, Hold and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see Table 47) to the ΔtIS and ΔtIH derating value (see Table 49 and Table 50) respectively.

Example: tIS (total setup time) = tIS(base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{Ref}(DC) and the first crossing of V_{IH}(AC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{Ref}(DC) and the first crossing of Vil(AC)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'V_{Ref}(DC) to ac region', use nominal slew rate for derating value (see Figure 16). If the actual signal is later than the nominal slew rate line anywhere between shaded 'V_{Ref}(DC) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 18).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(DC)max and the first crossing of V_{Ref}(DC). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(DC)min and the first crossing of V_{Ref}(DC). If the actual signal is always later than the nominal slew rate line between shaded 'dc to V_{Ref}(DC) region', use nominal slew rate for derating value (see Figure 17). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V_{Ref}(DC) region', the slew rate of a tangent line to the actual signal from the dc level to V_{Ref}(DC) level is used for derating value (see Figure 19).

For a valid transition the input signal has to remain above/below $V_{IH/IL}$(AC) for some time t_{VAC} (see Table 50).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}$(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(AC).

For slew rates in between the values listed in Table 49, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

[Table 48] CA and $\overline{CS}$ Setup and Hold Base-Values for 1V/ns

unit [ps]	LPDDR2		reference
	800	667	
tIS(base)	70	150	VIH/L(ac)=VREF(dc)+/-220mV
tIH(base)	160	240	VIH/L(dc)=VREF(dc)+/-130mV

NOTE :
1) ac/dc referenced for 1V/ns CA and $\overline{CS}$ slew rate and 2V/ns differential CK-$\overline{CK}$ slew rate.

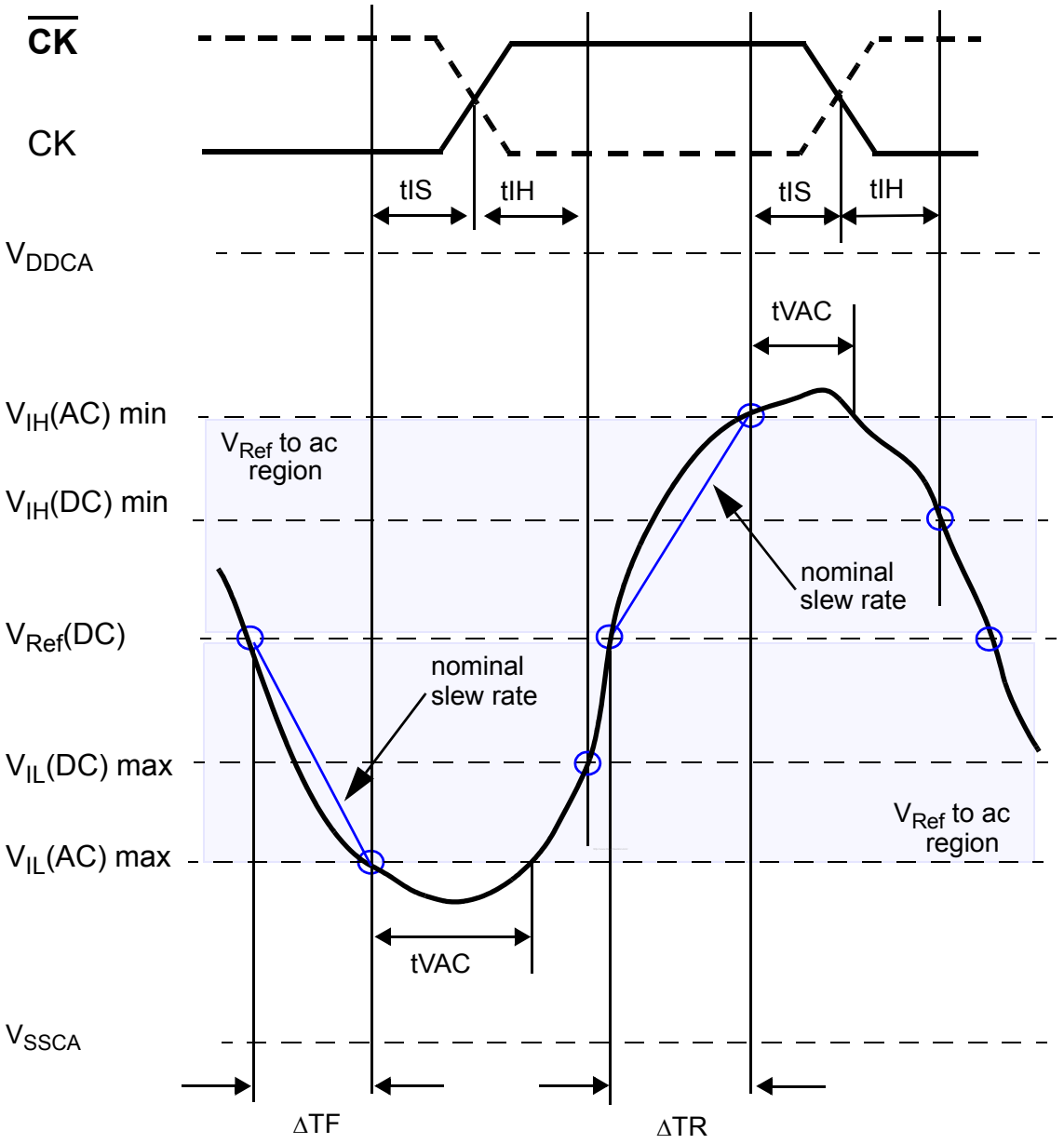
[Table 49] Derating values LPDDR2 tIS/tIH - ac/dc based AC220

ΔtIS, ΔtIH derating in [ps] AC/DC based AC220 Threshold -> $V_{IH}(AC)=V_{Ref}(DC)+220mV$, $V_{IL}(AC)=V_{Ref}(DC)-220mV$ DC100 Threshold -> $V_{IH}(DC)=V_{Ref}(DC)+130mV$, $V_{IL}(DC)=V_{Ref}(DC)-130mV$																	
		CK,$\overline{CK}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA Slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

NOTE :
1) Cell contents shaded in red are defined as 'not supported'.

[Table 50] Required time t_{VAC} above $V_{IH}(AC)$ {below $V_{IL}(AC)$} for valid transition

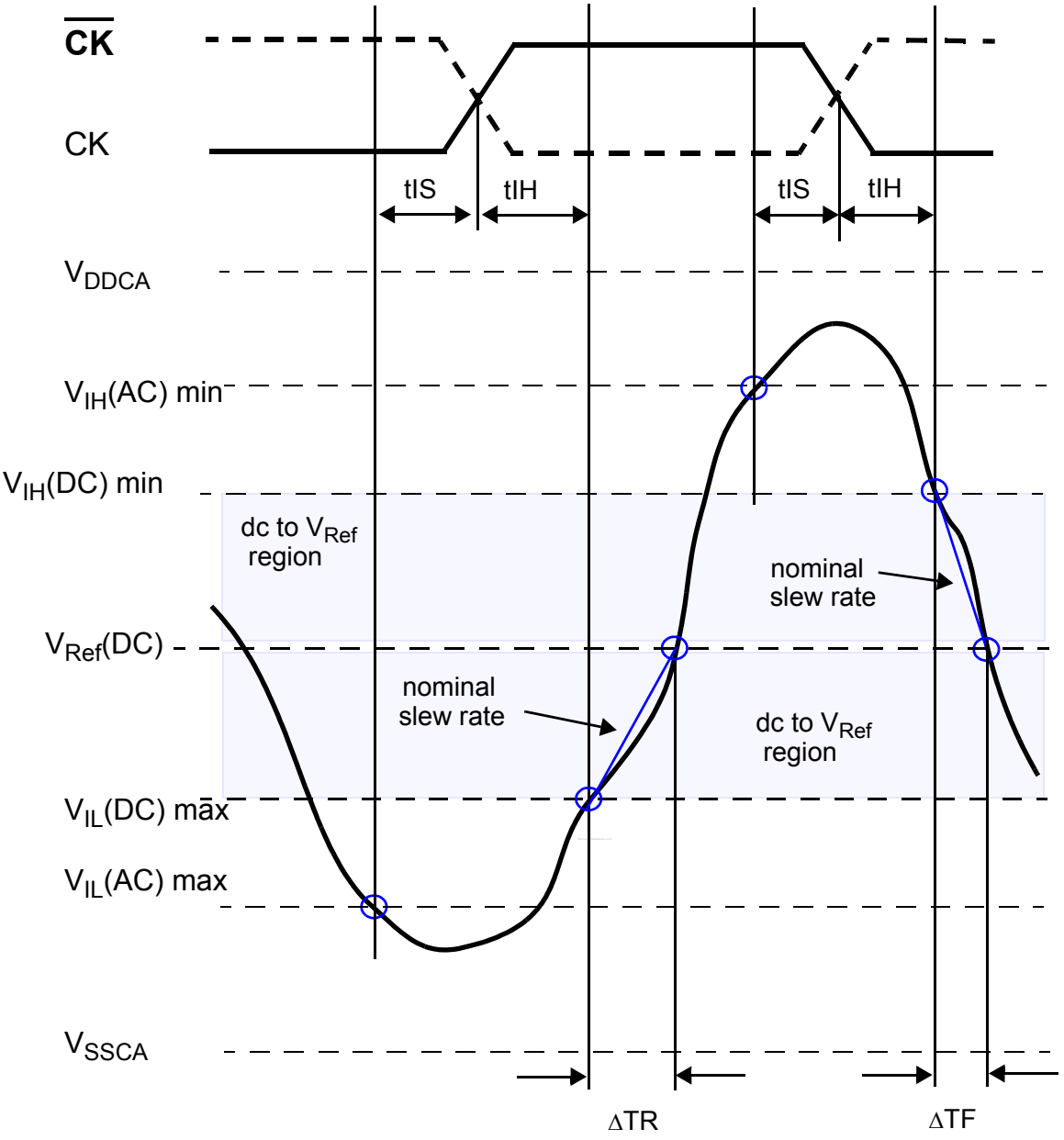
Slew Rate [V/ns]	t_{VAC} @ 220mV [ps]	
	min	max
> 2.0	175	-
2.0	170	-
1.5	167	-
1.0	163	-
0.9	162	-
0.8	161	-
0.7	159	-
0.6	155	-
0.5	150	-
< 0.5	150	-



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{Ref}(DC) - V_{IL}(AC)max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH}(AC)min - V_{Ref}(DC)}{\Delta TR}$$

Figure 16. Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} for CA and $\overline{CS}$ with respect to clock.



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{Ref}(DC) - V_{IL}(DC)max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH}(DC)min - V_{Ref}(DC)}{\Delta TF}$$

Figure 17. Illustration of nominal slew rate for hold time t_{IH} for CA and $\overline{CS}$ with respect to clock

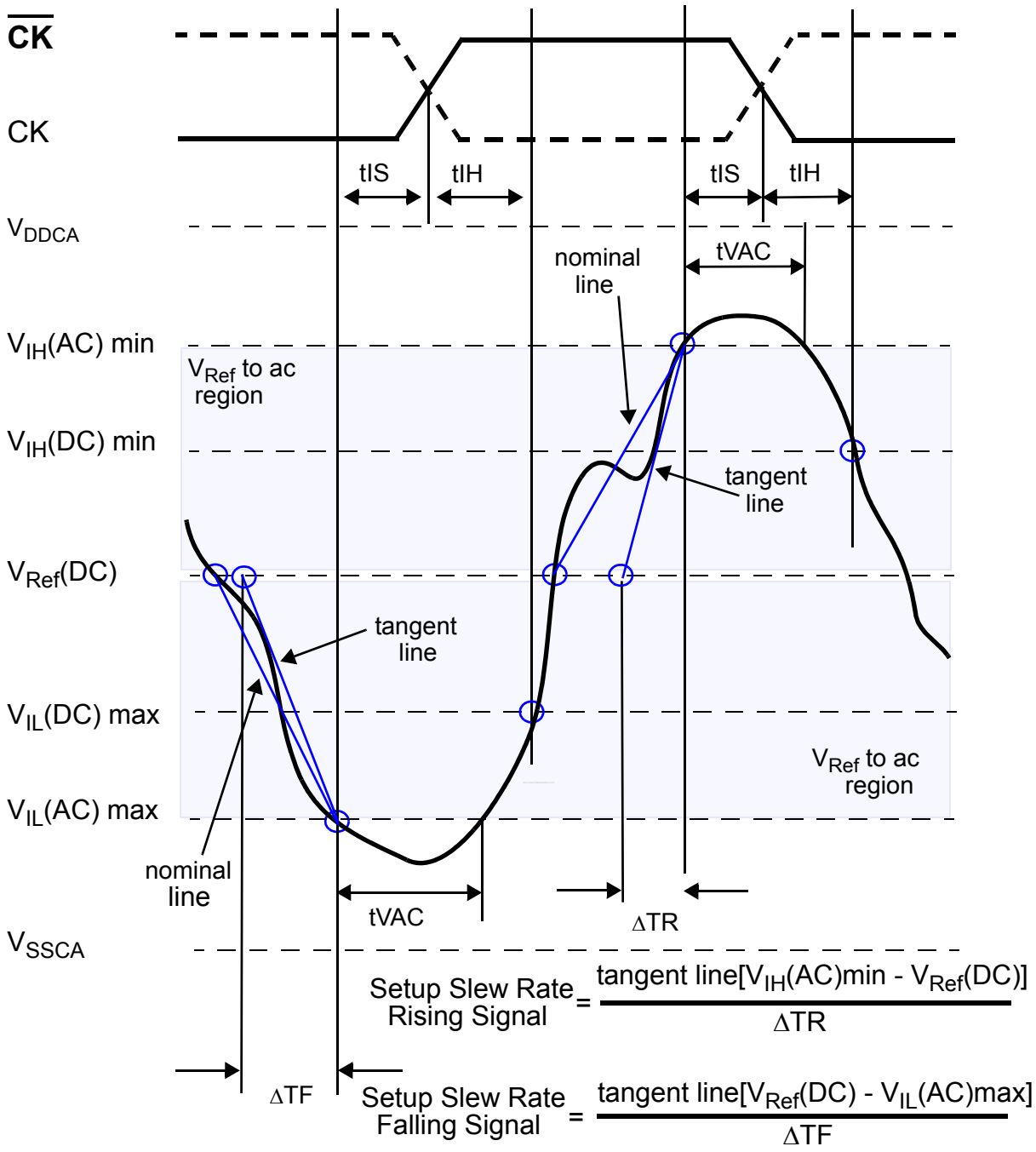
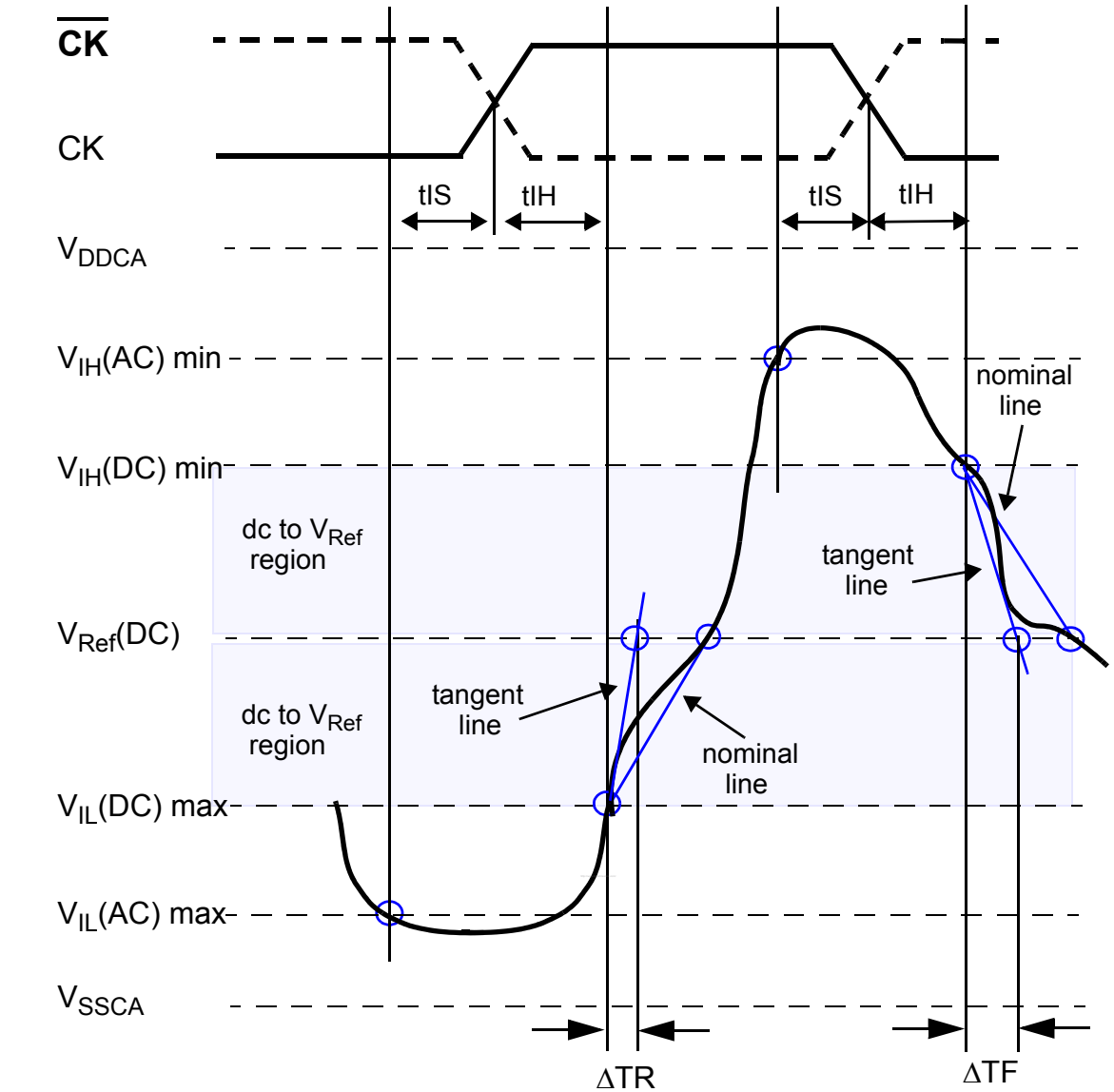


Figure 18. Illustration of tangent line for setup time t_{IS} for CA and $\overline{CS}$ with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{Ref}(DC) - V_{IL}(DC)max \text{]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [} V_{IH}(DC)min - V_{Ref}(DC) \text{]}}{\Delta TF}$$

Figure 19. Illustration of tangent line for for hold time t_{IH} for CA and $\overline{CS}$ with respect to clock

15.6 Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 51) to the ΔtDS and ΔtDH (see Table 52 and Table 54) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{Ref}(DC) and the first crossing of V_{IH}(AC)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{Ref}(DC) and the first crossing of V_{IL}(AC)max (see Figure 20). If the actual signal is always earlier than the nominal slew rate line between shaded 'V_{Ref}(DC) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'V_{Ref}(DC) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 22).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{IL}(DC)max and the first crossing of V_{Ref}(DC). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{IH}(DC)min and the first crossing of V_{Ref}(DC) (see Figure 21). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to V_{Ref}(DC) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V_{Ref}(DC) region', the slew rate of a tangent line to the actual signal from the dc level to V_{Ref}(DC) level is used for derating value (see Figure 23).

For a valid transition the input signal has to remain above/below $V_{IH/IL}$(AC) for some time t_{VAC} (see Table 53).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}$(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(AC).

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization

[Table 51] Data Setup and Hold Base-Values

[ps]	LPDDR2		reference
	800	667	
tDS(base)	50	130	VIH/L(ac)=VREF(dc)+/-220mV
tDH(base)	140	220	VIH/L(dc)=VREF(dc)+/-130mV

NOTE :
1) ac/dc referenced for 1V/ns CA slew rate and 2V/ns differential DQS-$\overline{DQS}$ slew rate.

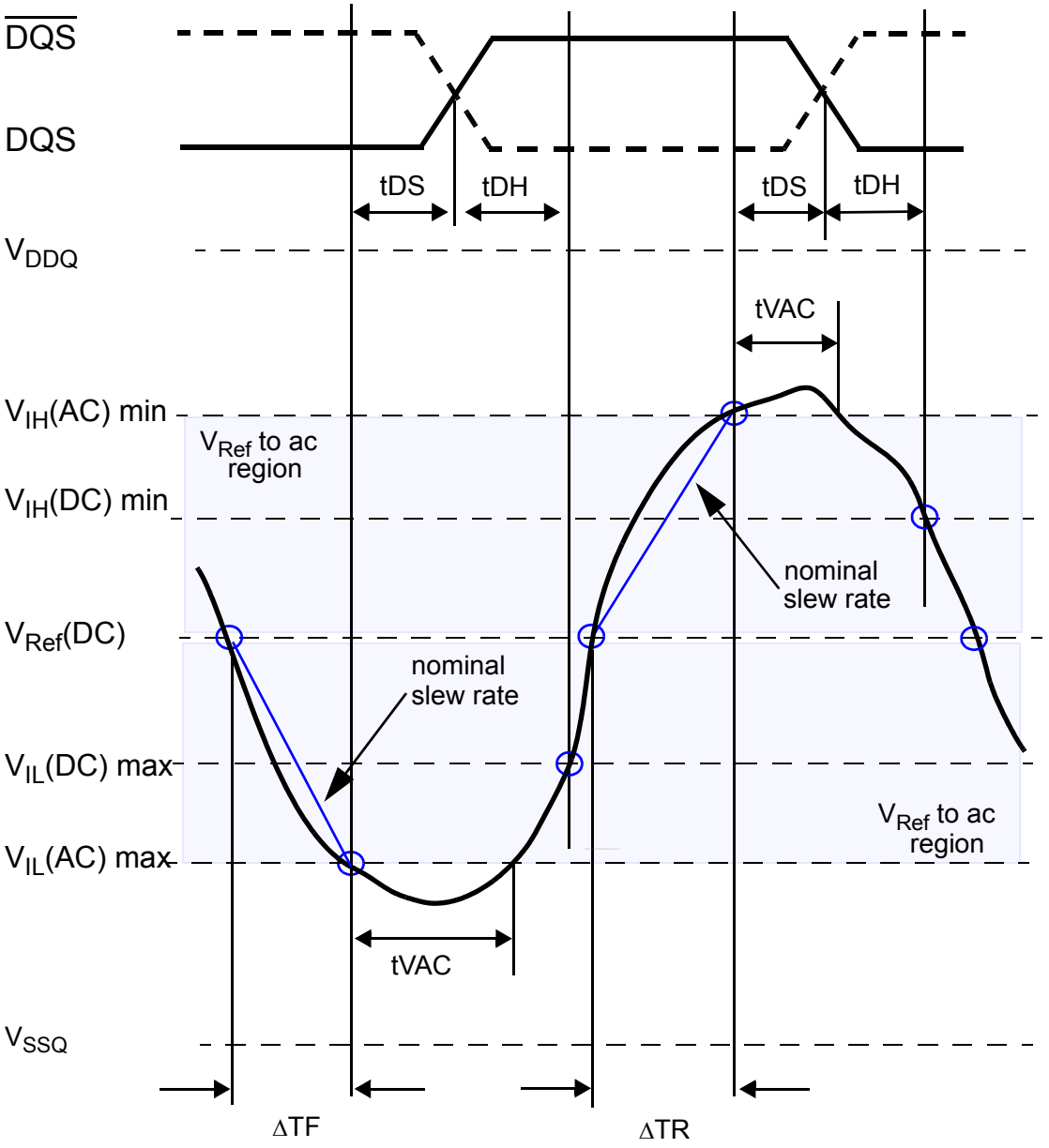
[Table 52] Derating values LPDDR2 tDS/tDH - ac/dc based AC220

ΔtDS, ΔDH derating in [ps] AC/DC based[1)] AC220 Threshold -> $V_{IH}(AC)=V_{Ref}(DC)+220mV$, $V_{IL}(AC)=V_{Ref}(DC)-220mV$ DC130 Threshold -> $V_{IH}(DC)=V_{Ref}(DC)+130mV$, $V_{IL}(DC)=V_{Ref}(DC)-130mV$																	
		DQS, $\overline{DQS}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
	1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
	0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
	0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
	0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
	0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

NOTE :
1) Cell contents shaded in red are defined as 'not supported'.

[Table 53] Required time t_{VAC} above $V_{IH}(AC)$ {below $V_{IL}(AC)$} for valid transition

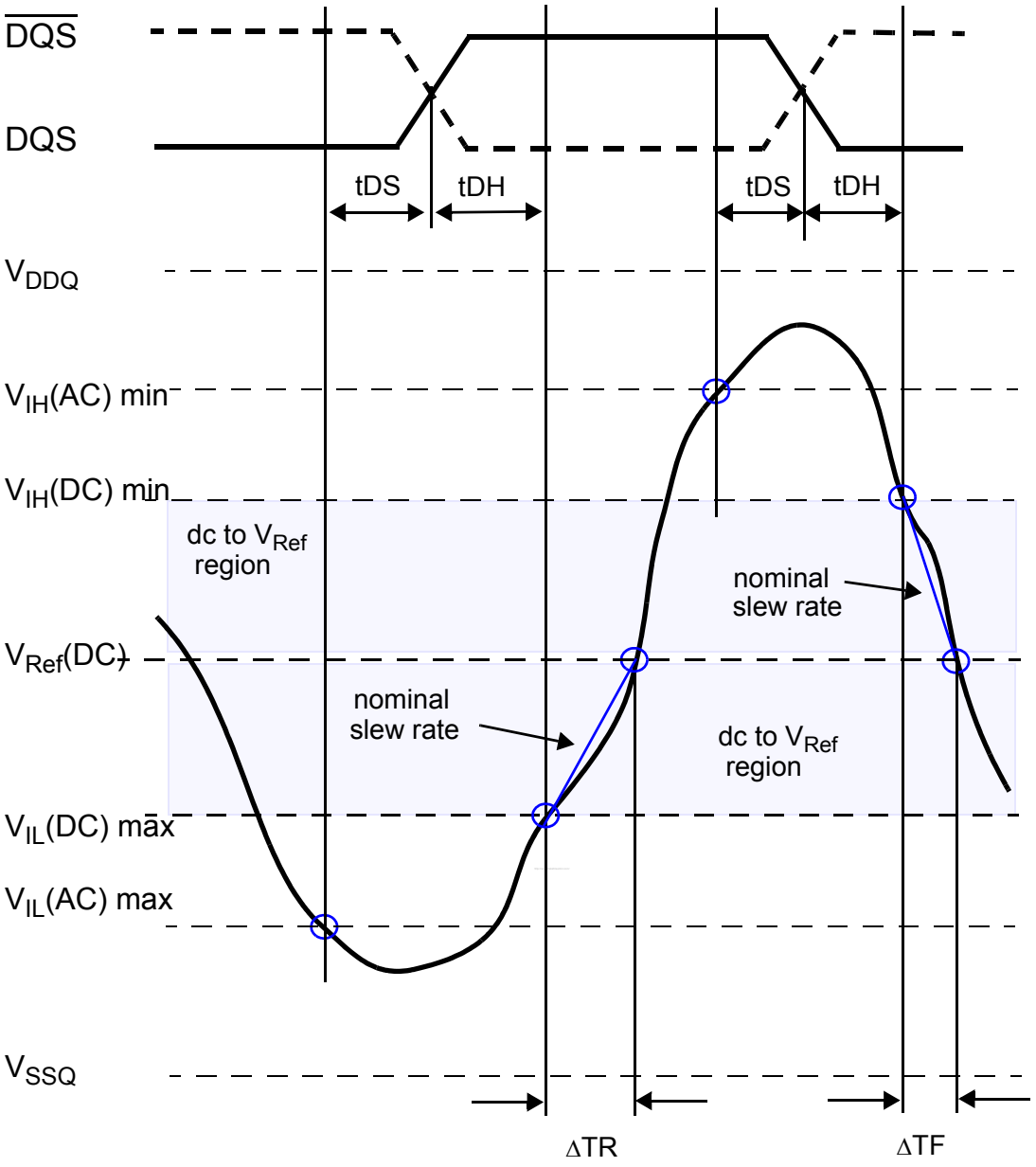
Slew Rate [V/ns]	t_{VAC} @ 220mV [ps]	
	min	max
> 2.0	175	-
2.0	170	-
1.5	167	-
1.0	163	-
0.9	162	-
0.8	161	-
0.7	159	-
0.6	155	-
0.5	150	-
< 0.5	150	-



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{Ref}(DC) - V_{IL}(AC)max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH}(AC)min - V_{Ref}(DC)}{\Delta TR}$$

Figure 20. Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{Ref}(DC) - V_{IL}(DC)max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH}(DC)min - V_{Ref}(DC)}{\Delta TF}$$

Figure 21. Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe

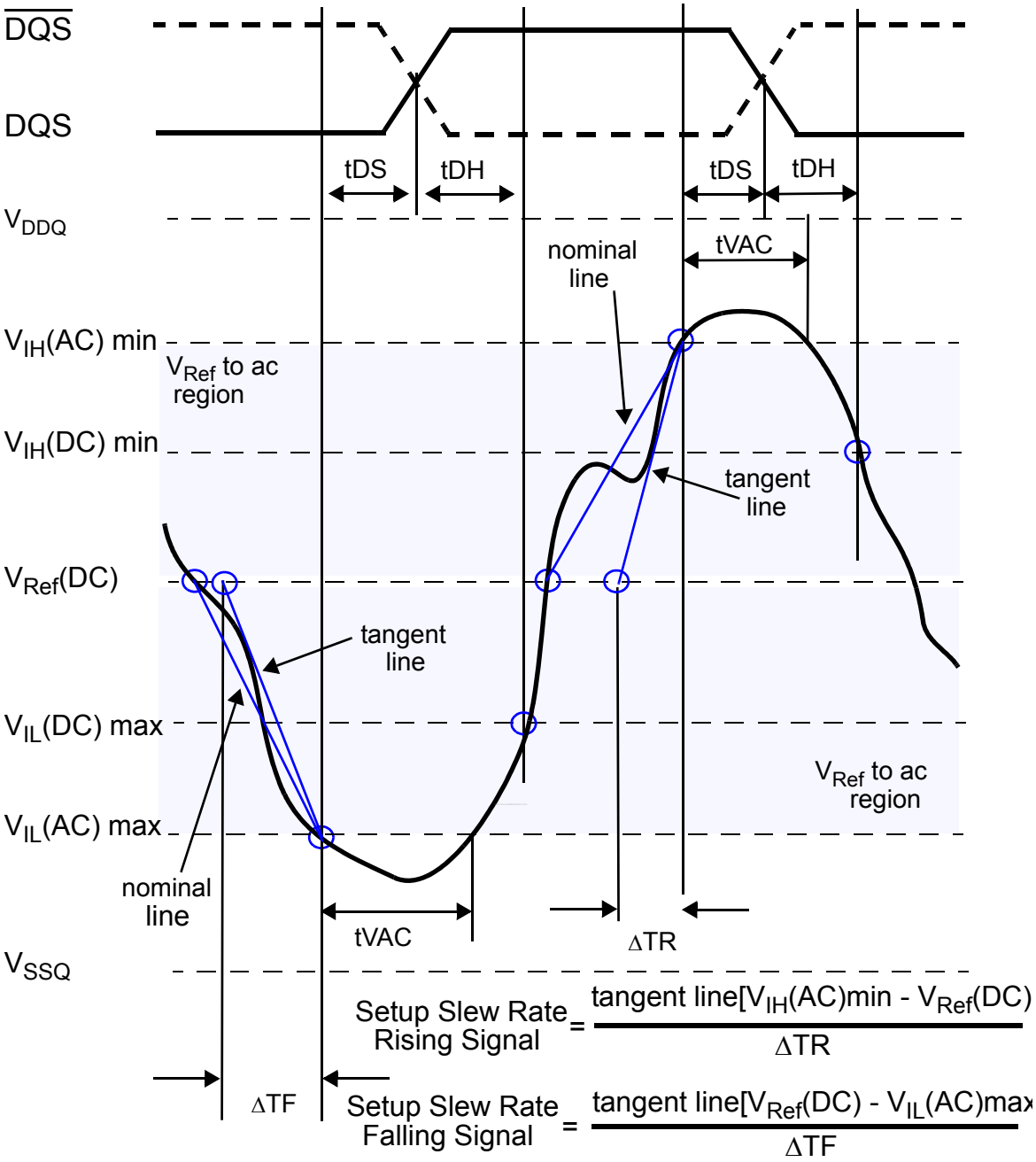
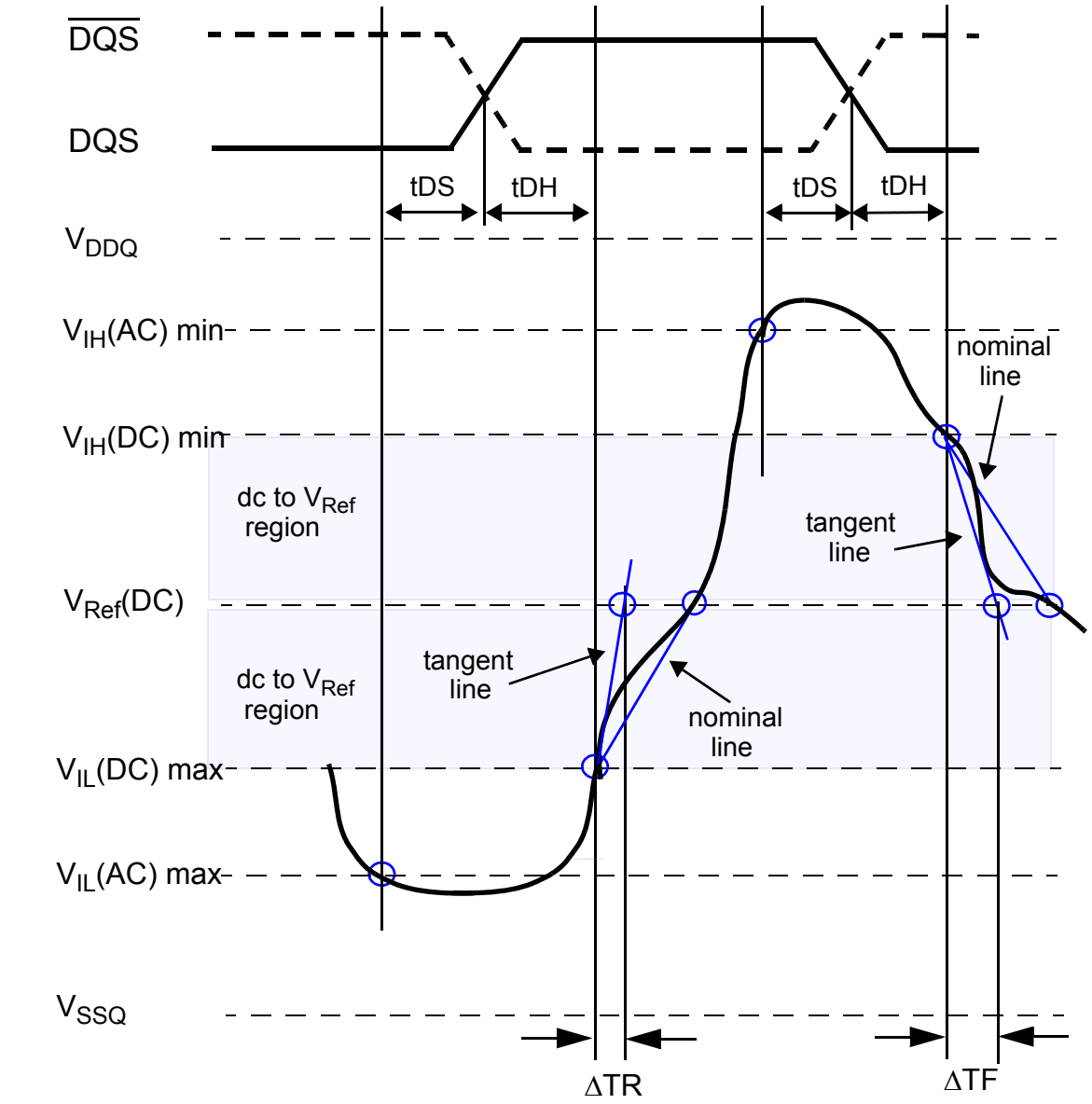


Figure 22. Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{Ref}(DC) - V_{IL}(DC)max \text{]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [} V_{IH}(DC)min - V_{Ref}(DC) \text{]}}{\Delta TF}$$

Figure 23. Illustration of tangent line for for hold time t_{DH} for DQ with respect to strobe