8Mx16
SDRAM 54CSP

(V_{DD}/V_{DDQ} 3.0V/3.0V & 3.3V/3.3V)

Revision 0.6

November 2001

Revision History

Revision 0.0 (February 21. 2001, Target)
• First generation of 128Mb Low Power SDRAM without special function (V_{DD} 3.0V, V_{DDQ} 3.0V)

Revision 0.1 (June 4. 2001, Target)
• Addition of DC Current value.

Revision 0.2 (June 20. 2001, Target)
• Changed device name from low power sdram to mobile dram.

Revision 0.3 (August 1. 2001, Target)
• Change of tSAC from 6ns to 6.5ns in case of -1L part, from 7ns to 7.5ns in case of -15 part.
• Change of tOH from 3ns to 3.5ns.
• Change V_{IH} min. from 2.0 V to 0.8xV_{DDQ} and V_{OH} min. from 2.4V to 0.9xV_{DDQ}.

Revision 0.4 (October 6. 2001, Preliminary)
• Changed DC current.
• Changed of CL2 tSAC from 6ns to 7ns and CL3 tSAC from 6.5ns to 7ns for -75 part.
• Changed of CL2 tSAC from 6.5ns to 8ns and CL1 tSAC from 18ns to 20ns for -1L part.
• Changed of tOH from 3ns to 2.5ns.
• Changed of tSS from 2.5ns to 2.0ns for -75 part and from 3.0ns to 2.5ns for -1L part.
• Integration of VDDQ 1.8V device and 2.5V device.
• Changed VIH min. from 0.8xVDDQ to 0.9xVDDQ and VOH min. from 0.9xVDDQ to 0.95xVDDQ.
• Changed VIL max. from 0.8V to 0.3V and VOL min. from 0.4V to 0.2V.
• Changed IOH from -0.1mA to -2mA and IOL from 0.1mA to 2mA.
• Erased -15 bin and added -1H bin.

Revision 0.5 (October 12. 2001, Preliminary)
• Changed VIH min. from 0.9xVDDQ to 2.0V and VOH min. from 0.95xVDDQ to 2.4V.
• Changed VIL max. from 0.3V to 0.8V and VOL min. from 0.2V to 0.4V.

Revision 0.6 (November 7. 2001, Preliminary)
• Changed VIH min. from 2.0V to 2.2V and VIL max. from 0.8V to 0.5V.

2M x 16Bit x 4 Banks SDRAM in 54CSP

FEATURES

- 3.0V & 3.3V power supply.
- LVTTL compatible with multiplexed address.
- Four banks operation.
- MRS cycle with address key programs.
  - -. CAS latency (1 & 2 & 3).
  - -. Burst length (1, 2, 4, 8 & Full page).
  - -. Burst type (Sequential & Interleave).
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation.
- DQM for masking.
- Auto refresh.
- 64ms refresh period (4K cycle).
- Commercial Temperature Operation (-25°C ~ 70°C).
  Extended Temperature Operation (-25°C ~ 85°C).

GENERAL DESCRIPTION

The K4S281633D is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 2,097,152 words by 16 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

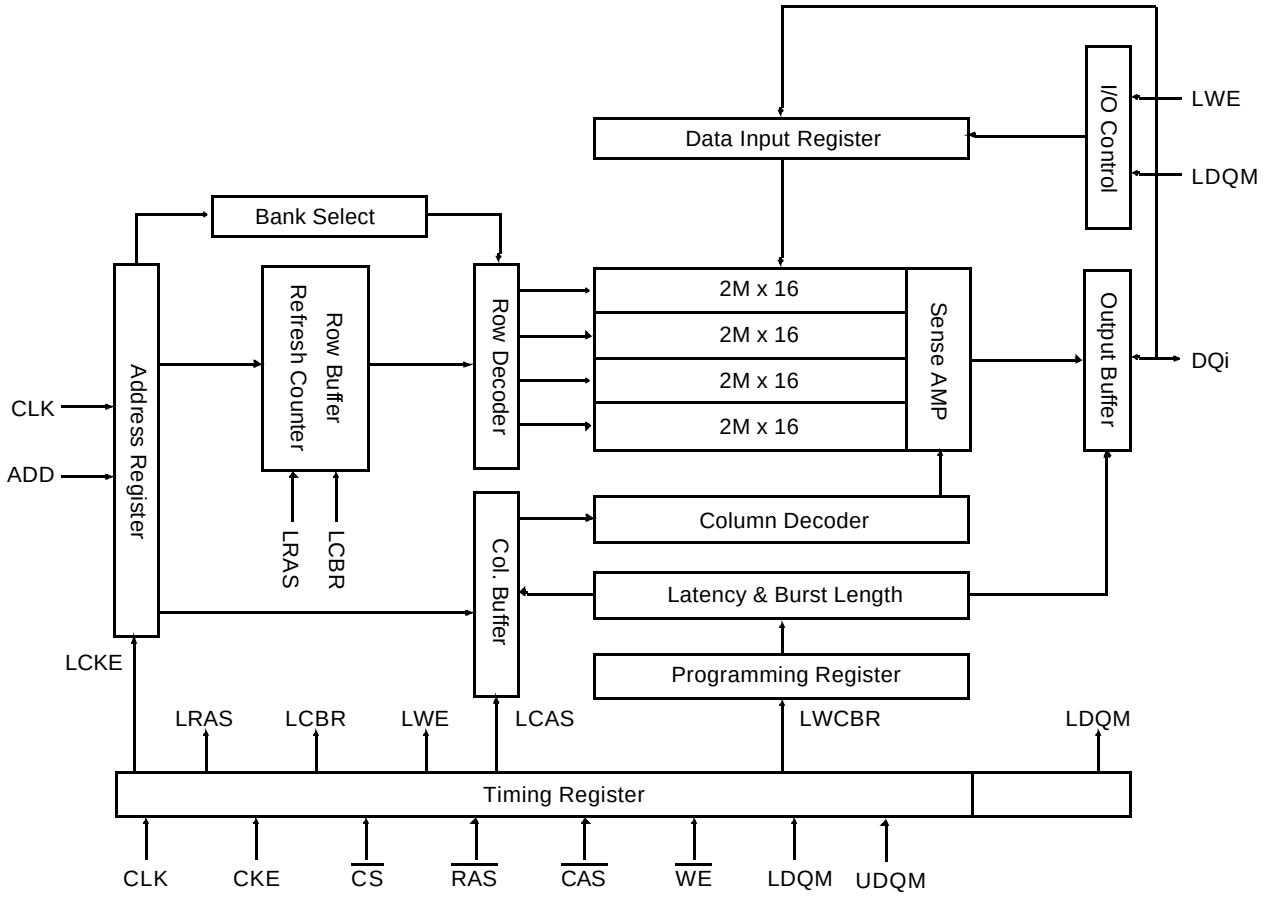
ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S281633D-RL/N75	133MHz(CL=3) 100MHz(CL=2)	LVTTL	54 CSP
K4S281633D-RL/N1H	100MHz(CL=2)		
K4S281633D-RL/N1L	100MHz(CL=3)*1		

-RN ; Low Power, Operating Temperature : -25’ C~85’ C.
-RL ; Low Power, Operating Temperature : -25’ C~70’ C.

Note : 1. In case of 40MHz Frequency, CL1 can be supported.

FUNCTIONAL BLOCK DIAGRAM



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Package Dimension and Pin Configuration

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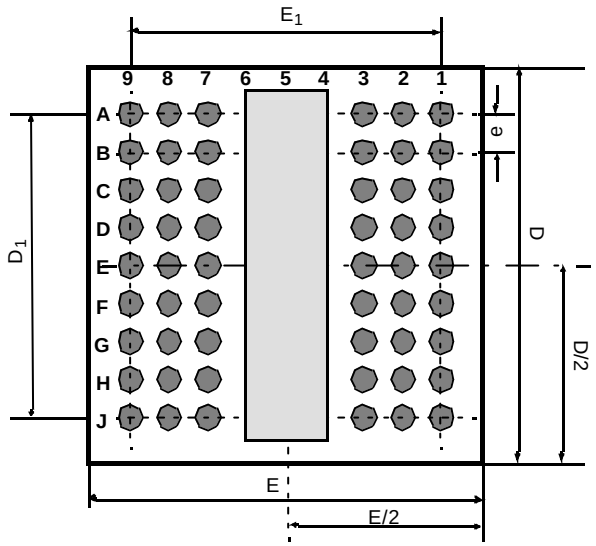
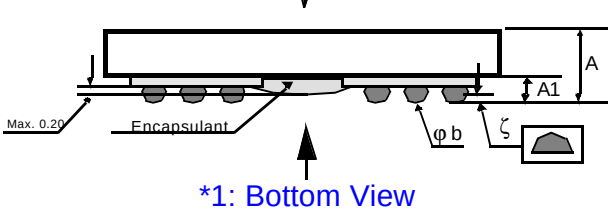


< Top View*2 >

54Ball(6x9) CSP						
	1	2	3	7	8	9
A	V_{SS}	DQ15	V_{SSQ}	V_{DDQ}	DQ0	V_{DD}
B	DQ14	DQ13	V_{DDQ}	V_{SSQ}	DQ2	DQ1
C	DQ12	DQ11	V_{SSQ}	V_{DDQ}	DQ4	DQ3
D	DQ10	DQ9	V_{DDQ}	V_{SSQ}	DQ6	DQ5
E	DQ8	NC	V_{SS}	V_{DD}	LDQM	DQ7
F	UDQM	CLK	CKE	$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
G	NC	A11	A9	BA0	BA1	$\overline{CS}$
H	A8	A7	A6	A0	A1	A10
J	V_{SS}	A5	A4	A3	A2	V_{DD}

*2: Top View



*1: Bottom View

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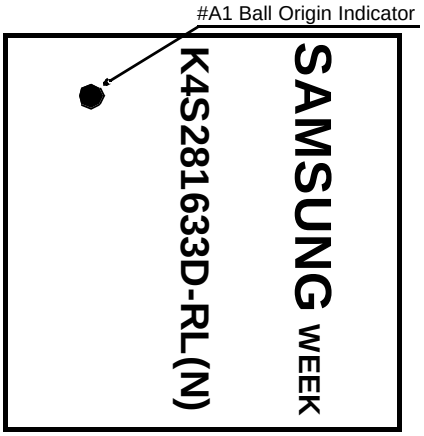


Pin Name	Pin Function
CLK	*System Clock*
$\overline{CS}$	*Chip Select*
CKE	*Clock Enable*
A_0 ~ A_{11}	*Address*
BA_0 ~ BA_1	*Bank Select Address*
$\overline{RAS}$	*Row Address Strobe*
$\overline{CAS}$	*Column Address Strobe*
$\overline{WE}$	*Write Enable*
L(U)DQM	*Data Input/Output Mask*
DQ_0 ~ $_{15}$	*Data Input/Output*
V_{DD}/V_{SS}	*Power Supply/Ground*
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*

[Unit:mm]

Symbol	Min	Typ	Max
A	0.90	0.95	1.00
A_1	0.30	0.35	0.40
E	-	8.00	-
E_1	-	6.40	-
D	-	8.00	-
D_1	-	6.40	-
e	-	0.80	-
φb	0.40	0.45	0.50
ζ	-	-	0.08

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A =-25°C ~ 70°C (Commercial), -25°C ~ 85°C (Extended))

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	2.7	3.0	3.6	V	
	V_{DDQ}	2.7	3.0	3.6	V	
Input logic high voltage	V_{IH}	2.2	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.5	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Note : 1. V_{IH} (max) = 5.3V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.0V, T_A = 23°C, f = 1MHz, V_{REF} =0.9V ± 50 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	2.0	4.0	pF	
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	2.0	4.0	pF	
Address	C_{ADD}	2.0	4.0	pF	
DQ_0 ~ DQ_{15}	C_{OUT}	3.5	6.0	pF	

DC CHARACTERISTICS

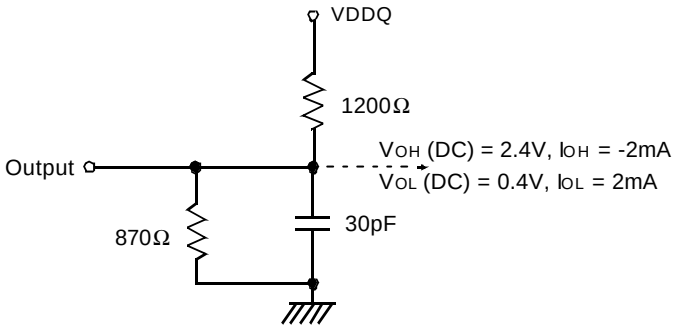
Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A =-25°C ~ 70°C (Commercial), -25°C ~ 85°C (Extended))

Parameter	Symbol	Test Condition		Version			Unit	Note
				-75	-1H	-1L		
Operating Current (One Bank Active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		80	75	75	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		0.5			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		0.5				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		12			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		10				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		7			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		7				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		23			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		20			mA	
Operating Current (Burst Mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs		130	130	110	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		170	170	155	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	-RL	500			uA	3
			-RN				uA	4

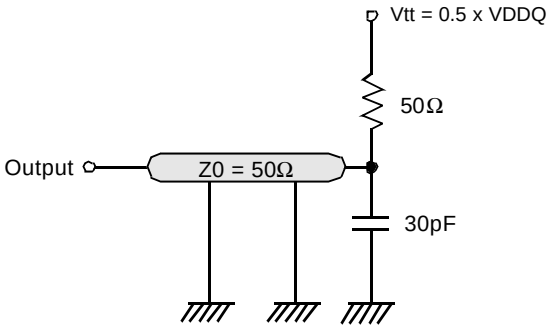
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S281633D-RL**
4. K4S281633D-RN**
5. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS (V_{DD} = 2.7V ~ 3.6V, T_A =-25°C ~ 70°C (Commercial), -25°C ~ 85°C (Extended))

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	0.5 x VDDQ	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	0.5 x VDDQ	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			- 75	-1H	-1L		
Row active to row active delay		tRRD(min)	15	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	24	ns	1
Row active time		tRAS(min)	45	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	65	70	84	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2
Last data in to Active delay		tDAL (min)	2 CLK + tRP			-	
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		-		0		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	- 75		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		12			
	CAS latency=1		-		-		25			
CLK to valid output delay	CAS latency=3	tSAC		5.4		7		7	ns	1,2
	CAS latency=2			7		7		8		
	CAS latency=1			-		-		20		
Output data hold time	CAS latency=3	tOH	2.5		2.5		2.5		ns	2
	CAS latency=2		2.5		2.5		2.5			
	CAS latency=1		-		-		2.5			
CLK high pulse width		tCH	2.5		3		3		ns	3
CLK low pulse width		tCL	2.5		3		3		ns	3
Input setup time		tSS	2.0		2.5		2.5		ns	3
Input hold time		tSH	1.0		1.5		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		7		7	ns	
	CAS latency=2			7		7		8		
	CAS latency=1			-		-		20		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_{9} ~ A_{0}	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are the same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with Normal MRS

Address	BA0 ~ BA1*1	A11 ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	"0" Setting for Normal MRS	RFU	W.B.L	Test Mode		CAS Latency			BT	Burst Length		

Normal MRS Mode

Test Mode			CAS Latency				Burst Type			Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type		A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential		0	0	0	1	1
0	1	Reserved	0	0	1	1	1	Interleave		0	0	1	2	2
1	0	Reserved	0	1	0	2	Mode Select			0	1	0	4	4
1	1	Reserved	0	1	1	3	BA1	BA0	Mode	0	1	1	8	8
Write Burst Length			1	0	0	Reserved	0	0	Setting for Nor-mal MRS	1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved				1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved				1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved				1	1	1	Full Page	Reserved

Full Page Length : 256(x16)

Power Up Sequence

1. Apply power and start clock, Attempt to maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Power is applied to VDD and VDDQ (simultaneously).
3. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
4. Issue precharge commands for all banks of the devices.
5. Issue 2 or more auto-refresh commands.
6. Issue a mode register set command to initialize the mode register.

Note : 1. In order to assert normal MRS, BA0 and BA1 should set "0" absolutely.