

**512Mb B-die DDR2 SDRAM Specification
Version 1.4**

February 2005

Contents

0. Ordering Information

1. Key Feature

2. Package Pinout/Mechanical Dimension & Addressing

- 2.1 Package Pinout & Mechanical Dimension
- 2.2 Input/Output Function Description
- 2.3 Addressing

3. Absolute Maximum Rating

4. AC & DC Operating Conditions & Specifications

0. Ordering Information

| Organization | DDR2-533 4-4-4 | DDR2-400 3-3-3 | Package |
|--------------|-----------------|-----------------|-----------|
| 128Mx4 | K4T51043QB-GCD5 | K4T51043QB-GCCC | Leaded |
| | K4T51043QB-ZCD5 | K4T51043QB-ZCCC | Lead-Free |
| 64Mx8 | K4T51083QB-GCD5 | K4T51083QB-GCCC | Leaded |
| | K4T51083QB-ZCD5 | K4T51083QB-ZCCC | Lead-Free |
| 32Mx16 | K4T51163QB-GCD5 | K4T51163QB-GCCC | Leaded |
| | K4T51163QB-ZCD5 | K4T51163QB-ZCCC | Lead-Free |

Note : Speed bin is in order of CL-tRCD-tRP

1. Key Features

| Speed | DDR2-533 4-4-4 | DDR2-400 3-3-3 | Units |
|-------------|-------------------|-------------------|-------|
| CAS Latency | 4 | 3 | tCK |
| tRCD(min) | 15 | 15 | ns |
| tRP(min) | 15 | 15 | ns |
| tRC(min) | 55 | 55 | ns |

- JEDEC standard 1.8V ± 0.1V Power Supply
- VDDQ = 1.8V ± 0.1V
- 200 MHz f_{CK} for 400Mb/sec/pin, 267MHz f_{CK} for 533Mb/sec/pin
- 4 Banks
- Posted \overline{CAS}
- Programmable \overline{CAS} Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1, 2, 3 and 4
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4, 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95 °C
- Package: 60ball FBGA - 128Mx4/64Mx8, 84ball FBGA - 32Mx16
- All of Lead-free products are compliant for RoHS

The 512Mb DDR2 SDRAM is organized as a 32Mbit x 4 I/Os x 4 banks, 16Mbit x 8 I/Os x 4banks or 8Mbit x 16 I/Os x 4 banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 533Mb/sec/pin (DDR2-533) for general applications.

The chip is designed to comply with the following key DDR2 SDRAM features such as posted CAS with additive latency, write latency = read latency -1, Off-Chip Driver(OCD) impedance adjustment and On Die Termination.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and \overline{CK} falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and \overline{DQS}) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a $\overline{RAS}/\overline{CAS}$ multiplexing style. For example, 512Mb(x4) device receive 14/11/2 addressing.

The 512Mb DDR2 device operates with a single 1.8V ± 0.1V power supply and 1.8V ± 0.1V VDDQ.

The 512Mb DDR2 device is available in 60ball FBGAs(x4/x8) and in 84ball FBGAs(x16).

Note: The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Note : This data sheet is an abstract of full DDR2 specification and does not cover the common features which are described in "Samsung's DDR2 SDRAM Device Operation & Timing Diagram"

2. Package Pinout/Mechanical Dimension & Addressing

2.1 Package Pinout

x4 package pinout (Top View) : 60ball FBGA Package

| 1 | 2 | 3 | | 7 | 8 | 9 |
|------|------|-----------------|---|------------------|------------------|------|
| VDD | NC | VSS | A | VSSQ | \overline{DQS} | VDDQ |
| NC | VSSQ | DM | B | DQS | VSSQ | NC |
| VDDQ | DQ1 | VDDQ | C | VDDQ | DQ0 | VDDQ |
| NC | VSSQ | DQ3 | D | DQ2 | VSSQ | NC |
| VDDL | VREF | VSS | E | VSSDL | CK | VDD |
| | CKE | \overline{WE} | F | \overline{RAS} | \overline{CK} | ODT |
| NC | BA0 | BA1 | G | \overline{CAS} | \overline{CS} | |
| | A10 | A1 | H | A2 | A0 | VDD |
| VSS | A3 | A5 | J | A6 | A4 | |
| | A7 | A9 | K | A11 | A8 | VSS |
| VDD | A12 | NC | L | NC | A13 | |

Notes:

1. Pin B3 has identical capacitance as pin B7.
2. VDDL and VSSDL are power and ground for the DLL.

Ball Locations (x4)

- : Populated Ball
- + : Depopulated Ball

Top View (See the balls through the Package)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|
| A | ● | ● | ● | + | + | + | ● | ● | ● |
| B | ● | ● | ● | + | + | + | ● | ● | ● |
| C | ● | ● | ● | + | + | + | ● | ● | ● |
| D | ● | ● | ● | + | + | + | ● | ● | ● |
| E | ● | ● | ● | + | + | + | ● | ● | ● |
| F | + | ● | ● | + | + | + | ● | ● | ● |
| G | ● | ● | ● | + | + | + | ● | ● | + |
| H | + | ● | ● | + | + | + | ● | ● | ● |
| J | ● | ● | ● | + | + | + | ● | ● | + |
| K | + | ● | ● | + | + | + | ● | ● | ● |
| L | ● | ● | ● | + | + | + | ● | ● | + |

x8 package pinout (Top View) : 60ball FBGA Package

| 1 | 2 | 3 | | 7 | 8 | 9 |
|------|-------------|-------------|---|-------|------|------|
| VDD | NU/ RDQS | VSS | A | VSSQ | DQS | VDDQ |
| DQ6 | VSSQ | DM/ RDQS | B | DQS | VSSQ | DQ7 |
| VDDQ | DQ1 | VDDQ | C | VDDQ | DQ0 | VDDQ |
| DQ4 | VSSQ | DQ3 | D | DQ2 | VSSQ | DQ5 |
| VDDL | VREF | VSS | E | VSSDL | CK | VDD |
| | CKE | WE | F | RAS | CK | ODT |
| NC | BA0 | BA1 | G | CAS | CS | |
| | A10 | A1 | H | A2 | A0 | VDD |
| VSS | A3 | A5 | J | A6 | A4 | |
| | A7 | A9 | K | A11 | A8 | VSS |
| VDD | A12 | NC | L | NC | A13 | |

Notes:

1. Pins B3 and A2 have identical capacitance as pins B7 and A8.
2. For a read, when enabled, strobe pair RDQS & RDQS are identical in function and timing to strobe pair DQS & DQS and input masking function is disabled.
3. The function of DM or RDQS/RDQS are enabled by EMRS command.
4. VDDL and VSSDL are power and ground for the DLL.

Ball Locations (x8)

- : Populated Ball
- + : Depopulated Ball

Top View (See the balls through the Package)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|
| A | ● | ● | ● | + | + | + | ● | ● | ● |
| B | ● | ● | ● | + | + | + | ● | ● | ● |
| C | ● | ● | ● | + | + | + | ● | ● | ● |
| D | ● | ● | ● | + | + | + | ● | ● | ● |
| E | ● | ● | ● | + | + | + | ● | ● | ● |
| F | + | ● | ● | + | + | + | ● | ● | ● |
| G | ● | ● | ● | + | + | + | ● | ● | + |
| H | + | ● | ● | + | + | + | ● | ● | ● |
| J | ● | ● | ● | + | + | + | ● | ● | + |
| K | + | ● | ● | + | + | + | ● | ● | ● |
| L | ● | ● | ● | + | + | + | ● | ● | + |

x16 package pinout (Top View) : 84ball FBGA Package

| 1 | 2 | 3 | | 7 | 8 | 9 |
|------|------|------------------------|---|-------------------------|--------------------------|------|
| VDD | NC | VSS | A | VSSQ | $\overline{\text{UDQS}}$ | VDDQ |
| UDQ6 | VSSQ | UDM | B | UDQS | VSSQ | UDQ7 |
| VDDQ | UDQ1 | VDDQ | C | VDDQ | UDQ0 | VDDQ |
| UDQ4 | VSSQ | UDQ3 | D | UDQ2 | VSSQ | UDQ5 |
| VDD | NC | VSS | E | VSSQ | $\overline{\text{LDQS}}$ | VDDQ |
| LDQ6 | VSSQ | LDM | F | LDQS | VSSQ | LDQ7 |
| VDDQ | LDQ1 | VDDQ | G | VDDQ | LDQ0 | VDDQ |
| LDQ4 | VSSQ | LDQ3 | H | LDQ2 | VSSQ | LDQ5 |
| VDDL | VREF | VSS | J | VSSDL | CK | VDD |
| | CKE | $\overline{\text{WE}}$ | K | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$ | ODT |
| NC | BA0 | BA1 | L | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$ | |
| | A10 | A1 | M | A2 | A0 | VDD |
| VSS | A3 | A5 | N | A6 | A4 | |
| | A7 | A9 | P | A11 | A8 | VSS |
| VDD | A12 | NC | R | NC | NC | |

Note :

1. VDDL and VSSDL are power and ground for the DLL.

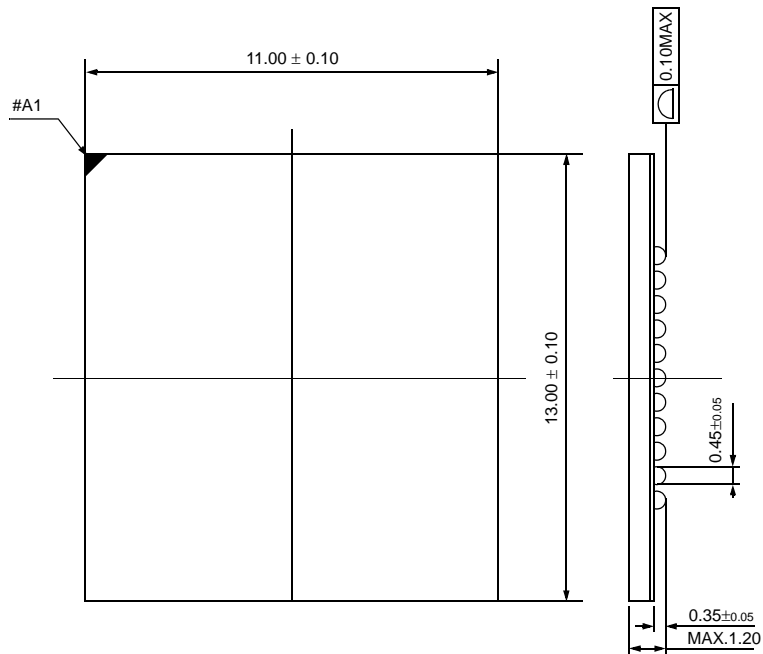
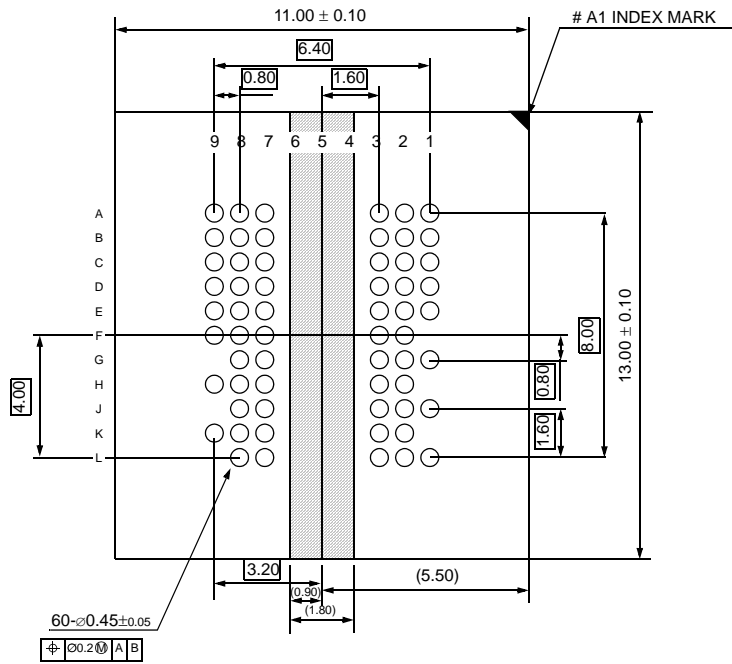
Ball Locations (x16)

● : Populated Ball
 + : Depopulated Ball

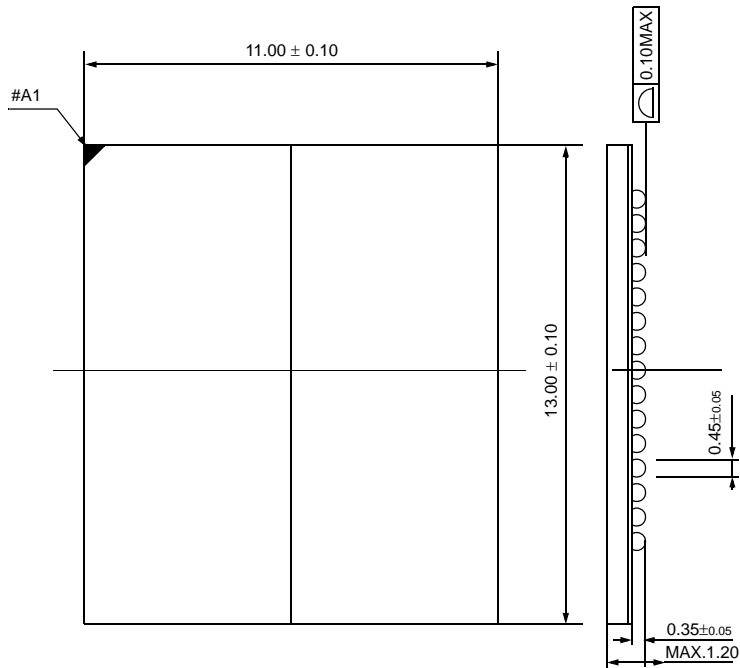
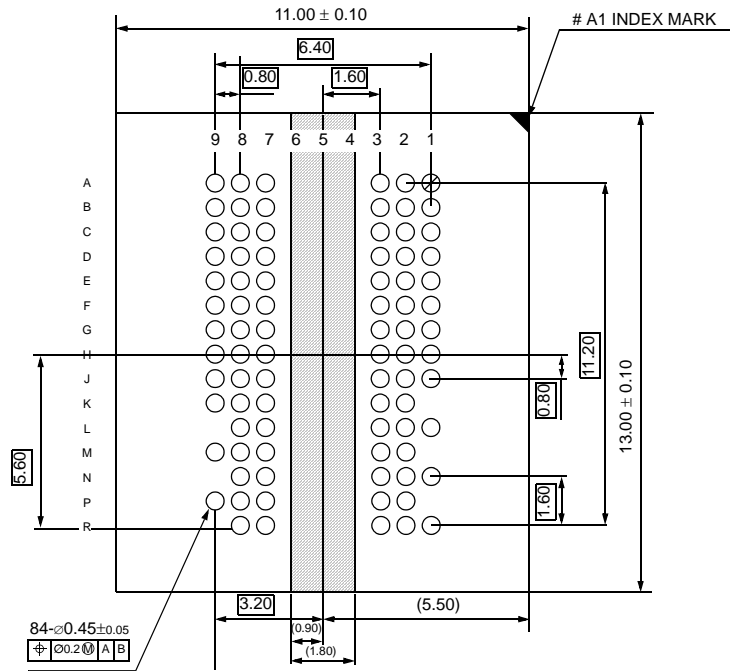
Top View
 (See the balls through the Package)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|
| A | ● | ● | ● | + | + | + | ● | ● | ● |
| B | ● | ● | ● | + | + | + | ● | ● | ● |
| C | ● | ● | ● | + | + | + | ● | ● | ● |
| D | ● | ● | ● | + | + | + | ● | ● | ● |
| E | ● | ● | ● | + | + | + | ● | ● | ● |
| F | ● | ● | ● | + | + | + | ● | ● | ● |
| G | ● | ● | ● | + | + | + | ● | ● | ● |
| H | ● | ● | ● | + | + | + | ● | ● | ● |
| J | ● | ● | ● | + | + | + | ● | ● | ● |
| K | + | ● | ● | + | + | + | ● | ● | ● |
| L | ● | ● | ● | + | + | + | ● | ● | + |
| M | + | ● | ● | + | + | + | ● | ● | ● |
| N | ● | ● | ● | + | + | + | ● | ● | + |
| P | + | ● | ● | + | + | + | ● | ● | ● |
| R | ● | ● | ● | + | + | + | ● | ● | + |

FBGA Package Dimension(x4/x8)



FBGA Package Dimension(x16)



2.2 Input/Output Functional Description

| Symbol | Type | Function |
|--|--------------|---|
| CK, \overline{CK} | Input | Clock: CK and \overline{CK} are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of \overline{CK} . Output (read) data is referenced to the crossings of CK and \overline{CK} (both directions of crossing). |
| CKE | Input | Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, V_{REF} must be maintained to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, \overline{CK} , ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh. |
| \overline{CS} | Input | Chip Select: All commands are masked when \overline{CS} is registered HIGH. \overline{CS} provides for external Rank selection on systems with multiple Ranks. \overline{CS} is considered part of the command code. |
| ODT | Input | On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, \overline{DQS} , RDQS, \overline{RDQS} , and DM signal for x4/x8 configurations. For x16 configuration, ODT is applied to each DQ, UDQS/ \overline{UDQS} , LDQS/ \overline{LDQS} , UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register Set(EMRS) is programmed to disable ODT. |
| \overline{RAS} , \overline{CAS} , \overline{WE} | Input | Command Inputs: \overline{RAS} , \overline{CAS} and \overline{WE} (along with \overline{CS}) define the command being entered. |
| DM | Input | Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/ \overline{RDQS} is enabled by EMRS command. |
| BA0 - BA1 | Input | Bank Address Inputs: BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle. |
| A0 - A13 | Input | Address Inputs: Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands. |
| DQ | Input/Output | Data Input/ Output: Bi-directional data bus. |
| DQS, \overline{DQS} (LDQS), \overline{LDQS} (UDQS), \overline{UDQS} (RDQS), \overline{RDQS} | Input/Output | Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals \overline{DQS} , \overline{LDQS} , \overline{UDQS} , and \overline{RDQS} to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals. |
| NC | | No Connect: No internal electrical connection is present. |
| V_{DD}/V_{DDQ} | Supply | Power Supply: 1.8V +/- 0.1V, DQ Power Supply: 1.8V +/- 0.1V |
| V_{SS}/V_{SSQ} | Supply | Ground, DQ Ground |
| V_{DDL} | Supply | DLL Power Supply: 1.8V +/- 0.1V |
| V_{SSDL} | Supply | DLL Ground |
| V_{REF} | Supply | Reference voltage |

In this data sheet, "differential DQS signals" refers to any of the following with A10 = 0 of EMRS(1)

x4 DQS/ \overline{DQS}
x8 DQS/ \overline{DQS} if EMRS(1)[A11] = 0
x8 DQS/ \overline{DQS} , RDQS/ \overline{RDQS} , \overline{UDQS} if EMRS(1)[A11] = 1
x16 LDQS/ \overline{LDQS} and UDQS/ \overline{UDQS}

"single-ended DQS signals" refers to any of the following with A10 = 1 of EMRS(1)

x4 DQS
x8 DQS if EMRS(1) [A11] = 0
x8 DQS, RDQS, if EMRS(1) [A11] = 1
x16 LDQS and UDQS

2.3 512Mb Addressing

| Configuration | 128Mb x4 | 64Mb x 8 | 32Mb x16 |
|----------------|--|----------------------------------|----------------------------------|
| # of Bank | 4 | 4 | 4 |
| Bank Address | BA0,BA1 | BA0,BA1 | BA0,BA1 |
| Auto precharge | A ₁₀ /AP | A ₁₀ /AP | A ₁₀ /AP |
| Row Address | A ₀ ~ A ₁₃ | A ₀ ~ A ₁₃ | A ₀ ~ A ₁₂ |
| Column Address | A ₀ ~ A ₉ ,A ₁₁ | A ₀ ~ A ₉ | A ₀ ~ A ₉ |

* Reference information: The following tables are address mapping information for other densities.

256Mb

| Configuration | 64Mb x4 | 32Mb x 8 | 16Mb x16 |
|----------------|--|----------------------------------|----------------------------------|
| # of Bank | 4 | 4 | 4 |
| Bank Address | BA0,BA1 | BA0,BA1 | BA0,BA1 |
| Auto precharge | A ₁₀ /AP | A ₁₀ /AP | A ₁₀ /AP |
| Row Address | A ₀ ~ A ₁₂ | A ₀ ~ A ₁₂ | A ₀ ~ A ₁₂ |
| Column Address | A ₀ ~ A ₉ ,A ₁₁ | A ₀ ~ A ₉ | A ₀ ~ A ₈ |

1Gb

| Configuration | 256Mb x4 | 128Mb x 8 | 64Mb x16 |
|----------------|--|----------------------------------|----------------------------------|
| # of Bank | 8 | 8 | 8 |
| Bank Address | BA0 ~ BA2 | BA0 ~ BA2 | BA0 ~ BA2 |
| Auto precharge | A ₁₀ /AP | A ₁₀ /AP | A ₁₀ /AP |
| Row Address | A ₀ ~ A ₁₃ | A ₀ ~ A ₁₃ | A ₀ ~ A ₁₂ |
| Column Address | A ₀ ~ A ₉ ,A ₁₁ | A ₀ ~ A ₉ | A ₀ ~ A ₉ |

2Gb

| Configuration | 512Mb x4 | 256Mb x 8 | 128Mb x16 |
|----------------|--|----------------------------------|----------------------------------|
| # of Bank | 8 | 8 | 8 |
| Bank Address | BA0 ~ BA2 | BA0 ~ BA2 | BA0 ~ BA2 |
| Auto precharge | A ₁₀ /AP | A ₁₀ /AP | A ₁₀ /AP |
| Row Address | A ₀ ~ A ₁₄ | A ₀ ~ A ₁₄ | A ₀ ~ A ₁₃ |
| Column Address | A ₀ ~ A ₉ ,A ₁₁ | A ₀ ~ A ₉ | A ₀ ~ A ₉ |

4Gb

| Configuration | 1 Gb x4 | 512Mb x 8 | 256Mb x16 |
|--------------------------|--|----------------------------------|----------------------------------|
| # of Bank | 8 | 8 | 8 |
| Bank Address | BA0 ~ BA2 | BA0 ~ BA2 | BA0 ~ BA2 |
| Auto precharge | A ₁₀ /AP | A ₁₀ /AP | A ₁₀ /AP |
| Row Address | A ₀ ~ A ₁₅ | A ₀ ~ A ₁₅ | A ₀ ~ A ₁₄ |
| Column Address/page size | A ₀ ~ A ₉ ,A ₁₁ | A ₀ ~ A ₉ | A ₀ ~ A ₉ |

3. Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | Notes |
|------------------------------------|-------------------------------------|-----------------|-------|-------|
| VDD | Voltage on VDD pin relative to Vss | - 1.0 V ~ 2.3 V | V | 1 |
| VDDQ | Voltage on VDDQ pin relative to Vss | - 0.5 V ~ 2.3 V | V | 1 |
| VDDL | Voltage on VDDL pin relative to Vss | - 0.5 V ~ 2.3 V | V | 1 |
| V _{IN} , V _{OUT} | Voltage on any pin relative to Vss | - 0.5 V ~ 2.3 V | V | 1 |
| T _{STG} | Storage Temperature | -55 to +100 | °C | 1, 2 |

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

4. AC & DC Operating Conditions

Recommended DC Operating Conditions (SSTL - 1.8)

| Symbol | Parameter | Rating | | | Units | Notes |
|--------|---------------------------|-----------|-----------|-----------|-------|-------|
| | | Min. | Typ. | Max. | | |
| VDD | Supply Voltage | 1.7 | 1.8 | 1.9 | V | |
| VDDL | Supply Voltage for DLL | 1.7 | 1.8 | 1.9 | V | 4 |
| VDDQ | Supply Voltage for Output | 1.7 | 1.8 | 1.9 | V | 4 |
| VREF | Input Reference Voltage | 0.49*VDDQ | 0.50*VDDQ | 0.51*VDDQ | mV | 1,2 |
| VTT | Termination Voltage | VREF-0.04 | VREF | VREF+0.04 | V | 3 |

There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.

- The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
- Peak to peak AC noise on VREF may not exceed +/-2% VREF(DC).
- VTT of transmitting device must track VREF of receiving device.
- AC parameters are measured with VDD, VDDQ and VDDL tied together.

Operating Temperature Condition

| Symbol | Parameter | Rating | Units | Notes |
|--------|-----------------------|---------|-------|-------|
| TOPER | Operating Temperature | 0 to 95 | °C | 1, 2 |

1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
2. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (tREFI=3.9 us) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

Input DC Logic Level

| Symbol | Parameter | Min. | Max. | Units | Notes |
|----------------------|---------------------|--------------|--------------|-------|-------|
| V _{IH} (DC) | DC input logic high | VREF + 0.125 | VDDQ + 0.3 | V | |
| V _{IL} (DC) | DC input logic low | - 0.3 | VREF - 0.125 | V | |

Input AC Logic Level

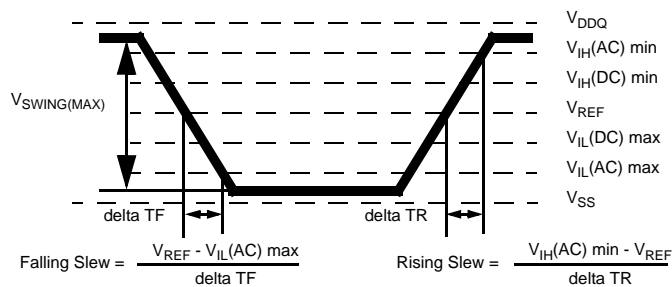
| Symbol | Parameter | Min. | Max. | Units | Notes |
|----------------------|---------------------|--------------|--------------|-------|-------|
| V _{IH} (AC) | AC input logic high | VREF + 0.250 | - | V | |
| V _{IL} (AC) | AC input logic low | - | VREF - 0.250 | V | |

AC Input Test Conditions

| Symbol | Condition | Value | Units | Notes |
|-------------------------|---|------------------------|-------|-------|
| V _{REF} | Input reference voltage | 0.5 * V _{DDQ} | V | 1 |
| V _{SWING(MAX)} | Input signal maximum peak to peak swing | 1.0 | V | 1 |
| SLEW | Input signal minimum slew rate | 1.0 | V/ns | 2, 3 |

Notes:

1. Input waveform timing is referenced to the input signal crossing through the V_{IH/IL}(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to V_{IH}(AC) min for rising edges and the range from V_{REF} to V_{IL}(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from V_{IL}(AC) to V_{IH}(AC) on the positive transitions and V_{IH}(AC) to V_{IL}(AC) on the negative transitions.



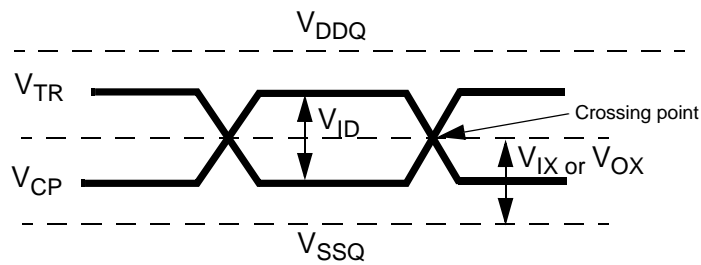
< AC Input Test Signal Waveform >

Differential input AC logic Level

| Symbol | Parameter | Min. | Max. | Units | Notes |
|---------------------|-------------------------------------|--------------------------------|--------------------------------|-------|-------|
| V _{ID(AC)} | AC differential input voltage | 0.5 | V _{DDQ} + 0.6 | V | 1 |
| V _{IX(AC)} | AC differential cross point voltage | 0.5 * V _{DDQ} - 0.175 | 0.5 * V _{DDQ} + 0.175 | V | 2 |

Notes:

1. V_{ID(AC)} specifies the input differential voltage |V_{TR} - V_{CP}| required for switching, where V_{TR} is the true input signal (such as CK, DQS, LDQS or UDQS) and V_{CP} is the complementary input signal (such as $\overline{\text{CK}}$, $\overline{\text{DQS}}$, $\overline{\text{LDQS}}$ or $\overline{\text{UDQS}}$). The minimum value is equal to V_{IH(AC)} - V_{IL(AC)}.
2. The typical value of V_{IX(AC)} is expected to be about 0.5 * V_{DDQ} of the transmitting device and V_{IX(AC)} is expected to track variations in V_{DDQ}. V_{IX(AC)} indicates the voltage at which differential input signals must cross.



< Differential signal levels >

Differential AC output parameters

| Symbol | Parameter | Min. | Max. | Units | Note |
|---------------------|-------------------------------------|--------------------------------|--------------------------------|-------|------|
| V _{OX(AC)} | AC differential cross point voltage | 0.5 * V _{DDQ} - 0.125 | 0.5 * V _{DDQ} + 0.125 | V | 1 |

Note :

1. The typical value of V_{OX(AC)} is expected to be about 0.5 * V_{DDQ} of the transmitting device and V_{OX(AC)} is expected to track variations in V_{DDQ}. V_{OX(AC)} indicates the voltage at which differential output signals must cross.

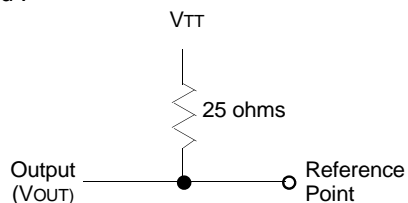
OCD default characteristics

| Description | Parameter | Min | Nom | Max | Unit | Notes |
|--|-----------|------|-----|------|------|-------------|
| Output impedance | | 12.6 | 18 | 23.4 | ohms | 1,2 |
| Output impedance step size for OCD calibration | | 0 | | 1.5 | ohms | 6 |
| Pull-up and pull-down mismatch | | 0 | | 4 | ohms | 1,2,3 |
| Output slew rate | Sout | 1.5 | | 5 | V/ns | 1,4,5,6,7,8 |

Notes:

1. Absolute Specifications ($0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +95^{\circ}\text{C}$; $V_{\text{DD}} = +1.8\text{V} \pm 0.1\text{V}$, $V_{\text{DDQ}} = +1.8\text{V} \pm 0.1\text{V}$)
2. Impedance measurement condition for output source dc current: $V_{\text{DDQ}} = 1.7\text{V}$; $V_{\text{OUT}} = 1420\text{mV}$; $(V_{\text{OUT}} - V_{\text{DDQ}})/I_{\text{oh}}$ must be less than 23.4 ohms for values of V_{OUT} between V_{DDQ} and $V_{\text{DDQ}} - 280\text{mV}$. Impedance measurement condition for output sink dc current: $V_{\text{DDQ}} = 1.7\text{V}$; $V_{\text{OUT}} = 280\text{mV}$; $V_{\text{OUT}}/I_{\text{ol}}$ must be less than 23.4 ohms for values of V_{OUT} between 0V and 280mV .
3. Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.
4. Slew rate measured from $V_{\text{IL}}(\text{AC})$ to $V_{\text{IH}}(\text{AC})$.
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near 18 ohms at nominal conditions across all process and represents only the DRAM uncertainty.

Output slew rate load :



7. DRAM output slew rate specification applies to 400Mb/sec/pin, 533Mb/sec/pin and 667Mb/sec/pin speed bins.
8. Timing skew due to DRAM output slew rate mis-match between $\text{DQS} / \overline{\text{DQS}}$ and associated DQs is included in tDQSQ and tQHS specification.

IDD Specification Parameters and Test Conditions

(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 5)

| Symbol | Proposed Conditions | Units | Notes |
|--------|--|-----------------------------|-------|
| IDD0 | Operating one bank active-precharge current; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RAS} = t_{RASmin}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA | |
| IDD1 | Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RAS} = t_{RASmin}(IDD)$, $t_{RCD} = t_{RCD}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | mA | |
| IDD2P | Precharge power-down current; All banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | mA | |
| IDD2Q | Precharge quiet standby current; All banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | mA | |
| IDD2N | Precharge standby current; All banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA | |
| IDD3P | Active power-down current; All banks open; $t_{CK} = t_{CK}(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | Fast PDN Exit MRS(12) = 0mA | mA |
| | | Slow PDN Exit MRS(12) = 1mA | mA |
| IDD3N | Active standby current; All banks open; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RASmax}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA | |
| IDD4W | Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RASmax}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA | |
| IDD4R | Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RASmax}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | mA | |
| IDD5B | Burst auto refresh current; $t_{CK} = t_{CK}(IDD)$; Refresh command at every $t_{RFC}(IDD)$ interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA | |
| IDD6 | Self refresh current; CK and CK\ at 0V; $CKE \leq 0.2V$; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING | Normal | mA |
| | | Low Power | mA |
| IDD7 | Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $t_{RCD}(IDD) - 1 \cdot t_{CK}(IDD)$; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RRD} = t_{RRD}(IDD)$, $t_{RCD} = 1 \cdot t_{CK}(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions | mA | |

Notes :

1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is specified by AC Parametric Test Condition
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS\, RDQS, RDQS\, LDQS, LDQS\, UDQS, and UDQS\. IDD values must be met with all combinations of EMRS bits 10 and 11.
5. Definitions for IDD
 - LOW is defined as $V_{in} \leq V_{ILAC(max)}$
 - HIGH is defined as $V_{in} \geq V_{IHAC(min)}$
 - STABLE is defined as inputs stable at a HIGH or LOW level
 - FLOATING is defined as inputs at $V_{REF} = V_{DDQ}/2$
 - SWITCHING is defined as:
 - inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and
 - inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

For purposes of IDD testing, the following parameters are utilized

| | DDR2-533 | DDR2-400 | |
|------------------------------|----------|----------|-------|
| Parameter | 4-4-4 | 3-3-3 | Units |
| CL(IDD) | 4 | 3 | tCK |
| t _{RC} (IDD) | 15 | 15 | ns |
| t _{RC} (IDD) | 60 | 55 | ns |
| t _{RRD} (IDD)-x4/x8 | 7.5 | 7.5 | ns |
| t _{RRD} (IDD)-x16 | 10 | 10 | ns |
| t _{CK} (IDD) | 3.75 | 5 | ns |
| t _{RASmin} (IDD) | 45 | 40 | ns |
| t _{RP} (IDD) | 15 | 15 | ns |
| t _{RFC} (IDD) | 105 | 105 | ns |

Detailed IDD7

The detailed timings are shown below for IDD7.

Legend: A = Active; RA = Read with Autoprecharge; D = Deselect

IDD7: Operating Current: All Bank Interleave Read operation

All banks are being interleaved at minimum t_{RC}(IDD) without violating t_{RRD}(IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. I_{OUT} = 0mA

Timing Patterns for 4 bank devices x4/ x8/ x16

-DDR2-400 3/3/3

A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D

-DDR2-533 4/4/4

A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D

DDR2 SDRAM IDD Spec Table

| Symbol | 128Mx4(K4T51043QB) | | Unit | Notes |
|---------|--------------------|-------------------|------|-------|
| | D5(DDR2-533@CL=4) | CC(DDR2-400@CL=3) | | |
| IDD0 | 100 | 95 | mA | |
| IDD1 | 110 | 100 | mA | |
| IDD2P | 8 | 8 | mA | |
| IDD2Q | 25 | 25 | mA | |
| IDD2N | 30 | 30 | mA | |
| IDD3P-F | 30 | 30 | mA | |
| IDD3P-S | 15 | 15 | mA | |
| IDD3N | 70 | 65 | mA | |
| IDD4W | 175 | 130 | mA | |
| IDD4R | 170 | 140 | mA | |
| IDD5B | 195 | 185 | mA | |
| IDD6 | Normal | 5.5 | 5.5 | mA |
| IDD7 | | 270 | 265 | mA |

| Symbol | 64Mx8(K4T51083QB) | | Unit | Notes |
|---------|-------------------|-------------------|------|-------|
| | D5(DDR2-533@CL=4) | CC(DDR2-400@CL=3) | | |
| IDD0 | 100 | 95 | mA | |
| IDD1 | 110 | 100 | mA | |
| IDD2P | 8 | 8 | mA | |
| IDD2Q | 25 | 25 | mA | |
| IDD2N | 30 | 30 | mA | |
| IDD3P-F | 30 | 30 | mA | |
| IDD3P-S | 15 | 15 | mA | |
| IDD3N | 70 | 65 | mA | |
| IDD4W | 200 | 145 | mA | |
| IDD4R | 180 | 145 | mA | |
| IDD5B | 195 | 185 | mA | |
| IDD6 | Normal | 5.5 | 5.5 | mA |
| IDD7 | | 275 | 270 | mA |

| Symbol | 32Mx16(K4T51163QB) | | Unit | Notes |
|---------|--------------------|-------------------|------|-------|
| | D5(DDR2-533@CL=4) | CC(DDR2-400@CL=3) | | |
| IDD0 | 120 | 115 | mA | |
| IDD1 | 145 | 125 | mA | |
| IDD2P | 8 | 8 | mA | |
| IDD2Q | 25 | 25 | mA | |
| IDD2N | 30 | 30 | mA | |
| IDD3P-F | 30 | 30 | mA | |
| IDD3P-S | 15 | 15 | mA | |
| IDD3N | 70 | 65 | mA | |
| IDD4W | 230 | 185 | mA | |
| IDD4R | 205 | 170 | mA | |
| IDD5B | 195 | 185 | mA | |
| IDD6 | Normal | 5.5 | 5.5 | mA |
| IDD7 | | 390 | 375 | mA |

Input/Output capacitance

| Parameter | Symbol | DDR2-400 DDR2-533 | | Units |
|---|--------|----------------------|------|-------|
| | | Min | Max | |
| Input capacitance, CK and \overline{CK} | CCK | 1.0 | 2.0 | pF |
| Input capacitance delta, CK and \overline{CK} | CDCK | x | 0.25 | pF |
| Input capacitance, all other input-only pins | CI | 1.0 | 2.0 | pF |
| Input capacitance delta, all other input-only pins | CDI | x | 0.25 | pF |
| Input/output capacitance, DQ, DM, DQS, \overline{DQS} | CIO | 2.5 | 4.0 | pF |
| Input/output capacitance delta, DQ, DM, DQS, \overline{DQS} | CDIO | x | 0.5 | pF |

Electrical Characteristics & AC Timing for DDR2-533/400

(0 °C ≤ T_{CASE} ≤ 95 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V)

Refresh Parameters by Device Density

| Parameter | Symbol | 256Mb | 512Mb | 1Gb | 2Gb | 4Gb | Units | |
|--|--------|-----------------------------------|-------|-------|-----|-------|-------|----|
| Refresh to active/Refresh command time | tRFC | 75 | 105 | 127.5 | 195 | 327.5 | ns | |
| Average periodic refresh interval | tREFI | 0 °C ≤ T _{CASE} ≤ 85 °C | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | μs |
| | | 85 °C < T _{CASE} ≤ 95 °C | 3.9 | 3.9 | 3.9 | 3.9 | 3.9 | μs |

Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

| Speed | DDR2-533(D5) | | DDR2-400(CC) | | Units |
|-----------------------|--------------|-------|--------------|-------|-------|
| Bin (CL - tRCD - tRP) | 4 - 4 - 4 | | 3 - 3 - 3 | | |
| Parameter | min | max | min | max | |
| tCK, CL=3 | 5 | 8 | 5 | 8 | ns |
| tCK, CL=4 | 3.75 | 8 | 5 | 8 | ns |
| tCK, CL=5 | - | - | - | - | ns |
| tRCD | 15 | | 15 | | ns |
| tRP | 15 | | 15 | | ns |
| tRC | 55 | | 55 | | ns |
| tRAS | 40 | 70000 | 40 | 70000 | ns |

Timing Parameters by Speed Grade

(Refer to notes for informations related to this table at the bottom)

| Parameter | Symbol | DDR2-533 | | DDR2-400 | | Units | Notes |
|--|-----------|---------------|---------|---------------|---------|-------|-------------|
| | | min | max | min | max | | |
| DQ output access time from CK/CK | tAC | -500 | +500 | -600 | +600 | ps | |
| DQS output access time from CK/CK | tDQSCK | -450 | +450 | -500 | +500 | ps | |
| CK high-level width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| CK low-level width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| CK half period | tHP | min(tCL, tCH) | x | min(tCL, tCH) | x | ps | 20,21 |
| Clock cycle time, CL=x | tCK | 3750 | 8000 | 5000 | 8000 | ps | 24 |
| DQ and DM input hold time | tDH(base) | 225 | x | 275 | x | ps | 15,16,17,20 |
| DQ and DM input setup time | tDS(base) | 100 | x | 150 | x | ps | 15,16,17,21 |
| Control & Address input pulse width for each input | tIPW | 0.6 | x | 0.6 | x | tCK | |
| DQ and DM input pulse width for each input | tDIPW | 0.35 | x | 0.35 | x | tCK | |
| Data-out high-impedance time from CK/CK | tHZ | x | tAC max | x | tAC max | ps | |
| DQS low-impedance time from CK/CK | tLZ(DQS) | tAC min | tAC max | tAC min | tAC max | ps | 27 |
| DQ low-impedance time from CK/CK | tLZ(DQ) | 2* tACmin | tAC max | 2* tACmin | tAC max | ps | 27 |
| DQS-DQ skew for DQS and associated DQ signals | tDQSQ | x | 300 | x | 350 | ps | 22 |
| DQ hold skew factor | tQHS | x | 400 | x | 450 | ps | 21 |
| DQ/DQS output hold time from DQS | tQH | tHP - tQHS | x | tHP - tQHS | x | ps | |
| First DQS latching transition to associated clock edge | tDQSS | -0.25 | 0.25 | -0.25 | 0.25 | tCK | |
| DQS input high pulse width | tDQSH | 0.35 | x | 0.35 | x | tCK | |
| DQS input low pulse width | tDQSL | 0.35 | x | 0.35 | x | tCK | |
| DQS falling edge to CK setup time | tDSS | 0.2 | x | 0.2 | x | tCK | |
| DQS falling edge hold time from CK | tDSH | 0.2 | x | 0.2 | x | tCK | |
| Mode register set command cycle time | tMRD | 2 | x | 2 | x | tCK | |
| Write postamble | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | 19 |

512Mb B-die DDR2 SDRAM

DDR2 SDRAM

| Parameter | Symbol | DDR2-533 | | DDR2-400 | | Units | Notes |
|---|-------------------|-----------|------------|-----------|------------|-------|-------------|
| | | min | max | min | max | | |
| Write preamble | tWPRE | 0.35 | x | 0.35 | x | tCK | |
| Address and control input hold time | tIH(base) | 375 | x | 475 | x | ps | 14,16,18,23 |
| Address and control input setup time | tIS(base) | 250 | x | 350 | x | ps | 14,16,18,22 |
| Read preamble | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | tCK | 28 |
| Read postamble | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | 28 |
| Active to active command period for 1KB page size products | tRRD | 7.5 | x | 7.5 | x | ns | 12 |
| Active to active command period for 2KB page size products | tRRD | 10 | x | 10 | x | ns | 12 |
| Four Activate Window for 1KB page size products | tFAW | 37.5 | | 37.5 | | ns | |
| Four Activate Window for 2KB page size products | tFAW | 50 | | 50 | | ns | |
| CAS to CAS command delay | tCCD | 2 | | 2 | | tCK | |
| Write recovery time | tWR | 15 | x | 15 | x | ns | |
| Auto precharge write recovery + precharge time | tDAL | WR+tRP | x | WR+tRP | x | tCK | 23 |
| Internal write to read command delay | tWTR | 7.5 | x | 10 | x | ns | 33 |
| Internal read to precharge command delay | tRTP | 7.5 | | 7.5 | | ns | 11 |
| Exit self refresh to a non-read command | tXSNR | tRFC + 10 | | tRFC + 10 | | ns | |
| Exit self refresh to a read command | tXSRD | 200 | | 200 | | tCK | |
| Exit precharge power down to any non-read command | tXP | 2 | x | 2 | x | tCK | |
| Exit active power down to read command | tXARD | 2 | x | 2 | x | tCK | 9 |
| Exit active power down to read command (slow exit, lower power) | tXARDS | 6 - AL | | 6 - AL | | tCK | 9, 10 |
| CKE minimum pulse width (high and low pulse width) | t _{CKE} | 3 | | 3 | | tCK | 36 |
| ODT turn-on delay | t _{AOND} | 2 | 2 | 2 | 2 | tCK | |
| ODT turn-on | t _{AON} | tAC(min) | tAC(max)+1 | tAC(min) | tAC(max)+1 | ns | 13, 25 |

| Parameter | Symbol | DDR2-533 | | DDR2-400 | | Units | Notes |
|---|-------------|---------------|---------------------|---------------|---------------------|-------|-------|
| | | min | max | min | max | | |
| ODT turn-on(Power-Down mode) | t_{AONPD} | $tAC(min)+2$ | $2tCK+tAC(max)+1$ | $tAC(min)+2$ | $2tCK+tAC(max)+1$ | ns | |
| ODT turn-off delay | t_{AOFD} | 2.5 | 2.5 | 2.5 | 2.5 | tCK | |
| ODT turn-off | t_{AOF} | $tAC(min)$ | $tAC(max)+0.6$ | $tAC(min)$ | $tAC(max)+0.6$ | ns | 26 |
| ODT turn-off (Power-Down mode) | t_{AOFDP} | $tAC(min)+2$ | $2.5tCK+tAC(max)+1$ | $tAC(min)+2$ | $2.5tCK+tAC(max)+1$ | ns | |
| ODT to power down entry latency | t_{ANPD} | 3 | | 3 | | tCK | |
| ODT power down exit latency | t_{AXPD} | 8 | | 8 | | tCK | |
| OCD drive mode output delay | t_{OIT} | 0 | 12 | 0 | 12 | ns | |
| Minimum time clocks remains ON after CKE asynchronously drops LOW | tDelay | $tIS+tCK+tIH$ | | $tIS+tCK+tIH$ | | ns | 24 |

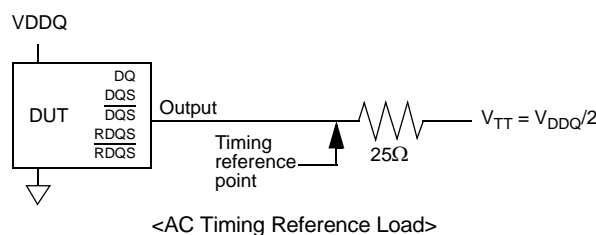
General notes, which may apply for all AC parameters

1. Slew Rate Measurement Levels

- Output slew rate for falling and rising edges is measured between $V_{TT} - 250$ mV and $V_{TT} + 250$ mV for single ended signals. For differential signals (e.g. $DQS - \overline{DQS}$) output slew rate is measured between $DQS - \overline{DQS} = -500$ mV and $DQS - \overline{DQS} = +500$ mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.
- Input slew rate for single ended signals is measured from dc-level to ac-level: from $V_{IL}(dc)$ to $V_{IH}(ac)$ for rising edges and from $V_{IH}(dc)$ and $V_{IL}(ac)$ for falling edges.
For differential signals (e.g. $CK - \overline{CK}$) slew rate for rising edges is measured from $CK - \overline{CK} = -250$ mV to $CK - \overline{CK} = +500$ mV (250mV to -500 mV for falling edges).
- V_{ID} is the magnitude of the difference between the input voltage on CK and the input voltage on \overline{CK} , or between DQS and \overline{DQS} for differential strobe.

2. DDR2 SDRAM AC timing reference load

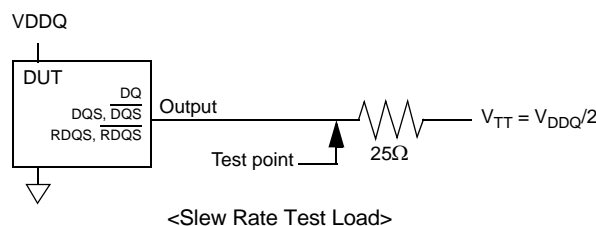
Following figure represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment or a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).



The output timing reference voltage level for single ended signals is the crosspoint with V_{TT} . The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. \overline{DQS}) signal.

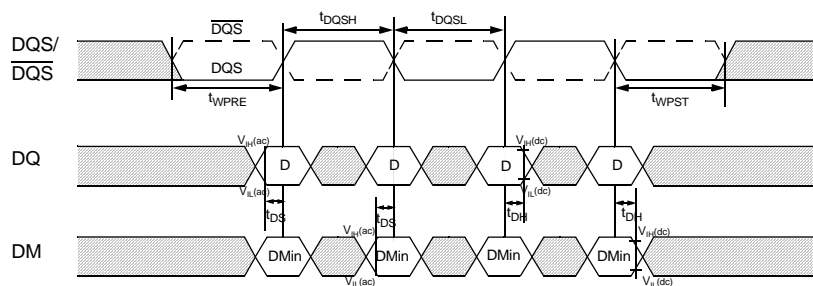
3. DDR2 SDRAM output slew rate test load

Output slew rate is characterized under the test conditions as shown in the following figure.

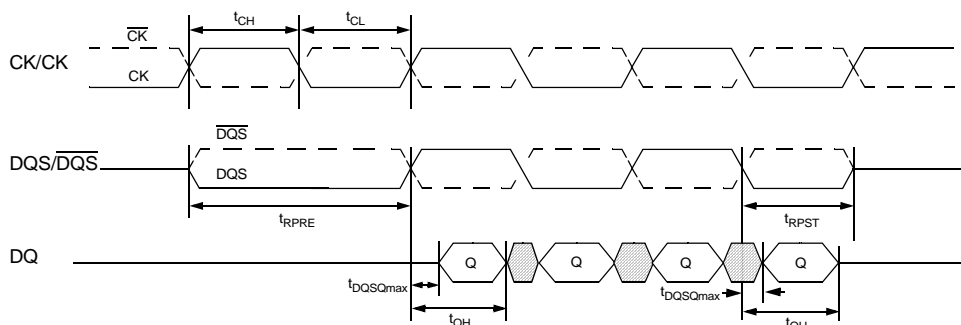


4. Differential data strobe

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, \overline{DQS} . This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, \overline{DQS} , must be tied externally to VSS through a 20 ohm to 10 K ohm resistor to insure proper operation.



<Data input (write) timing>



<Data output (read) timing>

5. AC timings are for linear signal transitions.

6. These parameters guarantee device behavior, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

7. All voltages are referenced to VSS.

8. Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

Specific Notes for dedicated AC parameters

- 9. User can choose which active power down exit timing to use via MRS(bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing.
- 10. AL = Additive Latency
- 11. This is a minimum requirement. Minimum read to precharge timing is AL + BL/2 providing the tRTP and tRAS(min) have been satisfied.
- 12. A minimum of two clocks (2 * tCK) is required irrespective of operating frequency
- 13. Timings are guaranteed with command/address input slew rate of 1.0 V/ns.
- 14. These parameters guarantee device behavior, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
- 15. Timings are guaranteed with data, mask, and (DQS/RDQS in singled ended mode) input slew rate of 1.0 V/ns.
- 16. Timings are guaranteed with CK/ \overline{CK} differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode.
- 17. tDS and tDH derating for DDR2-400 and DDR2-533

| | | ΔtDS, ΔtDH Derating Values (ALL units in 'ps', Note 1 applies to entire Table) | | | | | | | | | | | | | | | | | |
|-------------------|-----|--|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| | | DQS, \overline{DQS} Differential Slew Rate | | | | | | | | | | | | | | | | | |
| | | 4.0 V/ns | | 3.0 V/ns | | 2.0 V/ns | | 1.8 V/ns | | 1.6 V/ns | | 1.4V/ns | | 1.2V/ns | | 1.0V/ns | | 0.8V/ns | |
| | | ΔtD S | ΔtD H | ΔtD S | ΔtD H | ΔtD S | ΔtD H | ΔtD S | ΔtD H | ΔtD S | ΔtD H | ΔtD S | ΔtD H | ΔtD S | ΔtD H | ΔtD S | ΔtD H | ΔtD S | ΔtD H |
| DQ Slew rate V/ns | 2.0 | 125 | 45 | 125 | 45 | 125 | 45 | - | - | - | - | - | - | - | - | - | - | - | - |
| | 1.5 | 83 | 21 | 83 | 21 | 83 | 21 | 95 | 33 | - | - | - | - | - | - | - | - | - | - |
| | 1.0 | 0 | 0 | 0 | 0 | 0 | 0 | 12 | 12 | 24 | 24 | - | - | - | - | - | - | - | - |
| | 0.9 | - | - | -11 | -14 | -11 | -14 | 1 | -2 | 13 | 10 | 25 | 22 | - | - | - | - | - | - |
| | 0.8 | - | - | - | - | -25 | -31 | -13 | -19 | -1 | -7 | 11 | 5 | 23 | 17 | - | - | - | - |
| | 0.7 | - | - | - | - | - | - | -31 | -42 | -19 | -30 | -7 | -18 | 5 | -6 | 17 | 6 | - | - |
| | 0.6 | - | - | - | - | - | - | - | - | -43 | -59 | -31 | -47 | -19 | -35 | -7 | -23 | 5 | -11 |
| | 0.5 | - | - | - | - | - | - | - | - | - | - | -74 | -89 | -62 | -77 | -50 | -65 | -38 | -53 |
| | 0.4 | - | - | - | - | - | - | - | - | - | - | - | - | -127 | -140 | -115 | -128 | -103 | -116 |

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the datasheet tDS(base) and tDH(base) value to the delta tDS and delta tDH derating value respectively. Example: tDS (total setup time) = tDS(base) + delta tDS.

18. tIS and tIH (input setup and hold) derating.

| | | tIS, tIH Derating Values for DDR2-400, DDR2-533 | | | | | | Units | Notes |
|----------------------------------|------|---|-----------------|-----------------|-----------------|-----------------|-----------------|-------|-------|
| | | CK,CK Differential Slew Rate | | | | | | | |
| | | 2.0 V/ns | | 1.5 V/ns | | 1.0 V/ns | | | |
| Command/Address Slew rate (V/ns) | | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | | |
| 4.0 | +187 | +94 | +217 | +124 | +247 | +154 | ps | 1 | |
| 3.5 | +179 | +89 | +209 | +119 | +239 | +149 | ps | 1 | |
| 3.0 | +167 | +83 | +197 | +113 | +227 | +143 | ps | 1 | |
| 2.5 | +150 | +75 | +180 | +105 | +210 | +135 | ps | 1 | |
| 2.0 | +125 | +45 | +155 | +75 | +185 | +105 | ps | 1 | |
| 1.5 | +83 | +21 | +113 | +51 | +143 | +81 | ps | 1 | |
| 1.0 | 0 | 0 | +30 | +30 | +60 | 60 | ps | 1 | |
| 0.9 | -11 | -14 | +19 | +16 | +49 | +46 | ps | 1 | |
| 0.8 | -25 | -31 | +5 | -1 | +35 | +29 | ps | 1 | |
| 0.7 | -43 | -54 | -13 | -24 | +17 | +6 | ps | 1 | |
| 0.6 | -67 | -83 | -37 | -53 | -7 | -23 | ps | 1 | |
| 0.5 | -110 | -125 | -80 | -95 | -50 | -65 | ps | 1 | |
| 0.4 | -175 | -188 | -145 | -158 | -115 | -128 | ps | 1 | |
| 0.3 | -285 | -292 | -255 | -262 | -225 | -232 | ps | 1 | |
| 0.25 | -350 | -375 | -320 | -345 | -290 | -315 | ps | 1 | |
| 0.2 | -525 | -500 | -495 | -470 | -465 | -440 | ps | 1 | |
| 0.15 | -800 | -708 | -770 | -678 | -740 | -648 | ps | 1 | |

| | | Δt_{IS} and Δt_{IH} Derating Values for DDR2-667, DDR2-800 | | | | | | Units | Notes |
|----------------------------------|-------|--|-----------------|-----------------|-----------------|-----------------|-----------------|-------|-------|
| | | CK,CK Differential Slew Rate | | | | | | | |
| | | 2.0 V/ns | | 1.5 V/ns | | 1.0 V/ns | | | |
| Command/Address Slew rate (V/ns) | | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | | |
| 4.0 | +150 | +94 | +180 | +124 | +210 | +154 | ps | 1 | |
| 3.5 | +143 | +89 | +173 | +119 | +203 | +149 | ps | 1 | |
| 3.0 | +133 | +83 | +163 | +113 | +193 | +143 | ps | 1 | |
| 2.5 | +120 | +75 | +150 | +105 | +180 | +135 | ps | 1 | |
| 2.0 | +100 | +45 | +130 | +75 | +160 | +105 | ps | 1 | |
| 1.5 | +67 | +21 | +97 | +51 | +127 | +81 | ps | 1 | |
| 1.0 | 0 | 0 | +30 | +30 | +60 | +60 | ps | 1 | |
| 0.9 | -5 | -14 | +25 | +16 | +55 | +46 | ps | 1 | |
| 0.8 | -13 | -31 | +17 | -1 | +47 | +29 | ps | 1 | |
| 0.7 | -22 | -54 | +8 | -24 | +38 | +6 | ps | 1 | |
| 0.6 | -34 | -83 | -4 | -53 | +26 | -23 | ps | 1 | |
| 0.5 | -60 | -125 | -30 | -95 | 0 | -65 | ps | 1 | |
| 0.4 | -100 | -188 | -70 | -158 | -40 | -128 | ps | 1 | |
| 0.3 | -168 | -292 | -138 | -262 | -108 | -232 | ps | 1 | |
| 0.25 | -200 | -375 | -170 | -345 | -140 | -315 | ps | 1 | |
| 0.2 | -325 | -500 | -295 | -470 | -265 | -440 | ps | 1 | |
| 0.15 | -517 | -708 | -487 | -678 | -457 | -648 | ps | 1 | |
| 0.1 | -1000 | -1125 | -970 | -1095 | -940 | -1065 | ps | 1 | |

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the datasheet tIS(base) and tIH(base) value to the delta tIS and delta tIH derating value respectively. Example: tIS (total setup time) = tIS(base) + delta tIS

19. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

20. MIN (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH). For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.

21. tQH = tHP – tQHS, where:

tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for:

- 1) The pulse duration distortion of on-chip clock circuits; and
- 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

22. tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / DQS and associated DQ in any given cycle.

23. DAL = WR + RU{tRP(ns)/tCK(ns)}, where RU stands for round up.

WR refers to the tWR parameter stored in the MRS. For tRP, if the result of the division is not already an integer, round up to the next highest integer. tCK refers to the application clock period.

Example: For DDR533 at tCK = 3.75ns with tWR programmed to 4 clocks.

tDAL = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.

24. The clock frequency is allowed to change during self-refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required as described in DDR2 device operation

25. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.

26. ODT turn off time min is when the device starts to turn off ODT resistance.

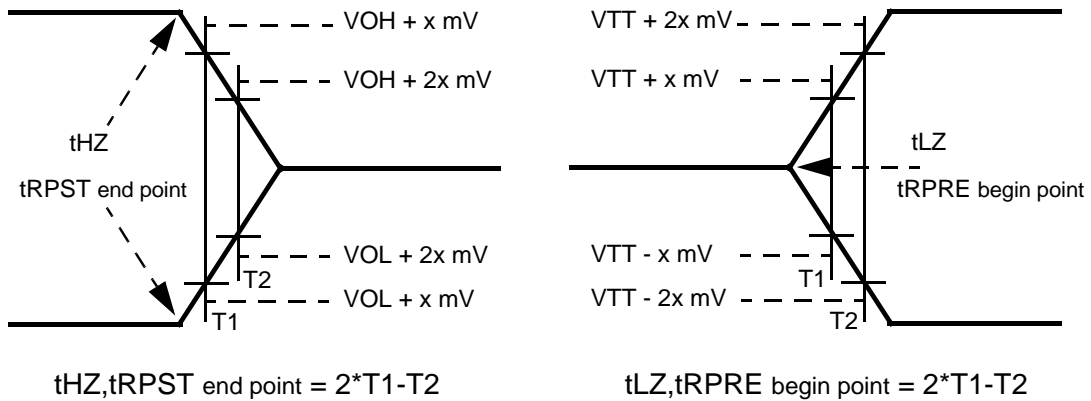
ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

27. tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begins driving (tLZ). Following figure shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

28. tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). Following figure shows a method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the cal-

ulation is consistent.

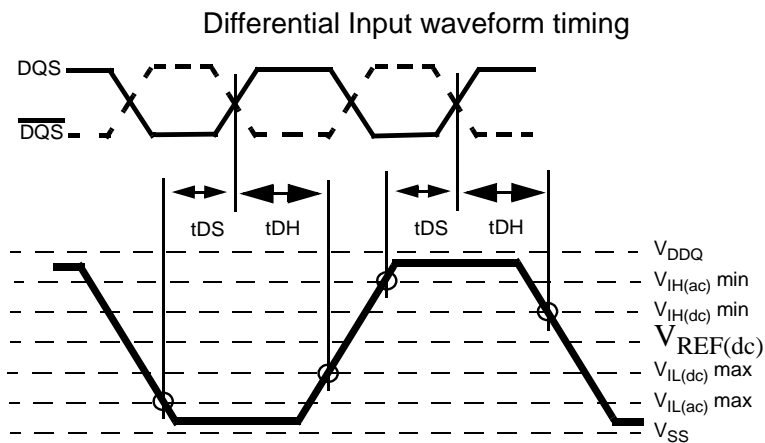
These notes are referenced in the "Timing parameters by speed grade" tables for DDR2-400/533/667 and DDR2-800.



<Test method for tLZ, tHZ, tRPRE and tRPST>

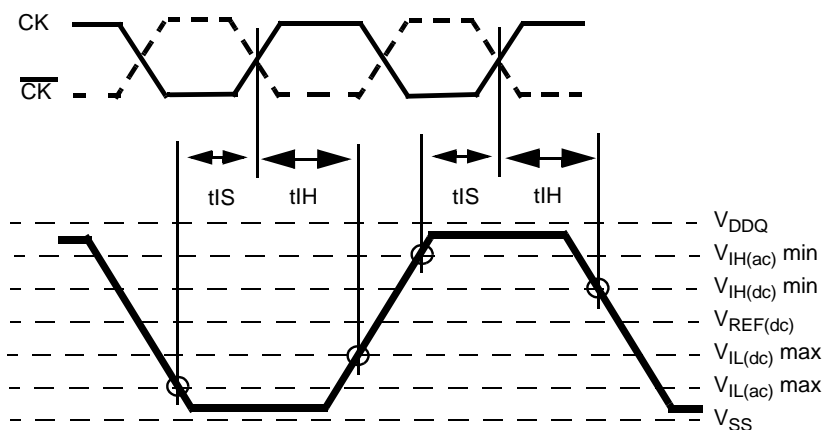
29. Input waveform timing with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the $V_{IH(ac)}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL(ac)}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test.

30. Input waveform timing with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the $V_{IH(dc)}$ level to the differential data strobe crosspoint for a rising signal and $V_{IL(dc)}$ to the differential data strobe crosspoint for a falling signal applied to the device under test.



31. Input waveform timing is referenced from the input signal crossing at the $V_{IH(ac)}$ level for a rising signal and $V_{IL(ac)}$ for a falling signal applied to the device under test.

32. Input waveform timing is referenced from the input signal crossing at the $V_{IH(dc)}$ level for a rising signal and $V_{IL(dc)}$ for a falling signal applied to the device under test.



33. $tWTR$ is at least two clocks ($2 * tCK$) independent of operation frequency.

34. Input waveform timing with single-ended data strobe enabled $MR[bit10] = 1$, is referenced from the input signal crossing at the $V_{IH(ac)}$ level to the single-ended data strobe crossing $V_{IH/L(dc)}$ at the start of its transition for a rising signal, and from the input signal crossing at the $V_{IL(ac)}$ level to the single-ended data strobe crossing $V_{IH/L(dc)}$ at the start of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between $V_{il(dc)max}$ and $V_{ih(dc)min}$.

35. Input waveform timing with single-ended data strobe enabled $MR[bit10] = 1$, is referenced from the input signal crossing at the $V_{IH(dc)}$ level to the single-ended data strobe crossing $V_{IH/L(ac)}$ at the end of its transition for a rising signal, and from the input signal crossing at the $V_{IL(dc)}$ level to the single-ended data strobe crossing $V_{IH/L(ac)}$ at the end of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between $V_{il(dc)max}$ and $V_{ih(dc)min}$.

36. $tCKEmin$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any cKE transition, CKE may not transition from its valid level during the time period of $tIS + 2*tCK + tIH$.

Revision History

Version 1.0 (Jan. 2004)

- Initial Release

Version 1.1 (Jun. 2004)

- Added Lead-Free part number in ordering information.
- Changed IDD2P
- Corrected Typo

Version 1.2 (Jan. 2005)

- Removed DDR2-667 SDRAM at this datasheet
- Revised current test AC spec condition
- Added derating table

Version 1.3 (Jan. 2005)

- Corrected typo

Version 1.4 (Feb. 2005)

- Corrected from 6.15mm to 5.5mm in dimension of x16 PKG