MCP Specification

512Mb (32M x16) Muxed Burst, Multi Bank SLC NOR Flash + 128Mb (8M x16) Multiplexed Synchronous Burst UtRAM2

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	Initial issue. - 512M Bit SLC Mux NOR Flash C-die_Ver 1.0 - 128M Bit Mux UtRAM2 C-die_Ver 1.0	Jun. 1, 2010	Preliminary	H.Y.Min
1.0	<Common> - Finalized.	Jun. 22, 2010	Final	H.Y.Min

1. Features

<Common>
• Operating Temperature : -25°C ~ 85°C
• Package : 56Ball FBGA Type - 8mm x 9.2mm x 1.2mmt
0.5mm ball pitch

<NOR Flash>
• ***This device has the Sync MRS option only (Extended Configuration Register)***
• Single Voltage, 1.7V to 1.95V for Read and Write operations
• Organization
- 33,554,432 x 16 bit (Word Mode Only)
• Multiplexed Data and Address for reduction of interconnections
- A/DQ0 ~ A/DQ15
• Read While Program/Erase Operation
• Multiple Bank Architecture
- 16 Banks (32Mb Partition)
• OTP Block : Extra 512-Word block
• Read Access Time (@ C_L=30pF)
- Asynchronous Random Access Time : 100ns
- Synchronous Random Access Time :95ns
- Burst Access Time :7ns (108MHz)
• Burst Length :
- Continuous Linear Burst
- Linear Burst : 8-word & 16-word with Wrap
• Block Architecture
- Uniform block part : Five hundred twelve 64Kword blocks
- Boot block part : Four 16Kword blocks and five hundred eleven 64Kword blocks (Bank 0 contains four 16 Kword blocks and thirty-one 64Kword blocks, Bank 1 ~ Bank 15 contain four hundred eighty 64Kword blocks)
• Reduce program time using the V_{PP}
• Support 512-word Buffer Program
• Power Consumption (Typical value, C_L=30pF)
- Synchronous Read Current : 35mA at 133MHz
- Program/Erase Current : 25mA
- Read While Program/Erase Current : 45mA
- Standby Mode/Auto Sleep Mode : 30uA
• Block Protection/Unprotection
- Using the software command sequence
- Last two boot blocks are protected by $\overline{WP}$=V_{IL} (Boot block part)
- Last one block (BA511) is protected by $\overline{WP}$=V_{IL} (Uniform block part)
- All blocks are protected by V_{PP}=V_{IL}
• Handshaking Feature
- Provides host system with minimum latency by monitoring RDY
• Erase Suspend/Resume
• Program Suspend/Resume
• Unlock Bypass Program/Erase
• Blank Check Feature
• Hardware Reset ($\overline{RESET}$)
• Data Polling and Toggle Bits
- Provides a software method of detecting the status of program or erase completion
• Endurance
- 100K Program/Erase cycles
• Support Common Flash Memory Interface
• Low Vcc Write Inhibit
• Output Driver Control by Configuration Register

<UtRAM2>
• Process technology: CMOS
• Organization: 8M x 16 bit
• Power supply voltage: 1.7V~1.95V
• Three state outputs
• Supports Configuration Register Set
- CRE pin set up
- Software set up
• Supports power saving modes
- PAR (Partial Array Refresh)
- Internal TCSR (Temperature Compensated Self Refresh)
• Supports driver strength optimization
• Support 2 operation modes
- Asynchronous mode
- Synchronous mode
• Random access time:70ns
• Synchronous burst operation
- Max. clock frequency : 108MHz
- Fixed and Variable read latency
- 4 / 8 / 16 / 32 and Continuous burst
- Wrap / No-wrap
- Latency :3(Variable) @ 108MHz
- Burst stop
- Burst read suspend
- Burst write data masking

2. General Description

The K5N1229ACD is a Multi Chip Package Memory which combines 512Mb SLC MuxNOR Flash Memory and 128Mb Multiplexed Synchronous Burst Uni-Transistor Random Access Memory2.

The 512Mb Muxed NOR Flash featuring single 1.8V power supply is a 512Mbit Muxed Burst Multi Bank Flash Memory organized as 32Mx16. The memory architecture of the device is designed to divide its memory arrays into 512blocks(Uniform block part)/515 blocks(Boot block part) with independent hardware protection. This block architecture provides highly flexible erase and program capability. The NOR Flash consists of sixteen banks. This device is capable of reading data from one bank while programming or erasing in the other bank. Regarding read access time, the device(for 66/83MHz) provides an 11ns burst access time and an 95ns initial access time at 66MHz. At 83MHz, the device(for 66/83MHz) provides an 9ns burst access time and an 95ns initial access time. At 108MHz, the device(for 108/133MHz) provides an 7ns burst access time and an 95ns initial access time. At 133MHz, the device(for 108/133MHz) provides an 6ns burst access time and an 95ns initial access time. The device performs a program operation in units of 16 bits (Word) and erases in units of a block. Single or multiple blocks can be erased. The block erase operation is completed within typically 0.6sec. The device requires 25mA as program/erase current in the extended temperature ranges.

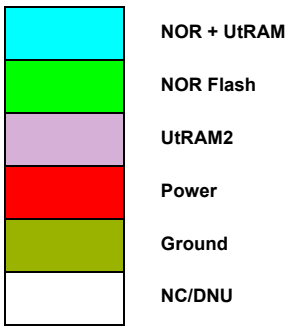
SAMSUNG's UtRAM products are designed to meet the request from the customers who want to cope with the fast growing mobile applications that need high-speed random access memory. UtRAM is the solution for the mobile market with its low cost, high density and high performance feature. device is fabricated by SAMSUNG′s advanced CMOS technology using one transistor memory cell. The device supports the traditional SRAM like asynchronous operation (asynchronous read and asynchronous write), the fully synchronous operation (synchronous burst read and synchronous burst write). These operation modes are defined through the configuration register setting. It supports the special features for the standby power saving. Those are the PAR(Partial Array Refresh) mode, and internal TCSR(Temperature Compensated Self Refresh). It also supports variable and fixed latency, driver strength settings, Burst sequence (wrap or No-wrap) options and a device ID register (DIDR).

The K5N1229ACD is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 56-ball FBGA Type.

3. Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC													NC
B														
C			NC	DNU			/LBc	/UBc			A24r	NC		
D			RDYr /WAITc	A21rc	VSSrc	CLKrc	VCCrc	/WErc	VPPr	A19rc	A17rc	A22rc		
E			VCCQrc	A16rc	A20rc	/AVDrc	A23r	/RESETr	/WPr	A18rc	/CEr	VSSQrc		
F			VSSrc	ADQ7rc	ADQ6rc	ADQ13rc	ADQ12rc	ADQ3rc	ADQ2rc	ADQ9rc	ADQ8rc	/OErc		
G			ADQ15rc	ADQ14rc	VSSQrc	ADQ5rc	ADQ4rc	ADQ11rc	ADQ10rc	VCCQrc	ADQ1rc	ADQ0rc		
H			NC	VCCrc			/CSc	CREc			DNU	NC		
J														
K	NC													NC

56 FBGA: Top View (Ball Down)



4. Pin Description

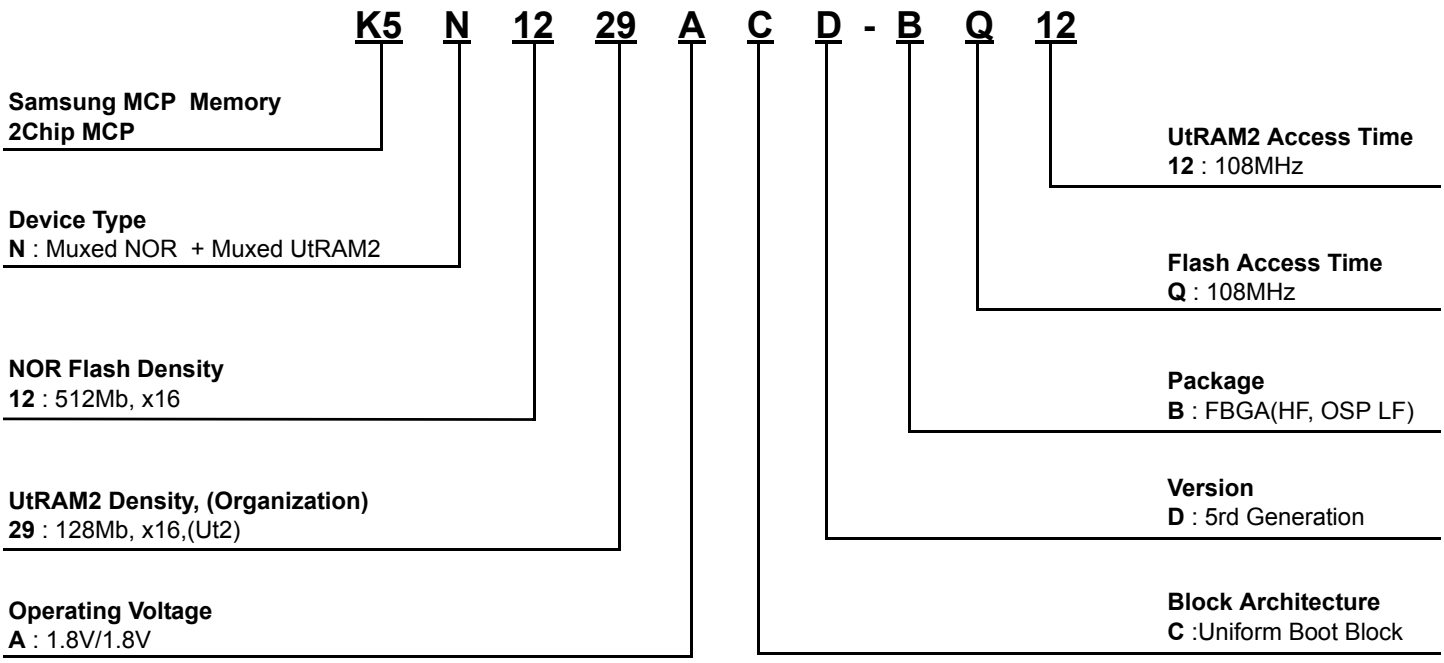
Pin Name	Pin Function(NOR Flash)
A23r, A24r	Address Input(NOR only)
/CEr	Chip Enable
/WPr	Write Enable
/RESETr	Hardware Reset
VPPr	Accelerates Programming

Pin Name	Pin Function(UtRAM2)
/LBc,/UBc	Lower Byte Enable, Upper Byte Enable
CREc	Control Register Enable
/CSc	Chip Enable

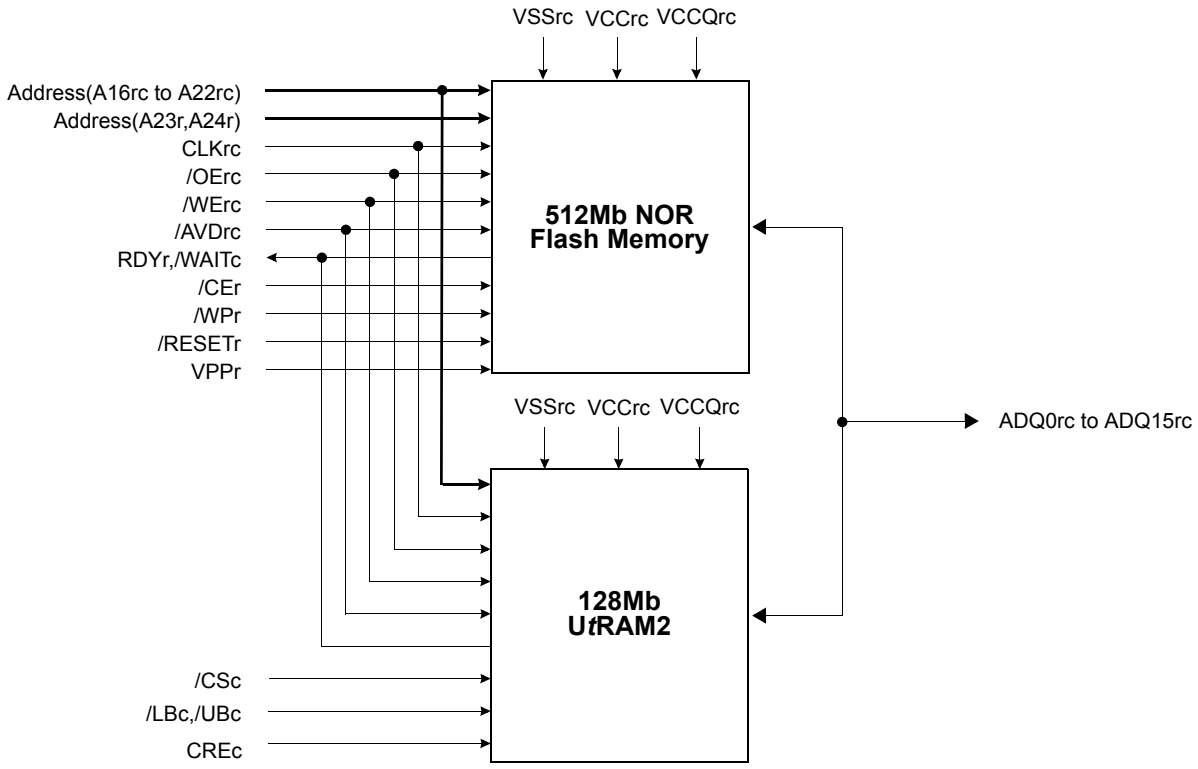
Pin Name	Pin Function(Common)
ADQ0rc ~ ADQ15rc	Multiplexed Address/Data Input/Output
A16rc ~ A22rc	Address Input
CLKrc	Clock
/OErc	Output Enable
/WErc	Write Enable
/AVDrc	Address Valid Input
RDYr /WAITc	Ready Out(NOR) Data Availability (UtRAM)
VCCrc	Power Supply
VCCQrc	Data Input/Output Power
VSSrc	Ground

Pin Name	Pin Function
DNU	Do Not Use
NC	No Connection

5. Ordering Information

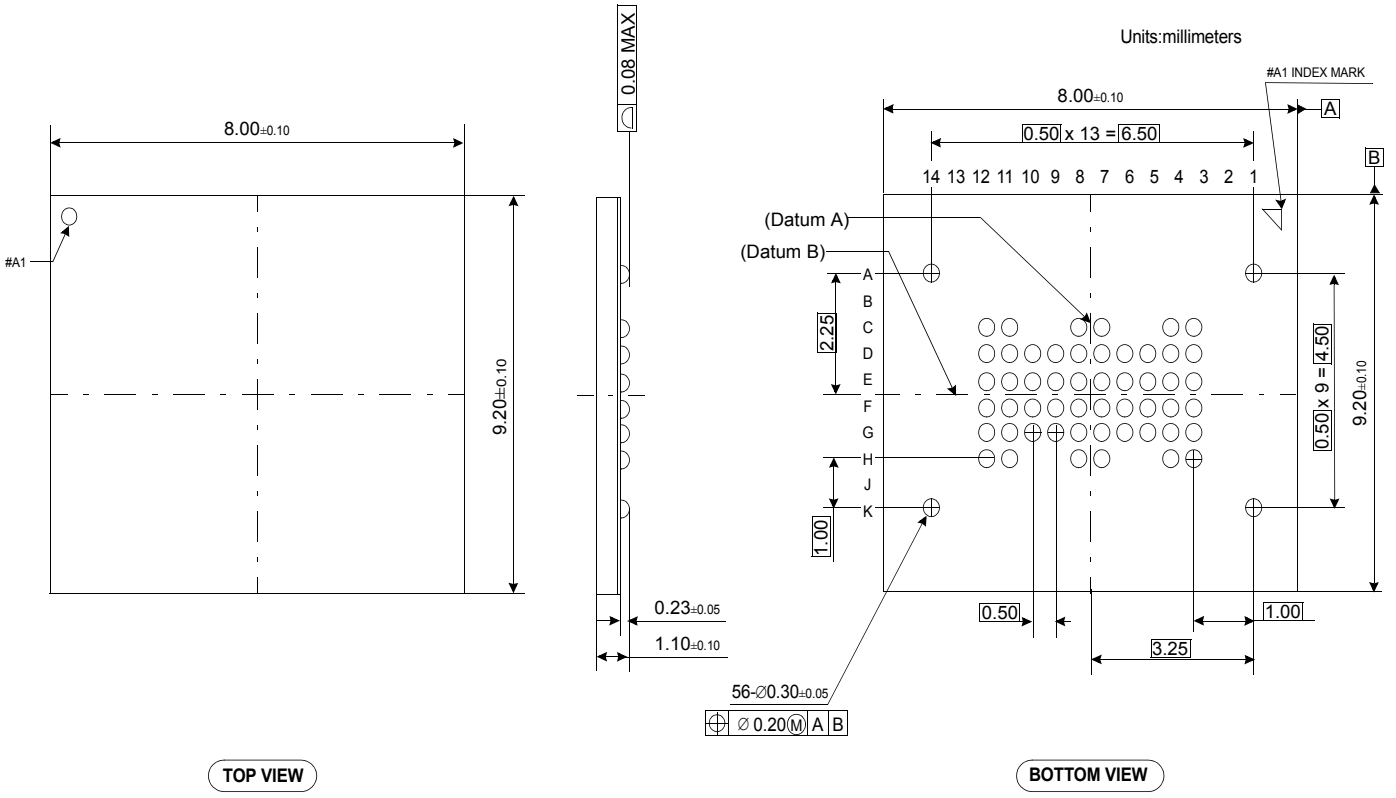


6. Functional Block Diagram



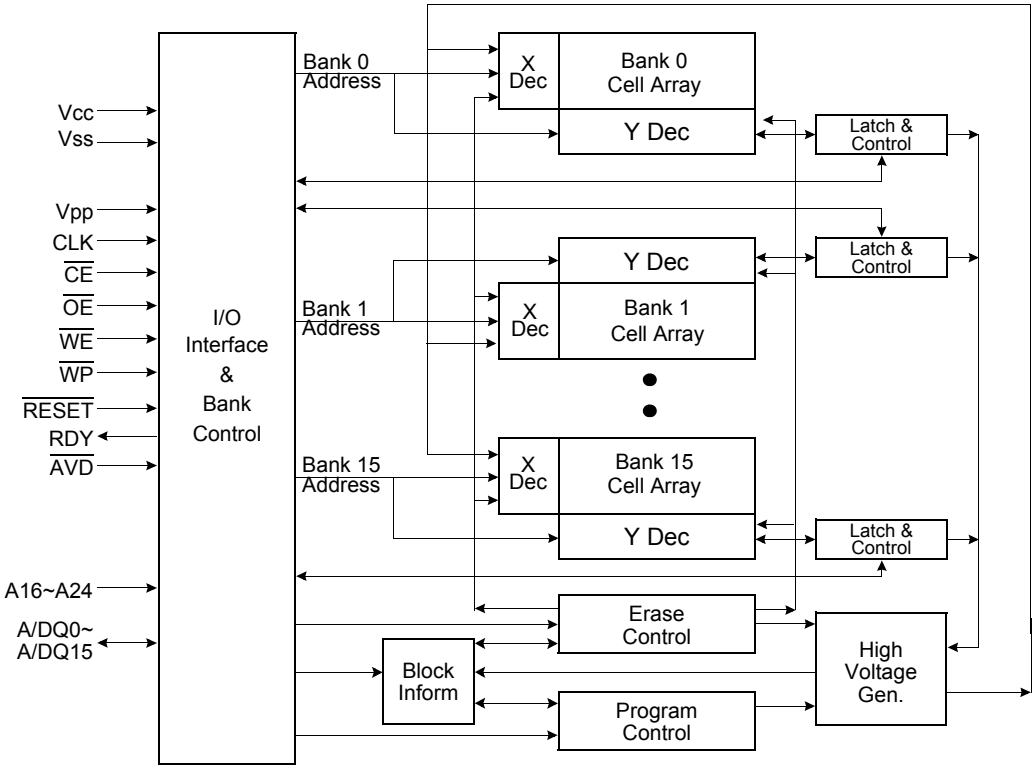
7. Package Dimension

56-Ball Fine pitch Ball Grid Array Package (measured in millimeters)



512Mb (32M x16) Mux NOR Flash C-die

1.0 FUNCTIONAL BLOCK DIAGRAM



[Table 1] PRODUCT LINE-UP

	Mode	Speed Option	1C (66MHz)	1D (83MHz)	1E (108MHz)	1F (133MHz)
V_{CC}=1.7V -1.95V	Synchronous/Burst	Max. Initial Access Time (t_{IAA}, ns)	95	95	95	95
		Max. Burst Access Time (t_{BA}, ns)	11	9	7	6
	Asynchronous	Max. Access Time (t_{AA}, ns)	100	100	100	100
		Max. $\overline{CE}$ Access Time (t_{CE}, ns)	100	100	100	100
		Max. $\overline{OE}$ Access Time (t_{OE}, ns)	15	15	15	15

[Table 2] DEVICE BANK DIVISIONS

Bank 0 ~ Bank 15	
Type	**Block Sizes**
512Mbit (Boot block part)	Four 16Kword blocks and five hundred eleven 64Kword blocks
512Mbit (Uniform block part)	Five hundred twelve 64Kword blocks

[Table 3] DEVICE BANK DIVISIONS (Uniform block)

Bank	Bank size	Quantity of Blocks	Block Size
0	32Mb	32	64 Kwords
1	32Mb	32	64 Kwords
2	32Mb	32	64 Kwords
3	32Mb	32	64 Kwords
4	32Mb	32	64 Kwords
5	32Mb	32	64 Kwords
6	32Mb	32	64 Kwords
7	32Mb	32	64 Kwords
8	32Mb	32	64 Kwords
9	32Mb	32	64 Kwords
10	32Mb	32	64 Kwords
11	32Mb	32	64 Kwords
12	32Mb	32	64 Kwords
13	32Mb	32	64 Kwords
14	32Mb	32	64 Kwords
15	32Mb	32	64 Kwords

[Table 4] DEVICE BANK DIVISIONS (Top Boot block)

Bank	Bank size	Quantity of Blocks	Block Size
0	32Mb	4	16 Kwords
		31	64 Kwords
1	32Mb	32	64 Kwords
2	32Mb	32	64 Kwords
3	32Mb	32	64 Kwords
4	32Mb	32	64 Kwords
5	32Mb	32	64 Kwords
6	32Mb	32	64 Kwords
7	32Mb	32	64 Kwords
8	32Mb	32	64 Kwords
9	32Mb	32	64 Kwords
10	32Mb	32	64 Kwords
11	32Mb	32	64 Kwords
12	32Mb	32	64 Kwords
13	32Mb	32	64 Kwords
14	32Mb	32	64 Kwords
15	32Mb	32	64 Kwords

[Table 5] DEVICE BANK DIVISIONS (Bottom Boot block)

Bank	Bank size	Quantity of Blocks	Block Size
15	32Mb	32	64 Kwords
14	32Mb	32	64 Kwords
13	32Mb	32	64 Kwords
12	32Mb	32	64 Kwords
11	32Mb	32	64 Kwords
10	32Mb	32	64 Kwords
9	32Mb	32	64 Kwords
8	32Mb	32	64 Kwords
7	32Mb	32	64 Kwords
6	32Mb	32	64 Kwords
5	32Mb	32	64 Kwords
4	32Mb	32	64 Kwords
3	32Mb	32	64 Kwords
2	32Mb	32	64 Kwords
1	32Mb	32	64 Kwords
0	32Mb	31	64 Kwords
		4	16 Kwords

2.0 PRODUCT INTRODUCTION

The device is an 512Mbit (536,870,912 bits) NOR-type Burst Flash memory. The device features 1.8V single voltage power supply operating within the range of 1.7V to 1.95V. The device is programmed by using the Channel Hot Electron (CHE) injection mechanism which is used to program EPROMs. The device is erased electrically by using Fowler-Nordheim tunneling mechanism. To provide highly flexible erase and program capability, the device adapts a block memory architecture that divides its memory array into 512 blocks (64-Kword x 512 blocks, Uniform block part) / 515 blocks (16-Kword x 4 + 64-Kword x 511, Boot block part). Programming is done in units of 16 bits (Word). All bits of data in one or multiple blocks can be erased when the device executes the erase operation. To prevent the device from accidental erasing or over-writing the programmed data, 512 / 515 memory blocks can be hardware protected. Regarding read access time, at 66MHz, the device(for 66/83MHz) provides a burst access of 11ns with initial access times of 95ns at 30pF. At 83MHz, the device(for 66/83MHz) provides a burst access of 9ns with initial access times of 95ns at 30pF. At 108MHz, the device(for 108/133MHz) provides a burst access of 7ns with initial access times of 95ns at 30pF. At 133MHz, the device(for 108/133MHz) provides a burst access of 6ns with initial access times of 95ns at 30pF. The command set of device is compatible with standard Flash devices. The device uses Chip Enable ($\overline{CE}$), Write Enable ($\overline{WE}$), Address Valid($\overline{AVD}$) and Output Enable ($\overline{OE}$) to control asynchronous read and write operation. For burst operations, the device additionally requires Ready (RDY) and Clock (CLK). Device operations are executed by selective command codes. The command codes to be combined with addresses and data are sequentially written to the command registers using microprocessor write timing. The command codes serve as inputs to an internal state machine which controls the program/erase circuitry. Register contents also internally latch addresses and data necessary to execute the program and erase operations. The device is implemented with Internal Program/Erase Routines to execute the program/erase operations. The Internal Program/Erase Routines are invoked by program/erase command sequences. The Internal Program Routine automatically programs and verifies data at specified addresses. The Internal Erase Routine automatically pre-programs the memory cell which is not programmed and then executes the erase operation. The device has means to indicate the status of completion of program/erase operations. The status can be indicated via Data polling of DQ7, or the Toggle bit (DQ6). Once the operations have been completed, the device automatically resets itself to the read mode. The device requires only 35mA as burst and asynchronous mode read current and 25mA for Buffer program/erase operations.

[Table 6] Device Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A16-24	A/DQ0-15	$\overline{RESET}$	CLK	$\overline{AVD}$
Asynchronous Read Operation	L	L	H	Add In	Add In/DOUT	H	L	⎍
Write	L	H	L	Add In	Add In / DIN	H	L	⎍
Standby	H	X	X	X	High-Z	H	X	X
Hardware Reset	X	X	X	X	High-Z	L	X	X
Load Initial Burst Address	L	H	H	Add In	Add In	H	⎍	⎍
Burst Read Operation	L	L	H	X	Burst DOUT	H	⎍	H
Terminate Burst Read Cycle	H	X	X	X	High-Z	H	X	X
Terminate Burst Read Cycle via $\overline{RESET}$	X	X	X	X	High-Z	L	X	X
Terminate Current Burst Read Cycle and Start New Burst Read Cycle	L	H	H	Add In	Add In	H	⎍	⎍

NOTE : L=VIL (Low), H=VIH (High), X=Don't Care.

3.0 COMMAND DEFINITIONS

The device operates by selecting and executing its operational modes. Each operational mode has its own command set. In order to select a certain mode, a proper command with specific address and data sequences must be written into the command register. Writing incorrect information which include address and data or writing an improper command will reset the device to the read mode. The defined valid register command sequences are stated in Table 8.

[Table 7] Command Sequences

Command Definitions		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Asynchronous Read	Add	1	RA					
	Data		RD					
Reset[5),20)]	Add	1	XXXH					
	Data		F0H					
Autoselect Manufacturer ID[6)]	Add	4	555H	2AAH	(DA)555H	(DA)X00H		
	Data		AAH	55H	90H	ECH		
Autoselect Device ID[6)]	Add	4	555H	2AAH	(DA)555H	(DA)X01H		
	Data		AAH	55H	90H	NOTE6		
Autoselect Block Protection Verify[7)]	Add	4	555H	2AAH	(BA)555H	(BA)X02H		
	Data		AAH	55H	90H	00H/01H		
Autoselect Handshaking [6), 8)]	Add	4	555H	2AAH	(DA)555H	(DA)X03H		
	Data		AAH	55H	90H	0H/1H		
Program	Add	4	555H	2AAH	555H	PA		
	Data		AAH	55H	A0H	PD		
Unlock Bypass	Add	3	555H	2AAH	555H			
	Data		AAH	55H	20H			
Unlock Bypass Program [9)]	Add	2	XXX	PA				
	Data		A0H	PD				
Unlock Bypass Block Erase[9)]	Add	2	XXX	BA				
	Data		80H	30H				
Unlock Bypass Chip Erase[9)]	Add	2	XXXH	XXXH				
	Data		80H	10H				
Unlock Bypass Reset	Add	2	XXXH	XXXH				
	Data		90H	00H				
Chip Erase	Add	6	555H	2AAH	555H	555H	2AAH	555H
	Data		AAH	55H	80H	AAH	55H	10H
Block Erase	Add	6	555H	2AAH	555H	555H	2AAH	BA
	Data		AAH	55H	80H	AAH	55H	30H
Erase Suspend [10)]	Add	1	(DA)XXXH					
	Data		B0H					
Erase Resume[11)]	Add	1	(DA)XXXH					
	Data		30H					
Program Suspend [12)]	Add	1	(DA)XXXH					
	Data		B0H					
Program Resume [11)]	Add	1	(DA)XXXH					
	Data		30H					
Block Protection/Unprotection [13)]	Add	3	XXX	XXX	ABP			
	Data		60H	60H	60H			
CFI Query [14)]	Add	1	(DA)X55H					
	Data		98H					
Blank check	Add	4	555H	2AAH	BA	BA		
	Data		AAH	55H	BCH	D0H		

Command Definitions		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Write to Buffer 15)	Add	3	555H	2AAH	BA	BA	PA	WBL
	Data		AAH	55H	25H	WC	PD	PD
Program buffer to Flash 15)	Add	1	BA					
	Data		29H					
Write to Buffer Abort Reset 16),20)	Add	3	555H	2AAH	XXX			
	Data		AAH	55H	F0H			
Set Burst Mode Configuration Register 17),18)	Add	3	555H	2AAH	NOTE 18			
	Data		AAH	55H	C0H			
Set Extended Configuration Register 17),19)	Add	3	555H	2AAH	NOTE 19			
	Data		AAH	55H	C5H			
Enter OTP Block Region	Add	3	555H	2AAH	XXX			
	Data		AAH	55H	70H			
Exit OTP Block Region	Add	4	555H	2AAH	555H	XXX		
	Data		AAH	55H	75H	00H		

NOTE :

1) RA : Read Address , PA : Program Address, RD : Read Data, PD : Program Data , BA : Block Address (A24 ~ A14), DA : Bank Address (A24 ~ A21)
ABP : Address of the block to be protected or unprotected , DI :Die revision ID, CR : Configuration Register Setting,
WBL : Write Buffer Location, WC : Word Count
2) The 4th cycle data of autoselect mode and RD are output data. The others are input data.
3) Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD, WC and Device ID.
4) Unless otherwise noted, address bits A24–A11 are don't cares.
5) The reset command is required to return to read mode.
If a bank entered the autoselect mode during the erase suspend mode, writing the reset command returns that bank to the erase suspend mode.
If a bank entered the autoselect mode during the program suspend mode, writing the reset command returns that bank to the program suspend mode.
If DQ5 goes high during the program or erase operation, writing the reset command returns that bank to read mode or erase suspend mode if that bank was in erase suspend mode.
6) The 3rd and 4th cycle bank address of autoselect mode must be same.
Device ID Data : Top(3010H), Bottom(3011H), Uniform(3012H)
7) Normal Block Protection Verify : 00H for an unprotected block and 01H for a protected block.
OTP Block Protect verify (with OTP Block Address after Entering OTP Block) : 00H for unlocked, and 01H for locked.
8) 0H for handshaking, 1H for non-handshaking
9) The unlock bypass command sequence is required prior to this command sequence.
10) The system may read and program in non-erasing blocks when in the erase suspend mode.
The system may enter the autoselect mode when in the erase suspend mode.
The erase suspend command is valid only during a block erase operation, and requires the bank address.
11) The erase/program resume command is valid only during the erase/program suspend mode, and requires the bank address.
12) This mode is used only to enable Data Read by suspending the Program operation.
13) Set ABP(Address of the block to be protected or unprotected) as either A6 = VIH, A1 = VIH and A0 = VIL for unprotected or A6 = VIL, A1 = VIH and A0 = VIL for protected.
14) Command is valid when the device is in Read mode or Autoselect mode.
15) For Buffer Program, Firstly Enter "Write to Buffer" Command sequence and then Enter Block Address and Word Count which is the number of word data will be programmed. Word Count is smaller than the number of data wanted to program by one, Example if 15 words are wanted to program then WC (Word Count) is 14. After Entering Command, Enter PA/PD's (Program Addresses/ Program Data). Finally Enter "Program buffer to Flash" Command sequence, This starts a buffer program operation. This Device supports 512-word Buffer Program.
There is some caution points.
- The number of PA/PD's which are entered must be same to WC+1
- PA's which are entered must be same A24~A9 address bits because Buffer Address is A24~A9 address and decided by PA entered firstly.
- If PA which are entered isn't same Buffer Address, then PA/PD which is entered may be ignored and this buffer programming operation is aborted.
To return to normal operation, hardware reset or "Write to Buffer Abort Reset" command is issued.
- Overwrite for program buffer is also prohibited.
16) Command sequence resets device for next command after aborted write-to-buffer operation.
17) See "Set Burst Mode Configuration Register" for details.
18) On the third cycle, the data should be "C0h", address bits A10-A0 should be 101_0101_0101b, and address bits A21-A11 set the code to be latched.
19) On the third cycle, the data should be "C5h", address bits A10-A0 should be 101_0101_0101b, and address bits A21-A11 set the code to be latched.
20) After software reset and write to buffer abort reset command, min. 5us recovery time is needed for normal read mode.

4.0 DEVICE OPERATION

The device has inputs/outputs that accept both address and data information. To write a command or command sequence (which includes programming data to the device and erasing blocks of memory), the system must drive CLK, $\overline{AVD}$ and $\overline{CE}$ to V_{IL} and $\overline{OE}$ to V_{IH} when providing an address to the device, and drive CLK, $\overline{WE}$ and $\overline{CE}$ to V_{IL} and $\overline{OE}$ to V_{IH} when writing commands or data.
The device provides the unlock bypass mode to save its program time for program operation. Unlike the standard program command sequence which is comprised of four bus cycles, only two program cycles are required to program a word in the unlock bypass mode. One block, multiple blocks, or the entire device can be erased. Table 17 indicates the address space that each block occupies. The device's address space is divided into sixteen banks. A "bank address" is the address bits required to uniquely select a bank. Similarly, a "block address" is the address bits required to uniquely select a block. I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

4.1 Read Mode

The device automatically enters to asynchronous read mode after device power-up. No commands are required to retrieve data in asynchronous mode. After completing an Internal Program/Erase Routine, each bank is ready to read array data. The reset command is required to return a bank to the read(or erase-suspend-read)mode if DQ5 goes high during an active program/erase operation, or if the bank is in the autoselect mode.
Sync MRS option (Extended Configuration Register)
The synchronous(burst) mode will automatically start on the rising edge of the CLK input while AVD is held low *after Extended Mode Register Setting to A13=0, A12=1.* If several CLKs exist in AVD low, the last rising edge is valid CLK.

4.1.1. Asynchronous Read Mode

For the asynchronous read mode a valid address should be asserted on A/DQ0-A/DQ15 and A16-A24, while driving CLK and $\overline{AVD}$ and $\overline{CE}$ to V_{IL}. $\overline{WE}$ and $\overline{OE}$ should remain at V_{IH}. Note that CLK must remain low for asynchronous read mode. The address is latched at the rising edge of $\overline{AVD}$, and then the system can drive $\overline{OE}$ to V_{IL}. The data will appear on A/DQ0-A/DQ15. Since the memory array is divided into sixteen banks, each bank remains enabled for read access until the command register contents are altered.
Address access time (t_{AA}) is equal to the delay from valid addresses to valid output data. The chip enable access time(t_{CE}) is the delay from the falling edge of $\overline{CE}$ to valid data at the outputs. The output enable access time(t_{OE}) is the delay from the falling edge of $\overline{OE}$ to valid data at the output. The asynchronous access time is measured from a valid address, falling edge of $\overline{AVD}$ or falling edge of $\overline{CE}$ whichever occurs last. To prevent the memory content from spurious altering during power transition, the initial state machine is set for reading array data upon device power-up, or after a hardware reset.

4.1.2. Synchronous (Burst) Read Mode

The device is capable of continuous linear burst operation and linear burst operation of a preset length. For the burst mode, the system should determine how many clock cycles are desired for the initial word(t_{IAA}) of each burst access and what mode of burst operation is desired using "Burst Mode Configuration Register" command sequences. See "Set Burst Mode Configuration" for further details. The status data also can be read by synchronous read mode with a bank address which is programming or erasing. This status data by synchronous read mode can be output and sustained until the system asserts $\overline{CE}$ high or $\overline{RESET}$ low or $\overline{AVD}$ low in conjunction with a new address. To initiate the synchro nous read again, a new address and $\overline{AVD}$ pulse is needed after the host has completed status reads or the device has completed the pro gram or erase operation.

4.1.2.1 . Continuous Linear Burst Read

Sync MRS option (Extended Configuration Register)
The synchronous(burst) mode will automatically start on the rising edge of the CLK input while AVD is held low *after Extended Mode Register Setting to A13=0, A12=1.* If several CLKs exist in AVD low, the last rising edge is valid CLK.

The initial word is output t_{IAA} after the rising edge of the last CLK cycle. Subsequent words are output t_{BA} after the rising edge of each successive clock cycle, which automatically increments the internal address counter. Note that the device has internal address boundary that occurs every 16 words. When the device is crossing the first word boundary, additional clock cycles are needed before data appears for the next address. The number of additional clock cycle can vary from zero to thirteen cycles, and the exact number of additional clock cycle depends on not olny the starting address of burst read but also programmable wait state setting. The RDY output indicates this condition to the system by pulsing low. The device will continue to output sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location until the system asserts $\overline{CE}$ high or $\overline{RESET}$ low or $\overline{AVD}$ low in conjunction with a new address.(See Table 7.) The reset command does not terminate the burst read operation. When it accesses the bank is programming or erasing, continuous burst read mode will output status data. And status data will be sustained until the system asserts $\overline{CE}$ high or $\overline{RESET}$ low or $\overline{AVD}$ low in conjunction with a new address. **Note that at least 10ns is needed to start next burst read operation from terminating previous burst read operation in the case of asserting $\overline{CE}$ high.**

8-, 16-Word Linear Burst Read

As well as the Continuous Linear Burst Mode, there are two(8 & 16 word) linear wrap mode, in which a fixed number of words are read from consecutive addresses. In these modes, the addresses for burst read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode.(See Table. 9)

[Table 8] Burst Address Groups(Wrap mode only)

Burst Mode	Group Size	Group Address Ranges
8 word	8 words	0-7h, 8-Fh, 10-17h, ...
16 word	16 words	0-Fh, 10-1Fh, 20-2Fh, ...

As an example: In wrap mode case, if the starting address in the 8-word mode is 2h, the address range to be read would be 0-7h, and the wrap burst sequence would be 2-3-4-5-6-7-0-1h. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group. In a similar manner, 16-word wrap mode begins its burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group.

4.2 Programmable Wait State

The programmable wait state feature indicates to the device the number of additional clock cycles that must elapse after $\overline{AVD}$ is driven from low to high for burst read mode. Upon power up, the number of total initial access cycles defaults to fourteen.

4.3 Handshaking

The handshaking feature allows the host system to simply monitor the RDY signal from the device to determine when the initial word of burst data is ready to be read. To set the number of initial cycle for optimal burst mode, the host should use the programmable wait state configuration.(See "Set Burst Mode Configuration Register" for details.) The rising edge of RDY after $\overline{OE}$ goes low indicates the initial word of valid burst data. (RDY can be low active by Extended configuration register A11 settng : RDY low indicates data valid) Using the autoselect command sequence, the handshaking feature will be verified in the device.

4.4 Set Burst Mode Configuration Register

The device uses a configuration register to set the various burst parameters : the number of initial cycles for burst and burst read mode. The burst mode configuration register must be set before the device enters burst mode. The burst mode configuration register is loaded with a three-cycle command sequences. On the third cycle, the data should be C0h, address bits A10-A0 should be 101_0101_0101b, and address bits A21-A11 set the code to be latched. The device returns to default setting after power up or hardware reset.

4.4.1. Programmable Wait State Configuration

This feature informs the device the number of clock cycles that must elapse after $\overline{AVD}$ is driven from low to high before data will be available. This value is determined by the input frequency of the device. Address bits A14-A11 determine the setting. (See Configuration Register table 10.) The Programmable wait state setting instructs the device to set a particular number of clock cycles for the initial access in burst mode. Note that hardware reset will revert the wait state to the default setting, that is 14 initial cycles.

4.4.2. Burst Read Mode Setting

The device supports three different burst read modes : continuous linear mode, 8 and 16 word linear burst modes with wrap.

4.4.3. RDY Configuration

By default, the RDY pin will be high whenever there is valid data on the output. (RDY can be low active by Extended configuration register A11 settng : RDY low indicates data valid) The device can be set so that RDY goes active one data cycle before active data. Address bit A18 determines this setting. The RDY pin behaves same way in word boundary crossing case.

[Table 9] Burst Mode Configuration Register Table

Address Bit	Function	Settings(Binary)
A21 A20 A19	Output Driver Control	000 = setting 0 001 = setting 1 010 = setting 2 (Reserve) 011 = setting 3 (Reserve) 100 = setting 4 (default) 101 = setting 5 (Reserve) 110 = setting 6 (Reserve) 111 = setting 7
A18	RDY Active	0 = RDY active with data(default) 1 = RDY active one clock cycle before data
A17 A16 A15	Burst Read Mode	000 = Continuous(default) 001 = 8-word linear with wrap 010 = 16-word linear with wrap 011 ~ 111 = Reserve
A14 A13 A12 A11	Programmable Wait State	0000 = Data is valid on the 4th active CLK edge after $\overline{AVD}$ transition to VIH 0001 = Data is valid on the 5th active CLK edge after $\overline{AVD}$ transition to VIH (40Mhz*) 0010 = Data is valid on the 6th active CLK edge after $\overline{AVD}$ transition to VIH (50/54Mhz*) 0011 = Data is valid on the 7th active CLK edge after $\overline{AVD}$ transition to VIH (60/66Mhz*) 0100 = Data is valid on the 8th active CLK edge after $\overline{AVD}$ transition to VIH (70Mhz*) 0101 = Data is valid on the 9th active CLK edge after $\overline{AVD}$ transition to VIH (80/83Mhz*) 0110 = Data is valid on the 10th active CLK edge after $\overline{AVD}$ transition to VIH (90/100Mhz*) 0111 = Data is valid on the 11th active CLK edge after $\overline{AVD}$ transition to VIH (108/110Mhz*) 1000 = Data is valid on the 12th active CLK edge after $\overline{AVD}$ transition to VIH (120Mhz*) 1001 = Data is valid on the 13th active CLK edge after $\overline{AVD}$ transition to VIH (133Mhz*,default) 1010 = Data is valid on the 14th active CLK edge after $\overline{AVD}$ transition to VIH 1011 = Data is valid on the 15th active CLK edge after $\overline{AVD}$ transition to VIH 1100 ~1111 = Reserve

NOTE :
Initial wait state should be set according to it's clock frequency. Table 10 recommend the program wait state for each clock frequencies.
Not 100% tested

[Table 10] Extended Configuration Register Table

Address Bit	Function	Settings(Binary)
A13 A12	Read Mode	00 = Asynchronous Read Mode(default) 01 = Synchronous Burst Read Mode 10 ~ 11 = Reserve
A11	RDY Polarity	0 = RDY signal is active high (default) 1 = RDY signal is active low

NOTE :
Default mode is asynchronous read mode. (A13=0, A12=0) In this mode device is still in asynchronous read even if it is in CLK rising while AVD low condition.
To use synchronous read mode, user should set Extended Configuration Register (A13=0, A12=1). In this mode both of asynchronous and synchronous read mode is available.
The synchronous(burst) mode should be started on the last rising edge of the CLK input while AVD is held low after Extended Mode Register Setting to A13=0, A12=1.

[Table 11] Burst Address Sequences

	Start Addr.	Burst Address Sequence		
		Continuous Burst	8-word Burst	16-word Burst
Wrap	0	0-1-2-3-4-5-6...	0-1-2-3-4-5-6-7	0-1-2-3 ... -D-E-F
	1	1-2-3-4-5-6-7...	1-2-3-4-5-6-7-0	1-2-3-4 ... -E-F-0
	2	2-3-4-5-6-7-8...	2-3-4-5-6-7-0-1	2-3-4-5 ... -F-0-1
	. .	. .	. .	. .

4.5 Output Driver Setting

The device supports four kinds of output driver setting for matching the system chracteristics. The users can tune the output driver impedance of the data and RDY outputs by address bits A21-A19. (See Configuration Register Table) Table 13 shows which output driver would be tuned and the strength according to A21-A19. Upon power-up or reset, the register will revert to the default setting.

[Table 12] Output Driver setting Table

Address Bits	Value	Function
A21-A19	000	Driver Multiplier : 1/3
	001	Driver Multiplier : 1/2
	010	Reserve
	011	Reserve
	100	Driver Multiplier : 1 (default)
	101	Reserve
	110	Reserve
	111	Driver Multiplier : 1.5

4.6 Autoselect Mode

By writing the autoselect command sequences to the system, the device enters the autoselect mode. This mode can be read only by asynchronous read mode. The system can then read autoselect codes from the internal register(which is separate from the memory array). Standard asynchronous read cycle timings apply in this mode. The device offers the Autoselect mode to identify manufacturer and device type by reading a binary code. In addition, this mode allows the host system to verify the block protection or unprotection. Table 14 shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is in the read mode, erase-suspend-read mode or program-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the device. The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the address and the autoselect command. Note that the block address is needed for the verification of block protection. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence. And the burst read should be prohibited during Autoselect Mode. To terminate the autoselect operation, write Reset command(F0H) into the command register.

[Table 13] Autoselect Mode Description

Description	Address	Read Data
Manufacturer ID	(DA) + 00H	ECH
Device ID	(DA) + 01H	**Top boot(3010H), Bottom boot(3011H), Uniform block(3012H)**
Block Protection/Unprotection	(BA) + 02H	01H (protected), 00H (unprotected)
Handshaking	(DA) + 03H	0H : handshaking, 1H : non-handshaking

4.7 Standby Mode

When the $\overline{CE}$ inputs is held at $V_{CC} \pm 0.2V$, and the system is not reading or writing, the device enters Stand-by mode to minimize the power consumption. In this mode, the device outputs are placed in the high impedence state, independent of the $\overline{OE}$ input. When the device is in either of these standby modes, the device requires standard access time (tCE) for read access before it is ready to read data. If the device is deselected during erasure or programming, the device draws active current until the operation is completed. I_{CC5} in the DC Characteristics table represents the standby current specification.

4.8 Automatic Sleep Mode

The device features Automatic Sleep Mode to minimize the device power consumption during both asynchronous and burst mode. When addresses remain stable for t_{AA}+60ns, the device automatically enables this mode. The Automatic sleep mode is depends on the $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ signal, so $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ signals are held at any state. In a sleep mode, output data is latched and always available to the system. When $\overline{OE}$ is active, the device provides new data without wait time. Automatic sleep mode current is equal to standby mode current.

4.9 Output Disable Mode

When the $\overline{OE}$ input is at V_{IH} , output from the device is disabled. The outputs are placed in the high impedance state.

4.10 Block Protection & Unprotection

To protect the block from accidental writes, the block protection/unprotection command sequence is used. On power up, all blocks in the device are protected. To unprotect a block, the system must write the block protection/unprotection command sequence. The first two cycles are written: addresses are don't care and data is 60h. Using the third cycle, the block address (ABP) and command (60h) is written, while specifying with addresses A6, A1 and A0 whether that block should be protected (A6 = V_{IL}, A1 = V_{IH}, A0 = V_{IL}) or unprotected (A6 = V_{IH}, A1 = V_{IH}, A0 = V_{IL}). After the third cycle, the system can continue to protect or unprotect additional cycles, or exit the sequence by writing F0h (reset command).
The device offers three types of data protection at the block level:

- The block protection/unprotection command sequence disables or re-enables both program and erase operations in any block.
- When $\overline{WP}$ is at V_{IL}, the two outermost blocks are protected.(Boot block part)
- When $\overline{WP}$ is at V_{IL}, the last one block (BA511) is protected.(Uniform block part)
- When V_{PP} is at V_{IL}, all blocks are protected.

Note that user never float the Vpp and $\overline{WP}$, that is, Vpp is always connected with V_{IH}, V_{IL} or V_{ID} and $\overline{WP}$ is V_{IH} or V_{IL}.

4.11 Hardware Reset

The device features a hardware method of resetting the device by the $\overline{RESET}$ input. When the $\overline{RESET}$ pin is held low(V_{IL}) for at least a period of tRP, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/write commands for the duration of the $\overline{RESET}$ pulse. The device also resets the internal state machine to asynchronous read mode. To ensure data integrity, the interrupted operation should be reinitiated once the device is ready to accept another command sequence. The $\overline{RESET}$ pin may be tied to the system reset pin. If a system reset occurs during the Internal Program or Erase Routine, the device will be automatically reset to the asynchronous read mode; this will enable the systems microprocessor to read the boot-up firmware from the Flash memory. If $\overline{RESET}$ is asserted during a program or erase operation, the device requires a time of tREADY (during Internal Routines) before the device is ready to read data again. If $\overline{RESET}$ is asserted when a program or erase operation is not executing, the reset operation is completed within a time of tREADY (not during Internal Routines). tRH is needed to read data after $\overline{RESET}$ returns to V_{IH}. Refer to the AC Characteristics tables for $\overline{RESET}$ parameters and to Figure 12 for the timing diagram. When $\overline{RESET}$ is at logic high, the device is in standard operation.

4.12 Software Reset

The reset command provides that the bank is reseted to read mode, erase-suspend-read mode or program-suspend-read mode. The addresses are in Don't Care state. The reset command may be written between the sequence cycles in an erase command sequence before erasing begins, or in an program command sequence before programming begins. If the device begins erasure or programming, the reset command is ignored until the operation is completed. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. The reset command valid between the sequence cycles in an autoselect command sequence. In an autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Also, if a bank entered the autoselect mode while in the Program Suspend mode, writing the reset command returns that bank to the program-suspend-read mode. If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode. (or erase-suspend-read mode if the bank was in Erase Suspend)

4.13 Program

The device can be programmed in units of a word. Programming is writing 0's into the memory array by executing the Internal Program Routine. In order to perform the Internal Program Routine, a four-cycle command sequence is necessary. The first two cycles are unlock cycles. The third cycle is assigned for the program setup command. In the last cycle, the address of the memory location and the data to be programmed at that location are written. The device automatically generates adequate program pulses and verifies the programmed cell margin by the Internal Program Routine. During the execution of the Routine, the system is not required to provide further controls or timings. During the Internal Program Routine, commands written to the device will be ignored.

4.14 Accelerated Program

The device provides accelerated program operations through the Vpp input. Using this mode, faster manufacturing throughput at the factory is possible. When V_{ID} is asserted on the Vpp input, the device automatically enters the Unlock Bypass mode, temporarily unprotects any protected blocks, and uses the higher voltage on the input to reduce the time required for program operations. In accelerated program mode, the system would use a two-cycle program command sequence for only a word program. By removing V_{ID} returns the device to normal operation mode.
Note that Read While Accelerated Program(Erase) and Program suspend(Erase suspend) mode are not guaranteed.

- Program/Erase cycling must be limited below 100cycles for optimum performance.
- Ambient temperature requirements : T_A = 30°C±10°C

4.15 Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 512-word in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initi-ated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the block address in which programming will occur. The fourth cycle writes the block address and the number of word locations, minus one, to be programmed. For example, if the system will program 19 unique address locations, then 12h should be written to the device. This tells the device how many write buffer addresses will be loaded with data. The number of locations to program cannot exceed the size of the write buffer or the operation will abort. The fifth cycle writes the first address location and data to be programmed. ***The write-buffer-page is selected by address bits A24(max.) ~ A9 entered at fifth cycle. All subsequent address/ data pairs must fall within the selected write-buffer-page, so that all subsequent addresses must have the same address bit A24(max.) ~ A9 as those entered at fifth cycle. Write buffer locations may be loaded in any order.***

Once the specified number of write buffer locations have been loaded, the system must then write the "Program Buffer to Flash" com mand at the block address. Any other command address/data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming. The write-buffer programming operation can be suspended using the standard program suspend/ resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

Note also that an address loaction cannot be loaded more than once into the write-buffer-page.

The Write Buffer Programming Sequence can be aborted in the following ways:

- Loading a value that is greater than the buffer size(512-word) during then number of word locations to Program step. (In case, WC > 1FFH @Table 8)
- The number of Program address/data pairs entered is different to the number of word locations initially defined with WC (@Table 8)
- Writing a Program address to have a different write-buffer-page with selected write-buffer-page (Address bits A24(max) ~ A9 are different)
- Writing non-exact "Program Buffer to Flash" command

The abort condition is indicated by DQ1 = 1, DQ7 = $\overline{\text{DATA}}$ (for the last address location loaded), DQ6 = toggle, and DQ5=0. A "Write-to-Buffer-Abort Reset" command sequence must be written to reset the device for the next operation. Note that the third cycle of Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

And from the third cycle to the last cycle of Write to Buffer command is also required when using Write-Buffer-Programming features in Unlock Bypass mode. A bit cannot be programmed from “0” back to a “1.” Attempting to do so may cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still “0.” Only erase operations can convert a “0” to a “1."

4.16 Accelerated Write Buffer Programming

The device provides accelerated Write Buffer Program operations through the Vpp input. Using this mode, faster manufacturing throughput at the factory is possible. When V_{ID} is asserted on the Vpp input, the device temporarily unprotects any protected blocks, and uses the higher voltage on the input to reduce the time required for program operations. In accelerated Write Buffer Program mode, the system must enter "Write to Buffer" and "Program Buffer to Flash" command sequence to be same as them of normal Write Buffer Programming. Note that the third cycle of "Write to Buffer Abort Reset" command sequence is required in an accelerated mode.

Note that Read While Accelerated Write Buffer Program and Program suspend mode are not guaranteed.

- Program/Erase cycling must be limited below 100cycles for optimum performance.
- Ambient temperature requirements : T_A = 30°C±10°C

4.17 Chip Erase

To erase a chip is to write 1′s into the entire memory array by executing the Internal Erase Routine. The Chip Erase requires six bus cycles to write the command sequence. The erase set-up command is written after first two "unlock" cycles. Then, there are two more write cycles prior to writing the chip erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory for an all zero data pattern prior to erasing. The automatic erase begins on the rising edge of the last $\overline{\text{WE}}$ pulse in the command sequence and terminates when DQ7 is "1". After that the device returns to the read mode.

4.18 Block Erase

To erase a block is to write 1′s into the desired memory block by executing the Internal Erase Routine. The Block Erase requires six bus cycles to write the command sequence shown in Table 8. After the first two "unlock" cycles, the erase setup command (80H) is written at the third cycle. Then there are two more "unlock" cycles followed by the Block Erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory prior to erasing it. The block address is latched on the rising edge of AVD , while the Block Erase command is latched on the rising edge of WE. Multiple blocks can be erased sequentially by writing the sixth bus-cycle. Upon completion of the last cycle for the Block Erase, additional block address and the Block Erase command (30H) can be written to perform the Multi-Block Erase. For the Multi-Block Erase, only sixth cycle(block address and 30H) is needed.(Similarly, only second cycle is needed in unlock bypass block erase.) An 50us (typical) "time window" is required between the Block Erase command writes. The Block Erase command must be written within the 50us "time window", otherwise the Block Erase command will be ignored. The 50us "time window" is reset when the falling edge of the WE occurs within the 50us of "time window" to latch the Block Erase command. During the 50us of "time window", any command other than the Block Erase or the Erase Suspend command written to the device will reset the device to read mode. After the 50us of "time window", the Block Erase command will initiate the Internal Erase Routine to erase the selected blocks. Any Block Erase address and command following the exceeded "time window" may or may not be accepted. No other commands will be recognized except the Erase Suspend command during Block Erase operation.
The device provides accelerated erase operations through the Vpp input. When V_{ID} is asserted on the Vpp input, the device automatically enters the Unlock Bypass mode, temporarily unprotects any protected blocks, and uses the higher voltage on the input to reduce the time required for erase. By removing V_{ID} returns the device to normal operation mode.

4.19 Blank check

The Blank Check operation is used one block at a time to check whether a block is completely erased or not. It is not available during Program Suspend or Erase Suspend. For using Blank Check, first issue the command which has 4-cycle and check the status. The Bank addressed in Blank Check Command is automatically changed to Status check mode, until Reset command (XXXH / F0H) is issued.
During a blank check operation, DQ status flags indicates a busy status (DQ6, DQ2 = toggle / DQ5=0). Upon completion, the DQ status flags indicates that Blank check operation is passed (DQ6 = toggle , DQ5=1 and DQ1=1). That means the block is completely erased.
In Blank check operation failure case, the DQ status flags indicates DQ6 = toggle , DQ5=1 and DQ1=0. The block is not completely erased.

No other commands will be recognized except status read operation during Blank Check operation. Blank Check cannot be suspended. After the completion of the Blank Check operation, any valid command can be issued after Reset command (XXXH / F0H).
NOTE that, unexpected power off or hardware reset during internal write routine may make blank check operation unavailable. And Blank check cannot be used in OTP block area.

4.20 Unlock Bypass

The device provides the unlock bypass mode to save its operation time. This mode is possible for program, block erase, chip erase, write to buffer and write to buffer abort reset operation.. There are two methods to enter the unlock bypass mode. The mode is invoked by the unlock bypass command sequence or the assertion of V_{ID} on V_{PP} pin. Unlike the standard program/erase command sequence that contains four bus cycles, the unlock bypass program/erase command sequence comprises only two bus cycles. The unlock bypass mode is engaged by issuing the unlock bypass command sequence which is comprised of three bus cycles. Writing first two unlock cycles is followed by a third cycle containing the unlock bypass command (20H). Once the device is in the unlock bypass mode, the unlock bypass program/erase command sequence is necessary. The unlock bypass program command sequence is comprised of only two bus cycles; writing the unlock bypass program command (A0H) is followed by the program address and data. This command sequence is the only valid one for programming the device in the unlock bypass mode. Also, The unlock bypass erase command sequence is comprised of two bus cycles; writing the unlock bypass block erase command(80H-30H) or writing the unlock bypass chip erase command(80H-10H). This command sequences are the only valid ones for erasing the device in the unlock bypass mode. The unlock bypass reset command sequence is the only valid command sequence to exit the unlock bypass mode. The unlock bypass reset command sequence consists of two bus cycles. The first cycle must contain the data (90H). The second cycle contains only the data (00H). Then, the device returns to the read mode.
To enter the unlock bypass mode in hardware level, the V_{ID} also can be used. By assertion V_{ID} on the V_{PP} pin, the device enters the unlock bypass mode. Also, the all blocks are temporarily unprotected when the device using the V_{ID} for unlock bypass mode. To exit the unlock bypass mode, just remove the asserted V_{ID} from the V_{PP} pin.(Note that user never float the Vpp, that is, Vpp is always connected with V_{IH}, V_{IL} or V_{ID}.).

4.21 Erase Suspend / Resume

The Erase Suspend command interrupts the Block Erase to read or program data in a block that is not being erased. Also, it is possible to protect or unprotect of the block that is not being erased in erase suspend mode. The Erase Suspend command is only valid during the Block Erase operation including the time window of 50us. The Erase Suspend command is not valid while the Chip Erase or the Internal Program Routine sequence is running. When the Erase Suspend command is written during a Block Erase operation, the device requires a maximum of 30us(recovery time) to suspend the erase operation. Therefore system must wait for 30us(recovery time) to read the data from the bank which include the block being erased. Otherwise, system can read the data immediately from a bank which don't include the block being erased without recovery time(max. 30us) after Erase Suspend command. And, after the maximum 30us recovery time, the device is availble for programming data in a block that is not being erased. But, when the Erase Suspend command is written during the block erase time window (50us), the device terminates the block erase time window and suspends the erase operation in about 2us. The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. When the Erase Resume command is executed, the Block Erase operation will resume. When the Erase Suspend or Erase Resume command is executed, the addresses are in the bank address which is operating in Erase Suspend or Erase Resume. **While erase can be suspended and resumed multiple times, a minimum 30us is required from resume to the next suspend.**

4.22 Program Suspend / Resume

The device provides the Program Suspend/Resume mode. This mode is used to enable Data Read by suspending the Program operation. The device accepts a Program Suspend command in Program mode(including Program operations performed during Erase Suspend) but other commands are ignored. After input of the Program Suspend command, 10us is needed to enter the Program Suspend Read mode. Therefore system must wait for 10us(recovery time) to read the data from the bank which include the block being programmed. Otherwise, system can read the data immediately from a bank which don't include block being programmed without recovery time(max.10us) after Program Suspend command. Like an Erase Suspend mode, the device can be returned to Program mode by using a Program Resume command. **While program can be suspended and resumed multiple times, a minimum 30us is required from resume to the next suspend.**

In the program suspend mode, protect/unprotect command is prohibited.

4.23 Read While Write Operation

The device is capable of reading data from one bank while writing in the other banks. This is so called the Read While Write operation. An erase operation may also be suspended to read from or program to another location within the same bank(except the block being erased). The Read While Write operation is prohibited during the chip erase operation. Figure 19 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the DC Characteristics table for read-while-write current specifications.

4.24 OTP Block Region

The OTP Block feature provides a 512-word Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The OTP Block is customer lockable and shipped with itself unlocked, allowing customers to untilize the that block in any manner they choose. The customer-lockable OTP Block has the Protection Verify Bit (DQ0) set to a "0" for Unlocked state or a "1" for Locked state.
The system accesses the OTP Block through a command sequence (see "Enter OTP Block / Exit OTP Block Command sequence" at Table 8). After the system has written the "Enter OTP Block" Command sequence, it may read the OTP Block by using the addresses (1FFFE00h~1FFFFFFh : Top Boot block device/Uniform block device, 0000000h-00001FFh : Bottom Boot block device) normally and may check the Protection Verify Bit (DQ0) by using the "Autoselect Block Protection Verify" Command sequence with OTP Block address. This mode of operation continues until the system issues the "Exit OTP Block" Command suquence, a hardware reset or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to main blocks. Note that the Accelerated function and unlock bypass modes are not available when the OTP Block is enabled.

Customer Lockable
In a Customer lockable device, The OTP Block is one-time programmable and can be locked only once. Note that the Accelerated programming and Unlock bypass functions are not available when programming the OTP Block. Locking operation to the OTP Block is started by writing the "Enter OTP Block" Command sequence, and then the "Block Protection" Command seqeunce (Table 8) with an OTP Block address. The Locking operation has to be above 100us. "Exit OTP Block" commnad sequence and Hardware reset makes locking operation finished and then exiting from OTP Block after 30us.

The OTP Block Lock operation must be used with caution since, once locked, there is no procedure available for unlocking and none of the bits in the OTP Block space can be modified in any way.

Suspend and resume operation are not supported during OTP protect, nor is OTP protect supported during any suspend operations. ***After entering OTP block, program/erase operation on main blocks is prohibited. Enter OTP block command is not allowed while other operation is excuting.***

4.25 Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than V_{LKO}. If the Vcc < V_{LKO} (Lock-Out Voltage), the command register and all internal program/erase circuits are disabled. Under this condition the device will reset itself to the read mode.Subsequent writes will be ignored until the Vcc level is greater than V_{LKO}. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above V_{LKO}.

4.26 Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on $\overline{OE}$, $\overline{CE}$, $\overline{AVD}$ or $\overline{WE}$ do not initiate a write cycle.

4.27 Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{OE}$ = V_{IL} , $\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

5.0 FLASH MEMORY STATUS FLAGS

The device has means to indicate its status of operation in the bank where a program or erase operation is in processes. Address must include bank address being executed internal routine operation. The status is indicated by raising the device status flag via corresponding DQ pins. The status data can be read during burst read mode by using $\overline{AVD}$ signal with a bank address. That means status read is supported in synchronous mode. If status read is performed, the data provided in the burst read is identical to the data in the initial access. To initiate the synchronous read again, a new address and $\overline{AVD}$ pulse is needed after the host has completed status reads or the device has completed the program or erase operation. The corresponding DQ pins are DQ7, DQ6, DQ5, DQ3, DQ2 and DQ1.

[Table 14] Hardware Sequence Flags

	Status		DQ7	DQ6	DQ5	DQ3	DQ2	DQ1
In Progress	Programming		$\overline{DQ7}$	Toggle	0	0	1	0
	Block Erase or Chip Erase or Blank check		0	Toggle	0	1	Toggle	0
	Erase Suspend Read	Erase Suspended Block	1	1	0	0	Toggle[1)]	0
	Erase Suspend Read	Non-Erase Suspended Block	Data	Data	Data	Data	Data	Data
	Erase Suspend Program	Non-Erase Suspended Block	$\overline{DQ7}$	Toggle	0	0	1	0
	Program Suspend Read	Program Suspended Block	DQ7	1	0	0	Toggle[1)]	0
	Program Suspend Read	Non- program Suspended Block	Data	Data	Data	Data	Data	Data
Exceeded Time Limits	Programming		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
	Block Erase or Chip Erase or Blank check Fail		0	Toggle	1	1	(NOTE 2)	0
	Blank check Pass		0	Toggle	1	1	(NOTE 2)	1
	Erase Suspend Program		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
Write-to-Buffer[3)]	BUSY state		$\overline{DQ7}$	Toggle	0	0	No Toggle	0
	Exceeded Timing Limits		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
	ABORT State		$\overline{DQ7}$	Toggle	0	0	No Toggle	1

NOTE :
1) DQ2 will toggle when the device performs successive read operations from the erase/program suspended block.
2) If DQ5 is High (exceeded timing limits), successive reads from a problem block will cause DQ2 to toggle.
3) Note that $\overline{DQ7}$ during Write-to-Buffer-Programming indicates the data-bar for DQ7 data for *the last loaded write-buffer address* location.

DQ7 : $\overline{\text{Data}}$ Polling

When an attempt to read the device is made while executing the Internal Program, the complement of the data is written to DQ7 as an indication of the Routine in progress. When the Routine is completed an attempt to access to the device will produce the true data written to DQ7. When a user attempts to read the block being erased or bank contains the block, DQ7 will be low. If the device is placed in the Erase/Program Suspend Mode, the status can be detected via the DQ7 pin. If the system tries to read an address which belongs to a block that is being erase suspended, DQ7 will be high. And, if the system tries to read an address which belongs to a block that is being program suspended, the output will be the true data of DQ7 itself. If a non-erase-suspended or non-program-suspended block address is read, the device will produce the true data to DQ7. If an attempt is made to program a protected block, DQ7 outputs complements the data for approximately 2us and the device then returns to the Read Mode without changing data in the block. If an attempt is made to erase a protected block, DQ7 outputs complement data in approximately 100us and the device then returns to the Read Mode without erasing the data in the block.

DQ6 : Toggle Bit

Toggle bit is another option to detect whether an Internal Routine is in progress or completed. Once the device is at a busy state, DQ6 will toggle. Toggling DQ6 will stop after the device completes its Internal Routine. If the device is in the Erase/Program Suspend Mode, an attempt to read an address that belongs to a block that is being erased or programmed will produce a high output of DQ6. If an address belongs to a block that is not being erased or programmed, toggling is halted and valid data is produced at DQ6. If an attempt is made to program a protected block, DQ6 toggles for approximately 2us and the device then returns to the Read Mode without changing the data in the block. If an attempt is made to erase a protected block, DQ6 toggles for approximately 100μs and the device then returns to the Read Mode without erasing the data in the block. #OE or #CE should be toggled in each toggle bit status read.

DQ5 : Exceed Timing Limits

If the Internal Program/Erase Routine extends beyond the timing limits, DQ5 will go High, indicating program/erase failure. Also the result of blank check can be checked by DQ5=1.

DQ3 : Block Erase Timer

The status of the multi-block erase operation can be detected via the DQ3 pin. DQ3 will go High if 50μs of the block erase time window expires. In this case, the Internal Erase Routine will initiate the erase operation.Therefore, the device will not accept further write commands until the erase operation is completed. DQ3 is Low if the block erase time window is not expired. Within the block erase time window, an additional block erase command (30H) can be accepted. To confirm that the block erase command has been accepted, the software may check the status of DQ3 following each block erase command.

DQ2 : Toggle Bit 2

The device generates a toggling pulse in DQ2 only if an Internal Erase Routine or an Erase/Program Suspend is in progress. When the device executes the Internal Erase Routine, DQ2 toggles if the bank including an erasing block is read. Although the Internal Erase Routine is in the Exceeded Time Limits, DQ2 toggles only if an erasing block in the Exceeded Time Limits is read. When the device is in the Erase/Program Suspend mode, DQ2 toggles only if an address in the erasing or programming block is read. If a non-erasing or non-programmed block address is read during the Erase/Program Suspend mode, then DQ2 will produce valid data. DQ2 will go High if the user tries to program a non-erase suspend block while the device is in the Erase Suspend mode. #OE or #CE should be toggled in each toggle bit status read.

DQ1 : Buffer Program Abort Indicator

DQ1 indocates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. Also DQ1 will go High if the blank check is passed. DQ1 will go low in the blank check failure.

RDY: Ready

Normally the RDY signal is used to indicate if new burst data is available at the rising edge of the clock cycle or not. If RDY is low state, data is not valid at expected time, and if high state, data is valid. Note that, if $\overline{CE}$ is low and $\overline{OE}$ is high, the RDY is high state.

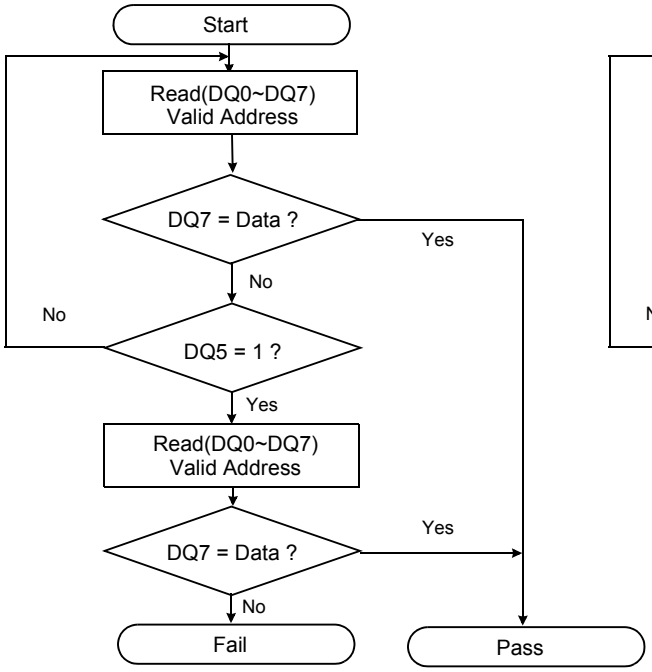


Figure 1. Data Polling Algorithms

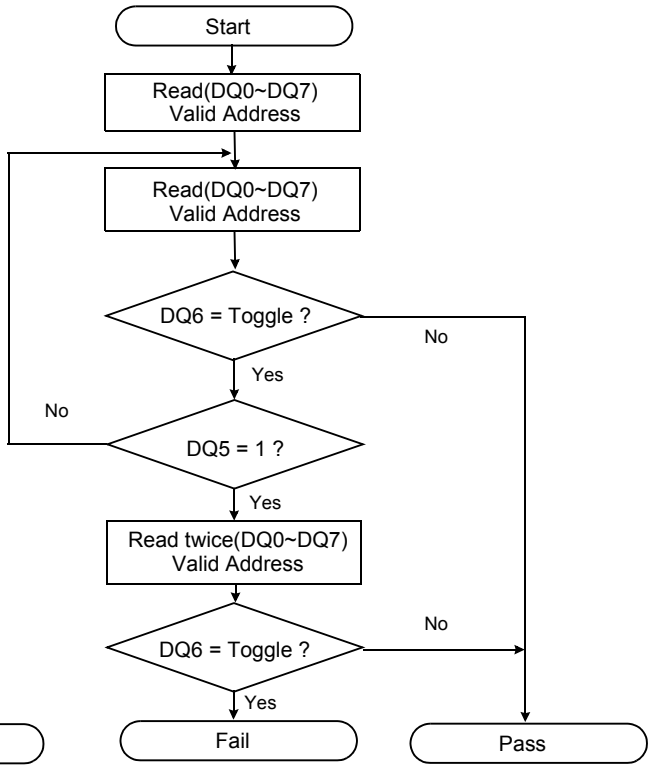


Figure 2. Toggle Bit Algorithms

6.0 Common Flash Memory Interface

Common Flash Memory Interface is contrived to increase the compatibility of host system software. It provides the specific information of the device, such as memory size and electrical features. Once this information has been obtained, the system software will know which command sets to use to enable flash writes, block erases, and control the flash component.
When the system writes the CFI command(98H) to address 55H , the device enters the CFI mode. And then if the system writes the address shown in Table 16, the system can read the CFI data. Query data are always presented on the lowest-order data outputs(DQ0-7) only. In word(x16) mode, the upper data outputs(DQ8-15) is 00h. To terminate this operation, the system must write the reset command.

[Table 15] Common Flash Memory Interface Code

Description	Addresses (Word Mode)	Data
Query Unique ASCII string "QRY"	10H 11H 12H	0051H 0052H 0059H
Primary OEM Command Set	13H 14H	0002H 0000H
Address for Primary Extended Table	15H 16H	0040H 0000H
Alternate OEM Command Set (00h = none exists)	17H 18H	0000H 0000H
Address for Alternate OEM Extended Table (00h = none exists)	19H 1AH	0000H 0000H
Vcc Min. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1BH	0017H
Vcc Max. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1CH	0019H
Vpp(Acceleration Program) Supply Minimum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	1DH	0085H
Vpp(Acceleration Program) Supply Maximum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	1EH	0095H
Typical timeout per single word write 2^N us	1FH	0007H
Typical timeout for Max buffer write 2^N us(00H = not supported)	20H	000AH
Typical timeout per individual block erase 2^N ms	21H	000AH
Typical timeout for full chip erase 2^N ms(00H = not supported)	22H	0013H
Max. timeout for word write 2^N times typical	23H	0003H
Max. timeout for buffer write 2^N times typical	24H	0003H
Max. timeout per individual block erase 2^N times typical	25H	0003H
Max. timeout for full chip erase 2^N times typical(00H = not supported)	26H	0003H
Device Size = 2^N byte	27H	001AH
Flash Device Interface description	28H 29H	0000H 0000H
Max. number of byte in multi-byte write = 2^N	2AH 2BH	000AH 0000H
Number of Erase Block Regions within device[1)]	2CH	0002H
Erase Block Region 1 Information (Boot block part) Bits 0~15: y+1=block number Bits 16~31: block size= z x 256bytes	2DH 2EH 2FH 30H	0003H 0000H 0080H 0000H

Description	Addresses (Word Mode)	Data
Erase Block Region 1 Information (Uniform block part) Bits 0~15: y+1=block number Bits 16~31: block size= z x 256bytes	2DH 2EH 2FH 30H	00FFH 0001H 0000H 0002H
Erase Block Region 2 Information (Boot block part)	31H 32H 33H 34H	00FEH 0001H 0000H 0002H
Erase Block Region 2 Information (Uniform block part)	31H 32H 33H 34H	0000H 0000H 0000H 0000H
Erase Block Region 3 Information	35H 36H 37H 38H	0000H 0000H 0000H 0000H
Erase Block Region 4 Information	39H 3AH 3BH 3CH	0000H 0000H 0000H 0000H
Query-unique ASCII string "PRI"	40H 41H 42H	0050H 0052H 0049H
Major version number, ASCII	43H	0031H
Minor version number, ASCII	44H	0031H
Address Sensitive Unlock(Bits 1-0) 0 = Required, 1= Not Required Silcon Revision Number(Bits 7-2)	45H	0000H
Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write	46H	0002H
Block Protect 00 = Not Supported, 01 = Supported	47H	0001H
Block Temporary Unprotect 00 = Not Supported, 01 = Supported	48H	0000H
Block Protect/Unprotect scheme 00 = Not Supported, 01 = Supported	49H	0001H
Simultaneous Operation 00 = Not Supported, 01 = Supported	4AH	0001H
Burst Mode Type 00 = Not Supported, 01 = Supported	4BH	0001H
Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page, 03 = 16 Word Page	4CH	0000H
Top/Bottom Boot/Uniform Block Flag 02H = Bottom Boot Device, 03H = Top Boot Device, 04H = Uniform Device	4DH	0003H
Max. Operating Clock Frequency (MHz) [2)]	4EH	0085H
RWW(Read While Write) Functionality Restriction (00H = non exists , 01H = exists)	4FH	0000H
Handshaking 00 = Not Supported at both mode, 01 = Supported at Sync. Mode 10 = Supported at Async. Mode, 11 = Supported at both Mode	50H	0001H

NOTE :
1) Uniform block part : Data is 01H
Boot block part : Data is 02H
2) Max. Operating Clock Frequency : Data is 85H in 108/133Mhz part , Data is 53H in 66/83Mhz part

7.0 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	Vcc	Vcc	-0.5 to +2.5	V
	V_{PP}	V_{IN}	-0.5 to +9.5	
	All Other Pins		-0.5 to +2.5	
Storage Temperature		T_{stg}	-65 to +100	°C
Short Circuit Output Current		I_{OS}	5	mA
Operating Temperature		T_A	-25 to + 85	°C

NOTE :

1) Minimum DC voltage is -0.5V on Input/ Output pins. During transitions, this level may fall to -2.0V for periods <20ns.
   Maximum DC voltage is Vcc+0.6V on input / output pins which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.
2) Minimum DC input voltage is -0.5V on V_{PP} . During transitions, this level may fall to -2.0V for periods <20ns.
   Maximum DC input voltage is +9.5V on V_{PP} which, during transitions, may overshoot to +12.0V for periods <20ns.
3) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8.0 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	1.7	1.8	1.95	V
Supply Voltage	Vss	0	0	0	V

NOTE : Voltage reference to GND

1) Data retention is not guaranteed on Operating condition Extended temperature(-25'C~85'C) over.

9.0 DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN}=V_{SS}$ to V_{CC}, $V_{CC}=V_{CC}$max		- 1.0	-	+ 1.0	μA
VPP Leakage Current	I_{LIP}	$V_{CC}=V_{CC}$max , $V_{PP}=V_{CC}$max		- 1.0	-	+ 1.0	μA
		$V_{CC}=V_{CC}$max , V_{PP}=9.5V		-	-	35	μA
Output Leakage Current	I_{LO}	$V_{OUT}=V_{SS}$ to V_{CC}, $V_{CC}=V_{CC}$max, $\overline{OE}=V_{IH}$		- 1.0	-	+ 1.0	μA
Active Burst Read Current	I_{CCB1}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$ (@133MHz)		-	35	55	mA
Active Asynchronous Read Current	I_{CC1}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	10MHz	-	35	55	mA
Active Write Current [2]	I_{CC2}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$, $\overline{WE}=V_{IL}$, $V_{PP}=V_{IH}$		-	25	40	mA
Read While Write Current	I_{CC3}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$		-	45	70	mA
Accelerated Program Current	I_{CC4}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$, V_{PP}=9.5V		-	20	30	mA
Standby Current	I_{CC5}	$\overline{CE}$= $\overline{RESET}$=VCC ± 0.2V		-	30	120	μA
Standby Current During Reset	I_{CC6}	$\overline{RESET}$ = V_{SS} ± 0.2V		-	30	120	μA
Automatic Sleep Mode [3]	I_{CC7}	$\overline{CE}=V_{SS}$ ± 0.2V, Other Pins=V_{IL} or V_{IH} V_{IL} = V_{SS} ± 0.2V, V_{IH} = V_{CC} ± 0.2V		-	30	120	μA
Input Low Voltage	V_{IL}			-0.5	-	0.4	V
Input High Voltage	V_{IH}			V_{CC}-0.4	-	V_{CC}+0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 μA , $V_{CC}=V_{CC}$min		-	-	0.1	V
Output High Voltage	V_{OH}	I_{OH} = -100 μA , $V_{CC}=V_{CC}$min		V_{CC}-0.1	-	-	V
Voltage for Accelerated Program	V_{ID}			8.5	9.0	9.5	V
Low VCC Lock-out Voltage	V_{LKO}			-	-	1.4	V
Vpp current in program/erase	I_{vpp}	V_{PP} = 9.5V		-	0.8	5	mA
		V_{PP} = 1.95V		-	-	50	μA

NOTE :

1) Maximum ICC specifications are tested with V_{CC} = V_{CC}max.

2) I_{CC} active while Internal Erase or Internal Program is in progress.

3) Device enters automatic sleep mode when addresses are stable for t_{AA} + 60ns.

10.0 VCC POWER-UP

Parameter	Symbol	All Speed Options		Unit
		Min	Max	
Vcc Setup Time	t_{VCS}	200	-	µs
Time between $\overline{RESET}$ (high) and $\overline{CE}$ (low)	t_{RH}	200	-	ns

NOTE : Not 100% tested.

SWITCHING WAVEFORMS

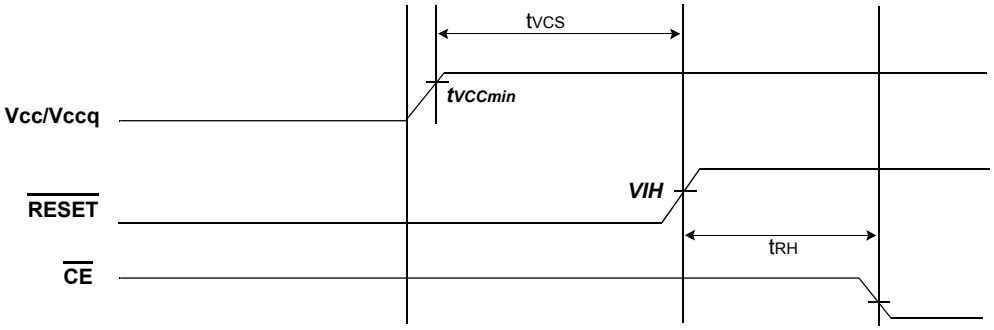


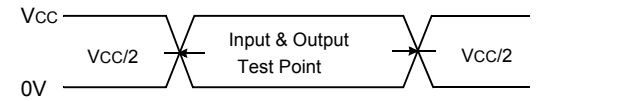
Figure 3. Vcc Power-up Diagram

11.0 CAPACITANCE (TA = 25 °C, VCC = 1.8V, f = 1.0MHz)

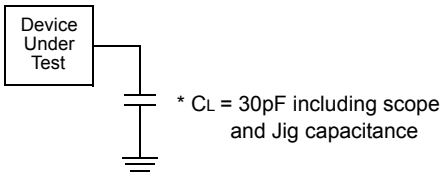
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	10	pF
Control Pin Capacitance	C_{IN2}	V_{IN}=0V	-	10	pF

12.0 AC TEST CONDITION

Parameter	Value
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	3ns(max)@66Mhz, 2.5ns(max)@83Mhz, 1.5ns(max)@108Mhz, 1ns(max)@133Mhz
Input and Output Timing Levels	Vcc/2
Output Load	CL = 30pF
Address to Address Skew	3ns(max)



Input Pulse and Test Point (including CLK characterization)



Output Load

13.0 AC CHARACTERISTICS

13.1 Synchronous/Burst Read

Parameter	Symbol	1C (66 MHz)		1D (83 MHz)		1E (108 MHz)		1F (133 MHz)		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Initial Access Time	t_{IAA}	-	95	-	95	-	95	-	95	ns
Burst Access Time Valid Clock to Output Delay	t_{BA}	-	11	-	9	-	7	-	6	ns
$\overline{AVD}$ Setup Time to CLK	t_{AVDS}	5	-	4	-	3.5	-	2.5	-	ns
$\overline{AVD}$ Hold Time from CLK	t_{AVDH}	2	-	2	-	2	-	2	-	ns
$\overline{AVD}$ High to $\overline{OE}$ Low	t_{AVDO}	0	-	0	-	0	-	0	-	ns
Address Setup Time to CLK	t_{ACS}	5	-	4	-	3.5	-	2.5	-	ns
Address Hold Time from CLK	t_{ACH}	6	-	5	-	2	-	2	-	ns
Data Hold Time from Next Clock Cycle	t_{BDH}	3	-	3	-	2	-	2	-	ns
Output Enable to RDY valid	t_{OER}	-	11	-	9	-	7	-	6	ns
$\overline{CE}$ Disable to High Z	t_{CEZ}	-	9	-	9	-	9	-	9	ns
$\overline{OE}$ Disable to High Z	t_{OEZ}	-	9	-	9	-	9	-	9	ns
$\overline{CE}$ Setup Time to CLK	t_{CES}	6	-	4.5	-	4	-	3.5	-	ns
$\overline{CE}$ Enable to RDY active	t_{RDY}	-	11	-	9	-	7	-	6	ns
CLK to RDY Setup Time	t_{RDYA}	-	11	-	9	-	7	-	6	ns
RDY Setup Time to CLK	t_{RDYS}	3	-	3	-	2	-	2	-	ns
CLK period	t_{CLK}	15.1	-	12.05	-	9.26	-	7.52	-	ns
CLK High or Low Time	$t_{CLKH/L}$	0.4x t_{CLK}	0.6x t_{CLK}	0.4x t_{CLK}	0.6x t_{CLK}	0.4x t_{CLK}	0.6x t_{CLK}	0.4x t_{CLK}	0.6x t_{CLK}	ns
CLK Fall or Rise Time	t_{CLKHCL}	-	3	-	2.5	-	1.5	-	1	ns

SWITCHING WAVEFORMS

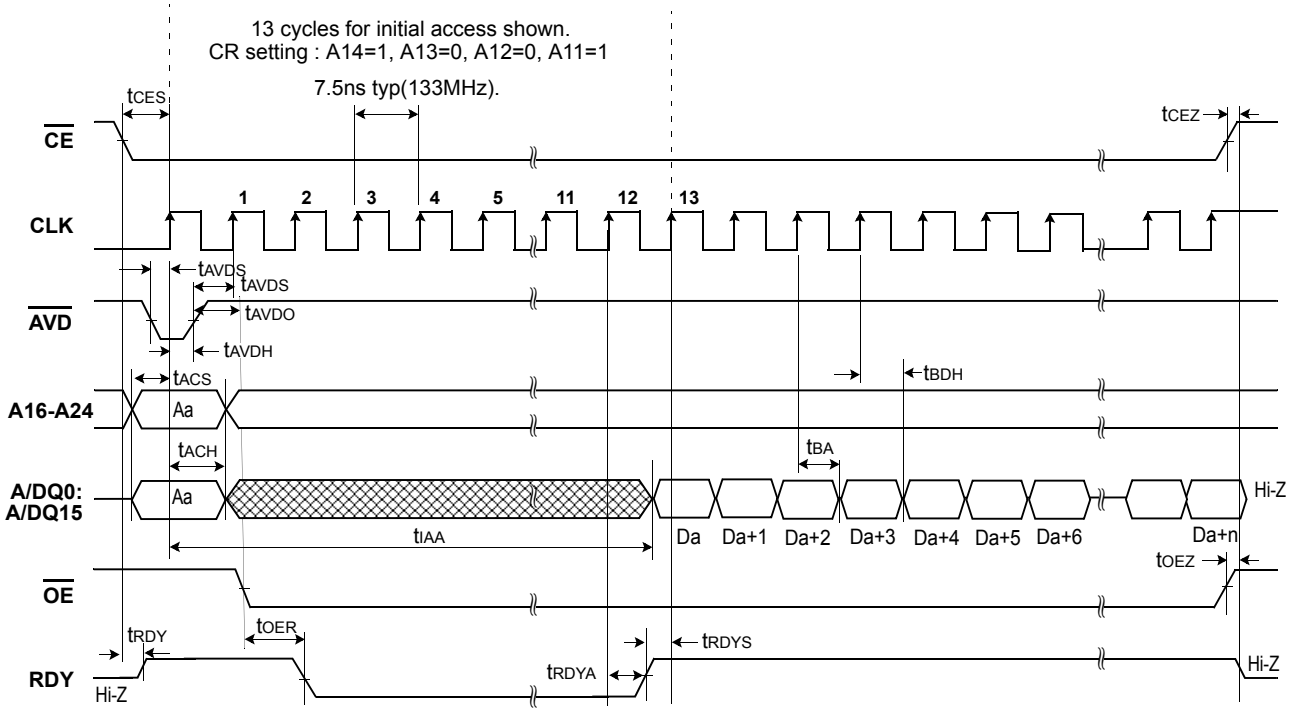


Figure 4. Continuous Burst Mode Read (133 MHz)

NOTE : In order to avoid a bus conflict the $\overline{OE}$ signal is enabled on the next rising edge after $\overline{AVD}$ is going high.

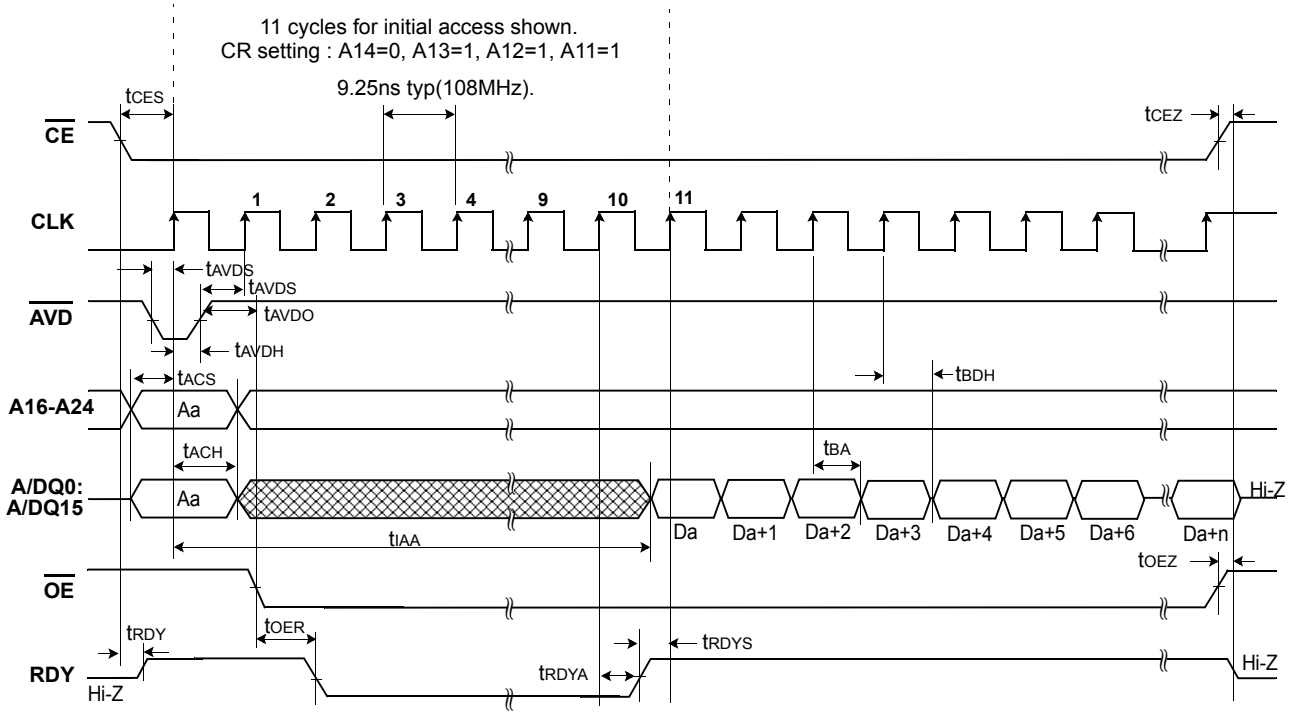


Figure 5. Continuous Burst Mode Read (108 MHz)

NOTE: In order to avoid a bus conflict the $\overline{OE}$ signal is enabled on the next rising edge after $\overline{AVD}$ is going high.

SWITCHING WAVEFORMS

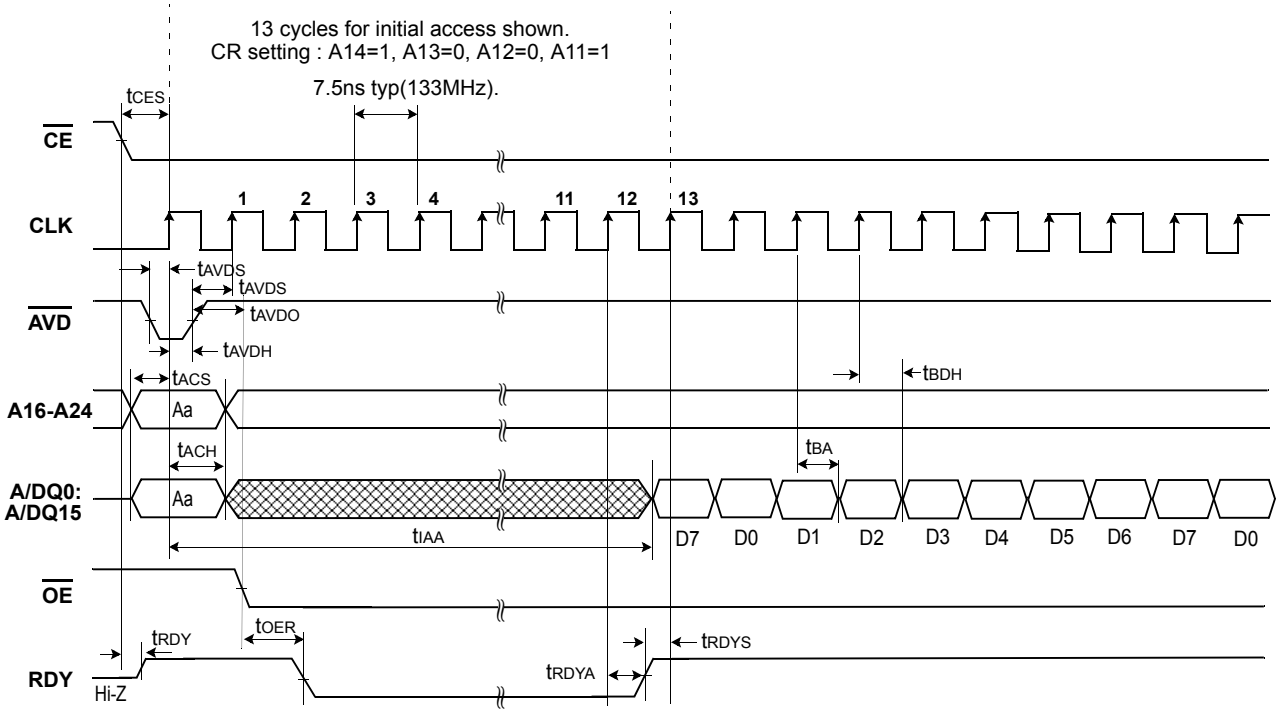


Figure 6. 8 word Linear Burst Mode with Wrap Around (133 MHz)

NOTE : In order to avoid a bus conflict the $\overline{OE}$ signal is enabled on the next rising edge after $\overline{AVD}$ is going high.

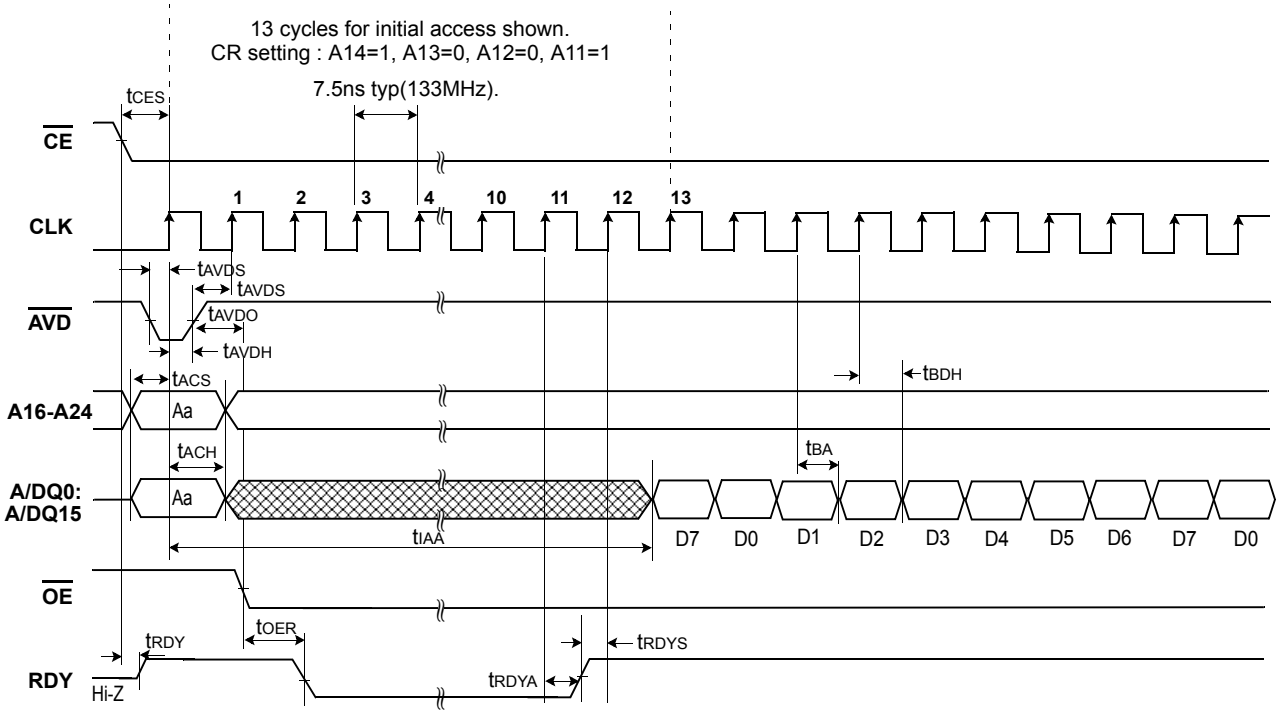


Figure 7. 8 word Linear Burst with RDY Set One Cycle Before Data (Wrap Around Mode, CR setting : A18=1)

NOTE : In order to avoid a bus conflict the $\overline{OE}$ signal is enabled on the next rising edge after $\overline{AVD}$ is going high.

SWITCHING WAVEFORMS

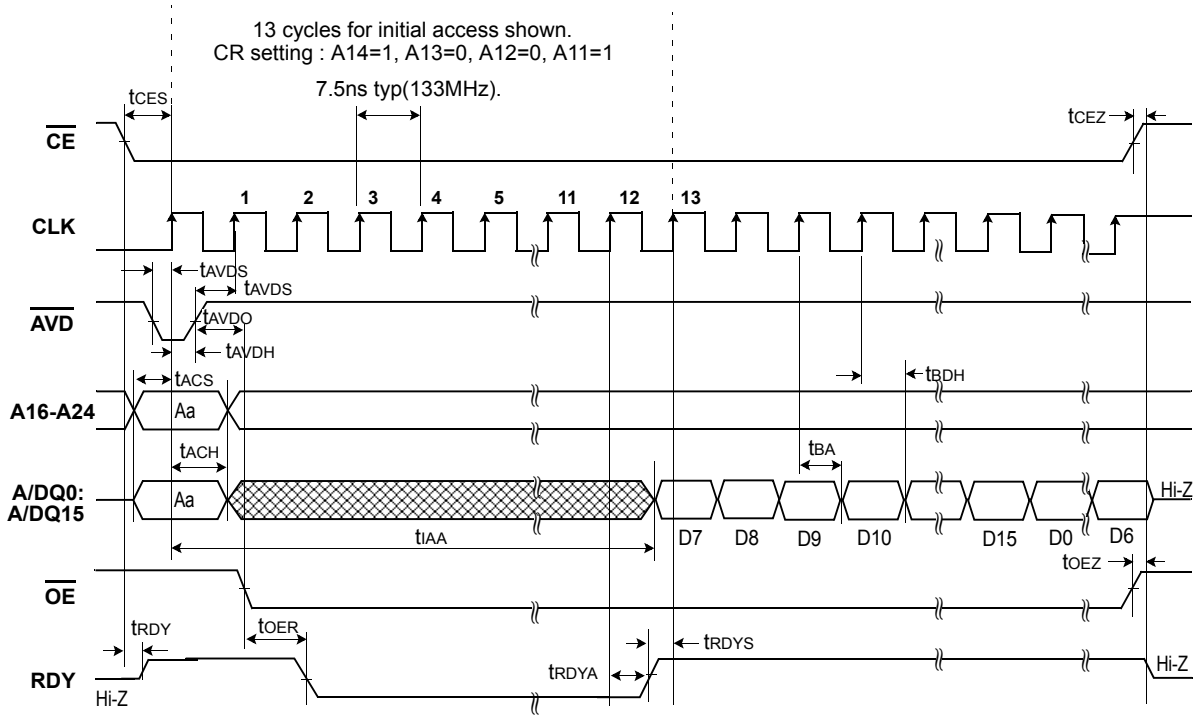


Figure 8. 16 word Linear Burst Mode with Wrap Around (133Mhz)

NOTE: In order to avoid a bus conflict the $\overline{OE}$ signal is enabled on the next rising edge after $\overline{AVD}$ is going high.

13.2 Asynchronous Read

Parameter		Symbol	All speed		Unit
			Min	Max	
Access Time from $\overline{CE}$ Low		t_{CE}	-	100	ns
Asynchronous Access Time		t_{AA}	-	100	ns
$\overline{AVD}$ Low time		t_{AVDP}	12	-	ns
Address Setup Time to rising Edge of AVD		t_{AAVDS}	5	-	ns
Address Hold Time from Rising Edge of AVD		t_{AAVDH}	2	-	ns
Output Enable to Output Valid		t_{OE}	-	15	ns
Output Enable Hold Time	Read	t_{OEH}	0	-	ns
	Toggle and $\overline{Data}$ Polling		10	-	ns
Output Disable to High Z*		t_{OEZ}	-	9	ns

NOTE: Not 100% tested.

SWITCHING WAVEFORMS
Asynchronous Mode Read (tCE)

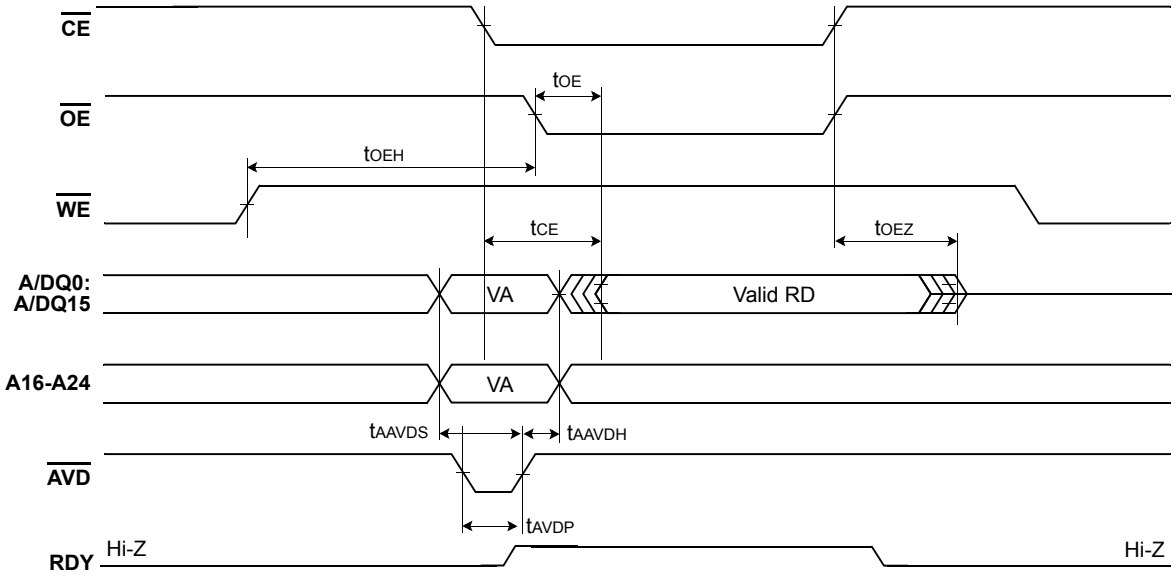
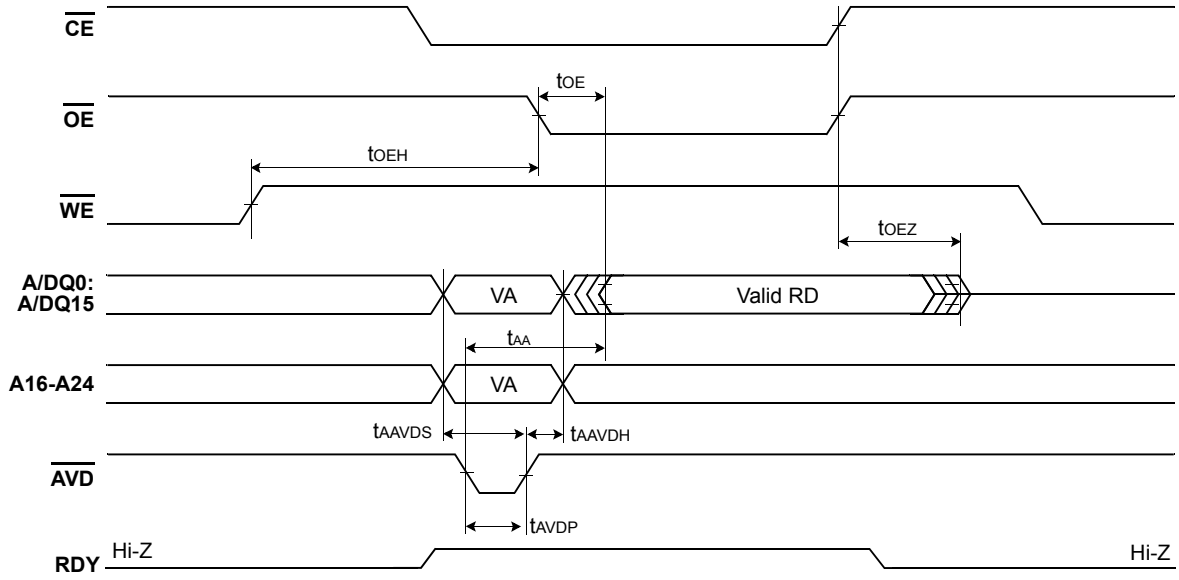


Figure 9. Asynchronous Mode Read (tCE)

NOTE : VA=Valid Read Address, RD=Read Data.
Asynchronous mode may not support read following four sequential invalid read condition within 200ns.

Asynchronous Mode Read (tAA)

Case 1 : Valid Address Transition occurs before $\overline{AVD}$ is driven to Low



Case 2 : Valid Address Transition occurs after $\overline{AVD}$ is driven to Low

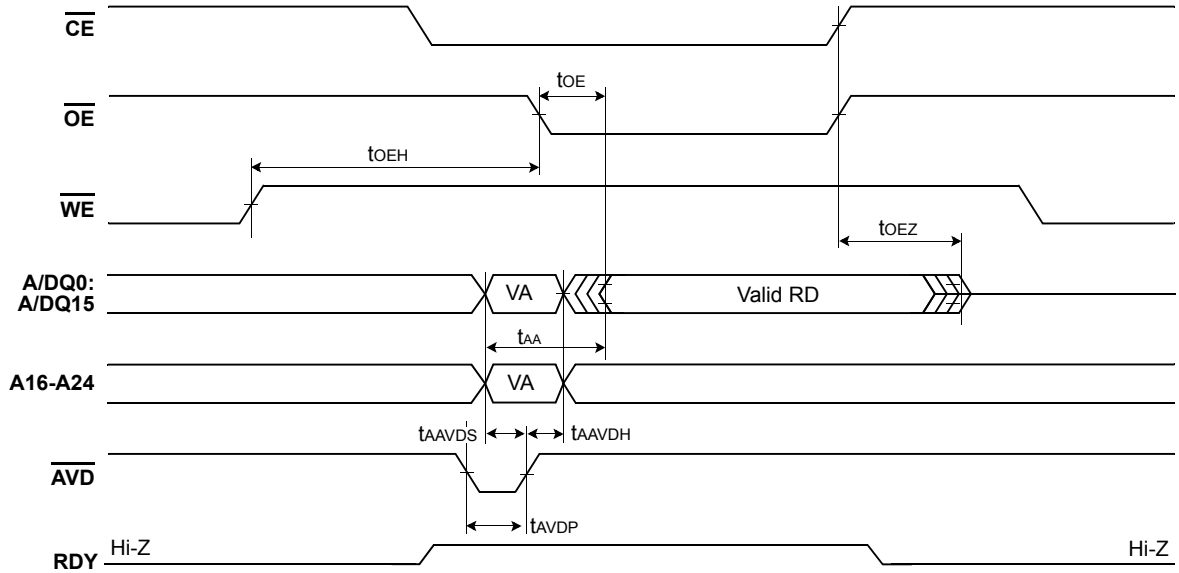


Figure 10. Asynchronous Mode Read (tAA)

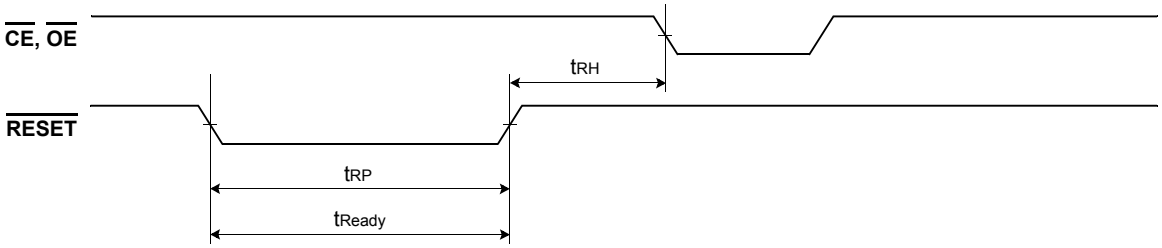
NOTE :
1) VA=Valid Read Address, RD=Read Data.
2) Asynchronous mode may not support read following four sequential invalid read condition within 200ns.

13.3 Hardware Reset($\overline{\text{RESET}}$)

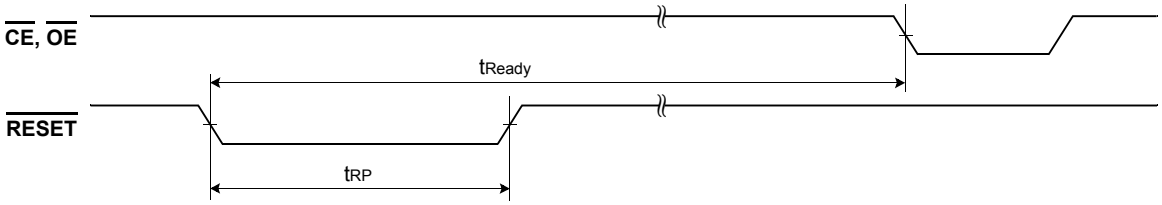
Parameter	Symbol	All Speed Options		Unit
		Min	Max	
$\overline{\text{RESET}}$ Pin Low(During Internal Routines) to Read Mode*	t_{Ready}	-	20	μs
$\overline{\text{RESET}}$ Pin Low(NOT During Internal Routines) to Read Mode*	t_{Ready}	-	500	ns
$\overline{\text{RESET}}$ Pulse Width	t_{RP}	200	-	ns
Reset High Time Before Read*	t_{RH}	200	-	ns

NOTE : Not 100% tested.

SWITCHING WAVEFORMS



Reset Timings NOT during Internal Routines



Reset Timings during Internal Routines

Figure 11. Reset Timings

13.4 Erase/Program Operation

Parameter	Symbol	All speed options			Unit
		Min	Typ	Max	
$\overline{WE}$ Cycle Time[1]	t_{WC}	75	-	-	ns
Address Setup Time	t_{AS}	5	-	-	ns
Address Hold Time	t_{AH}	2	-	-	ns
$\overline{AVD}$ Low Time	t_{AVDP}	12	-	-	ns
Data Setup Time	t_{DS}	30	-	-	ns
Data Hold Time	t_{DH}	0	-	-	ns
Read Recovery Time Before Write	t_{GHWL}	0	-	-	ns
$\overline{CE}$ Setup Time	t_{CS}	0	-	-	ns
$\overline{CE}$ Hold Time	t_{CH}	0	-	-	ns
$\overline{WE}$ High to $\overline{AVD}$ low	t_{WEA}	30	-	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	30	-	-	ns
$\overline{WE}$ Pulse Width High	t_{WPH}	45	-	-	ns
Latency Between Read and Write Operations	$t_{SR/W}$	0	-	-	ns
Word Programming Operation [2]	t_{PGM}	-	80	-	µs
Single word Buffer Program [2]	t_{PGM_BP}	-	250	-	µs
512-word Buffer Program [4]	t_{PGM_BP}	-	716.8	-	µs
Accelerated Programming Operation [3]	t_{ACCPGM}	-	80	-	µs
Accelerated Single word Buffer Program [3]	t_{ACCPGM_BP}	-	0.7	-	µs
Accelerated 512-word Buffer Program [4]	t_{ACCPGM_BP}	-	358.4	-	µs
Block Erase Operation (64KW block)	t_{BERS}	-	0.6	-	sec
Blank check Operation (64KW block)	t_{BLANK}	-	7	-	ms
VPP Rise and Fall Time	t_{VPP}	500	-	-	ns
VPP Setup Time (During Accelerated Programming)	t_{VPS}	1	-	-	µs

NOTE :
1) Not 100% tested.
2) Internal programming algorithm is optimized for Buffer Program, so Normal word programming or Single word Buffer Program use Buffer Program algorithm.
3) Internal programming algorithm for supporting Accelerated mode uses a method to double the number of words programmed simultaneously.
4) Typical 512-word Buffer Program time pays due regard to that Each program data pattern ("11", "10". "01", "00") has a same portion in 512-word Buffer.

13.5 Erase/Program Performance

Parameter		Limits			Unit	Comments
		Min.	Typ.	Max.		
Block Erase Time	64 Kword	-	0.6	3.0	sec	Includes 00h programming prior to erasure
	16 Kword	-	0.3	1.5		
Chip Erase Time (3)		-	307.8	1539		
Accelerated Block Erase Time	64 Kword	-	0.4	3.0		
	16 Kword	-	0.2	1.5		
Accelerated Chip Erase Time (3)		-	205.2	1026		
Word Programming Time		-	80	550	µs / word	Excludes system level over-head
512-word Buffer Programming Time		-	1.4	7		
Accelerated Word Programming Time		-	80	550		
Accelerated 512-word Buffer Programming Time		-	0.7	3.5		
Chip Buffer Programming Time		-	46.9	234.5	sec	
Accelerated Buffer Chip Programming Time		-	23.4	117		
Blank check time		-	7	-	milli sec	

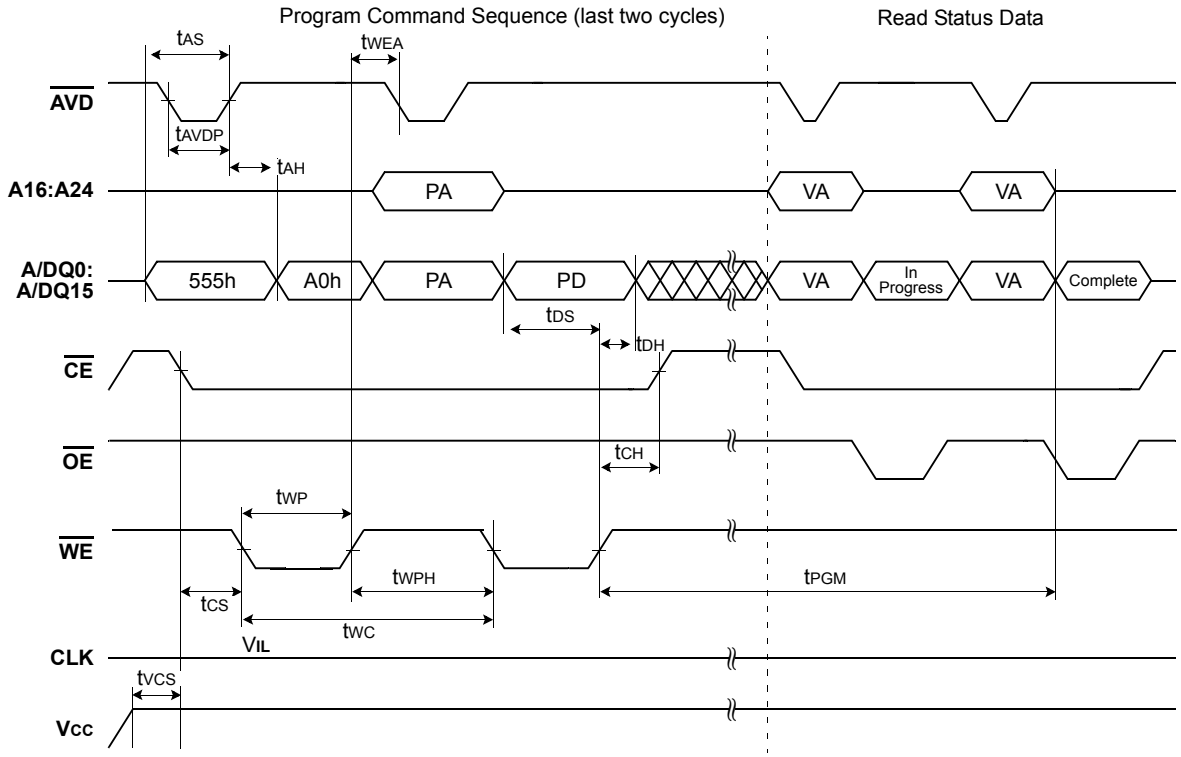
NOTE :

1)25°C, VCC = 1.8V, 100,000 cycles, typical pattern.

2) System-level overhead is defined as the time required to execute the two or four bus cycle command necessary to program each word.

3) Chip Erase time & Accel. Chip Erase time for boot block part

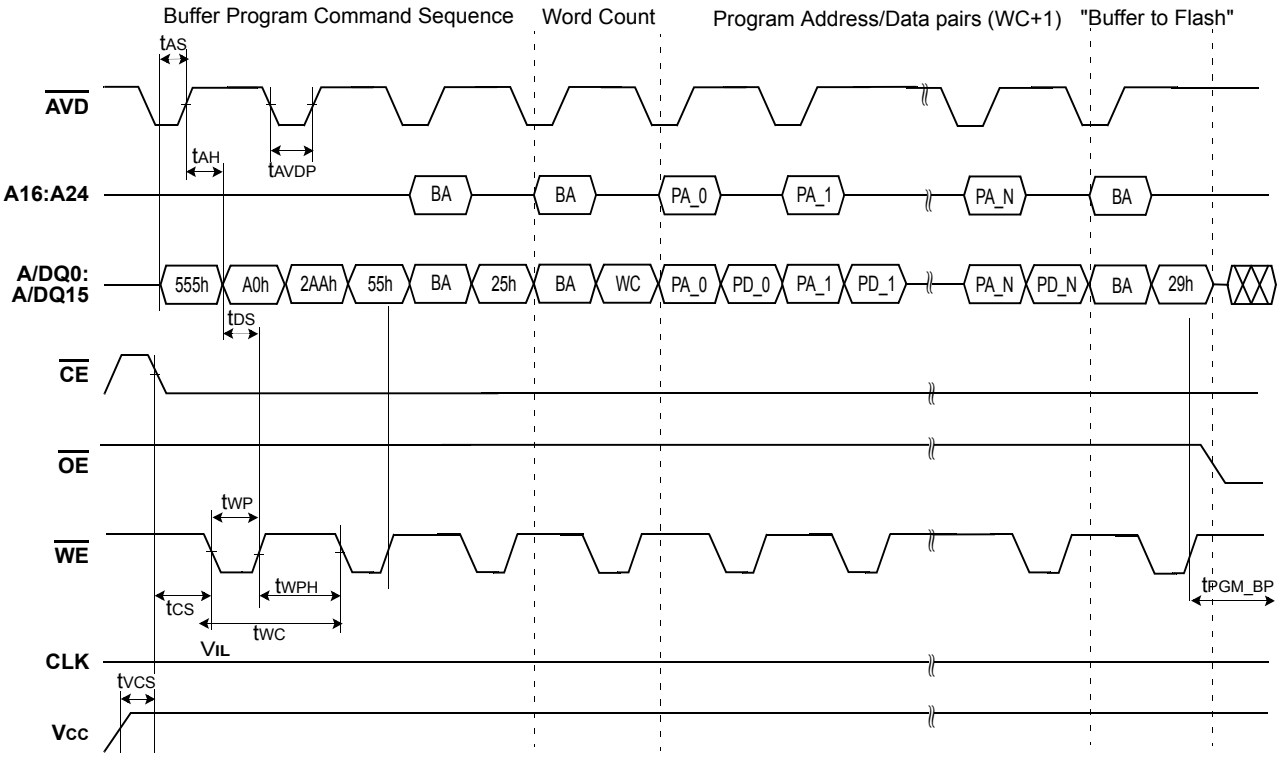
SWITCHING WAVEFORMS
Program Operations



NOTE :
1) PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
2) “In progress” and “complete” refer to status of program operation.
3) A16–A24 are don’t care during command sequence unlock cycles.
4) Status reads in this figure is asynchronous read, but status read in synchronous mode is also supported.

Figure 12. Program Operation Timing

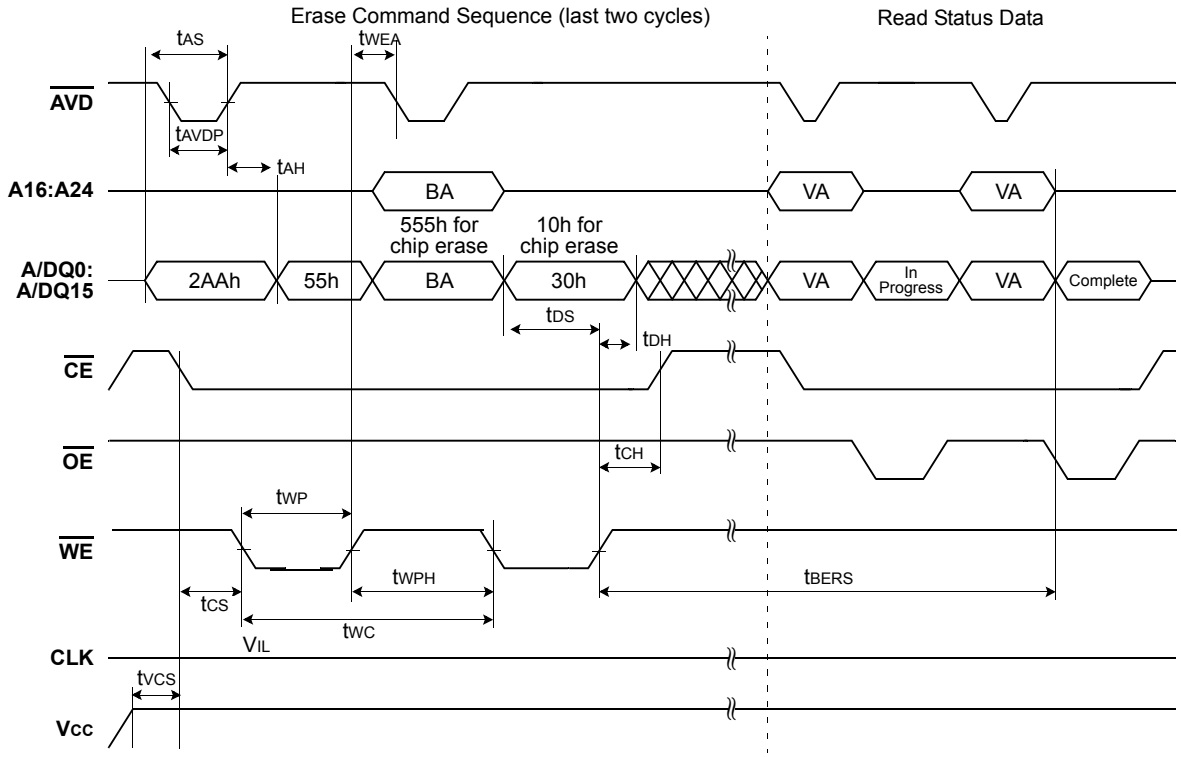
SWITCHING WAVEFORMS
Buffer Program Operations



NOTE :
1) BA = Block Address, WC = Word Count, PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
2) Sequential PA_1, PA_2, ... , PA_N must have same address bits A24(max.) ~ A9 as PA_0 entered firstly
3) The number of Program/Data pairs entered must be same as WC+1 because WC = N.
4) “In progress” and “complete” refer to status of program operation.
5) A16–A24 are don’t care during command sequence unlock cycles.
6) Status reads in this figure is asynchronous read, but status read in synchronous mode is also supported.

Figure 13. Buffer Program Operation Timing

SWITCHING WAVEFORMS
Erase Operation



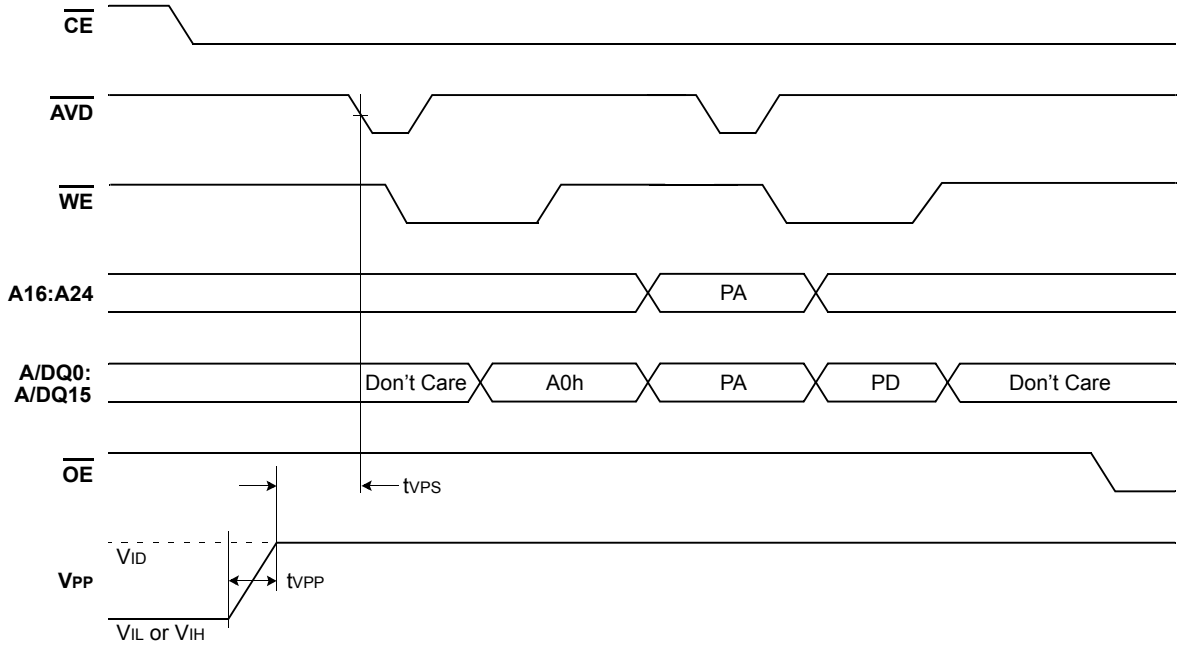
NOTE :

1) BA is the block address for Block Erase.
2) Address bits A16–A24 are don't cares during unlock cycles in the command sequence.
3) Status reads in this figure is asynchronous read, but status read in synchronous mode is also supported.

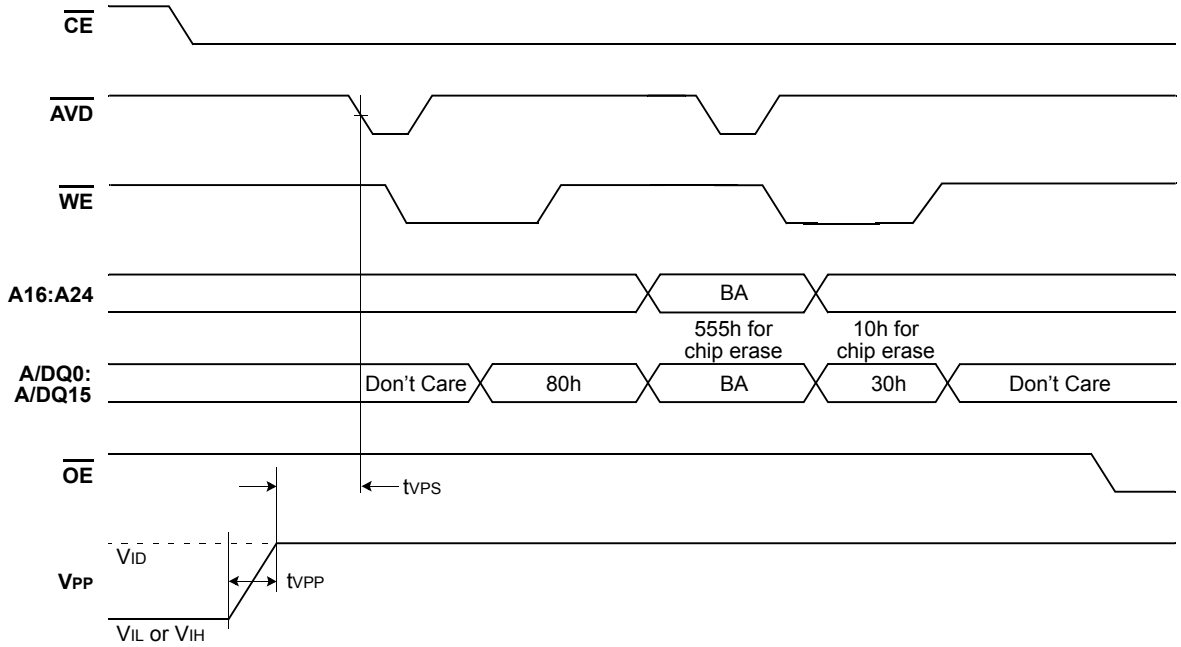
Figure 14. ChIp/Block Erase Operations

SWITCHING WAVEFORMS

Unlock Bypass Program Operations(Accelerated Program)



Unlock Bypass Block Erase Operations



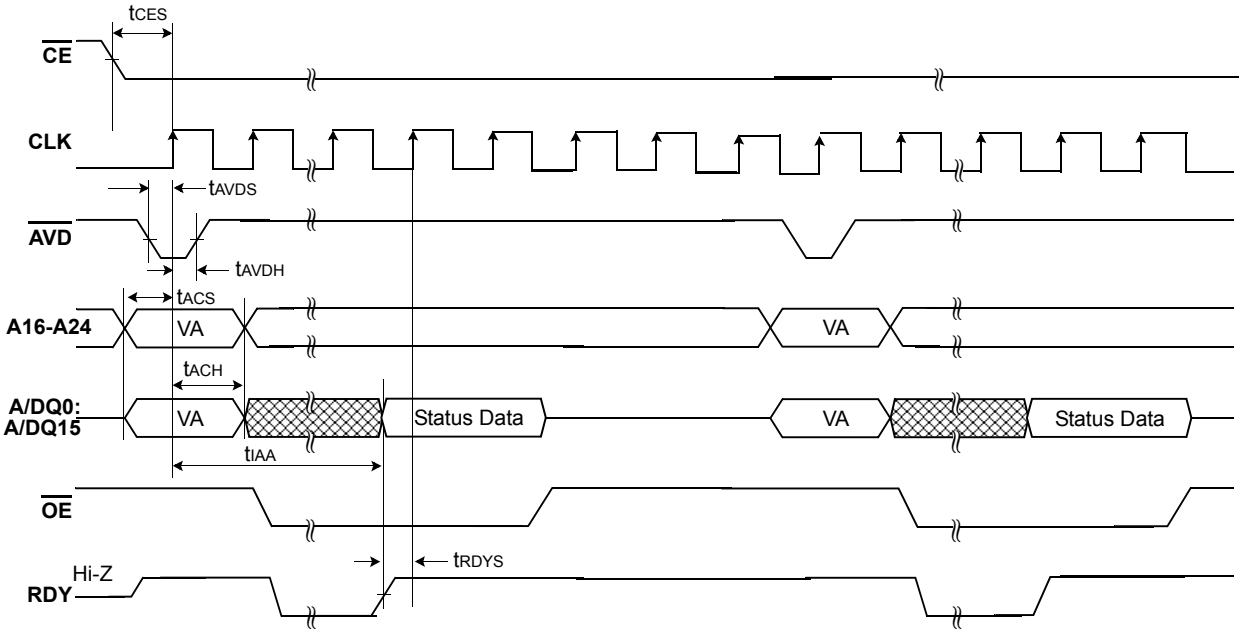
NOTE :

1) VPP can be left high for subsequent programming pulses.
2) Use setup and hold times from conventional program operations.
3) Conventional Program/Erase commands as well as Unlock Bypass Program/Erase commands can be used when the VID is applied to Vpp.

Figure 15. Unlock Bypass Operation Timings

SWITCHING WAVEFORMS

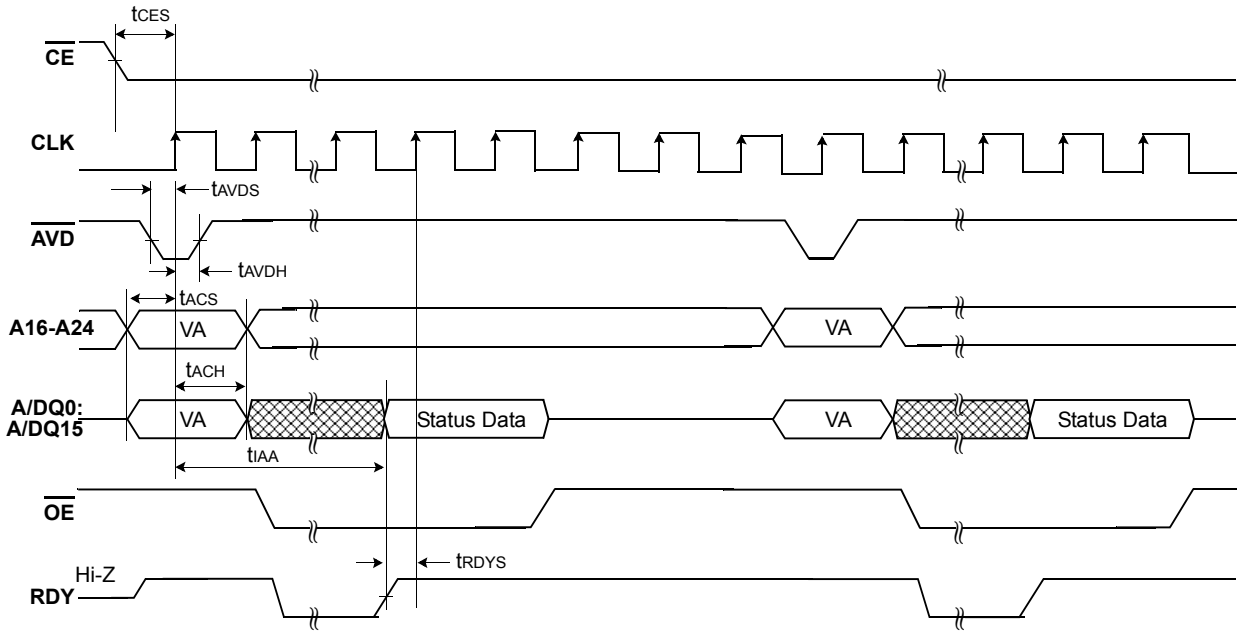
Data Polling Operations



NOTE :
1) VA = Valid Address. When the Internal Routine operation is complete, and Data Polling will output true data.

Figure 16. Data Polling Timings (During Internal Routine)

Toggle Bit Operations



NOTE :
1) VA = Valid Address. When the Internal Routine operation is complete, the toggle bits will stop toggling.

Figure 17. Toggle Bit Timings(During Internal Routine)

SWITCHING WAVEFORMS
Read While Write Operations

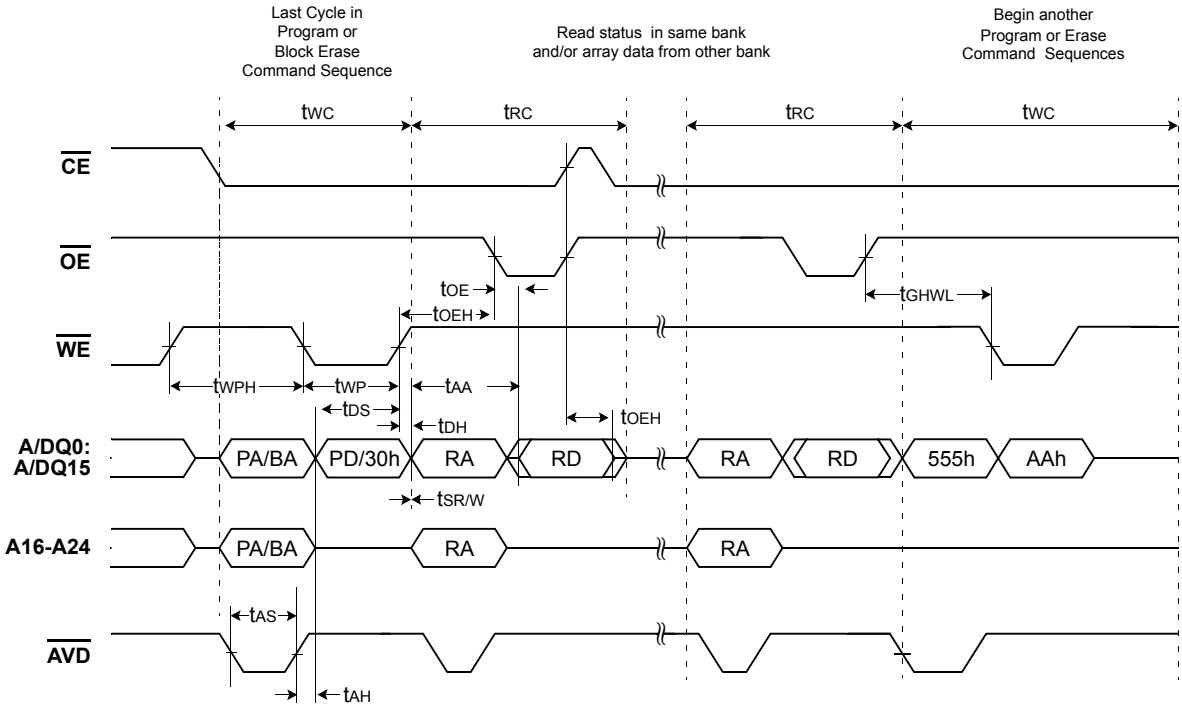


Figure 18. Read While Write Operation

NOTE :
Breakpoints in waveforms indicate that system may alternately read array data from the “non-busy bank” and checking the status of the program or erase operation in the “busy” bank.

14.0 Crossing of First Word Boundary in Burst Read Mode

The additional clock insertion for word boundary is needed only at the first crossing of word boundary. This means that no additional clock cycle is needed from 2nd word boundary crossing to the end of continuous burst read. Also, the number of additional clock cycle for the first word boundary can vary from zero to thirteen cycles, and the exact number of additional clock cycle depends on the starting address of burst read and programmable wait state settings.

For example, if the starting address is 16N+15 (the worst case) and programmable wait state setting(A14~A11) is "0011" (which means data is valid on the 7th active CLK edge after AVD transition to Vih), six additional clock cycle is needed.

Similarly, if the starting address is 16N+15 (the worst case) and programmable wait state setting(A14~A11) is "0010" (which means data is valid on the 6th active CLK edge after AVD transition to Vih), five additional clock cycle is needed.

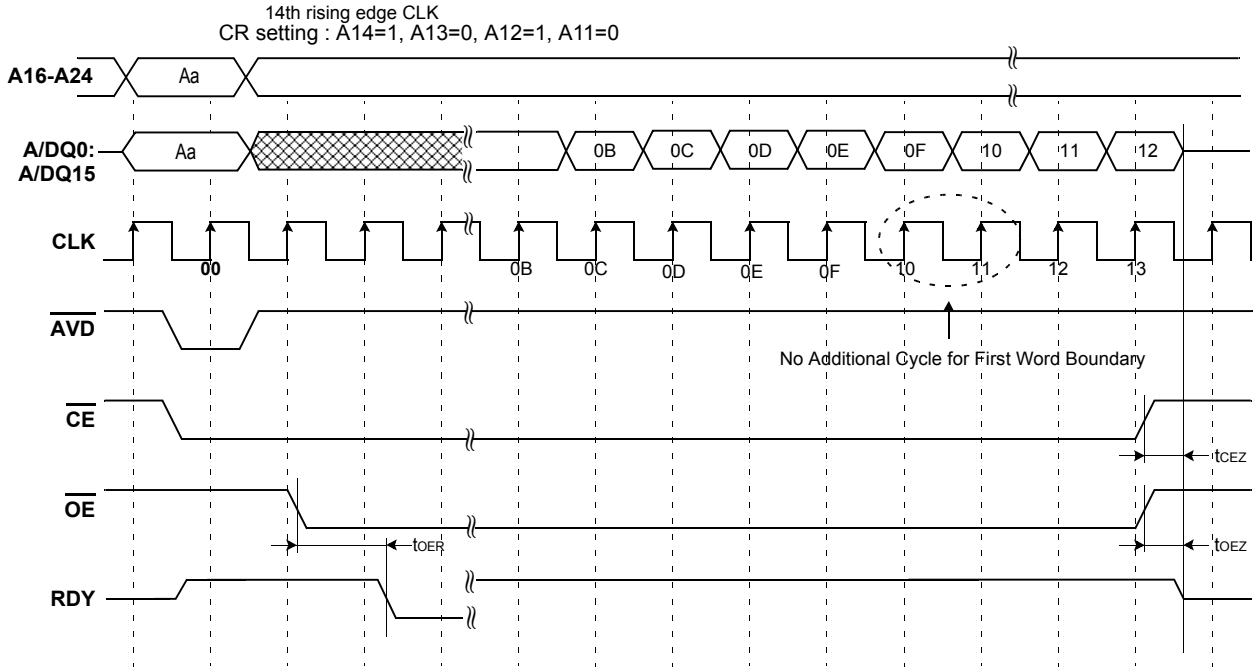
Below table shows the starting address vs. additional clock cycles for first word boundary.

Starting Address vs. Additional Clock Cycles for first word boundary

Srarting Address Group for Burst Read	The Residue of (Address/16)	LSB Bits of Address	Additional Clock Cycles for First Word Boundary [1]				
			A14~A11 "0000" Valid data : 4th CLK	A14~A11 "0001" Valid data : 5th CLK	A14~A11 "0010" Valid data : 6th CLK	...	A14~A11 "1010" Valid data : 14th CLK
16N	0	0000	0 cycle	0 cycle	0 cycle	...	0 cycle
16N+1	1	0001	0 cycle	0 cycle	0 cycle	...	0 cycle
16N+2	2	0010	0 cycle	0 cycle	0 cycle	...	0 cycle
16N+3	3	0011	0 cycle	0 cycle	0 cycle	...	1 cycle
16N+4	4	0100	0 cycle	0 cycle	0 cycle	...	2 cycle
16N+5	5	0101	0 cycle	0 cycle	0 cycle	...	3 cycle
16N+6	6	0110	0 cycle	0 cycle	0 cycle	...	4 cycle
16N+7	7	0111	0 cycle	0 cycle	0 cycle	...	5 cycle
16N+8	8	1000	0 cycle	0 cycle	0 cycle	...	6 cycle
16N+9	9	1001	0 cycle	0 cycle	0 cycle	...	7 cycle
16N+10	10	1010	0 cycle	0 cycle	0 cycle	...	8 cycle
16N+11	11	1011	0 cycle	0 cycle	1 cycle	...	9 cycle
16N+12	12	1100	0 cycle	1 cycle	2 cycle	...	10 cycle
16N+13	13	1101	1 cycle	2 cycle	3 cycle	...	11 cycle
16N+14	14	1110	2 cycle	3 cycle	4 cycle	...	12 cycle
16N+15	15	1111	3 cycle	4 cycle	5 cycle	...	13 cycle

NOTE :
1) Address bit A14~A11 means the programmable wait state on burst mode configuration register. Refer to Table 10.

Case 1 : Start from "16N" address group

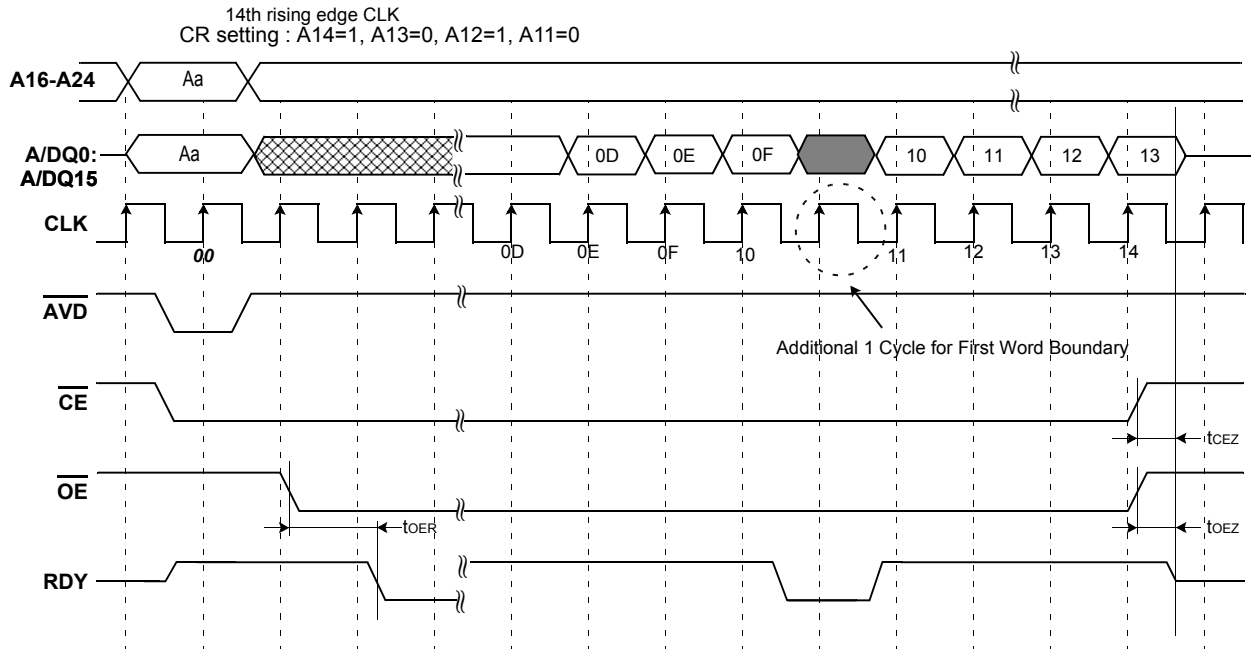


NOTE :

1) Address boundary occurs every 16 words beginning at address 000000FH , 000001FH , 000002FH , etc.
2) Address 000000H is also a boundary crossing.
3) No additional clock cycles are needed except for 1st boundary crossing.

Figure 19. Crossing of first word boundary in burst read mode.

Case 2 : Start from "16N+3" address group

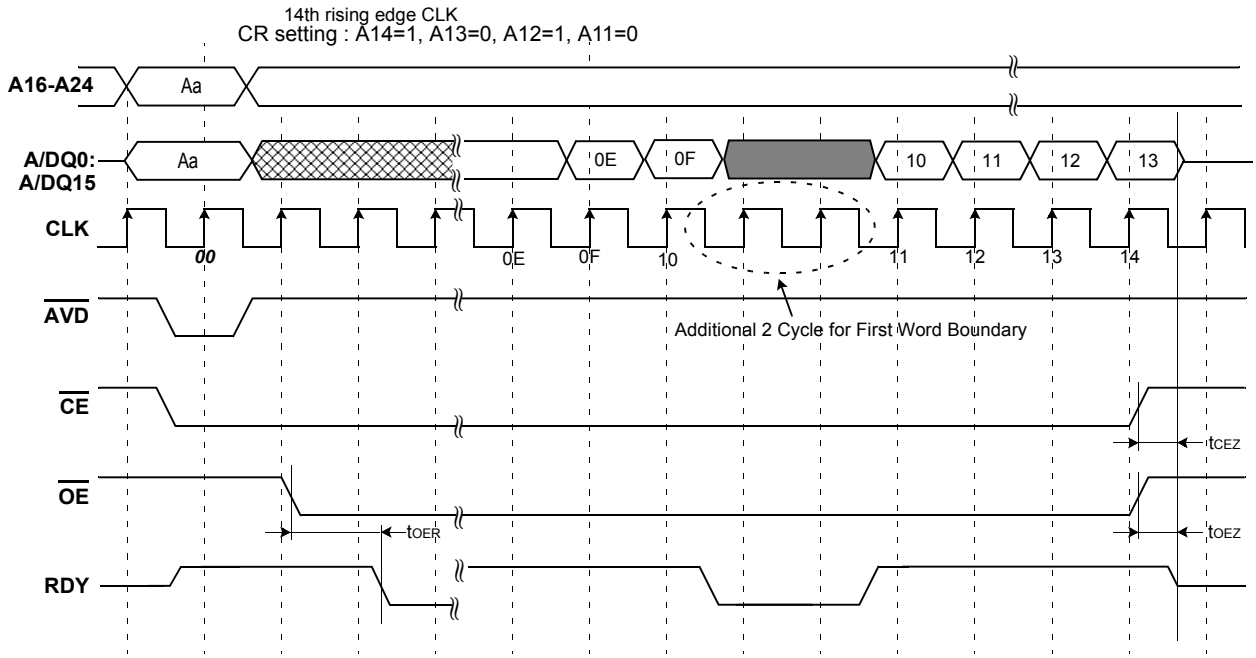


NOTE :

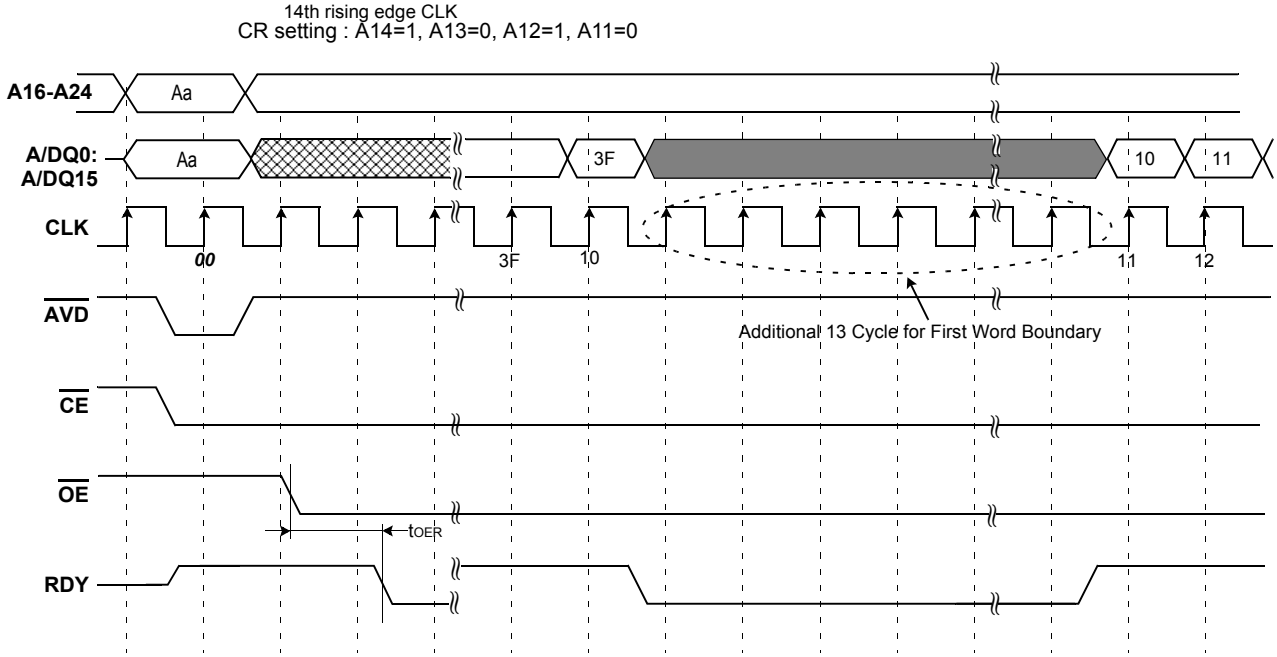
1) Address boundary occurs every 16 words beginning at address 000000FH , 000001FH , 000002FH , etc.
2) Address 000000H is also a boundary crossing.
3) No additional clock cycles are needed except for 1st boundary crossing.

Figure 20. Crossing of first word boundary in burst read mode.

Case3 : Start from "16N+4" address group



Case 4 : Start from "16N+15" address group



NOTE :

1) Address boundary occurs every 16 words beginning at address 000000FH , 000001FH , 000002FH , etc.
2) Address 000000H is also a boundary crossing.
3) No additional clock cycles are needed except for 1st boundary crossing.

Figure 21. Crossing of first word boundary in burst read mode.

[Table 16] Top Boot Block Address Table

Bank	Block	Block Size	(x16) Address Range
Bank 0	BA514	16 kwords	1FFC000h-1FFFFFFh
	BA513	16 kwords	1FF8000h-1FFBFFFh
	BA512	16 kwords	1FF4000h-1FF7FFFh
	BA511	16 kwords	1FF0000h-1FF3FFFh
	BA510	64 kwords	1FE0000h-1FEFFFFh
	BA509	64 kwords	1FD0000h-1FDFFFFh
	BA508	64 kwords	1FC0000h-1FCFFFFh
	BA507	64 kwords	1FB0000h-1FBFFFFh
	BA506	64 kwords	1FA0000h-1FAFFFFh
	BA505	64 kwords	1F90000h-1F9FFFFh
	BA504	64 kwords	1F80000h-1F8FFFFh
	BA503	64 kwords	1F70000h-1F7FFFFh
	BA502	64 kwords	1F60000h-1F6FFFFh
	BA501	64 kwords	1F50000h-1F5FFFFh
	BA500	64 kwords	1F40000h-1F4FFFFh
	BA499	64 kwords	1F30000h-1F3FFFFh
	BA498	64 kwords	1F20000h-1F2FFFFh
	BA497	64 kwords	1F10000h-1F1FFFFh
	BA496	64 kwords	1F00000h-1F0FFFFh
	BA495	64 kwords	1EF0000h-1EFFFFFh
	BA494	64 kwords	1EE0000h-1EEFFFFh
	BA493	64 kwords	1ED0000h-1EDFFFFh
	BA492	64 kwords	1EC0000h-1ECFFFFh
	BA491	64 kwords	1EB0000h-1EBFFFFh
	BA490	64 kwords	1EA0000h-1EAFFFFh
	BA489	64 kwords	1E90000h-1E9FFFFh
	BA488	64 kwords	1E80000h-1E8FFFFh
	BA487	64 kwords	1E70000h-1E7FFFFh
	BA486	64 kwords	1E60000h-1E6FFFFh
	BA485	64 kwords	1E50000h-1E5FFFFh
	BA484	64 kwords	1E40000h-1E4FFFFh
	BA483	64 kwords	1E30000h-1E3FFFFh
	BA482	64 kwords	1E20000h-1E2FFFFh
	BA481	64 kwords	1E10000h-1E1FFFFh
	BA480	64 kwords	1E00000h-1E0FFFFh
Bank 1	BA479	64 kwords	1DF0000h-1DFFFFFh
	BA478	64 kwords	1DE0000h-1DEFFFFh
	BA477	64 kwords	1DD0000h-1DDFFFFh
	BA476	64 kwords	1DC0000h-1DCFFFFh
	BA475	64 kwords	1DB0000h-1DBFFFFh
	BA474	64 kwords	1DA0000h-1DAFFFFh
	BA473	64 kwords	1D90000h-1D9FFFFh
	BA472	64 kwords	1D80000h-1D8FFFFh
	BA471	64 kwords	1D70000h-1D7FFFFh
	BA470	64 kwords	1D60000h-1D6FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 1	BA469	64 kwords	1D50000h-1D5FFFFh
	BA468	64 kwords	1D40000h-1D4FFFFh
	BA467	64 kwords	1D30000h-1D3FFFFh
	BA466	64 kwords	1D20000h-1D2FFFFh
	BA465	64 kwords	1D10000h-1D1FFFFh
	BA464	64 kwords	1D00000h-1D0FFFFh
	BA463	64 kwords	1CF0000h-1CFFFFFh
	BA462	64 kwords	1CE0000h-1CEFFFFh
	BA461	64 kwords	1CD0000h-1CDFFFFh
	BA460	64 kwords	1CC0000h-1CCFFFFh
	BA459	64 kwords	1CB0000h-1CBFFFFh
	BA458	64 kwords	1CA0000h-1CAFFFFh
	BA457	64 kwords	1C90000h-1C9FFFFh
	BA456	64 kwords	1C80000h-1C8FFFFh
	BA455	64 kwords	1C70000h-1C7FFFFh
	BA454	64 kwords	1C60000h-1C6FFFFh
	BA453	64 kwords	1C50000h-1C5FFFFh
	BA452	64 kwords	1C40000h-1C4FFFFh
	BA451	64 kwords	1C30000h-1C3FFFFh
	BA450	64 kwords	1C20000h-1C2FFFFh
	BA449	64 kwords	1C10000h-1C1FFFFh
	BA448	64 kwords	1C00000h-1C0FFFFh
Bank 2	BA447	64 kwords	1BF0000h-1BFFFFFh
	BA446	64 kwords	1BE0000h-1BEFFFFh
	BA445	64 kwords	1BD0000h-1BDFFFFh
	BA444	64 kwords	1BC0000h-1BCFFFFh
	BA443	64 kwords	1BB0000h-1BBFFFFh
	BA442	64 kwords	1BA0000h-1BAFFFFh
	BA441	64 kwords	1B90000h-1B9FFFFh
	BA440	64 kwords	1B80000h-1B8FFFFh
	BA439	64 kwords	1B70000h-1B7FFFFh
	BA438	64 kwords	1B60000h-1B6FFFFh
	BA437	64 kwords	1B50000h-1B5FFFFh
	BA436	64 kwords	1B40000h-1B4FFFFh
	BA435	64 kwords	1B30000h-1B3FFFFh
	BA434	64 kwords	1B20000h-1B2FFFFh
	BA433	64 kwords	1B10000h-1B1FFFFh
	BA432	64 kwords	1B00000h-1B0FFFFh
	BA431	64 kwords	1AF0000h-1AFFFFFh
	BA430	64 kwords	1AE0000h-1AEFFFFh
	BA429	64 kwords	1AD0000h-1ADFFFFh
	BA428	64 kwords	1AC0000h-1ACFFFFh
	BA427	64 kwords	1AB0000h-1ABFFFFh
	BA426	64 kwords	1AA0000h-1AAFFFFh
	BA425	64 kwords	1A90000h-1A9FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 2	BA424	64 kwords	1A80000h-1A8FFFFh
	BA423	64 kwords	1A70000h-1A7FFFFh
	BA422	64 kwords	1A60000h-1A6FFFFh
	BA421	64 kwords	1A50000h-1A5FFFFh
	BA420	64 kwords	1A40000h-1A4FFFFh
	BA419	64 kwords	1A30000h-1A3FFFFh
	BA418	64 kwords	1A20000h-1A2FFFFh
	BA417	64 kwords	1A10000h-1A1FFFFh
	BA416	64 kwords	1A00000h-1A0FFFFh
Bank 3	BA415	64 kwords	19F0000h-19FFFFFh
	BA414	64 kwords	19E0000h-19EFFFFh
	BA413	64 kwords	19D0000h-19DFFFFh
	BA412	64 kwords	19C0000h-19CFFFFh
	BA411	64 kwords	19B0000h-19BFFFFh
	BA410	64 kwords	19A0000h-19AFFFFh
	BA409	64 kwords	1990000h-199FFFFh
	BA408	64 kwords	1980000h-198FFFFh
	BA407	64 kwords	1970000h-197FFFFh
	BA406	64 kwords	1960000h-196FFFFh
	BA405	64 kwords	1950000h-195FFFFh
	BA404	64 kwords	1940000h-194FFFFh
	BA403	64 kwords	1930000h-193FFFFh
	BA402	64 kwords	1920000h-192FFFFh
	BA401	64 kwords	1910000h-191FFFFh
	BA400	64 kwords	1900000h-190FFFFh
	BA399	64 kwords	18F0000h-18FFFFFh
	BA398	64 kwords	18E0000h-18EFFFFh
	BA397	64 kwords	18D0000h-18DFFFFh
	BA396	64 kwords	18C0000h-18CFFFFh
	BA395	64 kwords	18B0000h-18BFFFFh
	BA394	64 kwords	18A0000h-18AFFFFh
	BA393	64 kwords	1890000h-189FFFFh
	BA392	64 kwords	1880000h-188FFFFh
	BA391	64 kwords	1870000h-187FFFFh
	BA390	64 kwords	1860000h-186FFFFh
	BA389	64 kwords	1850000h-185FFFFh
	BA388	64 kwords	1840000h-184FFFFh
	BA387	64 kwords	1830000h-183FFFFh
	BA386	64 kwords	1820000h-182FFFFh
	BA385	64 kwords	1810000h-181FFFFh
	BA384	64 kwords	1800000h-180FFFFh
Bank 4	BA383	64 kwords	17F0000h-17FFFFFh
	BA382	64 kwords	17E0000h-17EFFFFh
	BA381	64 kwords	17D0000h-17DFFFFh
	BA380	64 kwords	17C0000h-17CFFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 4	BA379	64 kwords	17B0000h-17BFFFFh
	BA378	64 kwords	17A0000h-17AFFFFh
	BA377	64 kwords	1790000h-179FFFFh
	BA376	64 kwords	1780000h-178FFFFh
	BA375	64 kwords	1770000h-177FFFFh
	BA374	64 kwords	1760000h-176FFFFh
	BA373	64 kwords	1750000h-175FFFFh
	BA372	64 kwords	1740000h-174FFFFh
	BA371	64 kwords	1730000h-173FFFFh
	BA370	64 kwords	1720000h-172FFFFh
	BA369	64 kwords	1710000h-171FFFFh
	BA368	64 kwords	1700000h-170FFFFh
	BA367	64 kwords	16F0000h-16FFFFFh
	BA366	64 kwords	16E0000h-16EFFFFh
	BA365	64 kwords	16D0000h-16DFFFFh
	BA364	64 kwords	16C0000h-16CFFFFh
	BA363	64 kwords	16B0000h-16BFFFFh
	BA362	64 kwords	16A0000h-16AFFFFh
	BA361	64 kwords	1690000h-169FFFFh
	BA360	64 kwords	1680000h-168FFFFh
	BA359	64 kwords	1670000h-167FFFFh
	BA358	64 kwords	1660000h-166FFFFh
	BA357	64 kwords	1650000h-165FFFFh
	BA356	64 kwords	1640000h-164FFFFh
	BA355	64 kwords	1630000h-163FFFFh
	BA354	64 kwords	1620000h-162FFFFh
	BA353	64 kwords	1610000h-161FFFFh
	BA352	64 kwords	1600000h-160FFFFh
Bank5	BA351	64 kwords	15F0000h-15FFFFFh
	BA350	64 kwords	15E0000h-15EFFFFh
	BA349	64 kwords	15D0000h-15DFFFFh
	BA348	64 kwords	15C0000h-15CFFFFh
	BA347	64 kwords	15B0000h-15BFFFFh
	BA346	64 kwords	15A0000h-15AFFFFh
	BA345	64 kwords	1590000h-159FFFFh
	BA344	64 kwords	1580000h-158FFFFh
	BA343	64 kwords	1570000h-157FFFFh
	BA342	64 kwords	1560000h-156FFFFh
	BA341	64 kwords	1550000h-155FFFFh
	BA340	64 kwords	1540000h-154FFFFh
	BA339	64 kwords	1530000h-153FFFFh
	BA338	64 kwords	1520000h-152FFFFh
	BA337	64 kwords	1510000h-151FFFFh
	BA336	64 kwords	1500000h-150FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 5	BA335	64 kwords	14F0000h-14FFFFFh
	BA334	64 kwords	14E0000h-14EFFFFh
	BA333	64 kwords	14D0000h-14DFFFFh
	BA332	64 kwords	14C0000h-14CFFFFh
	BA331	64 kwords	14B0000h-14BFFFFh
	BA330	64 kwords	14A0000h-14AFFFFh
	BA329	64 kwords	1490000h-149FFFFh
	BA328	64 kwords	1480000h-148FFFFh
	BA327	64 kwords	1470000h-147FFFFh
	BA326	64 kwords	1460000h-146FFFFh
	BA325	64 kwords	1450000h-145FFFFh
	BA324	64 kwords	1440000h-144FFFFh
	BA323	64 kwords	1430000h-143FFFFh
	BA322	64 kwords	1420000h-142FFFFh
	BA321	64 kwords	1410000h-141FFFFh
	BA320	64 kwords	1400000h-140FFFFh
Bank 6	BA319	64 kwords	13F0000h-13FFFFFh
	BA318	64 kwords	13E0000h-13EFFFFh
	BA317	64 kwords	13D0000h-13DFFFFh
	BA316	64 kwords	13C0000h-13CFFFFh
	BA315	64 kwords	13B0000h-13BFFFFh
	BA314	64 kwords	13A0000h-13AFFFFh
	BA313	64 kwords	1390000h-139FFFFh
	BA312	64 kwords	1380000h-138FFFFh
	BA311	64 kwords	1370000h-137FFFFh
	BA310	64 kwords	1360000h-136FFFFh
	BA309	64 kwords	1350000h-135FFFFh
	BA308	64 kwords	1340000h-134FFFFh
	BA307	64 kwords	1330000h-133FFFFh
	BA306	64 kwords	1320000h-132FFFFh
	BA305	64 kwords	1310000h-131FFFFh
	BA304	64 kwords	1300000h-130FFFFh
	BA303	64 kwords	12F0000h-12FFFFFh
	BA302	64 kwords	12E0000h-12EFFFFh
	BA301	64 kwords	12D0000h-12DFFFFh
	BA300	64 kwords	12C0000h-12CFFFFh
	BA299	64 kwords	12B0000h-12BFFFFh
	BA298	64 kwords	12A0000h-12AFFFFh
	BA297	64 kwords	1290000h-129FFFFh
	BA296	64 kwords	1280000h-128FFFFh
	BA295	64 kwords	1270000h-127FFFFh
	BA294	64 kwords	1260000h-126FFFFh
	BA293	64 kwords	1250000h-125FFFFh
	BA292	64 kwords	1240000h-124FFFFh
	BA291	64 kwords	1230000h-123FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 6	BA290	64 kwords	1220000h-122FFFFh
	BA289	64 kwords	1210000h-121FFFFh
	BA288	64 kwords	1200000h-120FFFFh
Bank 7	BA287	64 kwords	11F0000h-11FFFFFh
	BA286	64 kwords	11E0000h-11EFFFFh
	BA285	64 kwords	11D0000h-11DFFFFh
	BA284	64 kwords	11C0000h-11CFFFFh
	BA283	64 kwords	11B0000h-11BFFFFh
	BA282	64 kwords	11A0000h-11AFFFFh
	BA281	64 kwords	1190000h-119FFFFh
	BA280	64 kwords	1180000h-118FFFFh
	BA279	64 kwords	1170000h-117FFFFh
	BA278	64 kwords	1160000h-116FFFFh
	BA277	64 kwords	1150000h-115FFFFh
	BA276	64 kwords	1140000h-114FFFFh
	BA275	64 kwords	1130000h-113FFFFh
	BA274	64 kwords	1120000h-112FFFFh
	BA273	64 kwords	1110000h-111FFFFh
	BA272	64 kwords	1100000h-110FFFFh
	BA271	64 kwords	10F0000h-10FFFFFh
	BA270	64 kwords	10E0000h-10EFFFFh
	BA269	64 kwords	10D0000h-10DFFFFh
	BA268	64 kwords	10C0000h-10CFFFFh
	BA267	64 kwords	10B0000h-10BFFFFh
	BA266	64 kwords	10A0000h-10AFFFFh
	BA265	64 kwords	1090000h-109FFFFh
	BA264	64 kwords	1080000h-108FFFFh
	BA263	64 kwords	1070000h-107FFFFh
	BA262	64 kwords	1060000h-106FFFFh
	BA261	64 kwords	1050000h-105FFFFh
	BA260	64 kwords	1040000h-104FFFFh
	BA259	64 kwords	1030000h-103FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 7	BA258	64 kwords	1020000h-102FFFFh
	BA257	64 kwords	1010000h-101FFFFh
	BA256	64 kwords	1000000h-100FFFFh
Bank 8	BA255	64 kwords	0FF0000h-0FFFFFFh
	BA254	64 kwords	0FE0000h-0FEFFFFh
	BA253	64 kwords	0FD0000h-0FDFFFFh
	BA252	64 kwords	0FC0000h-0FCFFFFh
	BA251	64 kwords	0FB0000h-0FBFFFFh
	BA250	64 kwords	0FA0000h-0FAFFFFh
	BA249	64 kwords	0F90000h-0F9FFFFh
	BA248	64 kwords	0F80000h-0F8FFFFh
	BA247	64 kwords	0F70000h-0F7FFFFh
	BA246	64 kwords	0F60000h-0F6FFFFh
	BA245	64 kwords	0F50000h-0F5FFFFh
	BA244	64 kwords	0F40000h-0F4FFFFh
	BA243	64 kwords	0F30000h-0F3FFFFh
	BA242	64 kwords	0F20000h-0F2FFFFh
	BA241	64 kwords	0F10000h-0F1FFFFh
	BA240	64 kwords	0F00000h-0F0FFFFh
	BA239	64 kwords	0EF0000h-0EFFFFFh
	BA238	64 kwords	0EE0000h-0EEFFFFh
	BA237	64 kwords	0ED0000h-0EDFFFFh
	BA236	64 kwords	0EC0000h-0ECFFFFh
	BA235	64 kwords	0EB0000h-0EBFFFFh
	BA234	64 kwords	0EA0000h-0EAFFFFh
	BA233	64 kwords	0E90000h-0E9FFFFh
	BA232	64 kwords	0E80000h-0E8FFFFh
	BA231	64 kwords	0E70000h-0E7FFFFh
	BA230	64 kwords	0E60000h-0E6FFFFh
	BA229	64 kwords	0E50000h-0E5FFFFh
	BA228	64 kwords	0E40000h-0E4FFFFh
	BA227	64 kwords	0E30000h-0E3FFFFh
	BA226	64 kwords	0E20000h-0E2FFFFh
	BA225	64 kwords	0E10000h-0E1FFFFh
	BA224	64 kwords	0E00000h-0E0FFFFh
Bank 9	BA223	64 kwords	0DF0000h-0DFFFFFh
	BA222	64 kwords	0DE0000h-0DEFFFFh
	BA221	64 kwords	0DD0000h-0DDFFFFh
	BA220	64 kwords	0DC0000h-0DCFFFFh
	BA219	64 kwords	0DB0000h-0DBFFFFh
	BA218	64 kwords	0DA0000h-0DAFFFFh
	BA217	64 kwords	0D90000h-0D9FFFFh
	BA216	64 kwords	0D80000h-0D8FFFFh
	BA215	64 kwords	0D70000h-0D7FFFFh
	BA214	64 kwords	0D60000h-0D6FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 9	BA213	64 kwords	0D50000h-0D5FFFFh
	BA212	64 kwords	0D40000h-0D4FFFFh
	BA211	64 kwords	0D30000h-0D3FFFFh
	BA210	64 kwords	0D20000h-0D2FFFFh
	BA209	64 kwords	0D10000h-0D1FFFFh
	BA208	64 kwords	0D00000h-0D0FFFFh
	BA207	64 kwords	0CF0000h-0CFFFFFh
	BA206	64 kwords	0CE0000h-0CEFFFFh
	BA205	64 kwords	0CD0000h-0CDFFFFh
	BA204	64 kwords	0CC0000h-0CCFFFFh
	BA203	64 kwords	0CB0000h-0CBFFFFh
	BA202	64 kwords	0CA0000h-0CAFFFFh
	BA201	64 kwords	0C90000h-0C9FFFFh
	BA200	64 kwords	0C80000h-0C8FFFFh
	BA199	64 kwords	0C70000h-0C7FFFFh
	BA198	64 kwords	0C60000h-0C6FFFFh
	BA197	64 kwords	0C50000h-0C5FFFFh
	BA196	64 kwords	0C40000h-0C4FFFFh
	BA195	64 kwords	0C30000h-0C3FFFFh
	BA194	64 kwords	0C20000h-0C2FFFFh
	BA193	64 kwords	0C10000h-0C1FFFFh
	BA192	64 kwords	0C00000h-0C0FFFFh
Bank 10	BA191	64 kwords	0BF0000h-0BFFFFFh
	BA190	64 kwords	0BE0000h-0BEFFFFh
	BA189	64 kwords	0BD0000h-0BDFFFFh
	BA188	64 kwords	0BC0000h-0BCFFFFh
	BA187	64 kwords	0BB0000h-0BBFFFFh
	BA186	64 kwords	0BA0000h-0BAFFFFh
	BA185	64 kwords	0B90000h-0B9FFFFh
	BA184	64 kwords	0B80000h-0B8FFFFh
	BA183	64 kwords	0B70000h-0B7FFFFh
	BA182	64 kwords	0B60000h-0B6FFFFh
	BA181	64 kwords	0B50000h-0B5FFFFh
	BA180	64 kwords	0B40000h-0B4FFFFh
	BA179	64 kwords	0B30000h-0B3FFFFh
	BA178	64 kwords	0B20000h-0B2FFFFh
	BA177	64 kwords	0B10000h-0B1FFFFh
	BA176	64 kwords	0B00000h-0B0FFFFh
	BA175	64 kwords	0AF0000h-0AFFFFFh
	BA174	64 kwords	0AE0000h-0AEFFFFh
	BA173	64 kwords	0AD0000h-0ADFFFFh
	BA172	64 kwords	0AC0000h-0ACFFFFh
	BA171	64 kwords	0AB0000h-0ABFFFFh
	BA170	64 kwords	0AA0000h-0AAFFFFh
	BA169	64 kwords	0A90000h-0A9FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 10	BA168	64 kwords	0A80000h-0A8FFFFh
	BA167	64 kwords	0A70000h-0A7FFFFh
	BA166	64 kwords	0A60000h-0A6FFFFh
	BA165	64 kwords	0A50000h-0A5FFFFh
	BA164	64 kwords	0A40000h-0A4FFFFh
	BA163	64 kwords	0A30000h-0A3FFFFh
	BA162	64 kwords	0A20000h-0A2FFFFh
	BA161	64 kwords	0A10000h-0A1FFFFh
	BA160	64 kwords	0A00000h-0A0FFFFh
Bank 11	BA159	64 kwords	09F0000h-09FFFFFh
	BA158	64 kwords	09E0000h-09EFFFFh
	BA157	64 kwords	09D0000h-09DFFFFh
	BA156	64 kwords	09C0000h-09CFFFFh
	BA155	64 kwords	09B0000h-09BFFFFh
	BA154	64 kwords	09A0000h-09AFFFFh
	BA153	64 kwords	0990000h-099FFFFh
	BA152	64 kwords	0980000h-098FFFFh
	BA151	64 kwords	0970000h-097FFFFh
	BA150	64 kwords	0960000h-096FFFFh
	BA149	64 kwords	0950000h-095FFFFh
	BA148	64 kwords	0940000h-094FFFFh
	BA147	64 kwords	0930000h-093FFFFh
	BA146	64 kwords	0920000h-092FFFFh
	BA145	64 kwords	0910000h-091FFFFh
	BA144	64 kwords	0900000h-090FFFFh
	BA143	64 kwords	08F0000h-08FFFFFh
	BA142	64 kwords	08E0000h-08EFFFFh
	BA141	64 kwords	08D0000h-08DFFFFh
	BA140	64 kwords	08C0000h-08CFFFFh
	BA139	64 kwords	08B0000h-08BFFFFh
	BA138	64 kwords	08A0000h-08AFFFFh
	BA137	64 kwords	0890000h-089FFFFh
	BA136	64 kwords	0880000h-088FFFFh
	BA135	64 kwords	0870000h-087FFFFh
	BA134	64 kwords	0860000h-086FFFFh
	BA133	64 kwords	0850000h-085FFFFh
	BA132	64 kwords	0840000h-084FFFFh
	BA131	64 kwords	0830000h-083FFFFh
	BA130	64 kwords	0820000h-082FFFFh
	BA129	64 kwords	0810000h-081FFFFh
	BA128	64 kwords	0800000h-080FFFFh
Bank 12	BA127	64 kwords	07F0000h-07FFFFFh
	BA126	64 kwords	07E0000h-07EFFFFh
	BA125	64 kwords	07D0000h-07DFFFFh
	BA124	64 kwords	07C0000h-07CFFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 12	BA123	64 kwords	07B0000h-07BFFFFh
	BA122	64 kwords	07A0000h-07AFFFFh
	BA121	64 kwords	0790000h-079FFFFh
	BA120	64 kwords	0780000h-078FFFFh
	BA119	64 kwords	0770000h-077FFFFh
	BA118	64 kwords	0760000h-076FFFFh
	BA117	64 kwords	0750000h-075FFFFh
	BA116	64 kwords	0740000h-074FFFFh
	BA115	64 kwords	0730000h-073FFFFh
	BA114	64 kwords	0720000h-072FFFFh
	BA113	64 kwords	0710000h-071FFFFh
	BA112	64 kwords	0700000h-070FFFFh
	BA111	64 kwords	06F0000h-06FFFFFh
	BA110	64 kwords	06E0000h-06EFFFFh
	BA109	64 kwords	06D0000h-06DFFFFh
	BA108	64 kwords	06C0000h-06CFFFFh
	BA107	64 kwords	06B0000h-06BFFFFh
	BA106	64 kwords	06A0000h-06AFFFFh
	BA105	64 kwords	0690000h-069FFFFh
	BA104	64 kwords	0680000h-068FFFFh
	BA103	64 kwords	0670000h-067FFFFh
	BA102	64 kwords	0660000h-066FFFFh
	BA101	64 kwords	0650000h-065FFFFh
	BA100	64 kwords	0640000h-064FFFFh
	BA99	64 kwords	0630000h-063FFFFh
	BA98	64 kwords	0620000h-062FFFFh
	BA97	64 kwords	0610000h-061FFFFh
	BA96	64 kwords	0600000h-060FFFFh
Bank13	BA95	64 kwords	05F0000h-05FFFFFh
	BA94	64 kwords	05E0000h-05EFFFFh
	BA93	64 kwords	05D0000h-05DFFFFh
	BA92	64 kwords	05C0000h-05CFFFFh
	BA91	64 kwords	05B0000h-05BFFFFh
	BA90	64 kwords	05A0000h-05AFFFFh
	BA89	64 kwords	0590000h-059FFFFh
	BA88	64 kwords	0580000h-058FFFFh
	BA87	64 kwords	0570000h-057FFFFh
	BA86	64 kwords	0560000h-056FFFFh
	BA85	64 kwords	0550000h-055FFFFh
	BA84	64 kwords	0540000h-054FFFFh
	BA83	64 kwords	0530000h-053FFFFh
	BA82	64 kwords	0520000h-052FFFFh
	BA81	64 kwords	0510000h-051FFFFh
	BA80	64 kwords	0500000h-050FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 13	BA79	64 kwords	04F0000h-04FFFFFh
	BA78	64 kwords	04E0000h-04EFFFFh
	BA77	64 kwords	04D0000h-04DFFFFh
	BA76	64 kwords	04C0000h-04CFFFFh
	BA75	64 kwords	04B0000h-04BFFFFh
	BA74	64 kwords	04A0000h-04AFFFFh
	BA73	64 kwords	0490000h-049FFFFh
	BA72	64 kwords	0480000h-048FFFFh
	BA71	64 kwords	0470000h-047FFFFh
	BA70	64 kwords	0460000h-046FFFFh
	BA69	64 kwords	0450000h-045FFFFh
	BA68	64 kwords	0440000h-044FFFFh
	BA67	64 kwords	0430000h-043FFFFh
	BA66	64 kwords	0420000h-042FFFFh
	BA65	64 kwords	0410000h-041FFFFh
	BA64	64 kwords	0400000h-040FFFFh
Bank 14	BA63	64 kwords	03F0000h-03FFFFFh
	BA62	64 kwords	03E0000h-03EFFFFh
	BA61	64 kwords	03D0000h-03DFFFFh
	BA60	64 kwords	03C0000h-03CFFFFh
	BA59	64 kwords	03B0000h-03BFFFFh
	BA58	64 kwords	03A0000h-03AFFFFh
	BA57	64 kwords	0390000h-039FFFFh
	BA56	64 kwords	0380000h-038FFFFh
	BA55	64 kwords	0370000h-037FFFFh
	BA54	64 kwords	0360000h-036FFFFh
	BA53	64 kwords	0350000h-035FFFFh
	BA52	64 kwords	0340000h-034FFFFh
	BA51	64 kwords	0330000h-033FFFFh
	BA50	64 kwords	0320000h-032FFFFh
	BA49	64 kwords	0310000h-031FFFFh
	BA48	64 kwords	0300000h-030FFFFh
	BA47	64 kwords	02F0000h-02FFFFFh
	BA46	64 kwords	02E0000h-02EFFFFh
	BA45	64 kwords	02D0000h-02DFFFFh
	BA44	64 kwords	02C0000h-02CFFFFh
	BA43	64 kwords	02B0000h-02BFFFFh
	BA42	64 kwords	02A0000h-02AFFFFh
	BA41	64 kwords	0290000h-029FFFFh
	BA40	64 kwords	0280000h-028FFFFh
	BA39	64 kwords	0270000h-027FFFFh
	BA38	64 kwords	0260000h-026FFFFh
	BA37	64 kwords	0250000h-025FFFFh
	BA36	64 kwords	0240000h-024FFFFh
	BA35	64 kwords	0230000h-023FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 14	BA34	64 kwords	0220000h-022FFFFh
	BA33	64 kwords	0210000h-021FFFFh
	BA32	64 kwords	0200000h-020FFFFh
Bank 15	BA31	64 kwords	01F0000h-01FFFFFh
	BA30	64 kwords	01E0000h-01EFFFFh
	BA29	64 kwords	01D0000h-01DFFFFh
	BA28	64 kwords	01C0000h-01CFFFFh
	BA27	64 kwords	01B0000h-01BFFFFh
	BA26	64 kwords	01A0000h-01AFFFFh
	BA25	64 kwords	0190000h-019FFFFh
	BA24	64 kwords	0180000h-018FFFFh
	BA23	64 kwords	0170000h-017FFFFh
	BA22	64 kwords	0160000h-016FFFFh
	BA21	64 kwords	0150000h-015FFFFh
	BA20	64 kwords	0140000h-014FFFFh
	BA19	64 kwords	0130000h-013FFFFh
	BA18	64 kwords	0120000h-012FFFFh
	BA17	64 kwords	0110000h-011FFFFh
	BA16	64 kwords	0100000h-010FFFFh
	BA15	64 kwords	00F0000h-00FFFFFh
	BA14	64 kwords	00E0000h-00EFFFFh
	BA13	64 kwords	00D0000h-00DFFFFh
	BA12	64 kwords	00C0000h-00CFFFFh
	BA11	64 kwords	00B0000h-00BFFFFh
	BA10	64 kwords	00A0000h-00AFFFFh
	BA9	64 kwords	0090000h-009FFFFh
	BA8	64 kwords	0080000h-008FFFFh
	BA7	64 kwords	0070000h-007FFFFh
	BA6	64 kwords	0060000h-006FFFFh
	BA5	64 kwords	0050000h-005FFFFh
	BA4	64 kwords	0040000h-004FFFFh
	BA3	64 kwords	0030000h-003FFFFh
	BA2	64 kwords	0020000h-002FFFFh
	BA1	64 kwords	0010000h-001FFFFh
	BA0	64 kwords	0000000h-000FFFFh

[Table 17] Top Boot OTP Block Addresses

OTP	Block Address A24 ~ A8	Block Size	(x16) Address Range*
	1FFFFh	512 words	1FFFE00h-1FFFFFFh

After entering OTP Block, any issued addresses should be in the range of OTP block address.

[Table 18] Bottom Boot Block Address Table

Bank	Block	Block Size	(x16) Address Range
Bank 15	BA514	64 Kwords	1FF0000h-1FFFFFFh
	BA513	64 Kwords	1FE0000h-1FEFFFFh
	BA512	64 Kwords	1FD0000h-1FDFFFFh
	BA511	64 Kwords	1FC0000h-1FCFFFFh
	BA510	64 kwords	1FB0000h-1FBFFFFh
	BA509	64 kwords	1FA0000h-1FAFFFFh
	BA508	64 kwords	1F90000h-1F9FFFFh
	BA507	64 kwords	1F80000h-1F8FFFFh
	BA506	64 kwords	1F70000h-1F7FFFFh
	BA505	64 kwords	1F60000h-1F6FFFFh
	BA504	64 kwords	1F50000h-1F5FFFFh
	BA503	64 kwords	1F40000h-1F4FFFFh
	BA502	64 kwords	1F30000h-1F3FFFFh
	BA501	64 kwords	1F20000h-1F2FFFFh
	BA500	64 kwords	1F10000h-1F1FFFFh
	BA499	64 kwords	1F00000h-1F0FFFFh
	BA498	64 kwords	1EF0000h-1EFFFFFh
	BA497	64 kwords	1EE0000h-1EEFFFFh
	BA496	64 kwords	1ED0000h-1EDFFFFh
	BA495	64 kwords	1EC0000h-1ECFFFFh
	BA494	64 kwords	1EB0000h-1EBFFFFh
	BA493	64 kwords	1EA0000h-1EAFFFFh
	BA492	64 kwords	1E90000h-1E9FFFFh
	BA491	64 kwords	1E80000h-1E8FFFFh
	BA490	64 kwords	1E70000h-1E7FFFFh
	BA489	64 kwords	1E60000h-1E6FFFFh
	BA488	64 kwords	1E50000h-1E5FFFFh
	BA487	64 kwords	1E40000h-1E4FFFFh
	BA486	64 kwords	1E30000h-1E3FFFFh
	BA485	64 kwords	1E20000h-1E2FFFFh
	BA484	64 kwords	1E10000h-1E1FFFFh
	BA483	64 kwords	1E00000h-1E0FFFFh
Bank 14	BA482	64 kwords	1DF0000h-1DFFFFFh
	BA481	64 kwords	1DE0000h-1DEFFFFh
	BA480	64 kwords	1DD0000h-1DDFFFFh
	BA479	64 kwords	1DC0000h-1DCFFFFh
	BA478	64 kwords	1DB0000h-1DBFFFFh
	BA477	64 kwords	1DA0000h-1DAFFFFh
	BA476	64 kwords	1D90000h-1D9FFFFh
	BA475	64 kwords	1D80000h-1D8FFFFh
	BA474	64 kwords	1D70000h-1D7FFFFh
	BA473	64 kwords	1D60000h-1D6FFFFh
	BA472	64 kwords	1D50000h-1D5FFFFh
	BA471	64 kwords	1D40000h-1D4FFFFh
	BA470	64 kwords	1D30000h-1D3FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 14	BA469	64 kwords	1D20000h-1D2FFFFh
	BA468	64 kwords	1D10000h-1D1FFFFh
	BA467	64 kwords	1D00000h-1D0FFFFh
	BA466	64 kwords	1CF0000h-1CFFFFFh
	BA465	64 kwords	1CE0000h-1CEFFFFh
	BA464	64 kwords	1CD0000h-1CDFFFFh
	BA463	64 kwords	1CC0000h-1CCFFFFh
	BA462	64 kwords	1CB0000h-1CBFFFFh
	BA461	64 kwords	1CA0000h-1CAFFFFh
	BA460	64 kwords	1C90000h-1C9FFFFh
	BA459	64 kwords	1C80000h-1C8FFFFh
	BA458	64 kwords	1C70000h-1C7FFFFh
	BA457	64 kwords	1C60000h-1C6FFFFh
	BA456	64 kwords	1C50000h-1C5FFFFh
	BA455	64 kwords	1C40000h-1C4FFFFh
	BA454	64 kwords	1C30000h-1C3FFFFh
	BA453	64 kwords	1C20000h-1C2FFFFh
	BA452	64 kwords	1C10000h-1C1FFFFh
	BA451	64 kwords	1C00000h-1C0FFFFh
Bank 13	BA450	64 kwords	1BF0000h-1BFFFFFh
	BA449	64 kwords	1BE0000h-1BEFFFFh
	BA448	64 kwords	1BD0000h-1BDFFFFh
	BA447	64 kwords	1BC0000h-1BCFFFFh
	BA446	64 kwords	1BB0000h-1BBFFFFh
	BA445	64 kwords	1BA0000h-1BAFFFFh
	BA444	64 kwords	1B90000h-1B9FFFFh
	BA443	64 kwords	1B80000h-1B8FFFFh
	BA442	64 kwords	1B70000h-1B7FFFFh
	BA441	64 kwords	1B60000h-1B6FFFFh
	BA440	64 kwords	1B50000h-1B5FFFFh
	BA439	64 kwords	1B40000h-1B4FFFFh
	BA438	64 kwords	1B30000h-1B3FFFFh
	BA437	64 kwords	1B20000h-1B2FFFFh
	BA436	64 kwords	1B10000h-1B1FFFFh
	BA435	64 kwords	1B00000h-1B0FFFFh
	BA434	64 kwords	1AF0000h-1AFFFFFh
	BA433	64 kwords	1AE0000h-1AEFFFFh
	BA432	64 kwords	1AD0000h-1ADFFFFh
	BA431	64 kwords	1AC0000h-1ACFFFFh
	BA430	64 kwords	1AB0000h-1ABFFFFh
	BA429	64 kwords	1AA0000h-1AAFFFFh
	BA428	64 kwords	1A90000h-1A9FFFFh
	BA427	64 kwords	1A80000h-1A8FFFFh
	BA426	64 kwords	1A70000h-1A7FFFFh
	BA425	64 kwords	1A60000h-1A6FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 13	BA424	64 kwords	1A50000h-1A5FFFFh
	BA423	64 kwords	1A40000h-1A4FFFFh
	BA422	64 kwords	1A30000h-1A3FFFFh
	BA421	64 kwords	1A20000h-1A2FFFFh
	BA420	64 kwords	1A10000h-1A1FFFFh
	BA419	64 kwords	1A00000h-1A0FFFFh
Bank 12	BA418	64 kwords	19F0000h-19FFFFFh
	BA417	64 kwords	19E0000h-19EFFFFh
	BA416	64 kwords	19D0000h-19DFFFFh
	BA415	64 kwords	19C0000h-19CFFFFh
	BA414	64 kwords	19B0000h-19BFFFFh
	BA413	64 kwords	19A0000h-19AFFFFh
	BA412	64 kwords	1990000h-199FFFFh
	BA411	64 kwords	1980000h-198FFFFh
	BA410	64 kwords	1970000h-197FFFFh
	BA409	64 kwords	1960000h-196FFFFh
	BA408	64 kwords	1950000h-195FFFFh
	BA407	64 kwords	1940000h-194FFFFh
	BA406	64 kwords	1930000h-193FFFFh
	BA405	64 kwords	1920000h-192FFFFh
	BA404	64 kwords	1910000h-191FFFFh
	BA403	64 kwords	1900000h-190FFFFh
	BA402	64 kwords	18F0000h-18FFFFFh
	BA401	64 kwords	18E0000h-18EFFFFh
	BA400	64 kwords	18D0000h-18DFFFFh
	BA399	64 kwords	18C0000h-18CFFFFh
	BA398	64 kwords	18B0000h-18BFFFFh
	BA397	64 kwords	18A0000h-18AFFFFh
	BA396	64 kwords	1890000h-189FFFFh
	BA395	64 kwords	1880000h-188FFFFh
	BA394	64 kwords	1870000h-187FFFFh
	BA393	64 kwords	1860000h-186FFFFh
	BA392	64 kwords	1850000h-185FFFFh
	BA391	64 kwords	1840000h-184FFFFh
	BA390	64 kwords	1830000h-183FFFFh
	BA389	64 kwords	1820000h-182FFFFh
	BA388	64 kwords	1810000h-181FFFFh
	BA387	64 kwords	1800000h-180FFFFh
Bank 11	BA386	64 kwords	17F0000h-17FFFFFh
	BA385	64 kwords	17E0000h-17EFFFFh
	BA384	64 kwords	17D0000h-17DFFFFh
	BA383	64 kwords	17C0000h-17CFFFFh
	BA382	64 kwords	17B0000h-17BFFFFh
	BA381	64 kwords	17A0000h-17AFFFFh
	BA380	64 kwords	1790000h-179FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 11	BA379	64 kwords	1780000h-178FFFFh
	BA378	64 kwords	1770000h-177FFFFh
	BA377	64 kwords	1760000h-176FFFFh
	BA376	64 kwords	1750000h-175FFFFh
	BA375	64 kwords	1740000h-174FFFFh
	BA374	64 kwords	1730000h-173FFFFh
	BA373	64 kwords	1720000h-172FFFFh
	BA372	64 kwords	1710000h-171FFFFh
	BA371	64 kwords	1700000h-170FFFFh
	BA370	64 kwords	16F0000h-16FFFFFh
	BA369	64 kwords	16E0000h-16EFFFFh
	BA368	64 kwords	16D0000h-16DFFFFh
	BA367	64 kwords	16C0000h-16CFFFFh
	BA366	64 kwords	16B0000h-16BFFFFh
	BA365	64 kwords	16A0000h-16AFFFFh
	BA364	64 kwords	1690000h-169FFFFh
	BA363	64 kwords	1680000h-168FFFFh
	BA362	64 kwords	1670000h-167FFFFh
	BA361	64 kwords	1660000h-166FFFFh
	BA360	64 kwords	1650000h-165FFFFh
	BA359	64 kwords	1640000h-164FFFFh
	BA358	64 kwords	1630000h-163FFFFh
	BA357	64 kwords	1620000h-162FFFFh
	BA356	64 kwords	1610000h-161FFFFh
	BA355	64 kwords	1600000h-160FFFFh
Bank 10	BA354	64 kwords	15F0000h-15FFFFFh
	BA353	64 kwords	15E0000h-15EFFFFh
	BA352	64 kwords	15D0000h-15DFFFFh
	BA351	64 kwords	15C0000h-15CFFFFh
	BA350	64 kwords	15B0000h-15BFFFFh
	BA349	64 kwords	15A0000h-15AFFFFh
	BA348	64 kwords	1590000h-159FFFFh
	BA347	64 kwords	1580000h-158FFFFh
	BA346	64 kwords	1570000h-157FFFFh
	BA345	64 kwords	1560000h-156FFFFh
	BA344	64 kwords	1550000h-155FFFFh
	BA343	64 kwords	1540000h-154FFFFh
	BA342	64 kwords	1530000h-153FFFFh
	BA341	64 kwords	1520000h-152FFFFh
	BA340	64 kwords	1510000h-151FFFFh
	BA339	64 kwords	1500000h-150FFFFh
	BA338	64 kwords	14F0000h-14FFFFFh
	BA337	64 kwords	14E0000h-14EFFFFh
	BA336	64 kwords	14D0000h-14DFFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 10	BA335	64 kwords	14C0000h-14CFFFFh
	BA334	64 kwords	14B0000h-14BFFFFh
	BA333	64 kwords	14A0000h-14AFFFFh
	BA332	64 kwords	1490000h-149FFFFh
	BA331	64 kwords	1480000h-148FFFFh
	BA330	64 kwords	1470000h-147FFFFh
	BA329	64 kwords	1460000h-146FFFFh
	BA328	64 kwords	1450000h-145FFFFh
	BA327	64 kwords	1440000h-144FFFFh
	BA326	64 kwords	1430000h-143FFFFh
	BA325	64 kwords	1420000h-142FFFFh
	BA324	64 kwords	1410000h-141FFFFh
	BA323	64 kwords	1400000h-140FFFFh
Bank 9	BA322	64 kwords	13F0000h-13FFFFFh
	BA321	64 kwords	13E0000h-13EFFFFh
	BA320	64 kwords	13D0000h-13DFFFFh
	BA319	64 kwords	13C0000h-13CFFFFh
	BA318	64 kwords	13B0000h-13BFFFFh
	BA317	64 kwords	13A0000h-13AFFFFh
	BA316	64 kwords	1390000h-139FFFFh
	BA315	64 kwords	1380000h-138FFFFh
	BA314	64 kwords	1370000h-137FFFFh
	BA313	64 kwords	1360000h-136FFFFh
	BA312	64 kwords	1350000h-135FFFFh
	BA311	64 kwords	1340000h-134FFFFh
	BA310	64 kwords	1330000h-133FFFFh
	BA309	64 kwords	1320000h-132FFFFh
	BA308	64 kwords	1310000h-131FFFFh
	BA307	64 kwords	1300000h-130FFFFh
	BA306	64 kwords	12F0000h-12FFFFFh
	BA305	64 kwords	12E0000h-12EFFFFh
	BA304	64 kwords	12D0000h-12DFFFFh
	BA303	64 kwords	12C0000h-12CFFFFh
	BA302	64 kwords	12B0000h-12BFFFFh
	BA301	64 kwords	12A0000h-12AFFFFh
	BA300	64 kwords	1290000h-129FFFFh
	BA299	64 kwords	1280000h-128FFFFh
	BA298	64 kwords	1270000h-127FFFFh
	BA297	64 kwords	1260000h-126FFFFh
	BA296	64 kwords	1250000h-125FFFFh
	BA295	64 kwords	1240000h-124FFFFh
	BA294	64 kwords	1230000h-123FFFFh
	BA293	64 kwords	1220000h-122FFFFh
	BA292	64 kwords	1210000h-121FFFFh
	BA291	64 kwords	1200000h-120FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 8	BA290	64 kwords	11F0000h-11FFFFFh
	BA289	64 kwords	11E0000h-11EFFFFh
	BA288	64 kwords	11D0000h-11DFFFFh
	BA287	64 kwords	11C0000h-11CFFFFh
	BA286	64 kwords	11B0000h-11BFFFFh
	BA285	64 kwords	11A0000h-11AFFFFh
	BA284	64 kwords	1190000h-119FFFFh
	BA283	64 kwords	1180000h-118FFFFh
	BA282	64 kwords	1170000h-117FFFFh
	BA281	64 kwords	1160000h-116FFFFh
	BA280	64 kwords	1150000h-115FFFFh
	BA279	64 kwords	1140000h-114FFFFh
	BA278	64 kwords	1130000h-113FFFFh
	BA277	64 kwords	1120000h-112FFFFh
	BA276	64 kwords	1110000h-111FFFFh
	BA275	64 kwords	1100000h-110FFFFh
	BA274	64 kwords	10F0000h-10FFFFFh
	BA273	64 kwords	10E0000h-10EFFFFh
	BA272	64 kwords	10D0000h-10DFFFFh
	BA271	64 kwords	10C0000h-10CFFFFh
	BA270	64 kwords	10B0000h-10BFFFFh
	BA269	64 kwords	10A0000h-10AFFFFh
	BA268	64 kwords	1090000h-109FFFFh
	BA267	64 kwords	1080000h-108FFFFh
	BA266	64 kwords	1070000h-107FFFFh
	BA265	64 kwords	1060000h-106FFFFh
	BA264	64 kwords	1050000h-105FFFFh
	BA263	64 kwords	1040000h-104FFFFh
	BA262	64 kwords	1030000h-103FFFFh
	BA261	64 kwords	1020000h-102FFFFh
	BA260	64 kwords	1010000h-101FFFFh
	BA259	64 kwords	1000000h-100FFFFh
Bank 7	BA258	64 kwords	0FF0000h-0FFFFFFh
	BA257	64 kwords	0FE0000h-0FEFFFFh
	BA256	64 kwords	0FD0000h-0FDFFFFh
	BA255	64 kwords	0FC0000h-0FCFFFFh
	BA254	64 kwords	0FB0000h-0FBFFFFh
	BA253	64 kwords	0FA0000h-0FAFFFFh
	BA252	64 kwords	0F90000h-0F9FFFFh
	BA251	64 kwords	0F80000h-0F8FFFFh
	BA250	64 kwords	0F70000h-0F7FFFFh
	BA249	64 kwords	0F60000h-0F6FFFFh
	BA248	64 kwords	0F50000h-0F5FFFFh
	BA247	64 kwords	0F40000h-0F4FFFFh
	BA246	64 kwords	0F30000h-0F3FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 7	BA245	64 kwords	0F20000h-0F2FFFFh
	BA244	64 kwords	0F10000h-0F1FFFFh
	BA243	64 kwords	0F00000h-0F0FFFFh
	BA242	64 kwords	0EF0000h-0EFFFFFh
	BA241	64 kwords	0EE0000h-0EEFFFFh
	BA240	64 kwords	0ED0000h-0EDFFFFh
	BA239	64 kwords	0EC0000h-0ECFFFFh
	BA238	64 kwords	0EB0000h-0EBFFFFh
	BA237	64 kwords	0EA0000h-0EAFFFFh
	BA236	64 kwords	0E90000h-0E9FFFFh
	BA235	64 kwords	0E80000h-0E8FFFFh
	BA234	64 kwords	0E70000h-0E7FFFFh
	BA233	64 kwords	0E60000h-0E6FFFFh
	BA232	64 kwords	0E50000h-0E5FFFFh
	BA231	64 kwords	0E40000h-0E4FFFFh
	BA230	64 kwords	0E30000h-0E3FFFFh
	BA229	64 kwords	0E20000h-0E2FFFFh
	BA228	64 kwords	0E10000h-0E1FFFFh
	BA227	64 kwords	0E00000h-0E0FFFFh
Bank 6	BA226	64 kwords	0DF0000h-0DFFFFFh
	BA225	64 kwords	0DE0000h-0DEFFFFh
	BA224	64 kwords	0DD0000h-0DDFFFFh
	BA223	64 kwords	0DC0000h-0DCFFFFh
	BA222	64 kwords	0DB0000h-0DBFFFFh
	BA221	64 kwords	0DA0000h-0DAFFFFh
	BA220	64 kwords	0D90000h-0D9FFFFh
	BA219	64 kwords	0D80000h-0D8FFFFh
	BA218	64 kwords	0D70000h-0D7FFFFh
	BA217	64 kwords	0D60000h-0D6FFFFh
	BA216	64 kwords	0D50000h-0D5FFFFh
	BA215	64 kwords	0D40000h-0D4FFFFh
	BA214	64 kwords	0D30000h-0D3FFFFh
	BA213	64 kwords	0D20000h-0D2FFFFh
	BA212	64 kwords	0D10000h-0D1FFFFh
	BA211	64 kwords	0D00000h-0D0FFFFh
	BA210	64 kwords	0CF0000h-0CFFFFFh
	BA209	64 kwords	0CE0000h-0CEFFFFh
	BA208	64 kwords	0CD0000h-0CDFFFFh
	BA207	64 kwords	0CC0000h-0CCFFFFh
	BA206	64 kwords	0CB0000h-0CBFFFFh
	BA205	64 kwords	0CA0000h-0CAFFFFh
	BA204	64 kwords	0C90000h-0C9FFFFh
	BA203	64 kwords	0C80000h-0C8FFFFh
	BA202	64 kwords	0C70000h-0C7FFFFh
	BA201	64 kwords	0C60000h-0C6FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 6	BA200	64 kwords	0C50000h-0C5FFFFh
	BA199	64 kwords	0C40000h-0C4FFFFh
	BA198	64 kwords	0C30000h-0C3FFFFh
	BA197	64 kwords	0C20000h-0C2FFFFh
	BA196	64 kwords	0C10000h-0C1FFFFh
	BA195	64 kwords	0C00000h-0C0FFFFh
Bank 5	BA194	64 kwords	0BF0000h-0BFFFFFh
	BA193	64 kwords	0BE0000h-0BEFFFFh
	BA192	64 kwords	0BD0000h-0BDFFFFh
	BA191	64 kwords	0BC0000h-0BCFFFFh
	BA190	64 kwords	0BB0000h-0BBFFFFh
	BA189	64 kwords	0BA0000h-0BAFFFFh
	BA188	64 kwords	0B90000h-0B9FFFFh
	BA187	64 kwords	0B80000h-0B8FFFFh
	BA186	64 kwords	0B70000h-0B7FFFFh
	BA185	64 kwords	0B60000h-0B6FFFFh
	BA184	64 kwords	0B50000h-0B5FFFFh
	BA183	64 kwords	0B40000h-0B4FFFFh
	BA182	64 kwords	0B30000h-0B3FFFFh
	BA181	64 kwords	0B20000h-0B2FFFFh
	BA180	64 kwords	0B10000h-0B1FFFFh
	BA179	64 kwords	0B00000h-0B0FFFFh
	BA178	64 kwords	0AF0000h-0AFFFFFh
	BA177	64 kwords	0AE0000h-0AEFFFFh
	BA176	64 kwords	0AD0000h-0ADFFFFh
	BA175	64 kwords	0AC0000h-0ACFFFFh
	BA174	64 kwords	0AB0000h-0ABFFFFh
	BA173	64 kwords	0AA0000h-0AAFFFFh
	BA172	64 kwords	0A90000h-0A9FFFFh
	BA171	64 kwords	0A80000h-0A8FFFFh
	BA170	64 kwords	0A70000h-0A7FFFFh
	BA169	64 kwords	0A60000h-0A6FFFFh
	BA168	64 kwords	0A50000h-0A5FFFFh
	BA167	64 kwords	0A40000h-0A4FFFFh
	BA166	64 kwords	0A30000h-0A3FFFFh
	BA165	64 kwords	0A20000h-0A2FFFFh
	BA164	64 kwords	0A10000h-0A1FFFFh
	BA163	64 kwords	0A00000h-0A0FFFFh
Bank 4	BA162	64 kwords	09F0000h-09FFFFFh
	BA161	64 kwords	09E0000h-09EFFFFh
	BA160	64 kwords	09D0000h-09DFFFFh
	BA159	64 kwords	09C0000h-09CFFFFh
	BA158	64 kwords	09B0000h-09BFFFFh
	BA157	64 kwords	09A0000h-09AFFFFh
	BA156	64 kwords	0990000h-099FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 4	BA155	64 kwords	0980000h-098FFFFh
	BA154	64 kwords	0970000h-097FFFFh
	BA153	64 kwords	0960000h-096FFFFh
	BA152	64 kwords	0950000h-095FFFFh
	BA151	64 kwords	0940000h-094FFFFh
	BA150	64 kwords	0930000h-093FFFFh
	BA149	64 kwords	0920000h-092FFFFh
	BA148	64 kwords	0910000h-091FFFFh
	BA147	64 kwords	0900000h-090FFFFh
	BA146	64 kwords	08F0000h-08FFFFFh
	BA145	64 kwords	08E0000h-08EFFFFh
	BA144	64 kwords	08D0000h-08DFFFFh
	BA143	64 kwords	08C0000h-08CFFFFh
	BA142	64 kwords	08B0000h-08BFFFFh
	BA141	64 kwords	08A0000h08AFFFFh
	BA140	64 kwords	0890000h-089FFFFh
	BA139	64 kwords	0880000h-088FFFFh
	BA138	64 kwords	0870000h-087FFFFh
	BA137	64 kwords	0860000h-086FFFFh
	BA136	64 kwords	0850000h-085FFFFh
	BA135	64 kwords	0840000h-084FFFFh
	BA134	64 kwords	0830000h-083FFFFh
	BA133	64 kwords	0820000h-082FFFFh
	BA132	64 kwords	0810000h-081FFFFh
	BA131	64 kwords	0800000h-080FFFFh
Bank 3	BA130	64 kwords	07F0000h-07FFFFFh
	BA129	64 kwords	07E0000h-07EFFFFh
	BA128	64 kwords	07D0000h-07DFFFFh
	BA127	64 kwords	07C0000h-07CFFFFh
	BA126	64 kwords	07B0000h-07BFFFFh
	BA125	64 kwords	07A0000h-07AFFFFh
	BA124	64 kwords	0790000h-079FFFFh
	BA123	64 kwords	0780000h-078FFFFh
	BA122	64 kwords	0770000h-077FFFFh
	BA121	64 kwords	0760000h-076FFFFh
	BA120	64 kwords	0750000h-075FFFFh
	BA119	64 kwords	0740000h-074FFFFh
	BA118	64 kwords	0730000h-073FFFFh
	BA117	64 kwords	0720000h-072FFFFh
	BA116	64 kwords	0710000h-071FFFFh
	BA115	64 kwords	0700000h-070FFFFh
	BA114	64 kwords	06F0000h-06FFFFFh
	BA113	64 kwords	06E0000h-06EFFFFh
	BA112	64 kwords	06D0000h-06DFFFFh
	BA111	64 kwords	06C0000h-06CFFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 3	BA110	64 kwords	06B0000h-06BFFFFh
	BA109	64 kwords	06A0000h-06AFFFFh
	BA108	64 kwords	0690000h-069FFFFh
	BA107	64 kwords	0680000h-068FFFFh
	BA106	64 kwords	0670000h-067FFFFh
	BA105	64 kwords	0660000h-066FFFFh
	BA104	64 kwords	0650000h-065FFFFh
	BA103	64 kwords	0640000h-064FFFFh
	BA102	64 kwords	0630000h-063FFFFh
	BA101	64 kwords	0620000h-062FFFFh
	BA100	64 kwords	0610000h-061FFFFh
	BA99	64 kwords	0600000h-060FFFFh
Bank 2	BA98	64 kwords	05F0000h-05FFFFFh
	BA97	64 kwords	05E0000h-05EFFFFh
	BA96	64 kwords	05D0000h-05DFFFFh
	BA95	64 kwords	05C0000h-05CFFFFh
	BA94	64 kwords	05B0000h-05BFFFFh
	BA93	64 kwords	05A0000h-05AFFFFh
	BA92	64 kwords	0590000h-059FFFFh
	BA91	64 kwords	0580000h-058FFFFh
	BA90	64 kwords	0570000h-057FFFFh
	BA89	64 kwords	0560000h-056FFFFh
	BA88	64 kwords	0550000h-055FFFFh
	BA87	64 kwords	0540000h-054FFFFh
	BA86	64 kwords	0530000h-053FFFFh
	BA85	64 kwords	0520000h-052FFFFh
	BA84	64 kwords	0510000h-051FFFFh
	BA83	64 kwords	0500000h-050FFFFh
	BA82	64 kwords	04F0000h-04FFFFFh
	BA81	64 kwords	04E0000h-04EFFFFh
	BA80	64 kwords	04D0000h-04DFFFFh
	BA79	64 kwords	04C0000h-04CFFFFh
	BA78	64 kwords	04B0000h-04BFFFFh
	BA77	64 kwords	04A0000h-04AFFFFh
	BA76	64 kwords	0490000h-049FFFFh
	BA75	64 kwords	0480000h-048FFFFh
	BA74	64 kwords	0470000h-047FFFFh
	BA73	64 kwords	0460000h-046FFFFh
	BA72	64 kwords	0450000h-045FFFFh
	BA71	64 kwords	0440000h-044FFFFh
	BA70	64 kwords	0430000h-043FFFFh
	BA69	64 kwords	0420000h-042FFFFh
	BA68	64 kwords	0410000h-041FFFFh
	BA67	64 kwords	0400000h-040FFFFh
Bank 1	BA66	64 kwords	03F0000h-03FFFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 1	BA65	64 kwords	03E0000h-03EFFFFh
	BA64	64 kwords	03D0000h-03DFFFFh
	BA63	64 kwords	03C0000h-03CFFFFh
	BA62	64 kwords	03B0000h-03BFFFFh
	BA61	64 kwords	03A0000h-03AFFFFh
	BA60	64 kwords	0390000h-039FFFFh
	BA59	64 kwords	0380000h-038FFFFh
	BA58	64 kwords	0370000h-037FFFFh
	BA57	64 kwords	0360000h-036FFFFh
	BA56	64 kwords	0350000h-035FFFFh
	BA55	64 kwords	0340000h-034FFFFh
	BA54	64 kwords	0330000h-033FFFFh
	BA53	64 kwords	0320000h-032FFFFh
	BA52	64 kwords	0310000h-031FFFFh
	BA51	64 kwords	0300000h-030FFFFh
	BA50	64 kwords	02F0000h-02FFFFFh
	BA49	64 kwords	02E0000h-02EFFFFh
	BA48	64 kwords	02D0000h-02DFFFFh
	BA47	64 kwords	02C0000h-02CFFFFh
	BA46	64 kwords	02B0000h-02BFFFFh
	BA45	64 kwords	02A0000h-02AFFFFh
	BA44	64 kwords	0290000h-029FFFFh
	BA43	64 kwords	0280000h-028FFFFh
	BA42	64 kwords	0270000h-027FFFFh
	BA41	64 kwords	0260000h-026FFFFh
	BA40	64 kwords	0250000h-025FFFFh
	BA39	64 kwords	0240000h-024FFFFh
	BA38	64 kwords	0230000h-023FFFFh
	BA37	64 kwords	0220000h-022FFFFh
	BA36	64 kwords	0210000h-021FFFFh
	BA35	64 kwords	0200000h-020FFFFh
Bank 0	BA34	64 kwords	01F0000h-01FFFFFh
	BA33	64 kwords	01E0000h-01EFFFFh
	BA32	64 kwords	01D0000h-01DFFFFh
	BA31	64 kwords	01C0000h-01CFFFFh
	BA30	64 kwords	01B0000h-01BFFFFh
	BA29	64 kwords	01A0000h-01AFFFFh
	BA28	64 kwords	0190000h-019FFFFh
	BA27	64 kwords	0180000h-018FFFFh
	BA26	64 kwords	0170000h-017FFFFh
	BA25	64 kwords	0160000h-016FFFFh
	BA24	64 kwords	0150000h-015FFFFh
	BA23	64 kwords	0140000h-014FFFFh
	BA22	64 kwords	0130000h-013FFFFh
	BA21	64 kwords	0120000h-012FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 0	BA20	64 kwords	0110000h-011FFFFh
	BA19	64 kwords	0100000h-010FFFFh
	BA18	64 kwords	00F0000h-00FFFFFh
	BA17	64 kwords	00E0000h-00EFFFFh
	BA16	64 kwords	00D0000h-00DFFFFh
	BA15	64 kwords	00C0000h-00CFFFFh
	BA14	64 kwords	00B0000h-00BFFFFh
	BA13	64 kwords	00A0000h-00AFFFFh
	BA12	64 kwords	0090000h-009FFFFh
	BA11	64 kwords	0080000h-008FFFFh
	BA10	64 kwords	0070000h-007FFFFh
	BA9	64 kwords	0060000h-006FFFFh
	BA8	64 kwords	0050000h-005FFFFh
	BA7	64 kwords	0040000h-004FFFFh
	BA6	64 kwords	0030000h-003FFFFh
	BA5	64 kwords	0020000h-002FFFFh
	BA4	64 kwords	0010000h-001FFFFh
	BA3	16 kwords	000C000h-000FFFFh
	BA2	16 kwords	0008000h-000BFFFh
	BA1	16 kwords	0004000h-0007FFFh
	BA0	16 kwords	0000000h-0003FFFh

[Table 19] Bottom Boot OTP Block Addresses

OTP	Block Address A24 ~ A8	Block Size	(x16) Address Range*
	00000h	512 words	0000000h-00001FFh

After entering OTP Block, any issued addresses should be in the range of OTP block address.

[Table 20] Uniform Block Address Table

Bank	Block	Block Size	(x16) Address Range
Bank 0	BA511	64 kwords	1FF0000h-1FFFFFFh
	BA510	64 kwords	1FE0000h-1FEFFFFh
	BA509	64 kwords	1FD0000h-1FDFFFFh
	BA508	64 kwords	1FC0000h-1FCFFFFh
	BA507	64 kwords	1FB0000h-1FBFFFFh
	BA506	64 kwords	1FA0000h-1FAFFFFh
	BA505	64 kwords	1F90000h-1F9FFFFh
	BA504	64 kwords	1F80000h-1F8FFFFh
	BA503	64 kwords	1F70000h-1F7FFFFh
	BA502	64 kwords	1F60000h-1F6FFFFh
	BA501	64 kwords	1F50000h-1F5FFFFh
	BA500	64 kwords	1F40000h-1F4FFFFh
	BA499	64 kwords	1F30000h-1F3FFFFh
	BA498	64 kwords	1F20000h-1F2FFFFh
	BA497	64 kwords	1F10000h-1F1FFFFh
	BA496	64 kwords	1F00000h-1F0FFFFh
	BA495	64 kwords	1EF0000h-1EFFFFFh
	BA494	64 kwords	1EE0000h-1EEFFFFh
	BA493	64 kwords	1ED0000h-1EDFFFFh
	BA492	64 kwords	1EC0000h-1ECFFFFh
	BA491	64 kwords	1EB0000h-1EBFFFFh
	BA490	64 kwords	1EA0000h-1EAFFFFh
	BA489	64 kwords	1E90000h-1E9FFFFh
	BA488	64 kwords	1E80000h-1E8FFFFh
	BA487	64 kwords	1E70000h-1E7FFFFh
	BA486	64 kwords	1E60000h-1E6FFFFh
	BA485	64 kwords	1E50000h-1E5FFFFh
	BA484	64 kwords	1E40000h-1E4FFFFh
	BA483	64 kwords	1E30000h-1E3FFFFh
	BA482	64 kwords	1E20000h-1E2FFFFh
	BA481	64 kwords	1E10000h-1E1FFFFh
	BA480	64 kwords	1E00000h-1E0FFFFh
Bank 1	BA479	64 kwords	1DF0000h-1DFFFFFh
	BA478	64 kwords	1DE0000h-1DEFFFFh
	BA477	64 kwords	1DD0000h-1DDFFFFh
	BA476	64 kwords	1DC0000h-1DCFFFFh
	BA475	64 kwords	1DB0000h-1DBFFFFh
	BA474	64 kwords	1DA0000h-1DAFFFFh
	BA473	64 kwords	1D90000h-1D9FFFFh
	BA472	64 kwords	1D80000h-1D8FFFFh
	BA471	64 kwords	1D70000h-1D7FFFFh
	BA470	64 kwords	1D60000h-1D6FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 1	BA469	64 kwords	1D50000h-1D5FFFFh
	BA468	64 kwords	1D40000h-1D4FFFFh
	BA467	64 kwords	1D30000h-1D3FFFFh
	BA466	64 kwords	1D20000h-1D2FFFFh
	BA465	64 kwords	1D10000h-1D1FFFFh
	BA464	64 kwords	1D00000h-1D0FFFFh
	BA463	64 kwords	1CF0000h-1CFFFFFh
	BA462	64 kwords	1CE0000h-1CEFFFFh
	BA461	64 kwords	1CD0000h-1CDFFFFh
	BA460	64 kwords	1CC0000h-1CCFFFFh
	BA459	64 kwords	1CB0000h-1CBFFFFh
	BA458	64 kwords	1CA0000h-1CAFFFFh
	BA457	64 kwords	1C90000h-1C9FFFFh
	BA456	64 kwords	1C80000h-1C8FFFFh
	BA455	64 kwords	1C70000h-1C7FFFFh
	BA454	64 kwords	1C60000h-1C6FFFFh
	BA453	64 kwords	1C50000h-1C5FFFFh
	BA452	64 kwords	1C40000h-1C4FFFFh
	BA451	64 kwords	1C30000h-1C3FFFFh
	BA450	64 kwords	1C20000h-1C2FFFFh
	BA449	64 kwords	1C10000h-1C1FFFFh
	BA448	64 kwords	1C00000h-1C0FFFFh
Bank 2	BA447	64 kwords	1BF0000h-1BFFFFFh
	BA446	64 kwords	1BE0000h-1BEFFFFh
	BA445	64 kwords	1BD0000h-1BDFFFFh
	BA444	64 kwords	1BC0000h-1BCFFFFh
	BA443	64 kwords	1BB0000h-1BBFFFFh
	BA442	64 kwords	1BA0000h-1BAFFFFh
	BA441	64 kwords	1B90000h-1B9FFFFh
	BA440	64 kwords	1B80000h-1B8FFFFh
	BA439	64 kwords	1B70000h-1B7FFFFh
	BA438	64 kwords	1B60000h-1B6FFFFh
	BA437	64 kwords	1B50000h-1B5FFFFh
	BA436	64 kwords	1B40000h-1B4FFFFh
	BA435	64 kwords	1B30000h-1B3FFFFh
	BA434	64 kwords	1B20000h-1B2FFFFh
	BA433	64 kwords	1B10000h-1B1FFFFh
	BA432	64 kwords	1B00000h-1B0FFFFh
	BA431	64 kwords	1AF0000h-1AFFFFFh
	BA430	64 kwords	1AE0000h-1AEFFFFh
	BA429	64 kwords	1AD0000h-1ADFFFFh
	BA428	64 kwords	1AC0000h-1ACFFFFh
	BA427	64 kwords	1AB0000h-1ABFFFFh
	BA426	64 kwords	1AA0000h-1AAFFFFh
	BA425	64 kwords	1A90000h-1A9FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 2	BA424	64 kwords	1A80000h-1A8FFFFh
	BA423	64 kwords	1A70000h-1A7FFFFh
	BA422	64 kwords	1A60000h-1A6FFFFh
	BA421	64 kwords	1A50000h-1A5FFFFh
	BA420	64 kwords	1A40000h-1A4FFFFh
	BA419	64 kwords	1A30000h-1A3FFFFh
	BA418	64 kwords	1A20000h-1A2FFFFh
	BA417	64 kwords	1A10000h-1A1FFFFh
	BA416	64 kwords	1A00000h-1A0FFFFh
Bank 3	BA415	64 kwords	19F0000h-19FFFFFh
	BA414	64 kwords	19E0000h-19EFFFFh
	BA413	64 kwords	19D0000h-19DFFFFh
	BA412	64 kwords	19C0000h-19CFFFFh
	BA411	64 kwords	19B0000h-19BFFFFh
	BA410	64 kwords	19A0000h-19AFFFFh
	BA409	64 kwords	1990000h-199FFFFh
	BA408	64 kwords	1980000h-198FFFFh
	BA407	64 kwords	1970000h-197FFFFh
	BA406	64 kwords	1960000h-196FFFFh
	BA405	64 kwords	1950000h-195FFFFh
	BA404	64 kwords	1940000h-194FFFFh
	BA403	64 kwords	1930000h-193FFFFh
	BA402	64 kwords	1920000h-192FFFFh
	BA401	64 kwords	1910000h-191FFFFh
	BA400	64 kwords	1900000h-190FFFFh
	BA399	64 kwords	18F0000h-18FFFFFh
	BA398	64 kwords	18E0000h-18EFFFFh
	BA397	64 kwords	18D0000h-18DFFFFh
	BA396	64 kwords	18C0000h-18CFFFFh
	BA395	64 kwords	18B0000h-18BFFFFh
	BA394	64 kwords	18A0000h-18AFFFFh
	BA393	64 kwords	1890000h-189FFFFh
	BA392	64 kwords	1880000h-188FFFFh
	BA391	64 kwords	1870000h-187FFFFh
	BA390	64 kwords	1860000h-186FFFFh
	BA389	64 kwords	1850000h-185FFFFh
	BA388	64 kwords	1840000h-184FFFFh
	BA387	64 kwords	1830000h-183FFFFh
	BA386	64 kwords	1820000h-182FFFFh
	BA385	64 kwords	1810000h-181FFFFh
	BA384	64 kwords	1800000h-180FFFFh
Bank 4	BA383	64 kwords	17F0000h-17FFFFFh
	BA382	64 kwords	17E0000h-17EFFFFh
	BA381	64 kwords	17D0000h-17DFFFFh
	BA380	64 kwords	17C0000h-17CFFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 4	BA379	64 kwords	17B0000h-17BFFFFh
	BA378	64 kwords	17A0000h-17AFFFFh
	BA377	64 kwords	1790000h-179FFFFh
	BA376	64 kwords	1780000h-178FFFFh
	BA375	64 kwords	1770000h-177FFFFh
	BA374	64 kwords	1760000h-176FFFFh
	BA373	64 kwords	1750000h-175FFFFh
	BA372	64 kwords	1740000h-174FFFFh
	BA371	64 kwords	1730000h-173FFFFh
	BA370	64 kwords	1720000h-172FFFFh
	BA369	64 kwords	1710000h-171FFFFh
	BA368	64 kwords	1700000h-170FFFFh
	BA367	64 kwords	16F0000h-16FFFFFh
	BA366	64 kwords	16E0000h-16EFFFFh
	BA365	64 kwords	16D0000h-16DFFFFh
	BA364	64 kwords	16C0000h-16CFFFFh
	BA363	64 kwords	16B0000h-16BFFFFh
	BA362	64 kwords	16A0000h-16AFFFFh
	BA361	64 kwords	1690000h-169FFFFh
	BA360	64 kwords	1680000h-168FFFFh
	BA359	64 kwords	1670000h-167FFFFh
	BA358	64 kwords	1660000h-166FFFFh
	BA357	64 kwords	1650000h-165FFFFh
	BA356	64 kwords	1640000h-164FFFFh
	BA355	64 kwords	1630000h-163FFFFh
	BA354	64 kwords	1620000h-162FFFFh
	BA353	64 kwords	1610000h-161FFFFh
	BA352	64 kwords	1600000h-160FFFFh
Bank5	BA351	64 kwords	15F0000h-15FFFFFh
	BA350	64 kwords	15E0000h-15EFFFFh
	BA349	64 kwords	15D0000h-15DFFFFh
	BA348	64 kwords	15C0000h-15CFFFFh
	BA347	64 kwords	15B0000h-15BFFFFh
	BA346	64 kwords	15A0000h-15AFFFFh
	BA345	64 kwords	1590000h-159FFFFh
	BA344	64 kwords	1580000h-158FFFFh
	BA343	64 kwords	1570000h-157FFFFh
	BA342	64 kwords	1560000h-156FFFFh
	BA341	64 kwords	1550000h-155FFFFh
	BA340	64 kwords	1540000h-154FFFFh
	BA339	64 kwords	1530000h-153FFFFh
	BA338	64 kwords	1520000h-152FFFFh
	BA337	64 kwords	1510000h-151FFFFh
	BA336	64 kwords	1500000h-150FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 5	BA335	64 kwords	14F0000h-14FFFFFh
	BA334	64 kwords	14E0000h-14EFFFFh
	BA333	64 kwords	14D0000h-14DFFFFh
	BA332	64 kwords	14C0000h-14CFFFFh
	BA331	64 kwords	14B0000h-14BFFFFh
	BA330	64 kwords	14A0000h-14AFFFFh
	BA329	64 kwords	1490000h-149FFFFh
	BA328	64 kwords	1480000h-148FFFFh
	BA327	64 kwords	1470000h-147FFFFh
	BA326	64 kwords	1460000h-146FFFFh
	BA325	64 kwords	1450000h-145FFFFh
	BA324	64 kwords	1440000h-144FFFFh
	BA323	64 kwords	1430000h-143FFFFh
	BA322	64 kwords	1420000h-142FFFFh
	BA321	64 kwords	1410000h-141FFFFh
	BA320	64 kwords	1400000h-140FFFFh
Bank 6	BA319	64 kwords	13F0000h-13FFFFFh
	BA318	64 kwords	13E0000h-13EFFFFh
	BA317	64 kwords	13D0000h-13DFFFFh
	BA316	64 kwords	13C0000h-13CFFFFh
	BA315	64 kwords	13B0000h-13BFFFFh
	BA314	64 kwords	13A0000h-13AFFFFh
	BA313	64 kwords	1390000h-139FFFFh
	BA312	64 kwords	1380000h-138FFFFh
	BA311	64 kwords	1370000h-137FFFFh
	BA310	64 kwords	1360000h-136FFFFh
	BA309	64 kwords	1350000h-135FFFFh
	BA308	64 kwords	1340000h-134FFFFh
	BA307	64 kwords	1330000h-133FFFFh
	BA306	64 kwords	1320000h-132FFFFh
	BA305	64 kwords	1310000h-131FFFFh
	BA304	64 kwords	1300000h-130FFFFh
	BA303	64 kwords	12F0000h-12FFFFFh
	BA302	64 kwords	12E0000h-12EFFFFh
	BA301	64 kwords	12D0000h-12DFFFFh
	BA300	64 kwords	12C0000h-12CFFFFh
	BA299	64 kwords	12B0000h-12BFFFFh
	BA298	64 kwords	12A0000h-12AFFFFh
	BA297	64 kwords	1290000h-129FFFFh
	BA296	64 kwords	1280000h-128FFFFh
	BA295	64 kwords	1270000h-127FFFFh
	BA294	64 kwords	1260000h-126FFFFh
	BA293	64 kwords	1250000h-125FFFFh
	BA292	64 kwords	1240000h-124FFFFh
	BA291	64 kwords	1230000h-123FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 6	BA290	64 kwords	1220000h-122FFFFh
	BA289	64 kwords	1210000h-121FFFFh
	BA288	64 kwords	1200000h-120FFFFh
Bank 7	BA287	64 kwords	11F0000h-11FFFFFh
	BA286	64 kwords	11E0000h-11EFFFFh
	BA285	64 kwords	11D0000h-11DFFFFh
	BA284	64 kwords	11C0000h-11CFFFFh
	BA283	64 kwords	11B0000h-11BFFFFh
	BA282	64 kwords	11A0000h-11AFFFFh
	BA281	64 kwords	1190000h-119FFFFh
	BA280	64 kwords	1180000h-118FFFFh
	BA279	64 kwords	1170000h-117FFFFh
	BA278	64 kwords	1160000h-116FFFFh
	BA277	64 kwords	1150000h-115FFFFh
	BA276	64 kwords	1140000h-114FFFFh
	BA275	64 kwords	1130000h-113FFFFh
	BA274	64 kwords	1120000h-112FFFFh
	BA273	64 kwords	1110000h-111FFFFh
	BA272	64 kwords	1100000h-110FFFFh
	BA271	64 kwords	10F0000h-10FFFFFh
	BA270	64 kwords	10E0000h-10EFFFFh
	BA269	64 kwords	10D0000h-10DFFFFh
	BA268	64 kwords	10C0000h-10CFFFFh
	BA267	64 kwords	10B0000h-10BFFFFh
	BA266	64 kwords	10A0000h-10AFFFFh
	BA265	64 kwords	1090000h-109FFFFh
	BA264	64 kwords	1080000h-108FFFFh
	BA263	64 kwords	1070000h-107FFFFh
	BA262	64 kwords	1060000h-106FFFFh
	BA261	64 kwords	1050000h-105FFFFh
	BA260	64 kwords	1040000h-104FFFFh
	BA259	64 kwords	1030000h-103FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 7	BA258	64 kwords	1020000h-102FFFFh
	BA257	64 kwords	1010000h-101FFFFh
	BA256	64 kwords	1000000h-100FFFFh
Bank 8	BA255	64 kwords	0FF0000h-0FFFFFFh
	BA254	64 kwords	0FE0000h-0FEFFFFh
	BA253	64 kwords	0FD0000h-0FDFFFFh
	BA252	64 kwords	0FC0000h-0FCFFFFh
	BA251	64 kwords	0FB0000h-0FBFFFFh
	BA250	64 kwords	0FA0000h-0FAFFFFh
	BA249	64 kwords	0F90000h-0F9FFFFh
	BA248	64 kwords	0F80000h-0F8FFFFh
	BA247	64 kwords	0F70000h-0F7FFFFh
	BA246	64 kwords	0F60000h-0F6FFFFh
	BA245	64 kwords	0F50000h-0F5FFFFh
	BA244	64 kwords	0F40000h-0F4FFFFh
	BA243	64 kwords	0F30000h-0F3FFFFh
	BA242	64 kwords	0F20000h-0F2FFFFh
	BA241	64 kwords	0F10000h-0F1FFFFh
	BA240	64 kwords	0F00000h-0F0FFFFh
	BA239	64 kwords	0EF0000h-0EFFFFFh
	BA238	64 kwords	0EE0000h-0EEFFFFh
	BA237	64 kwords	0ED0000h-0EDFFFFh
	BA236	64 kwords	0EC0000h-0ECFFFFh
	BA235	64 kwords	0EB0000h-0EBFFFFh
	BA234	64 kwords	0EA0000h-0EAFFFFh
	BA233	64 kwords	0E90000h-0E9FFFFh
	BA232	64 kwords	0E80000h-0E8FFFFh
	BA231	64 kwords	0E70000h-0E7FFFFh
	BA230	64 kwords	0E60000h-0E6FFFFh
	BA229	64 kwords	0E50000h-0E5FFFFh
	BA228	64 kwords	0E40000h-0E4FFFFh
	BA227	64 kwords	0E30000h-0E3FFFFh
	BA226	64 kwords	0E20000h-0E2FFFFh
	BA225	64 kwords	0E10000h-0E1FFFFh
	BA224	64 kwords	0E00000h-0E0FFFFh
Bank 9	BA223	64 kwords	0DF0000h-0DFFFFFh
	BA222	64 kwords	0DE0000h-0DEFFFFh
	BA221	64 kwords	0DD0000h-0DDFFFFh
	BA220	64 kwords	0DC0000h-0DCFFFFh
	BA219	64 kwords	0DB0000h-0DBFFFFh
	BA218	64 kwords	0DA0000h-0DAFFFFh
	BA217	64 kwords	0D90000h-0D9FFFFh
	BA216	64 kwords	0D80000h-0D8FFFFh
	BA215	64 kwords	0D70000h-0D7FFFFh
	BA214	64 kwords	0D60000h-0D6FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 9	BA213	64 kwords	0D50000h-0D5FFFFh
	BA212	64 kwords	0D40000h-0D4FFFFh
	BA211	64 kwords	0D30000h-0D3FFFFh
	BA210	64 kwords	0D20000h-0D2FFFFh
	BA209	64 kwords	0D10000h-0D1FFFFh
	BA208	64 kwords	0D00000h-0D0FFFFh
	BA207	64 kwords	0CF0000h-0CFFFFFh
	BA206	64 kwords	0CE0000h-0CEFFFFh
	BA205	64 kwords	0CD0000h-0CDFFFFh
	BA204	64 kwords	0CC0000h-0CCFFFFh
	BA203	64 kwords	0CB0000h-0CBFFFFh
	BA202	64 kwords	0CA0000h-0CAFFFFh
	BA201	64 kwords	0C90000h-0C9FFFFh
	BA200	64 kwords	0C80000h-0C8FFFFh
	BA199	64 kwords	0C70000h-0C7FFFFh
	BA198	64 kwords	0C60000h-0C6FFFFh
	BA197	64 kwords	0C50000h-0C5FFFFh
	BA196	64 kwords	0C40000h-0C4FFFFh
	BA195	64 kwords	0C30000h-0C3FFFFh
	BA194	64 kwords	0C20000h-0C2FFFFh
	BA193	64 kwords	0C10000h-0C1FFFFh
	BA192	64 kwords	0C00000h-0C0FFFFh
Bank 10	BA191	64 kwords	0BF0000h-0BFFFFFh
	BA190	64 kwords	0BE0000h-0BEFFFFh
	BA189	64 kwords	0BD0000h-0BDFFFFh
	BA188	64 kwords	0BC0000h-0BCFFFFh
	BA187	64 kwords	0BB0000h-0BBFFFFh
	BA186	64 kwords	0BA0000h-0BAFFFFh
	BA185	64 kwords	0B90000h-0B9FFFFh
	BA184	64 kwords	0B80000h-0B8FFFFh
	BA183	64 kwords	0B70000h-0B7FFFFh
	BA182	64 kwords	0B60000h-0B6FFFFh
	BA181	64 kwords	0B50000h-0B5FFFFh
	BA180	64 kwords	0B40000h-0B4FFFFh
	BA179	64 kwords	0B30000h-0B3FFFFh
	BA178	64 kwords	0B20000h-0B2FFFFh
	BA177	64 kwords	0B10000h-0B1FFFFh
	BA176	64 kwords	0B00000h-0B0FFFFh
	BA175	64 kwords	0AF0000h-0AFFFFFh
	BA174	64 kwords	0AE0000h-0AEFFFFh
	BA173	64 kwords	0AD0000h-0ADFFFFh
	BA172	64 kwords	0AC0000h-0ACFFFFh
	BA171	64 kwords	0AB0000h-0ABFFFFh
	BA170	64 kwords	0AA0000h-0AAFFFFh
	BA169	64 kwords	0A90000h-0A9FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 10	BA168	64 kwords	0A80000h-0A8FFFFh
	BA167	64 kwords	0A70000h-0A7FFFFh
	BA166	64 kwords	0A60000h-0A6FFFFh
	BA165	64 kwords	0A50000h-0A5FFFFh
	BA164	64 kwords	0A40000h-0A4FFFFh
	BA163	64 kwords	0A30000h-0A3FFFFh
	BA162	64 kwords	0A20000h-0A2FFFFh
	BA161	64 kwords	0A10000h-0A1FFFFh
	BA160	64 kwords	0A00000h-0A0FFFFh
Bank 11	BA159	64 kwords	09F0000h-09FFFFFh
	BA158	64 kwords	09E0000h-09EFFFFh
	BA157	64 kwords	09D0000h-09DFFFFh
	BA156	64 kwords	09C0000h-09CFFFFh
	BA155	64 kwords	09B0000h-09BFFFFh
	BA154	64 kwords	09A0000h-09AFFFFh
	BA153	64 kwords	0990000h-099FFFFh
	BA152	64 kwords	0980000h-098FFFFh
	BA151	64 kwords	0970000h-097FFFFh
	BA150	64 kwords	0960000h-096FFFFh
	BA149	64 kwords	0950000h-095FFFFh
	BA148	64 kwords	0940000h-094FFFFh
	BA147	64 kwords	0930000h-093FFFFh
	BA146	64 kwords	0920000h-092FFFFh
	BA145	64 kwords	0910000h-091FFFFh
	BA144	64 kwords	0900000h-090FFFFh
	BA143	64 kwords	08F0000h-08FFFFFh
	BA142	64 kwords	08E0000h-08EFFFFh
	BA141	64 kwords	08D0000h-08DFFFFh
	BA140	64 kwords	08C0000h-08CFFFFh
	BA139	64 kwords	08B0000h-08BFFFFh
	BA138	64 kwords	08A0000h-08AFFFFh
	BA137	64 kwords	0890000h-089FFFFh
	BA136	64 kwords	0880000h-088FFFFh
	BA135	64 kwords	0870000h-087FFFFh
	BA134	64 kwords	0860000h-086FFFFh
	BA133	64 kwords	0850000h-085FFFFh
	BA132	64 kwords	0840000h-084FFFFh
	BA131	64 kwords	0830000h-083FFFFh
	BA130	64 kwords	0820000h-082FFFFh
	BA129	64 kwords	0810000h-081FFFFh
	BA128	64 kwords	0800000h-080FFFFh
Bank 12	BA127	64 kwords	07F0000h-07FFFFFh
	BA126	64 kwords	07E0000h-07EFFFFh
	BA125	64 kwords	07D0000h-07DFFFFh
	BA124	64 kwords	07C0000h-07CFFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 12	BA123	64 kwords	07B0000h-07BFFFFh
	BA122	64 kwords	07A0000h-07AFFFFh
	BA121	64 kwords	0790000h-079FFFFh
	BA120	64 kwords	0780000h-078FFFFh
	BA119	64 kwords	0770000h-077FFFFh
	BA118	64 kwords	0760000h-076FFFFh
	BA117	64 kwords	0750000h-075FFFFh
	BA116	64 kwords	0740000h-074FFFFh
	BA115	64 kwords	0730000h-073FFFFh
	BA114	64 kwords	0720000h-072FFFFh
	BA113	64 kwords	0710000h-071FFFFh
	BA112	64 kwords	0700000h-070FFFFh
	BA111	64 kwords	06F0000h-06FFFFFh
	BA110	64 kwords	06E0000h-06EFFFFh
	BA109	64 kwords	06D0000h-06DFFFFh
	BA108	64 kwords	06C0000h-06CFFFFh
	BA107	64 kwords	06B0000h-06BFFFFh
	BA106	64 kwords	06A0000h-06AFFFFh
	BA105	64 kwords	0690000h-069FFFFh
	BA104	64 kwords	0680000h-068FFFFh
	BA103	64 kwords	0670000h-067FFFFh
	BA102	64 kwords	0660000h-066FFFFh
	BA101	64 kwords	0650000h-065FFFFh
	BA100	64 kwords	0640000h-064FFFFh
	BA99	64 kwords	0630000h-063FFFFh
	BA98	64 kwords	0620000h-062FFFFh
	BA97	64 kwords	0610000h-061FFFFh
	BA96	64 kwords	0600000h-060FFFFh
Bank13	BA95	64 kwords	05F0000h-05FFFFFh
	BA94	64 kwords	05E0000h-05EFFFFh
	BA93	64 kwords	05D0000h-05DFFFFh
	BA92	64 kwords	05C0000h-05CFFFFh
	BA91	64 kwords	05B0000h-05BFFFFh
	BA90	64 kwords	05A0000h-05AFFFFh
	BA89	64 kwords	0590000h-059FFFFh
	BA88	64 kwords	0580000h-058FFFFh
	BA87	64 kwords	0570000h-057FFFFh
	BA86	64 kwords	0560000h-056FFFFh
	BA85	64 kwords	0550000h-055FFFFh
	BA84	64 kwords	0540000h-054FFFFh
	BA83	64 kwords	0530000h-053FFFFh
	BA82	64 kwords	0520000h-052FFFFh
	BA81	64 kwords	0510000h-051FFFFh
	BA80	64 kwords	0500000h-050FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 13	BA79	64 kwords	04F0000h-04FFFFFh
	BA78	64 kwords	04E0000h-04EFFFFh
	BA77	64 kwords	04D0000h-04DFFFFh
	BA76	64 kwords	04C0000h-04CFFFFh
	BA75	64 kwords	04B0000h-04BFFFFh
	BA74	64 kwords	04A0000h-04AFFFFh
	BA73	64 kwords	0490000h-049FFFFh
	BA72	64 kwords	0480000h-048FFFFh
	BA71	64 kwords	0470000h-047FFFFh
	BA70	64 kwords	0460000h-046FFFFh
	BA69	64 kwords	0450000h-045FFFFh
	BA68	64 kwords	0440000h-044FFFFh
	BA67	64 kwords	0430000h-043FFFFh
	BA66	64 kwords	0420000h-042FFFFh
	BA65	64 kwords	0410000h-041FFFFh
	BA64	64 kwords	0400000h-040FFFFh
Bank 14	BA63	64 kwords	03F0000h-03FFFFFh
	BA62	64 kwords	03E0000h-03EFFFFh
	BA61	64 kwords	03D0000h-03DFFFFh
	BA60	64 kwords	03C0000h-03CFFFFh
	BA59	64 kwords	03B0000h-03BFFFFh
	BA58	64 kwords	03A0000h-03AFFFFh
	BA57	64 kwords	0390000h-039FFFFh
	BA56	64 kwords	0380000h-038FFFFh
	BA55	64 kwords	0370000h-037FFFFh
	BA54	64 kwords	0360000h-036FFFFh
	BA53	64 kwords	0350000h-035FFFFh
	BA52	64 kwords	0340000h-034FFFFh
	BA51	64 kwords	0330000h-033FFFFh
	BA50	64 kwords	0320000h-032FFFFh
	BA49	64 kwords	0310000h-031FFFFh
	BA48	64 kwords	0300000h-030FFFFh
	BA47	64 kwords	02F0000h-02FFFFFh
	BA46	64 kwords	02E0000h-02EFFFFh
	BA45	64 kwords	02D0000h-02DFFFFh
	BA44	64 kwords	02C0000h-02CFFFFh
	BA43	64 kwords	02B0000h-02BFFFFh
	BA42	64 kwords	02A0000h-02AFFFFh
	BA41	64 kwords	0290000h-029FFFFh
	BA40	64 kwords	0280000h-028FFFFh
	BA39	64 kwords	0270000h-027FFFFh
	BA38	64 kwords	0260000h-026FFFFh
	BA37	64 kwords	0250000h-025FFFFh
	BA36	64 kwords	0240000h-024FFFFh
	BA35	64 kwords	0230000h-023FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 14	BA34	64 kwords	0220000h-022FFFFh
	BA33	64 kwords	0210000h-021FFFFh
	BA32	64 kwords	0200000h-020FFFFh
Bank 15	BA31	64 kwords	01F0000h-01FFFFFh
	BA30	64 kwords	01E0000h-01EFFFFh
	BA29	64 kwords	01D0000h-01DFFFFh
	BA28	64 kwords	01C0000h-01CFFFFh
	BA27	64 kwords	01B0000h-01BFFFFh
	BA26	64 kwords	01A0000h-01AFFFFh
	BA25	64 kwords	0190000h-019FFFFh
	BA24	64 kwords	0180000h-018FFFFh
	BA23	64 kwords	0170000h-017FFFFh
	BA22	64 kwords	0160000h-016FFFFh
	BA21	64 kwords	0150000h-015FFFFh
	BA20	64 kwords	0140000h-014FFFFh
	BA19	64 kwords	0130000h-013FFFFh
	BA18	64 kwords	0120000h-012FFFFh
	BA17	64 kwords	0110000h-011FFFFh
	BA16	64 kwords	0100000h-010FFFFh
	BA15	64 kwords	00F0000h-00FFFFFh
	BA14	64 kwords	00E0000h-00EFFFFh
	BA13	64 kwords	00D0000h-00DFFFFh
	BA12	64 kwords	00C0000h-00CFFFFh
	BA11	64 kwords	00B0000h-00BFFFFh
	BA10	64 kwords	00A0000h-00AFFFFh
	BA9	64 kwords	0090000h-009FFFFh
	BA8	64 kwords	0080000h-008FFFFh
	BA7	64 kwords	0070000h-007FFFFh
	BA6	64 kwords	0060000h-006FFFFh
	BA5	64 kwords	0050000h-005FFFFh
	BA4	64 kwords	0040000h-004FFFFh
	BA3	64 kwords	0030000h-003FFFFh
	BA2	64 kwords	0020000h-002FFFFh
	BA1	64 kwords	0010000h-001FFFFh
	BA0	64 kwords	0000000h-000FFFFh

[Table 21] Uniform OTP Block Addresses

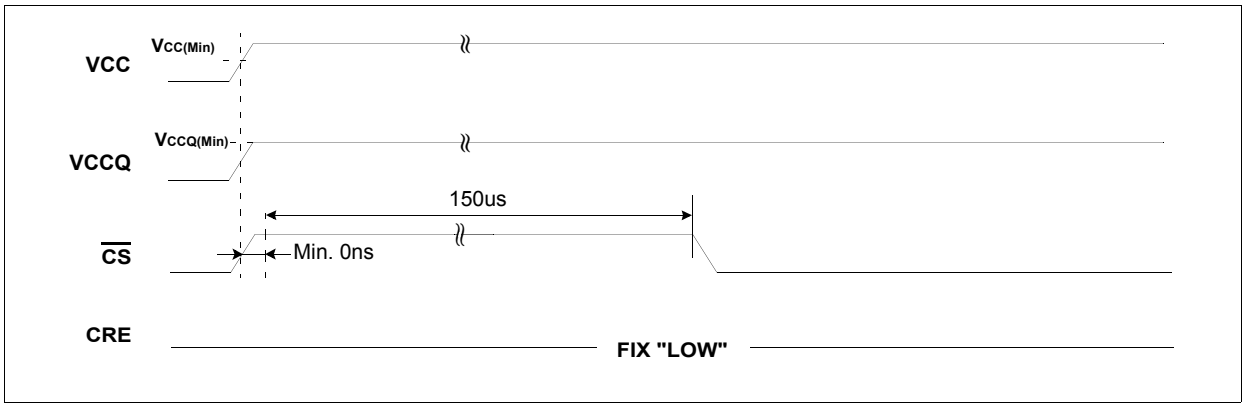
OTP	Block Address A24 ~ A8	Block Size	(x16) Address Range*
	1FFFFh	512 words	1FFFE00h-1FFFFFFh

After entering OTP Block, any issued addresses should be in the range of OTP block address.

128Mb (8M x16) Mux UtRAM2 C-die

1.0 POWER UP SEQUENCE

After V_{CC} and V_{CCQ} reach minimum operating voltage(1.7V), drive $\overline{CS}$ High. Then the device gets into the Power Up mode. Wait for minimum 150μs to get into the normal operation mode. During the Power Up mode, the standby current can not be guaranteed. To get the appropriate device operation, be sure to keep the following power up sequence. Asynch. mode is default mode and is set up after power up.



2.0 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to VCCQ+0.3V	V
Power supply voltage relative to Vss	V_{CC}, V_{CCQ}	-0.2 to 2.5V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-55 to 150	°C
Operating Temperature	T_A	-25 to 85	°C

NOTE :
1) Stresses greater than "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

3.0 RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage(Core)	V_{CC}	1.7	1.8	1.95	V
Power supply voltage(I/O)	V_{CCQ}	1.7	1.8	1.95	V
Ground	V_{SS}, V_{SSQ}	0	0	0	V
Input high voltage	V_{IH}	V_{CCQ}-0.4	-	V_{CCQ}+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.4	V

NOTE :
1) T_A= -25 to 85°C, otherwise specified.
2) Overshoot: V_{CCQ} +1.0V in case of pulse width ≤20ns. Overshoot is sampled, not 100% tested.
3) Undershoot: -1.0V in case of pulse width ≤20ns. Undershoot is sampled, not 100% tested.

4.0 CAPACITANCE

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	6	pF

NOTE :
1) Freq.=1MHz, T_A=25°C
2) Capacitance is sampled, not 100% tested.

5.0 DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions			Min	Typ	Max	Unit
Input Leakage Current		I_{LI}	$V_{IN}=V_{SS}$ to V_{CCQ}			-2	-	2	μA
Output Leakage Current		I_{LO}	$\overline{CS}=V_{IH}$, CRE=V_{IL}, $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{IO}=V_{SS}$ to V_{CCQ}			-5	-	5	μA
Average Operating Current (Async)		I_{CC2} 6)	Cycle time=min t_{RC}/min t_{WC}, I_{IO}=0mA 4), 100% duty, $\overline{CS}=V_{IL}$, CRE=V_{IL}, $V_{IN}=V_{IL}$ or V_{IH}			-	-	30	mA
Average Operating Current (Burst)	108Mhz	I_{CC3I}	V_{IN} = V_{CCQ} or 0V $\overline{CS}=V_{IL}$, I_{IO}=0mA 4)			-	-	30	mA
		I_{CC3R}				-	-	40	mA
		I_{CC3W}				-	-	35	mA
	80Mhz	I_{CC3I}				-	-	30	mA
		I_{CC3R}				-	-	40	mA
		I_{CC3W}				-	-	35	mA
	66Mhz	I_{CC3I}				-	-	30	mA
		I_{CC3R}				-	-	40	mA
		I_{CC3W}				-	-	35	mA
Output Low Voltage		V_{OL}	I_{OL}=0.2mA			-	-	0.2	V
Output High Voltage		V_{OH}	I_{OH}=-0.2mA			0.8xV_{CCQ}	-	-	V
Standby Current(CMOS)		I_{SB1} 1)	$\overline{CS}$ and $\overline{ADV}$=V_{CCQ}, CRE=0V, Other inputs=0V or V_{CCQ} (Toggle is not allowed) 5)	< 40°C		-	-	160	μA
				< 85°C		-	-	200	μA
Partial Refresh Current		I_{SBP} 2)	$\overline{CS}$ and $\overline{ADV}$=V_{CCQ}, CRE=0V, Other inputs=0V or V_{CCQ} (Toggle is not allowed) 5)	< 40°C	1/2 Block	-	-	150	μA
					1/4 Block	-	-	140	
					1/8 Block	-	-	130	
				< 85°C	1/2 Block	-	-	180	μA
					1/4 Block	-	-	175	
					1/8 Block	-	-	170	

NOTE :
1) I_{SB1} is measured after 500ms after $\overline{CS}$ high. CLK should be fixed at high or at Low.
2) Full Array Partial Refresh Current(I_{SBP}) is same as Standby Current(I_{SB1}).
3) Internal TCSR (Temperature Compensated Self Refresh) is used to optimize refresh cycle below 40°C.
4) I_{IO}=0mA; This parameter is specified with the outputs disabled to avoid external loading effects.
5) V_{IN}=0V; all inputs should not be toggle.
6) This parameter is for page disable mode, Clock should not be inserted between $\overline{ADV}$ low and $\overline{WE}$ low during Write operation.

6.0 CRE (CONTROL REGISTER ENABLE)

The configuration register values are written via A/DQ pins. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of $\overline{ADV}$, $\overline{CS}$, or $\overline{WE}$, whichever occurs first; $\overline{LB}$ and $\overline{UB}$ are “Don’t Care.” For reads, address inputs other than A[19:18] are “Don’t Care,” and register bits 15:0 are output as data ($\overline{ADV}$ HIGH) on A/DQ[15:0]. Immediately after performing a configuration register READ or WRITE operation, reading the memory array is highly recommended.

6.1 Bus Configuration Register

The BCR defines how the device interacts with the system memory bus. The BCR is accessed with CRE HIGH and A[19:18] = 10b, or through the register access software sequence with A/DQ = 0001h on the third cycle.

A19~A18	A/DQ15	A/DQ14	A/DQ13~A/DQ11	A/DQ10	A/DQ8	A/DQ5~A/DQ4	A/DQ3	A/DQ2~A/DQ0
RS	OM	IL	LC	WP	WC	DS	BW	BL

Register Select			Operating Mode		Initial Latency		Latency Count			
A19	A18	RS	A/DQ15	OM	A/DQ14	IL	A/DQ13	A/DQ12	A/DQ11	LC
0	0	RCR	0	Synch.	0	Variable (default)	0	0	0	Reserved
1	0	BCR	1	Asynch (default)	1	Fixed	0	0	1	Reserved
0	1	DIDR					0	1	0	2
							0	1	1	3 (default)
							1	0	0	4
							1	0	1	5
							1	1	0	6
							1	1	1	Reserved

Wait Polarity		Wait Config.		Driver Strength			Burst Wrap		Burst Length			
A/DQ10	WP	A/DQ8	WC	A/DQ5	A/DQ4	DS	A/DQ3	BW	A/DQ2	A/DQ1	A/DQ0	BL
0	Active Low	0	at data	0	0	Full Drive	0	Wrap	0	0	1	4 word
1	Active High (default)	1	1 CLK prior (default)	0	1	1/2 Drive (default)	1	No Wrap (default)	0	1	0	8 word
				1	0	1/4 Drive			0	1	1	16 word
				1	1	1/8 Drive			1	0	0	32 word
									1	1	1	Continuous (default)

NOTE :
1) A/DQ6, A/DQ7, A/DQ9, A16, A17, A20~A22 are reserved and should be ’0’
2) The registers are set automatically to default value.
3) Refresh command will be denied during continuous operation. $\overline{CS}$ low should not be longer than tBC(tCSM max. 2.5us)
4) If the register code is invalid, register will be set to default value.

6.2 Refresh Configuration Register

The refresh configuration register (RCR) defines how the device performs its self refresh. Altering the refresh parameters can reduce current consumption during standby mode. The RCR is accessed with CRE HIGH and A[19:18] = 00b; or through the register access software sequence with A/DQ = 0000h on the third cycle.

A19~A18	A/DQ2~A/DQ0
RS	PAR

Register Select			Partial Refresh			
A19	A18	RS	A/DQ2	A/DQ1	A/DQ0	PAR
0	0	RCR	0	0	0	Full Array (default)
1	0	BCR	0	0	1	Bottom 1/2 Array
0	1	DIDR	0	1	0	Bottom 1/4 Array
			0	1	1	Bottom 1/8 Array
			1	0	0	None of Array
			1	0	1	Top 1/2 Array
			1	1	0	Top 1/4 Array
			1	1	1	Top 1/8 Array

NOTE :
1) A/DQ3, A/DQ5~A/DQ15, A16, A17, A20~A22 are reserved and should be '0'
2) The registers are set automatically to default value.

6.3 Burst Length (BCR[2:0]) Default = Continuous Burst

Burst lengths define the number of words the device outputs during burst READ and WRITE operations. The device supports a burst length of 4, 8, 16, or 32 words or Continuous.

6.4 Burst Wrap (BCR[3]) Default = No Wrap

The burst-wrap option determines if a 4-, 8-, 16-, or 32-word READ or WRITE burst wraps within the burst length, or steps through sequential addresses.

[Table 1] Sequence and Burst Length

Burst Wrap		Starting Address	4 word Burst Length	8 word Burst Length	16 word Burst Length	32 word Burst Length	Continuous Burst
BCR[3]	Wrap	Decimal	Linear	Linear	Linear	Linear	Linear
WRAP	Yes	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0 - 1 - 2 ~ 29-30-31	0 - 1 - 2 - 3 - 4 - 5 ~
		1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1 - 2 - 3 ~ 30-31 - 0	1 - 2 - 3 - 4 - 5 - 6 ~
		2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2 - 3 - 4 ~ 31 - 0 - 1	2 - 3 - 4 - 5 - 6 - 7 ~
		3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3 - 4 - 5 ~ 0 - 1 - 2	3 - 4 - 5 - 6 - 7 - 8 ~
		~		~	~	~	~
		7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7 - 8 - 9 ~ 4 - 5 - 6	7 - 8 - 9 - 10-11-12 ~
		~			~	~	~
		15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17 ~ 12- 13- 14	15-16-17-18-19-20 ~
		~				~	~
		31				31- 0 - 1 ~ 28-29-30	31-32-33-34-35-36 ~
No WRAP	No	0	0-1-2-3	0- 1- 2- 3- 4- 5- 6 -7	0- 1- 2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15	0 - 1 - 2 ~ 29-30-31	0 - 1 - 2 - 3 - 4 - 5 ~
		1	1-2-3-4	1- 2- 3- 4- 5- 6- 7- 8	1- 2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16	1 - 2 - 3 ~ 30-31-32	1 - 2 - 3 - 4 - 5 - 6 ~
		2	2-3-4-5	2- 3- 4- 5- 6- 7- 8- 9	2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16-17	2 - 3 - 4 ~ 31-32-33	2 - 3 - 4 - 5 - 6 - 7 ~
		3	3-4-5-6	3- 4- 5- 6- 7- 8- 9-10	3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16-17-18	3 - 4 - 5 ~ 32-33-34	3 - 4 - 5 - 6 - 7 - 8 ~
		~		~	~	~	~
		7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-15-16-17-18-19-20-21-22	7 - 8 - 9 ~ 36-37-38	7 - 8 - 9 - 10-11-12 ~
		~			~	~	~
		15			15-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30	15-16-17 ~ 44-45-46	15-16-17-18-19-20 ~
		~				~	~
		31				31-32-33 ~ 60-61-62	31-32-33-34-35-36 ~

6.5 Drive Strength (BCR[5:4]) Default = 1/2 Drive Strength

The optimization of output driver strength is possible to adjust for the different data loadings. The device can minimize the noise generated on the data bus during read operation. The device supports full, 1/2 and 1/4 driver strength. The device's default mode is 1/2 driver strength. Outputs are configured at 1/2 drive strength during testing.

[Table 2] Drive Strength

Driver Strength	Full	1 / 2	1 / 4	1 / 8
Impedance(typ.)	25~30Ω	50Ω	100Ω	TBD
Recommendation	CL = 30pF to 50pF	CL = 15pF to 30pF 108 MHz at light load	CL = 15pF or lower	CL = 15pF or lower

NOTE :
1) Impedance values are typical values, not 100% tested.

6.6 WAIT Configuration (BCR[8]) Default = 1 CLK Prior.

The $\overline{WAIT}$ signal is output signal indicating the status of the data on the bus whether or not it is valid. $\overline{WAIT}$ configuration is to decide the timing when $\overline{WAIT}$ asserts or desserts. $\overline{WAIT}$ asserts (or desserts) one clock prior to the data when A/DQ8 is set to 1. ($\overline{WAIT}$ asserts (or desserts) at data clock when A/DQ8 is set to 0). $\overline{WAIT}$ polarity is to decide the $\overline{WAIT}$ signal level at which data is valid or invalid. Data is valid if $\overline{WAIT}$ signal is high when A/DQ10 is set to 0. (Data is valid if $\overline{WAIT}$ signal is low when A/DQ10 is set to 1). All the timing diagrams in this SPEC are illustrated based on following setup; A/DQ[10]:0 and A/DQ[8]:1.
Below timing shows $\overline{WAIT}$ signal's movement when word boundary crossing happens in No-wrap mode

6.7 WAIT Polarity (BCR[10]) Default = Active HIGH

The WAIT polarity bit indicates whether an asserted WAIT output should be HIGH or LOW. This bit will determine whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state.

No-Wrap. Word-line Crossing. LATENCY : 2. WP : Low Enable

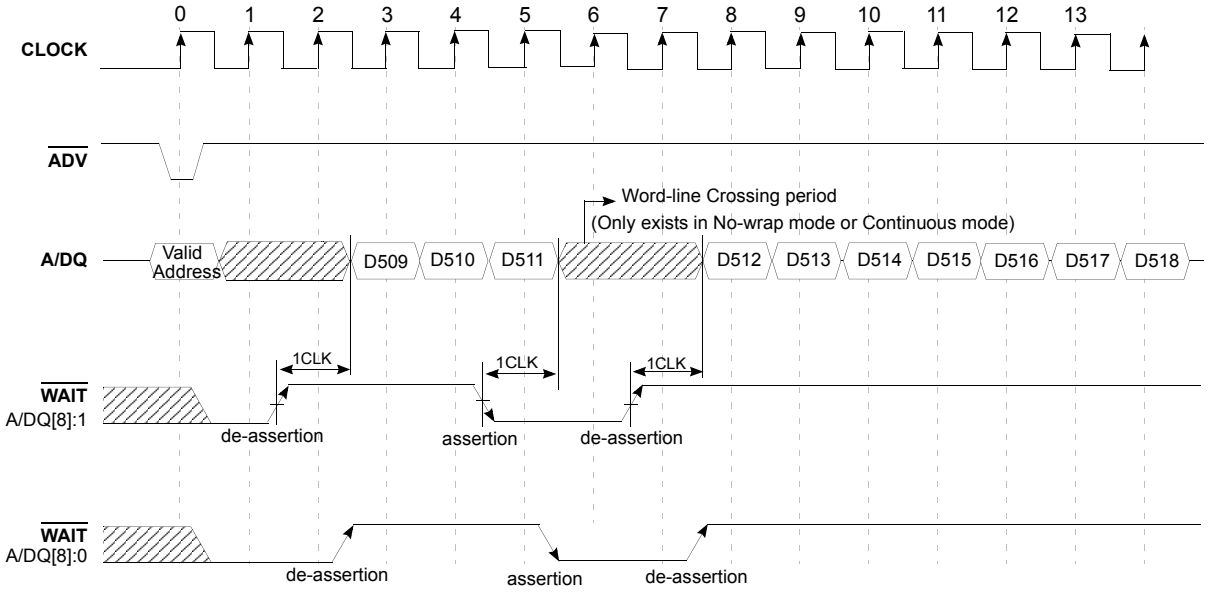


Figure 1. WAIT Configuration During Burst Operation

NOTE :
1)Non-default BCR setting: WAIT active LOW.

6.8 Operating Mode (BCR[15]) Default = Asynchronous Operation

The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.

6.9 Latency Counter (BCR[13:11]) Default = 3 Clock Latency

The latency counter bits determine how many clocks occur between the beginning of a READ or WRITE operation and the first data value transferred. For allowable latency codes.

6.10 Initial Access Latency (BCR[14]) Default = Variable

Variable initial access latency outputs data after the number of clocks set by the latency counter. However, WAIT must be monitored to detect delays caused by collisions with refresh operations. Fixed initial access latency outputs the first data at a consistent time that allows for worst-case refresh collisions. The latency counter must be configured to match the initial latency and the clock frequency. It is not necessary to monitor WAIT with fixed initial latency. The burst begins after the number of clock cycles configured by the latency counter.

[Table 3] Variable Latency Configuration Codes

BCR[13:11]	Latency Configuration	Latency		Max Input CLK Frequency (MHz)		
		Normal	Refresh Collision	108	80	66
010	2(3 clocks)	2	4	66(15ns)	19,2ns	40(25ns)
011	3(4 clocks)-default	3	6	108(9.26ns)	80(12.5ns)	66(15ns)
Others	Reserved	-	-	-	-	-

[Table 4] Fixed Latency Configuration Codes

BCR[13:11]	Latency Configuration	Latency Count (N)	Max Input CLK Frequency (MHz)		
			108	80	66
010	2 (3 clocks)	2	33 (30ns)	20 (50ns)	20 (50ns)
011	3 (4 clocks)	3	52 (19.2ns)	40 (25ns)	33 (30ns)
100	4 (5 clocks)	4	66 (15ns)	52 (19.2ns)	40 (25ns)
101	5 (6 clocks)	5	80 (12.5ns)	66 (15ns)	52 (19.2ns)
110	6 (7 clocks)	6	108 (9.26ns)	80 (12.5ns)	66 (15ns)
Others	Reserved	-	-	-	-

NOTE :
1) Latency is the number of clock cycles from the initiation of a burst operation until data appears. Data is transferred on the next clock cycle.

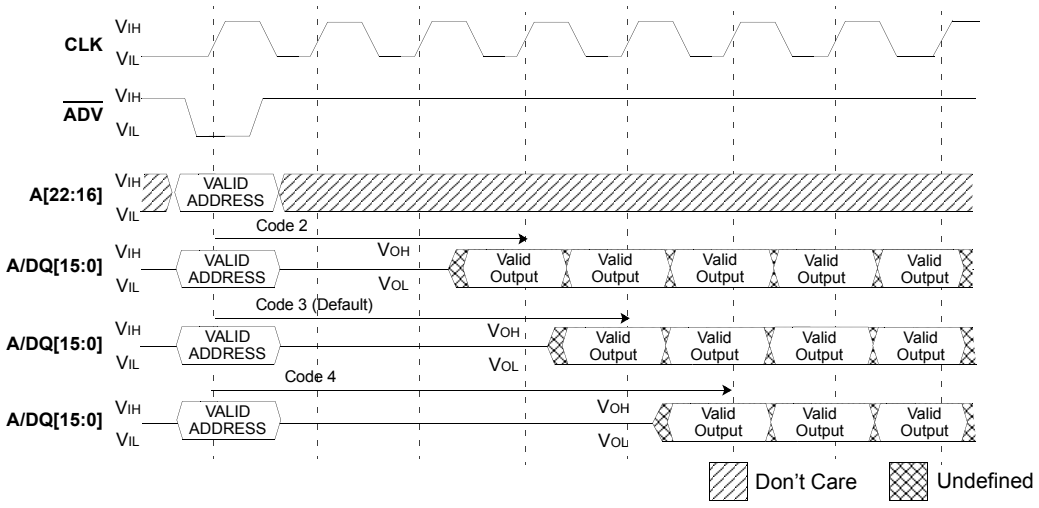


Figure 2. Latency Counter (Variable Initial Latency, No Refresh Collision)

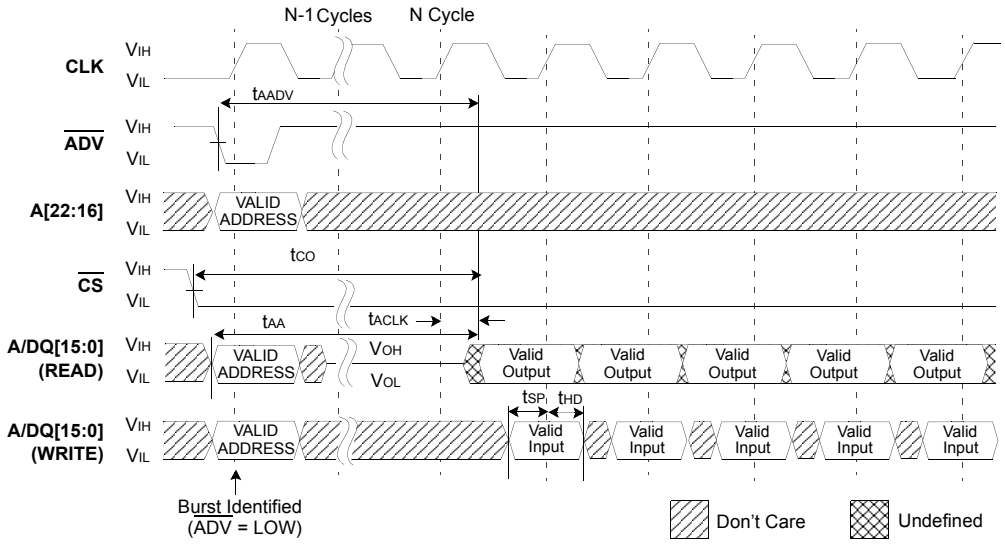


Figure 3. Latency Counter (Fixed Latency)

6.11 Partial Array Refresh (RCR[2:0] Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map.

[Table 5] Address Patterns for PAR (RCR[4] = 1)

RCR[2]	RCR[1]	RCR[0]	Active Section	Address Space	Size	Density
0	0	0	Full Die	000000h-7FFFFFh	8 Meg x 16	128Mb
0	0	1	One-half die	000000h-3FFFFFh	4 Meg x 16	64Mb
0	1	0	One-quarter of die	000000h-1FFFFFh	2 Meg x 16	32Mb
0	1	1	One-eighth of die	000000h-0FFFFFh	1 Meg x 16	16Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	400000h-7FFFFFh	4 Meg x 16	64Mb
1	1	0	One-quarter of die	600000h-7FFFFFh	2 Meg x 16	32Mb
1	1	1	One-eighth of die	700000h-7FFFFFh	1 Meg x 16	16Mb

6.12 Device Identification Register

The DIDR provides information on the device manufacturer, generation and the specific device configuration. This register is read-only. The DIDR is accessed with CRE HIGH and A[19:18] = 01b, or through the register access software sequence with A/DQ = 0002h on the third cycle.

[Table 6] Device Identification Register Mapping

Bit Field	DIDR[15]		DIDR[14:11]		DIDR[10:8])		DIDR[7:5]		DIDR[4:0]
Field name	Row Length		Device version		Device density		UtRAM generation		Vendor ID
	Length	Bit Setting	Version	Bit Setting	Density	Bit Setting	Generation	Bit Setting	Bit Setting
Options	512 words	1b	4th	0110	128Mb	011b	UtRAM2	010b	01100

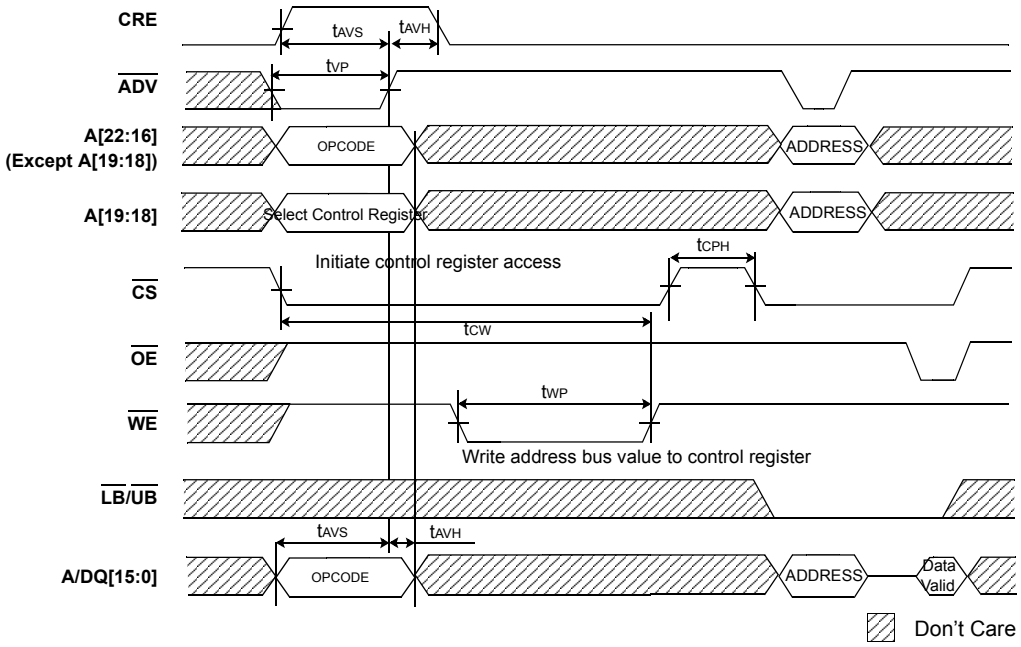


Figure 4. Configuration Register WRITE, Asynchronous Mode, Followed by READ ARRAY Operation

NOTE :
1) A[19:18] = 00b to load RCR, and 10b to load BCR.

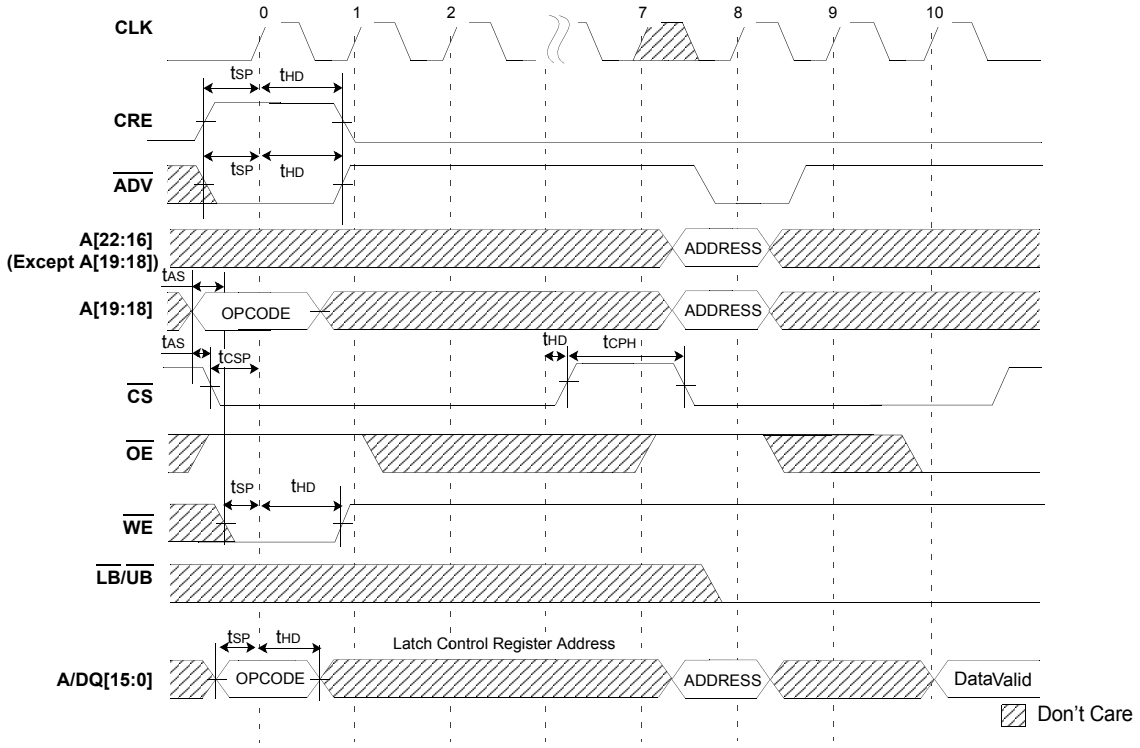


Figure 5. Configuration Register WRITE, Synchronous Mode Followed by READ ARRAY Operation

NOTE :
1) Non-default BCR settings for synchronous mode configuration register WRITE followed by READ ARRAY operation:
WAIT active LOW; WAIT asserted during delay.
2) A[19:18] = 00b to load RCR, and 10b to load BCR.
3) CS must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CS LOW cycles.

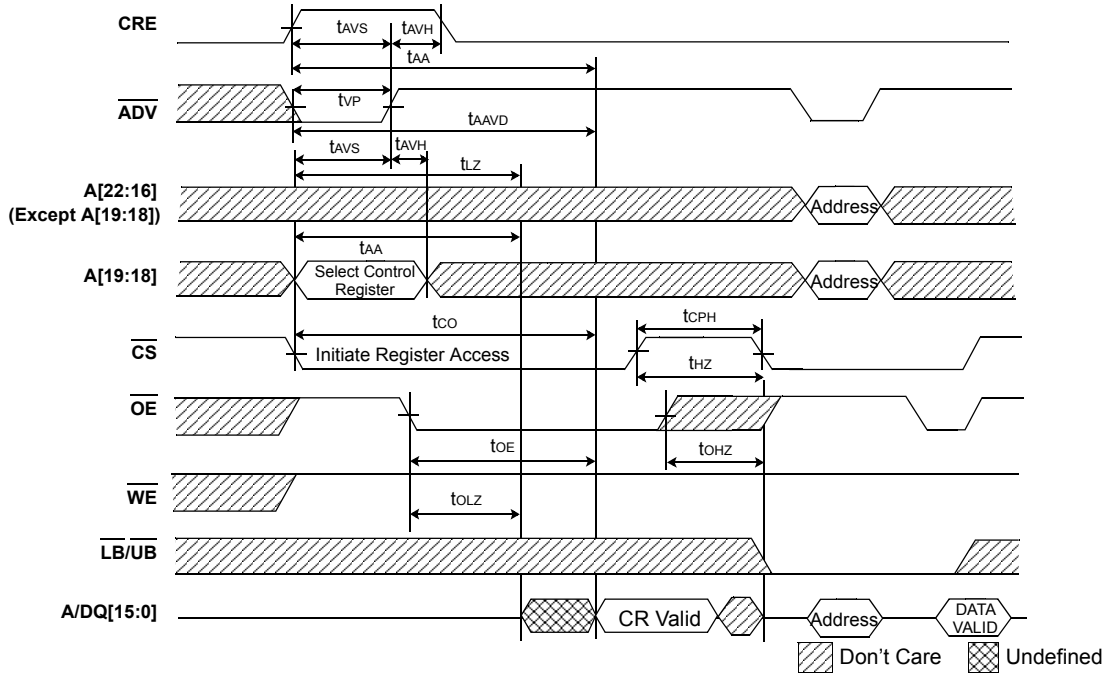


Figure 6. Register READ, Asynchronous Mode Followed by READ ARRAY Operation

NOTE :
1) A[19:18] = 00b to read RCR, 10b to read BCR, and 01b to read DIDR.

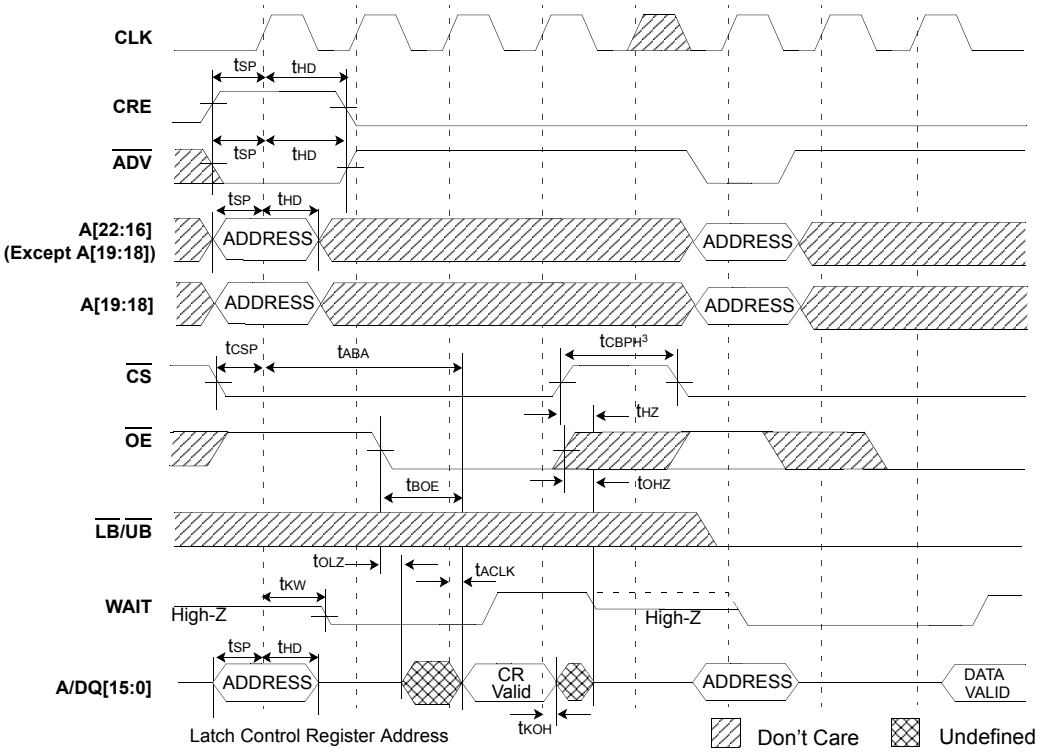


Figure 7. Register READ, Synchronous Mode Followed by READ ARRAY Operation

NOTE :
1) Non-default BCR settings for synchronous mode register READ followed by READ ARRAY operation: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2) A[19:18] = 00b to read RCR, 10b to read BCR, and 01b to read DIDR.
3) $\overline{CS}$ must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional $\overline{CS}$ LOW cycles.

6.13 Software Access

Software access of the registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be modified and all registers can be read using the software sequence. The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations. The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation. The address used during all READ and WRITE operations is the highest address of the device being accessed (3FFFFF); the contents of this address are not changed by using this sequence. The data value presented during the third operation (WRITE) in the sequence defines whether the BCR, RCR, or the DIDR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR; if the data is 0002h, the sequence will access the DIDR. During the fourth operation, A/DQ[15:0] transfer data in to or out of bits 15–0 of the registers. The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for CRE. If the software mechanism is used, CRE can simply be tied to VSS. The port line often used for CRE control purposes is no longer required.

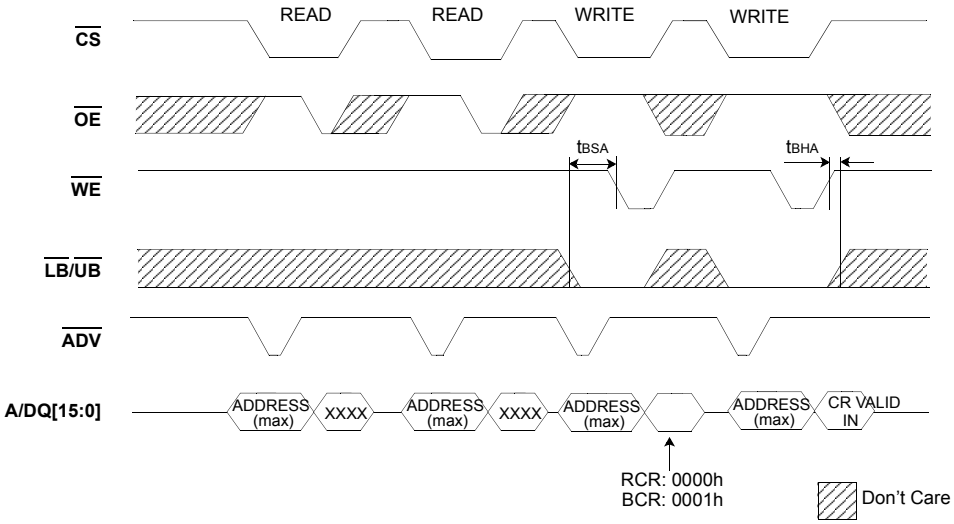


Figure 8. Load Configuration Register

NOTE :
1) /WE should be deasserted before /CS deasserting.

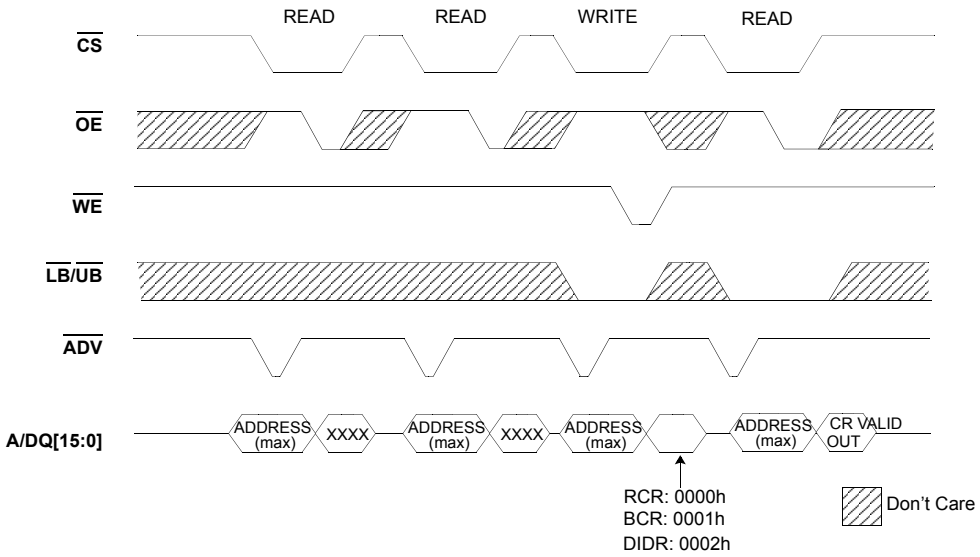


Figure 9. Read Configuration Register

NOTE :
1) /WE should be deasserted before /CS deasserting.
2) ALL Write Operation have tBSA, tBHA.

7.0 BUS OPERATING MODES

The bus interface supports asynchronous and burst mode read and write transfers. The specific interface supported is defined by the value loaded into the BCR.

7.1 Asynchronous Mode (default mode)

7.1.1 Asynchronous read operation

Asynchronous read operation starts when $\overline{CS}$, $\overline{OE}$ and $\overline{UB}$ or $\overline{LB}$ are asserted. $\overline{ADV}$ can be taken HIGH to capture the address. First data will be driven out of the A/DQ bus after random access time(tAA). $\overline{WE}$ should be de-asserted during read operation. The CLK input must be held static LOW during read operation. WAIT will be driven while the device is enabled and its state should be ignored.

7.1.2 Asynchronous write operation

Asynchronous write operation starts when $\overline{CS}$, $\overline{WE}$ and $\overline{UB}$ or $\overline{LB}$ are asserted. The data to be written is latched on the rising edge of $\overline{CS}$, $\overline{WE}$, or $\overline{LB}$/$\overline{UB}$ (whichever occurs first). $\overline{OE}$ is High during write operation. $\overline{WE}$ LOW time must be limited to tCSM. The CLK input must be held static LOW during write operation. $\overline{WAIT}$ signal is Hi-Z.

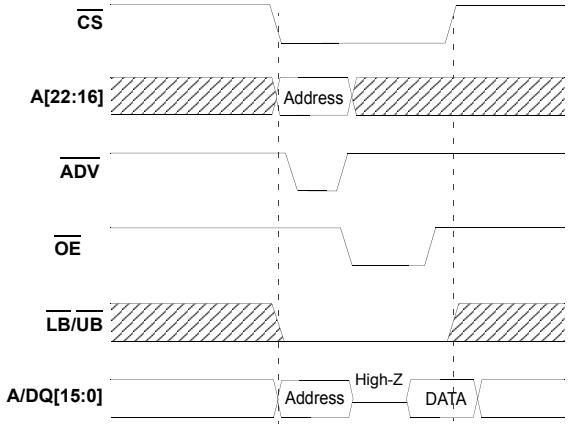


Figure 10. READ Operation $\overline{WE}$ = HIGH).

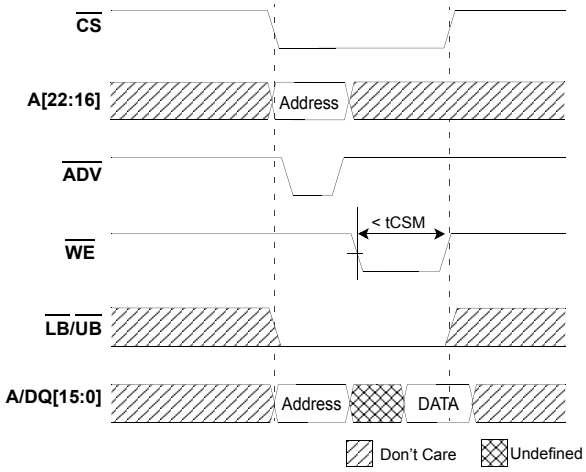


Figure 11. WRITE Operation $\overline{OE}$ = HIGH)

7.2 Functional Description (Asynch. mode)

Asynchfonous Mode BCR[15] = 1	Power	CLK	$\overline{ADV}$	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	CRE	UB / LB	WAIT	A/DQ[15:0]	Notes
Read	Active	L	⊓	L	L	H	L	L	Low-Z	Data out	1
Write	Active	L	⊓	L	H	L	L	L	Low-Z	Data in	1
Standby	Standby	L	H	H	X	X	L	X	High-Z	High-Z	2
No operation	Idle	L	X	L	X	X	L	X	Low-Z	X	1
Configuration register write	Active	L	L	L	H	L	H	X	Low-Z	High-Z	
Configuration register read	Active	L	⊓	L	L	H	H	L	Low-Z	Config. Reg.out	

NOTE :
1) The device will consume active power in this mode whenever addresses are changed.
2) When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.

8.0 Burst Mode Operation

8.1 synchronous Mode

8.1.1 Synchronous Burst Read Operation

Burst Read command is implemented when $\overline{ADV}$ is detected low at clock rising edge. $\overline{WE}$ should be de-asserted. Burst operation re-starts whenever $\overline{ADV}$ is detected low at clock rising edge even in the middle of operation.

8.1.2 Synchronous Burst Write Operation

Burst Write command is implemented when $\overline{ADV}$ & $\overline{WE}$ are detected low at clock rising edge. Burst Write operation re-starts whenever $\overline{ADV}$ is detected low at clock rising edge even in the middle of Burst Write operation.

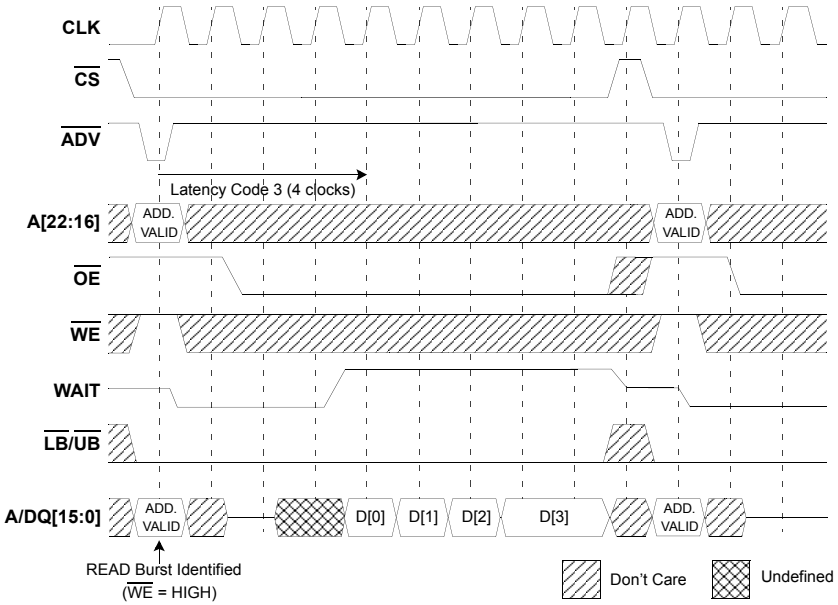


Figure 12. Burst Mode READ (4-word burst)

NOTE :
1) Non-default BCR settings for burst mode READ (4-word burst): Fixed or variable latency;
2) Latency code 3 (4 clocks); WAIT active LOW; WAIT asserted during delay.
3) Diagram in the figure above is representative of variable latency with no refresh collision or fixed-latency access.

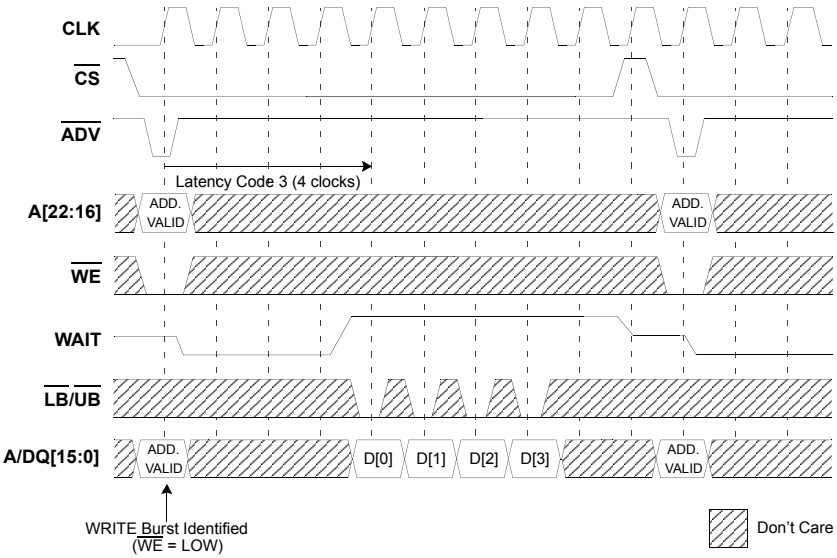


Figure 13. Burst Mode WRITE (4-word burst)

NOTE :
1) Non-default BCR settings for burst mode WRITE (4-word burst): Fixed or variable latency;
2) Latency code 3 (4 clocks); WAIT active LOW; WAIT asserted during delay.
3) tAS is need to Burst Write Operation.

The size of a burst can be specified in the BCR either as a fixed length or continuous. Fixed-length bursts consist of four, eight, sixteen, or thirty-two words. The initial latency for READ operations can be configured as fixed or variable (WRITE operations always use fixed latency). Variable latency allows minimum latency at high clock frequencies, but the controller must monitor WAIT to detect any conflict with refresh cycles. Fixed latency outputs the first data word after the worst-case access delay, including allowance for refresh collisions. The initial latency time and clock speed determine the latency count setting. Fixed latency is used when the controller cannot monitor WAIT. Fixed latency also provides improved performance at lower clock frequencies.

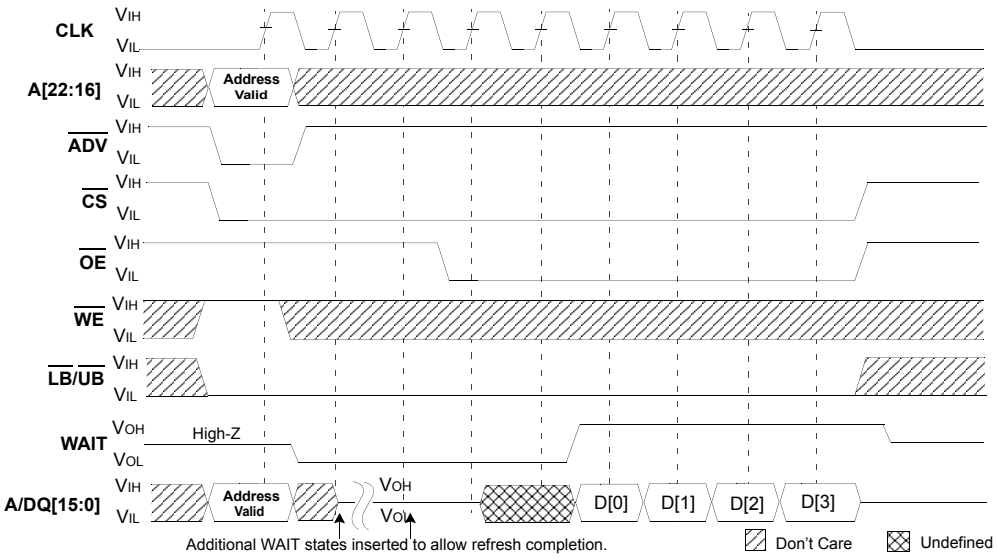


Figure 14. Refresh Collision During Variable-Latency READ Operation

NOTE :
1) Non-default BCR settings for refresh collision during variable-latency READ operation:
2) Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

8.2 Functional Description (Synch. mode)

Burst Mode BCR[15] = 0	Power	CLK	$\overline{ADV}$	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	CRE	$\overline{UB}$ / $\overline{LB}$	WAIT	A/DQ[15:0]	Notes
Standby	Standby	L	H	H	X	X	L	X	High-Z	High-Z	4
No operation	Idle	L	X	L	X	X	L	X	Low-Z	X	4
Initial burst read	Active	↑	L	L	X	H	L	L	Low-Z	Address	
Initial burst write	Active	↑	L	L	H	L	L	X	Low-Z	Address	
Burst continue	Active	↑	H	L	X	X	X	L	Low-Z	Data in or Data out	3
Burst suspend	Active	X	X	L	H	X	X	X	Low-Z	High-Z	3
Configuration register write	Active	↑	L	L	H	L	H	X	Low-Z	High-Z	
Configuration register read	Active	↑	L	L	L	H	H	L	Low-Z	Config. reg.out	

NOTE :
1) CLK must be LOW during async read and async write modes.
2) When $\overline{LB}$ and $\overline{UB}$ are in select mode (LOW), A/DQ[15:0] are affected. When only $\overline{LB}$ is in select mode, A/DQ[7:0] are affected. When only $\overline{UB}$ is in the select mode, A/DQ[15:8] are affected.
3) The device will consume active power in this mode whenever addresses are changed.
4) When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.

8.3 Burst Suspend

To access other devices on the same bus without the timing penalty of the initial latency for a new burst, burst mode can be suspended. Bursts are suspended by stopping CLK. CLK can be stopped HIGH or LOW. If another device will use the data bus while the burst is suspended, $\overline{OE}$ should be taken HIGH to disable the outputs. otherwise, $\overline{OE}$ can remain LOW. Note that the WAIT output will continue to be active, and as a result no other devices should directly share the WAIT connection to the controller. To continue the burst sequence, $\overline{OE}$ is taken LOW, then CLK is restarted after valid data is available on the bus. The $\overline{CS}$ LOW time is limited by refresh considerations. $\overline{CS}$ must not stay LOW longer than tCSM. If a burst suspension will cause $\overline{CS}$ to remain LOW for longer than tCSM, $\overline{CS}$ should be taken HIGH and the burst restarted with a new $\overline{CS}$ LOW/$\overline{ADV}$ LOW cycle.

8.4 Boundary Crossing

Continuous bursts or No wrap burst have the ability to start at a specified address and burst to the end of the address. It goes back to the first address and continues the burst operation. WAIT will be asserted at the boundary of the row and be desserted after crossing boundary of the row. There is no limitation for CS high time during Row Boundary Crossing.

8.5 WAIT Operation

The WAIT output is typically connected to a shared systemlevel WAIT signal. The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus. Once a READ or WRITE operation has been initiated, WAIT goes active to indicate that additional time is required before data can be transferred. For READ operations, WAIT will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into this device. When WAIT transitions to an inactive state, the data burst will progress on successive clock edges. $\overline{CS}$ must remain asserted during WAIT cycles (WAIT asserted and WAIT configuration BCR[8] = 1). Bringing $\overline{CS}$ HIGH during WAIT cycles may cause data corruption. (Note that for BCR[8] = 0, the actual WAIT cycles end one cycle after WAIT de-asserts. When using variable initial access latency (BCR[14] = 0), the WAIT output performs an arbitration role for READ operations launched while an on-chip refresh is in progress. If a collision occurs, WAIT is asserted for additional clock cycles until the refresh has completed. When the refresh operation has completed, the READ operation will continue normally. WAIT will be asserted but should be ignored during asynchronous READ and WRITE operations. By using fixed initial latency (BCR[14] = 1), this device can be used in burst mode without monitoring the WAIT signal. However, WAIT can still be used to determine when valid data is available at the start of the burst.

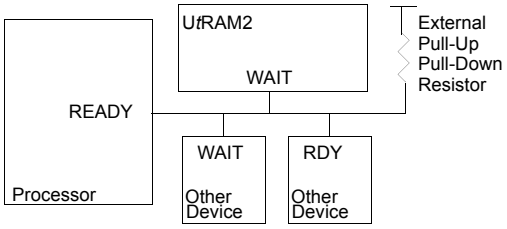


Figure 15. Wired or WAIT Configuration

8.6 LB / UB Operation

The $\overline{LB}$ enable and $\overline{UB}$ enable signals support byte-wide data WRITEs. During WRITE operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous WRITE cycle. The data to be written is latched on the rising edge of $\overline{CS}$, $\overline{WE}$ whichever occurs first and $\overline{LB}$, $\overline{UB}$ must have rising edge after $\overline{CS}$ or $\overline{WE}$ go high. $\overline{LB}$ and $\overline{UB}$ must be LOW during READ cycles. When both the $\overline{LB}$ and $\overline{UB}$ are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as $\overline{CS}$ remains LOW.

9.0 LOW-POWER OPERATION

9.1 Temperature Compensated Self Refresh

Temperature compensated self refresh (TCSR) allows for adequate refresh at different temperatures. This U*t*RAM2 device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The device continually adjusts the refresh rate to match that temperature.

9.2 Partial Array Refresh

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map. READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

9.3 AC Input/Output Reference Waveform & AC Output Load Circuit

NOTE :
1) AC test inputs are driven at VCCQ for a logic 1 and VSSQ for a logic 0. Input rise and fall times (10% to 90%) <1.6ns.
2) Input timing begins at VCCQ/2 and Output timing ends at VCCQ/2.
3) All tests are performed with the outputs configured for default setting of half drive strength (BCR[5:4] = 01b)

10.0 TIMING REQUIREMENTS

10.1 Asynchronous READ Cycle Timing Requirements

Parameter	Symbol	Min	Max	Unit	Notes
Address access time	t_{AA}		70	ns	
$\overline{ADV}$ access time	t_{AADV}		70	ns	
Address setup to $\overline{ADV}$ HIGH	t_{AVS}	5		ns	
Address hold from $\overline{ADV}$ HIGH	t_{AVH}	2		ns	
$\overline{LB}$/$\overline{UB}$ access time	t_{BA}		70	ns	
$\overline{LB}$/$\overline{UB}$ disable to DQ High-Z output	t_{BHZ}		8	ns	1
Maximum $\overline{CS}$ Pulse Width	t_{CSM}		2.5	us	4
$\overline{CS}$ or $\overline{ADV}$ LOW to WAIT valid	t_{CSW}	1	7.5	ns	
$\overline{CS}$ HIGH between subsequent Async Operations	t_{CPH}	15		ns	4
Chip select access time	t_{CO}		70	ns	
$\overline{CS}$ LOW to $\overline{ADV}$ HIGH	t_{CVS}	7		ns	
Chip disable to DQ and WAIT High-Z output	t_{HZ}		8	ns	1
Output enable to valid output	t_{OE}		20	ns	
Output disable to DQ High-Z output	t_{OHZ}		8	ns	1
Output ebable to Low-Z output	t_{OLZ}	5		ns	2
READ cycle time	t_{RC}	80		ns	
$\overline{ADV}$ pulse width LOW	t_{VP}	5		ns	

10.2 Asynchronous WRITE Cycle Timing Requirements

Parameter	Symbol	Min	Max	Unit	Notes
Address setup to $\overline{ADV}$ going HIGH	t_{AVS}	5		ns	
Address hold from $\overline{ADV}$ HIGH	t_{AVH}	2		ns	
Address valid to end of WRITE	t_{AW}	70		ns	
$\overline{LB}$/$\overline{UB}$ select to end of WRITE	t_{BW}	70		ns	
$\overline{CS}$ HIGH between subsequent async operations	t_{CPH}	15		ns	1
$\overline{CS}$ LOW to $\overline{ADV}$ HIGH	t_{CVS}	7		ns	2
Chip enable to end of WRITE	t_{CW}	70		ns	3
Data HOLD from WRITE time	t_{DH}	0		ns	
Data WRITE setup time	t_{DW}	20		ns	
Chip disable to WAIT High-Z output	t_{HZ}		8	ns	
End WRITE to Low-Z output	t_{OW}	5		ns	2
$\overline{ADV}$ pulse width	t_{VP}	5		ns	
$\overline{ADV}$ setup to end of WRITE	t_{VS}	70		ns	
WRITE to DQ High-Z output	t_{WHZ}		8	ns	2
$\overline{CS}$ or $\overline{ADV}$ LOW to WAIT valid	t_{CSW}	1	7.5	ns	
WRITE pulse width	t_{WP}	55		ns	3
WRITE recovery time	t_{WR}	0		ns	
/UB, /LB valid or mask setup time to beginning of write	t_{BSA}	0	-	ns	
/UB, /LB valid or mask hold time to end of write	t_{BHA}	0	-	ns	
Address Skew	t_{SKEW}	-	10	ns	

NOTE :
1) The High-Z timings measure a 100mV transition from either VOH or VOL toward VCCQ/2.
2) The Low-Z timings measure a 100mV transition away from the High-Z (VCCQ/2) level toward either VOH or VOL.
3) $\overline{WE}$ LOW time must be limited to tCSM (2.5μs).
4) A refresh opportunity must be provided every tCSM. $\overline{CS}$ must not remain LOW longer than tCSM.

10.3 Burst READ Cycle Timing Requirements

Parameter	Symbol	108MHz		80MHz		66MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address access time (fixed latency)	t_{AA}		70		70		70	ns	4
$\overline{ADV}$ access time (fixed latency)	t_{AADV}		70		70		70	ns	4
CLK to output delay	t_{ACLK}		7		9		11	ns	
Burst $\overline{OE}$ LOW to output delay	t_{BOE}		20		20		20	ns	
$\overline{CS}$ HIGH between subsequent burst or operations	t_{CBPH}	15		15		15		ns	3
Maximum $\overline{CS}$ pulse width LOW	t_{CSM}		2.5		2.5		2.5	us	3
$\overline{CS}$ or $\overline{ADV}$ LOW to WAIT valid	t_{CSW}	1	7.5	1	7.5	1	7.5	ns	
CLK period	t_{CLK}	9.26		12.5		15		ns	
Chip select access time (fixed latency)	t_{CO}		70		70		70	ns	4
$\overline{CS}$ setup time to active CLK edge	t_{CSP}	3		4		5		ns	
Hold time from active CLK edge	t_{HD}	2		2		2		ns	
Chip desable to DQ and WAIT High-Z output	t_{HZ}		8		8		8	ns	1
CLK rise or fall time	t_{KHKL}		1.6		1.8		2.0	ns	
CLK to WAIT valid	t_{KHTL}	2	7	2	9	2	11	ns	
Output HOLD from CLK	t_{KOH}	2		2		2		ns	
CLK HIGH or LOW time	t_{KP}	3		4		5		ns	
Output disable to DQ High-Z output	t_{OHZ}		8		8		8	ns	1
Output enable to Low-Z output	t_{OLZ}	5		5		5		ns	2
Setup time to active CLK edge	t_{SP}	3		3		3		ns	
$\overline{ADV}$ HIGH to $\overline{OE}$ LOW	t_{ADVO}	3		4		5		ns	
Address setup to $\overline{ADV}$ HIGH	t_{AVH}	2		2		2		ns	
$\overline{ADV}$ HIGH to CLK Rising	t_{AHCR}	2		2		2		ns	

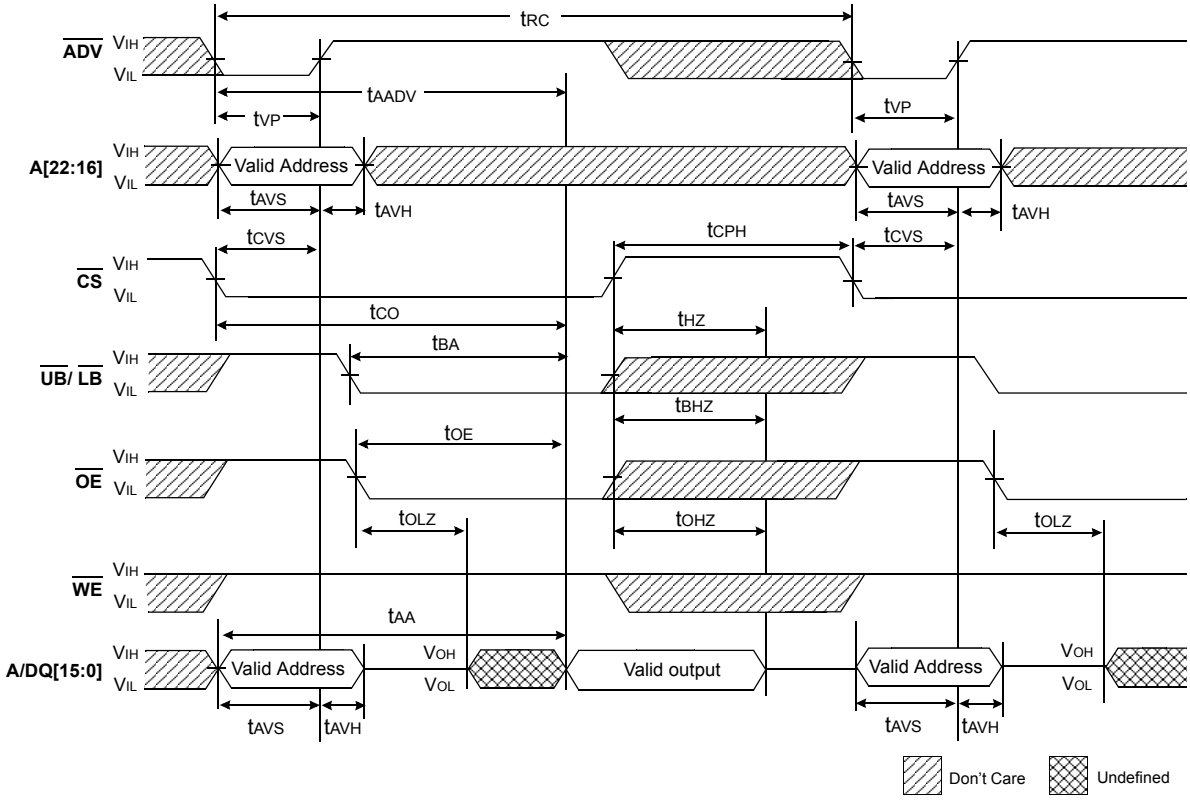
10.4 Burst WRITE Cycle Timing Requirements

Parameter	Symbol	108MHz		80MHz		66MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CS}$ HIGH between subseuent burst or mixed mode operations	t_{CBPH}	15		15		15		ns	3
Maximum $\overline{CS}$ pulse width LOW	t_{CSM}		2.5		2.5		2.5	us	3
$\overline{CS}$ LOW to WAIT valid	t_{CSW}	1	7.5	1	7.5	1	7.5	ns	
Clock period	t_{CLK}	9.26		12.5		15		ns	
$\overline{CS}$ setup to CLK active edge	t_{CSP}	3		4		5		ns	
Hold time from active CLK edge	t_{HD}	2		2		2		ns	
Chip disable to WAIT High-Z output	t_{HZ}		8		8		8	ns	1
Last clock to $\overline{ADV}$ LOW (fixed latency)	t_{KADV}	15		15		15		ns	
CLK rise or fall time	t_{KHKL}		1.6		1.8		2.0	ns	
Clock to WAIT valid	t_{KHTL}	2	7	2	9	2	11	ns	
CLK HIGH or LOW time	t_{KP}	3		4		5		ns	
Setup time to activate CLK edge	t_{SP}	3		3		3		ns	
Address Hold from $\overline{ADV}$ HIGH	t_{AVH}	2		2		2		ns	
$\overline{ADV}$ HIGH to CLK Rising	t_{AHCR}	2		2		2		ns	

NOTE :
1) The High-Z timings measure a 100mV transition from either VOH or VOL toward VCCQ/2.
2) The Low-Z timings measure a 100mV transition away from the High-Z (VCCQ/2) level toward either VOH or VOL.
3) A refresh opportunity must be provided every tCSM. $\overline{CS}$ must not remain LOW longer than tCSM.
4) tAA, tAADV, tCO guarantee at min set-up time.

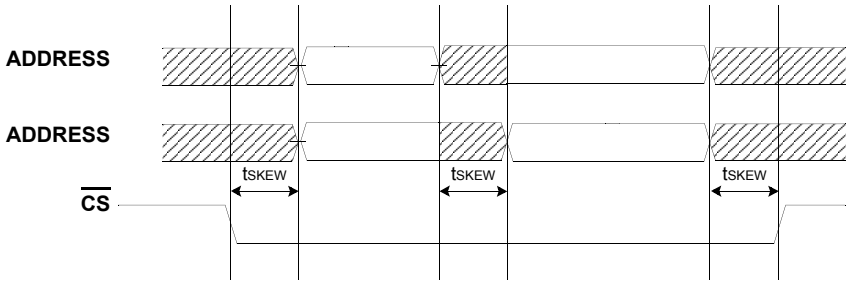
11.0 TIMING DIAGRAMS

11.1 Asynchronous READ ($\overline{CS}$ controlled)

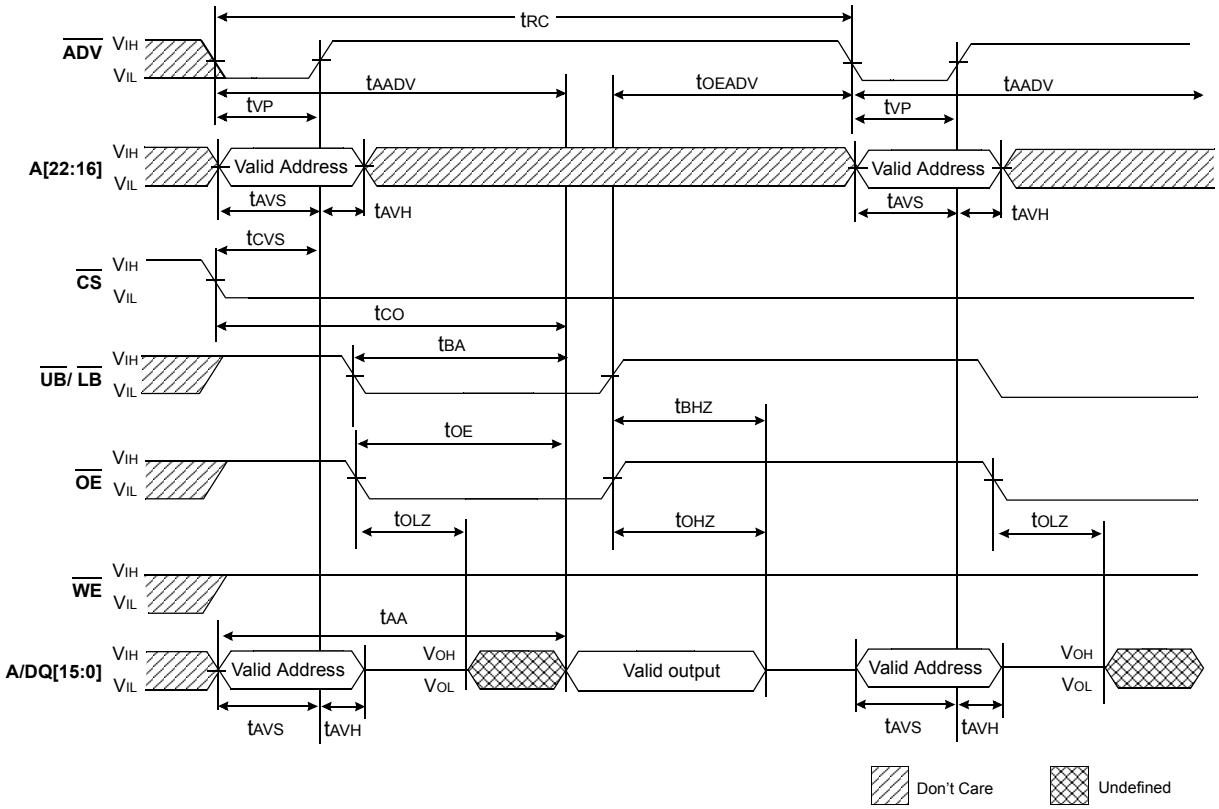


NOTE :
1) Don't care must be in VIL or VIH.
2) tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
3) At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.
4) tOE(max) is met only when $\overline{OE}$ becomes enabled after tAA(max).
5) If invalid address signals shorter than min. tRC are continuously repeated for over 2.5us, the device needs a normal read timing(tRC) or needs to sustain standby state for min. tRC at least once in every 2.5us.

11.1.1 Address Skew for Asynchronous Operation

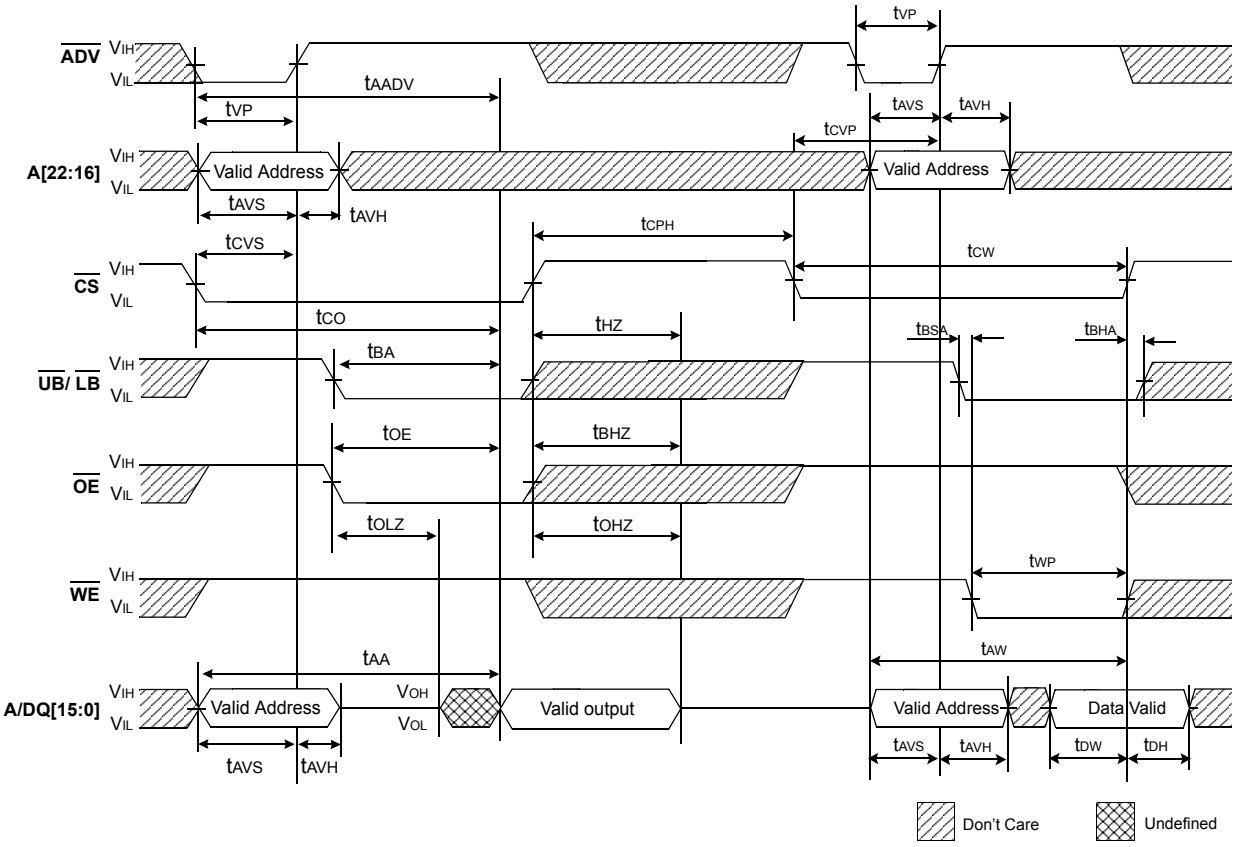


11.2 Asynchronous READ ($\overline{OE}$ controlled)

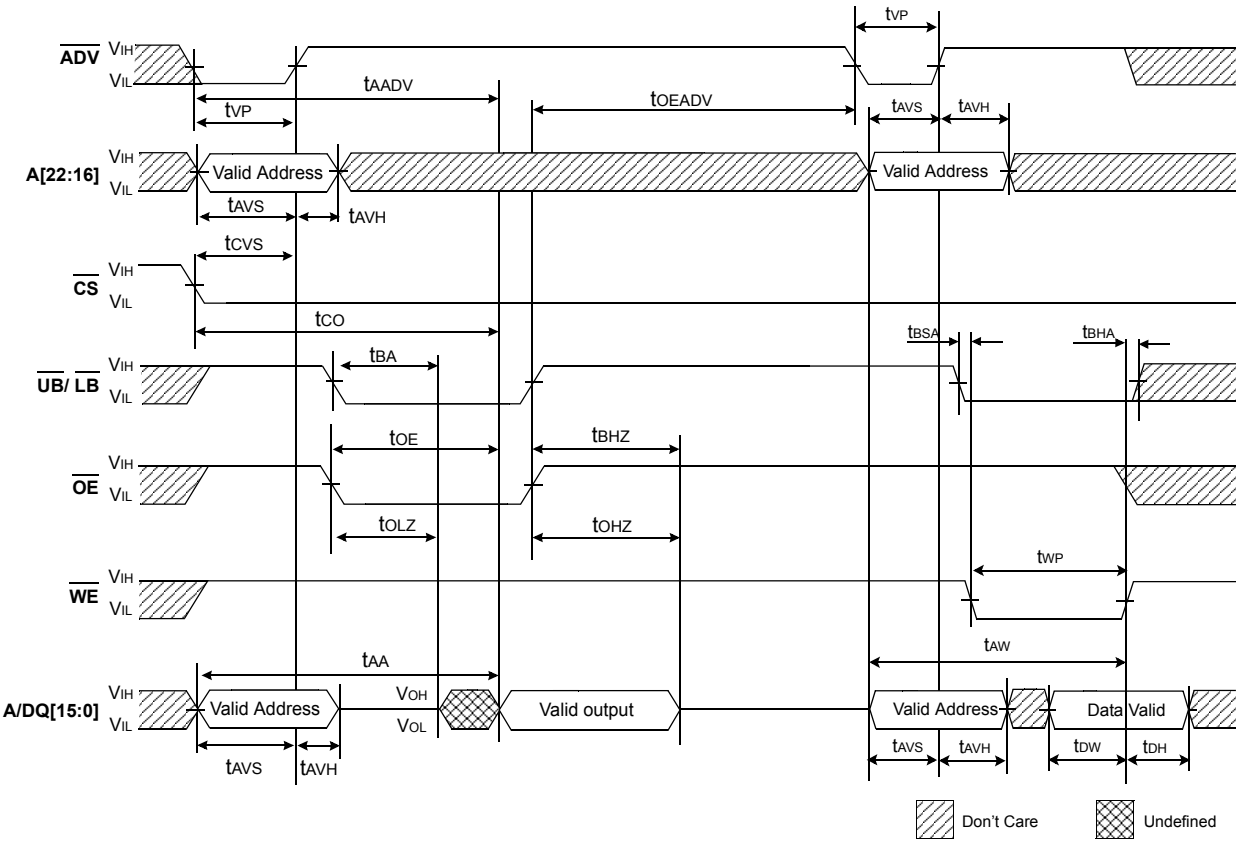


NOTE :
1) Don't care must be in V_{IL} or V_{IH}.
2) t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
3) At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
4) t_{OE}(max) is met only when $\overline{OE}$ becomes enabled after t_{AA}(max).
5) If invalid address signals shorter than min. t_{RC} are continuously repeated for over 2.5us, the device needs a normal read timing(t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 2.5us.

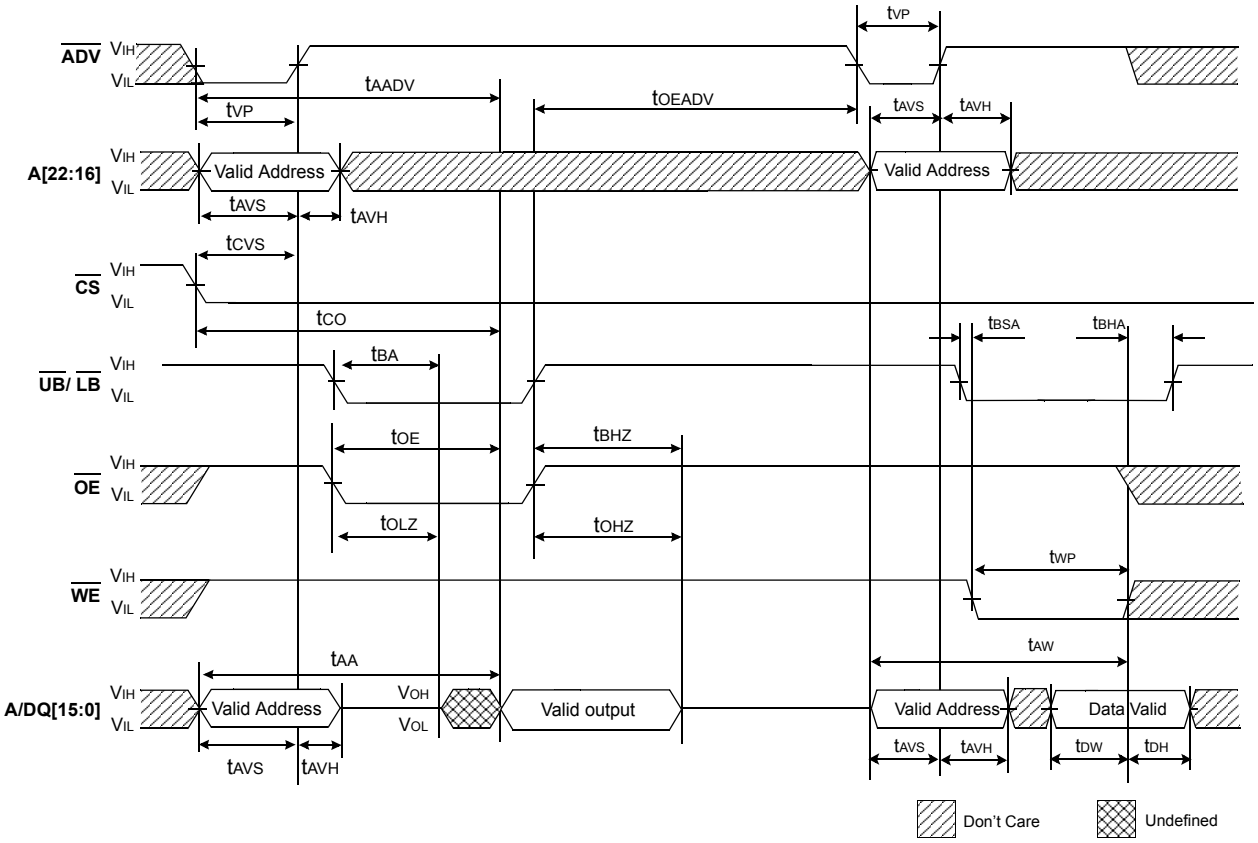
11.3 Asynchronous READ Followed by Asynchronous WRITE ($\overline{CS}$ Controlled)



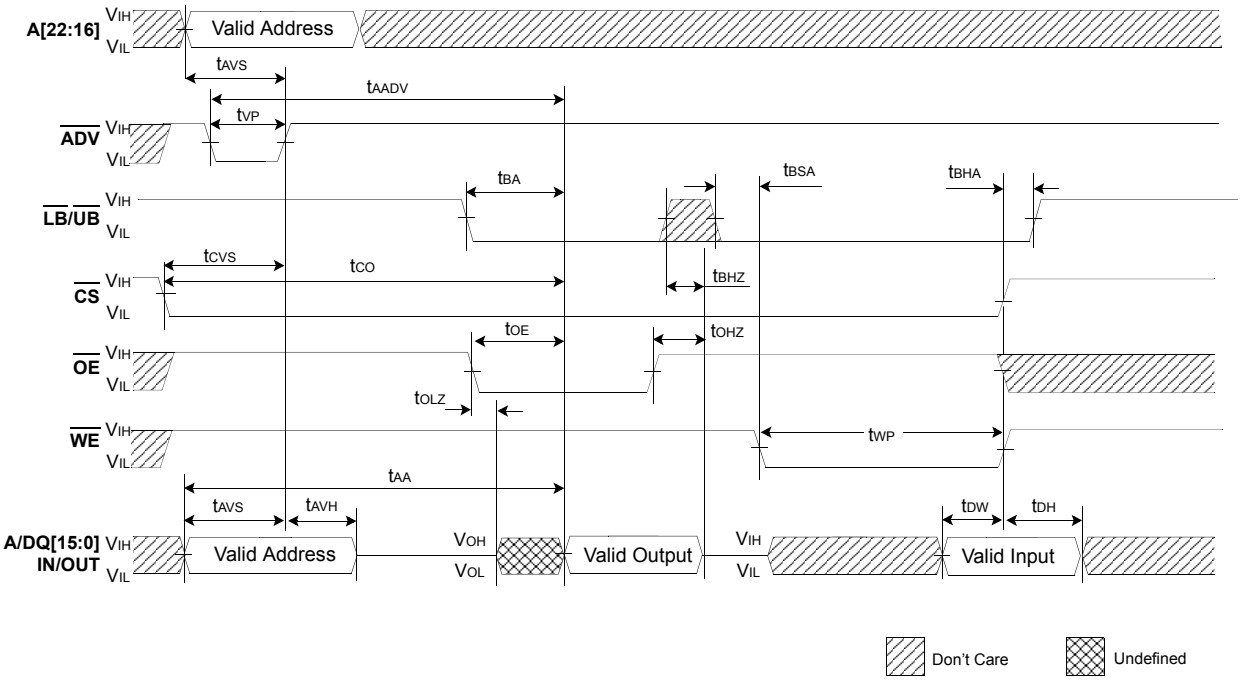
11.4 Asynchronous READ Followed by Asynchronous WRITE ($\overline{OE}$, $\overline{WE}$ Controlled)



11.5 Asynchronous READ Followed by Asynchrous WRITE ($\overline{UB}$, $\overline{LB}$ Controlled)

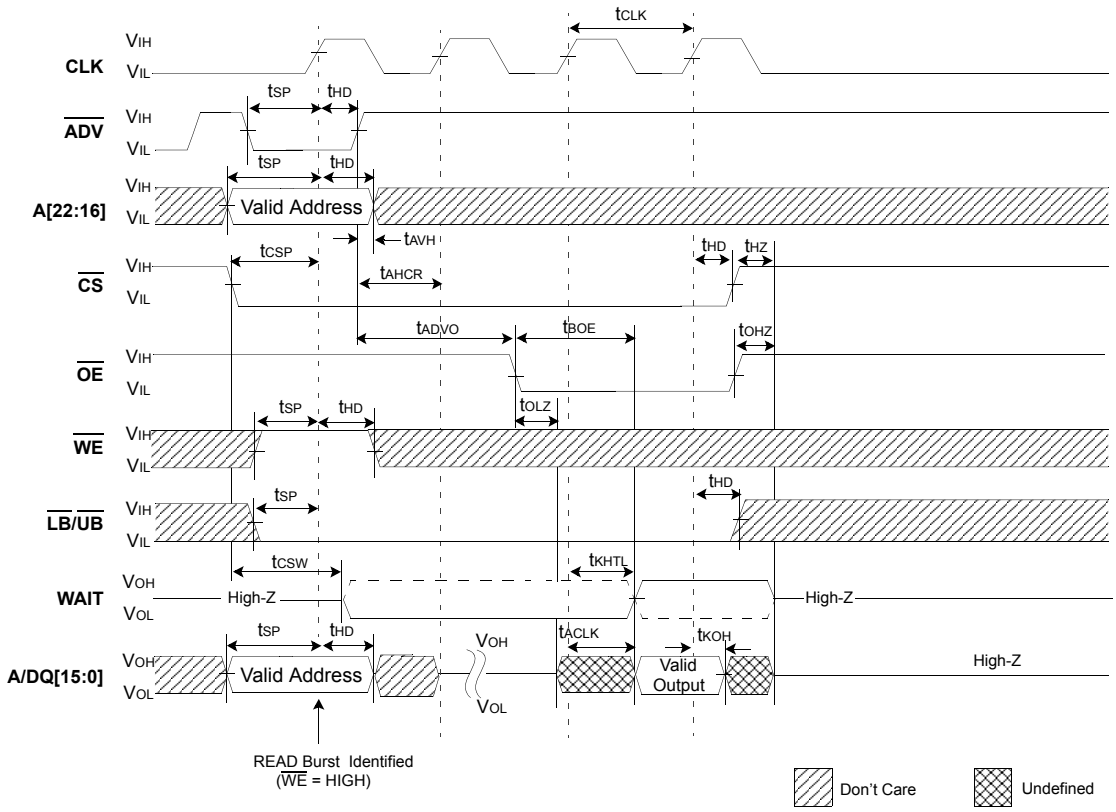


11.6 Asynchronous READ Followed by WRITE at the Same Address ($\overline{UB}$/$\overline{LB}$ Controlled)



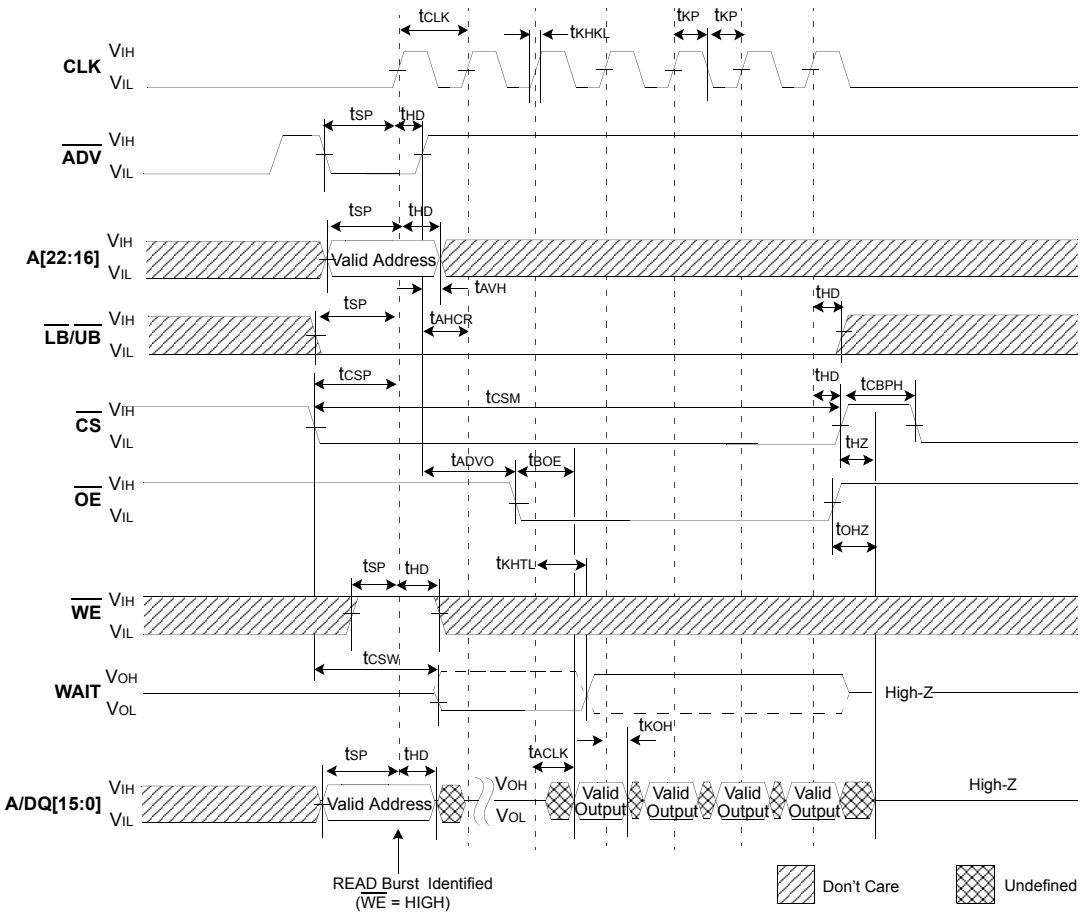
NOTE :
1) Don't care must be in VIL or VIH.

11.7 Single-Access Burst READ Operation—Variable Latency



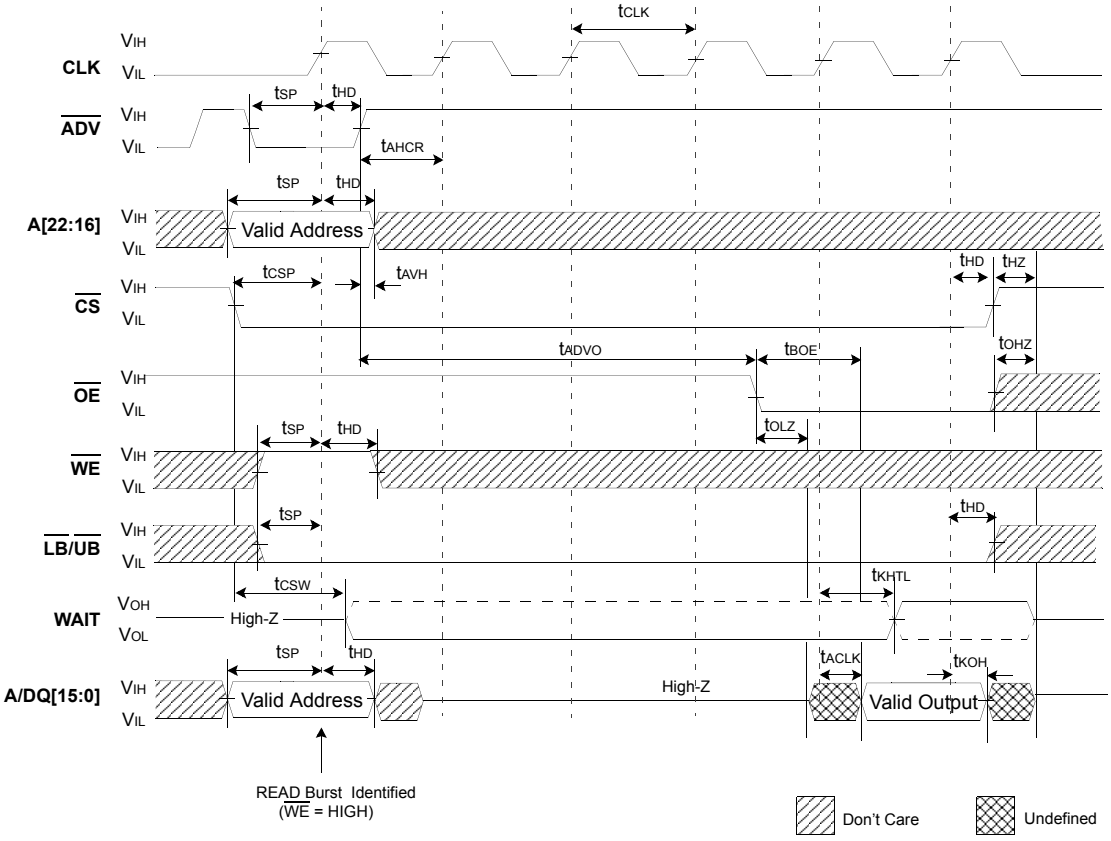
NOTE :
1) Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2) Don't care must be in VIL or VIH.

11.8 4-Word Burst READ Operation—Variable Latency



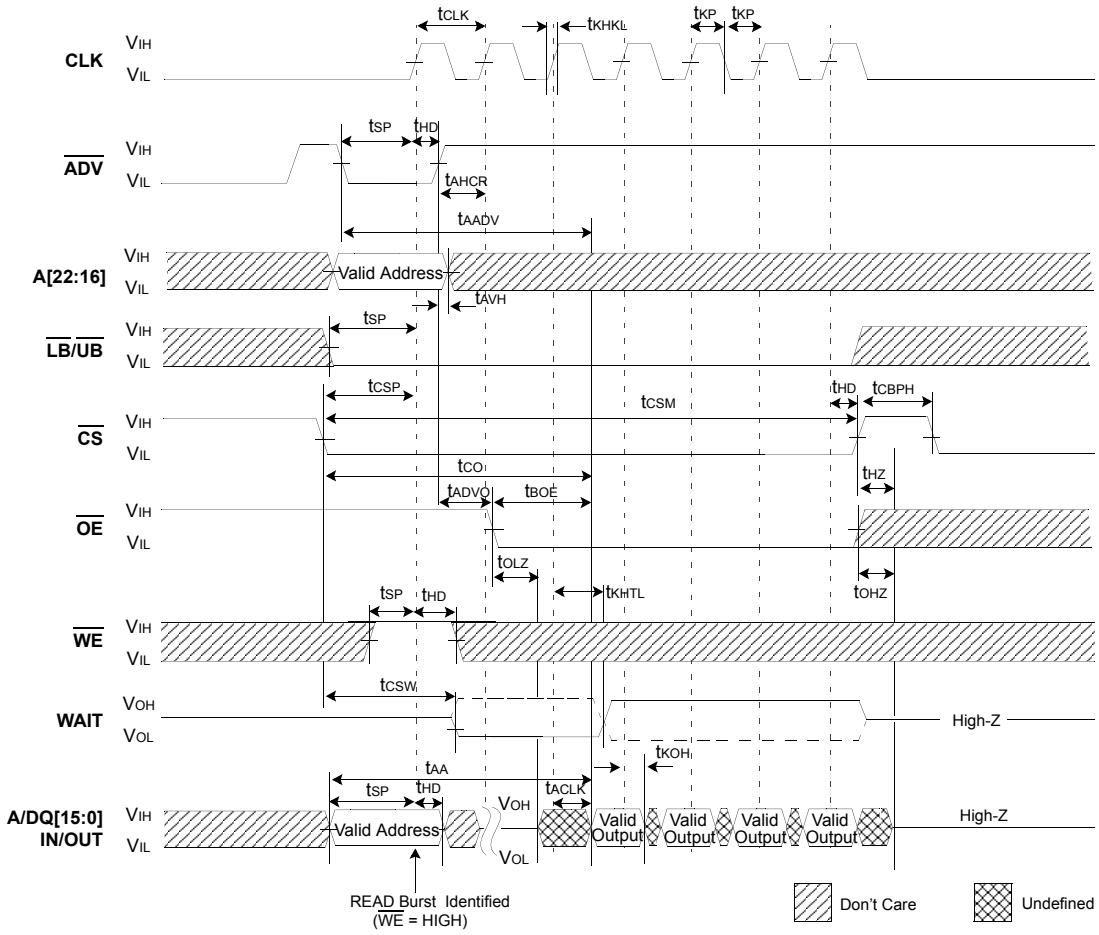
NOTE :
1) Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2) Don't care must be in VIL or VIH.

11.9 Single-Access Burst READ Operation—Fixed Latency



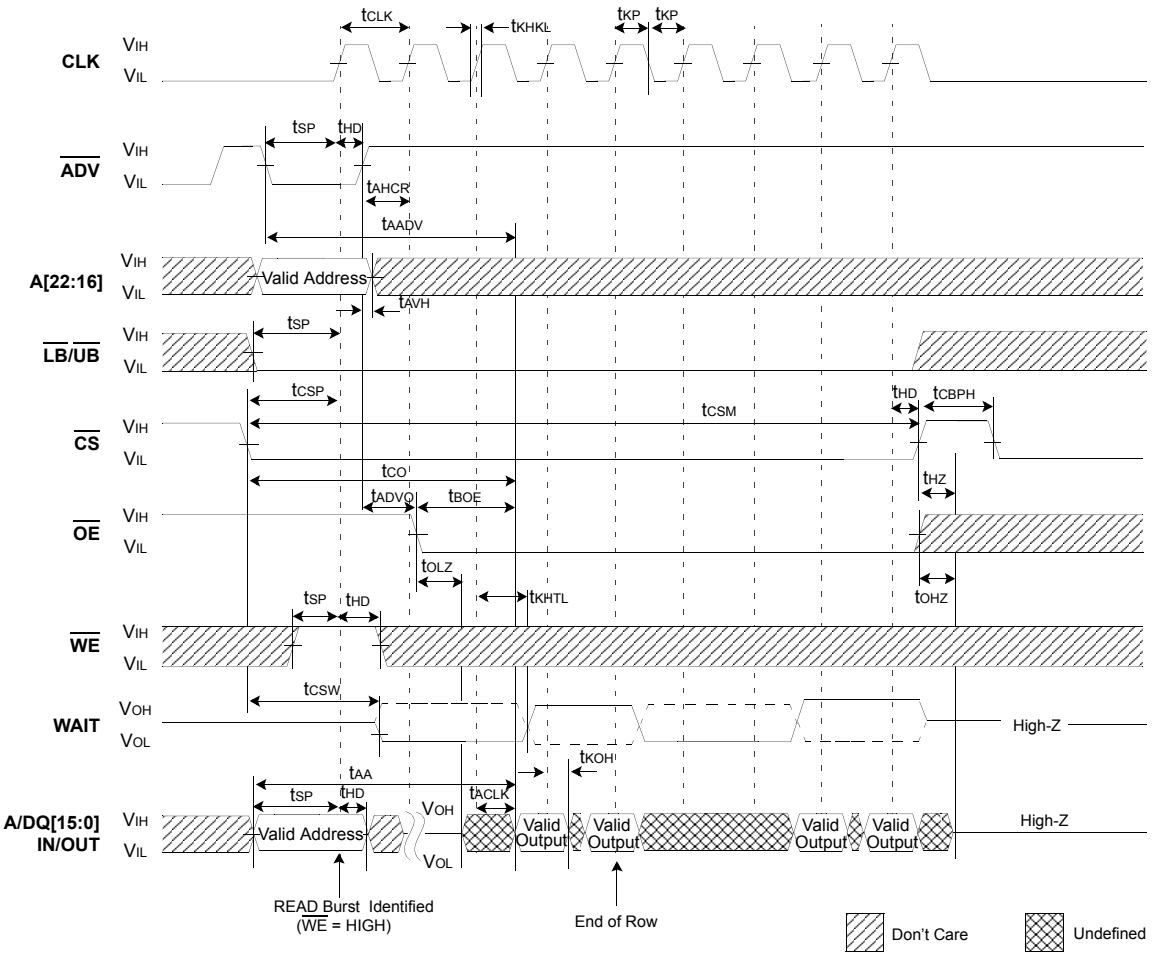
NOTE :
1) Non-default BCR settings: Fixed latency; latency code four (five clocks); WAIT active LOW; WAIT asserted during delay.
2) Don't care must be in VIL or VIH.

11.10 4-Word Burst READ Operation—Fixed Latency



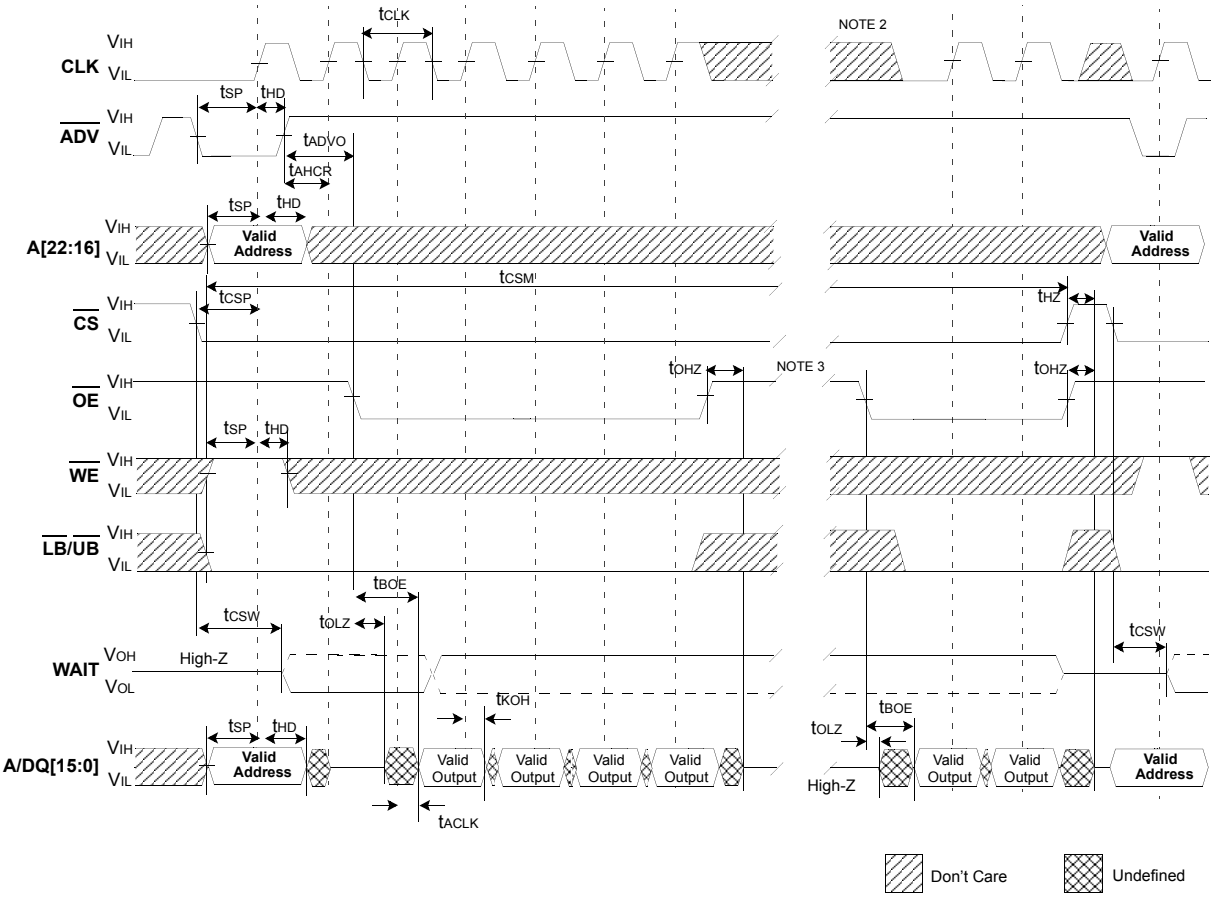
NOTE :
1) Non-default BCR settings: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2) Don't care must be in VIL or VIH.

11.11 4-Word Burst READ Operation - Row Boundary Crossing



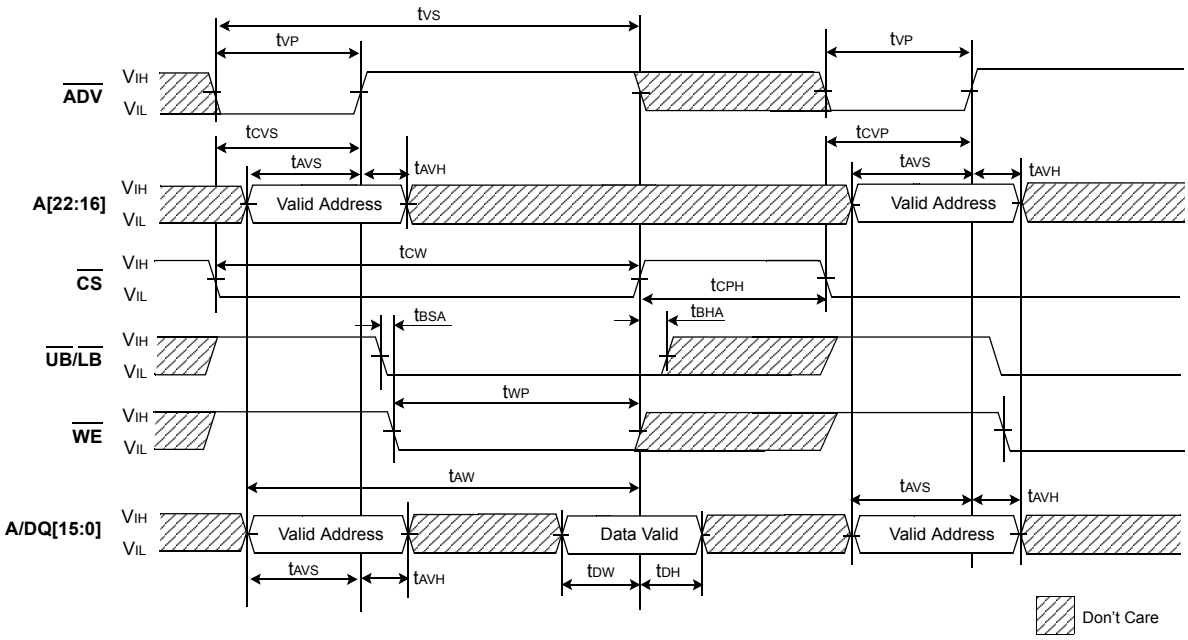
NOTE :
1) Non-default BCR settings: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2) Don't care must be in VIL or VIH.
3) There is no limitation for CS high time during Row Boundary Crossing.
4) There is no $\overline{ADV}$ low during Row Boundary Crossing.

11.12 READ Burst Suspend



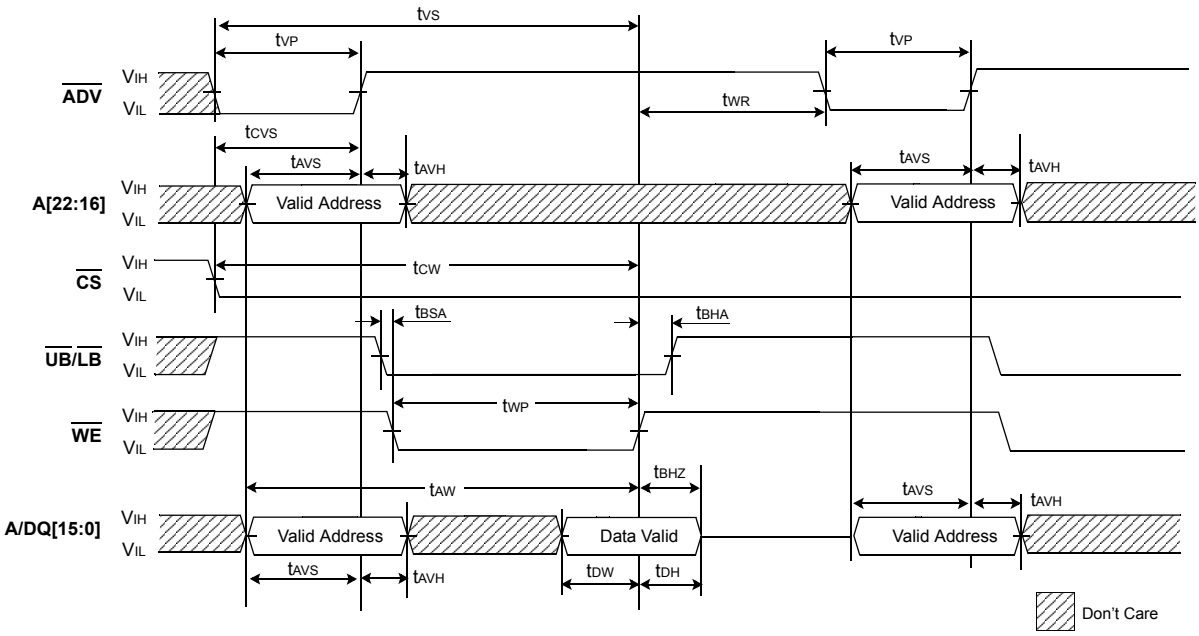
NOTE :
1) Non-default BCR settings for READ burst suspend: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2) CLK can be stopped LOW or HIGH, but must be static, with no LOW-to-HIGH transitions during burst suspend.
3) $\overline{OE}$ can stay LOW during burst suspend. If $\overline{OE}$ is LOW, A/DQ[15:0] will continue to output valid data.
4) Don't care must be in V_{IL} or V_{IH}.

11.13 Asynchronous WRITE ($\overline{CS}$ Controlled)



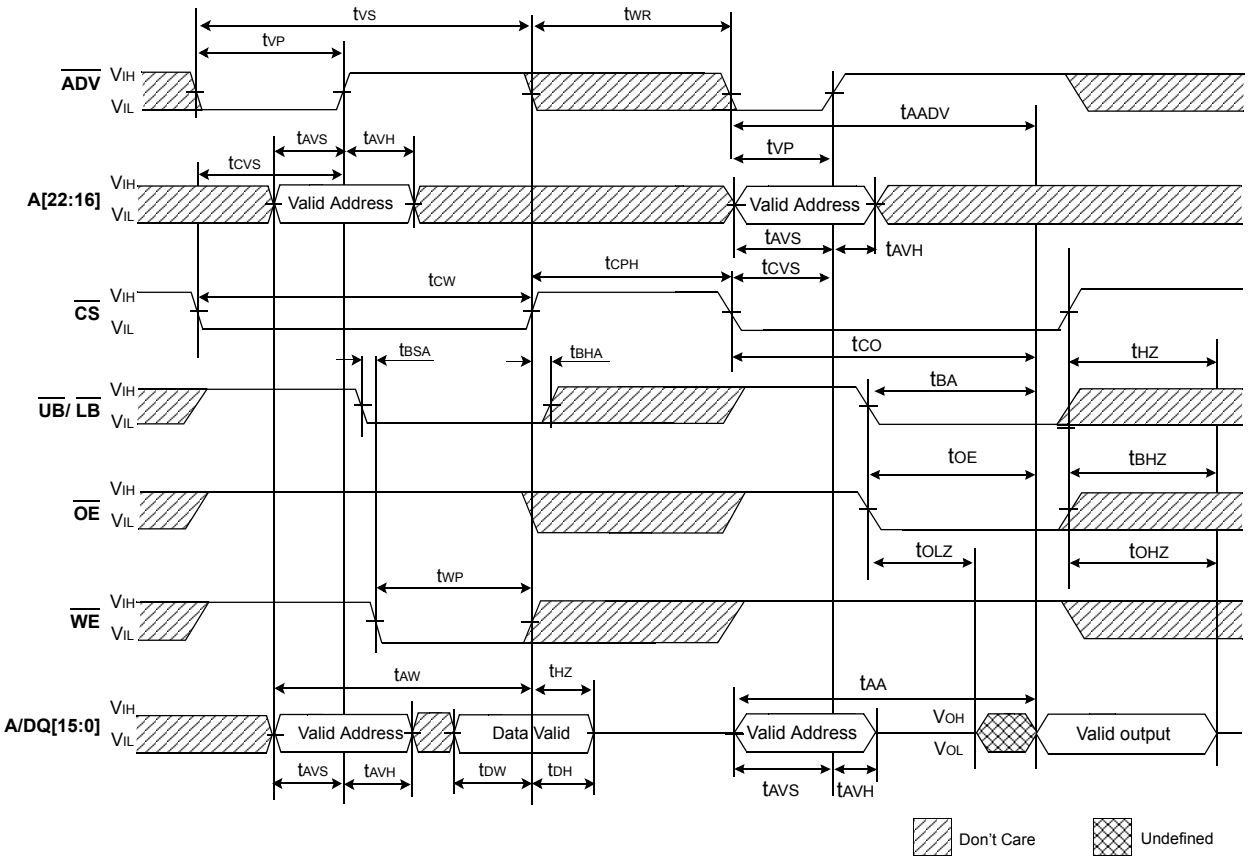
NOTE :
1) Don't care must be in VIL or VIH.
2) A write occurs during the overlap(tWP) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation.
3) tCW is measured from the $\overline{CS}$ going low to the end of write.
4) tAS is measured from the address valid to the beginning of write.
5) tWR is measured from the end of write to the address change. tWR is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.

11.14 Asynchronous WRITE ($\overline{WE}$, $\overline{UB}$/$\overline{LB}$ Controlled)

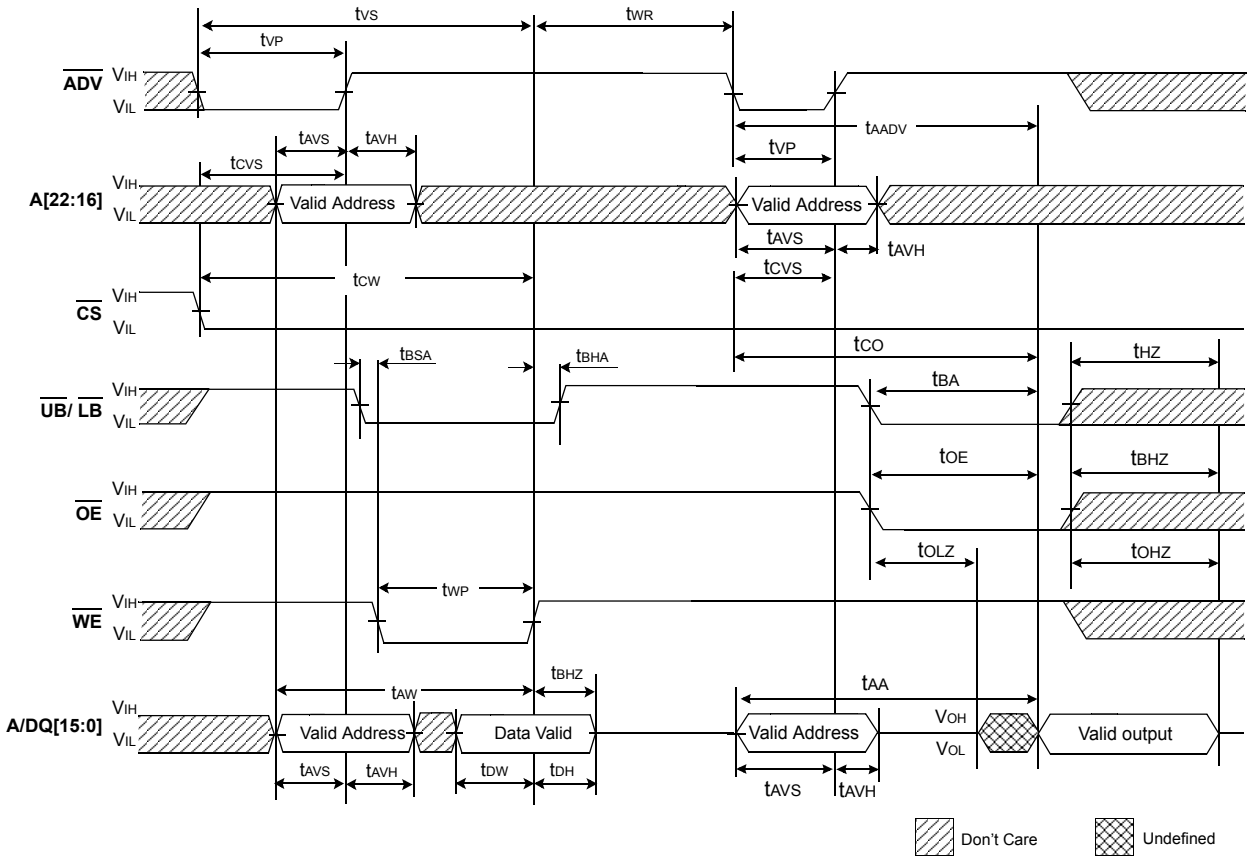


NOTE :
1) Don't care must be in V_{IL} or V_{IH}.
2) A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation.
3) t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
4) t_{AS} is measured from the address valid to the beginning of write.
5) t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.

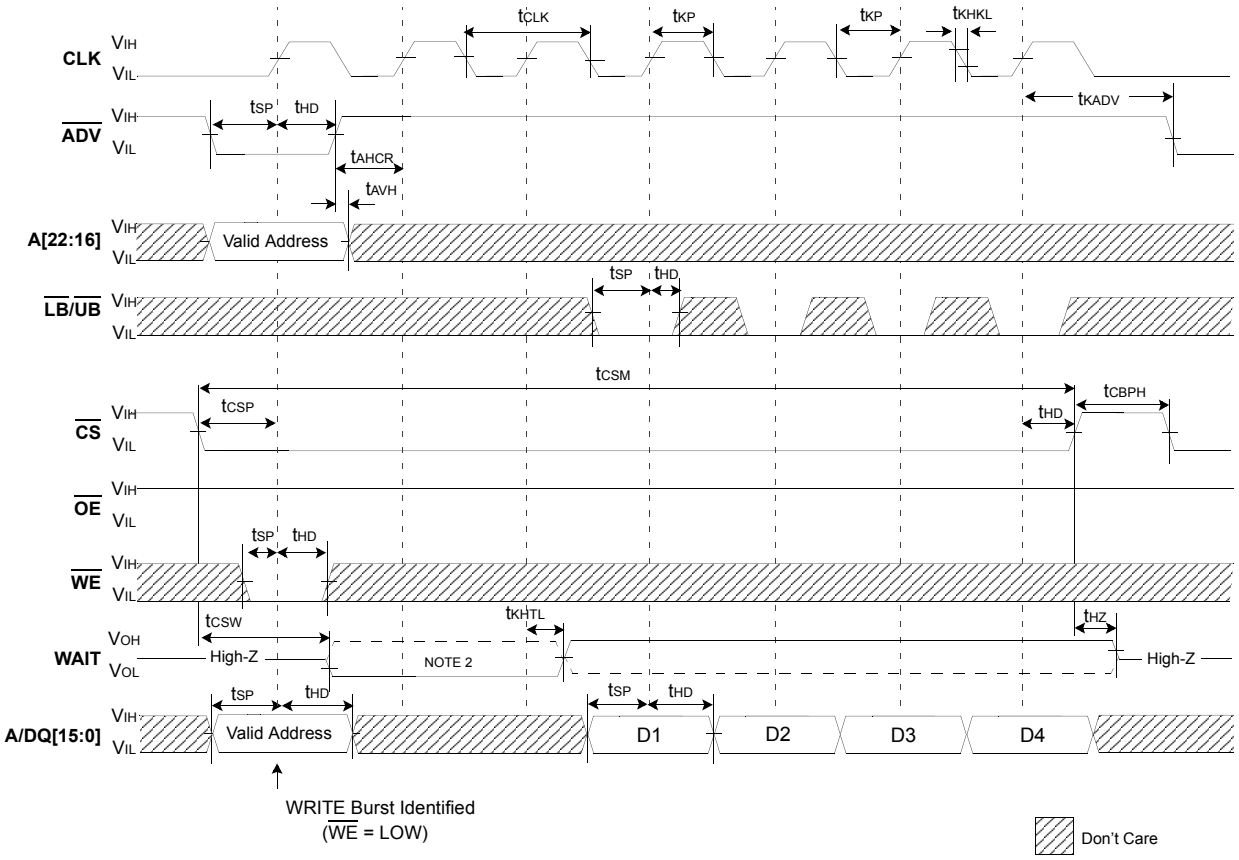
11.15 Asynchronous WRITE Followed by Asynchronous READ ($\overline{CS}$ Controlled)



11.16 Asynchronous WRITE Followed by Asynchronous READ ($\overline{OE}$, $\overline{WE}$ Controlled)

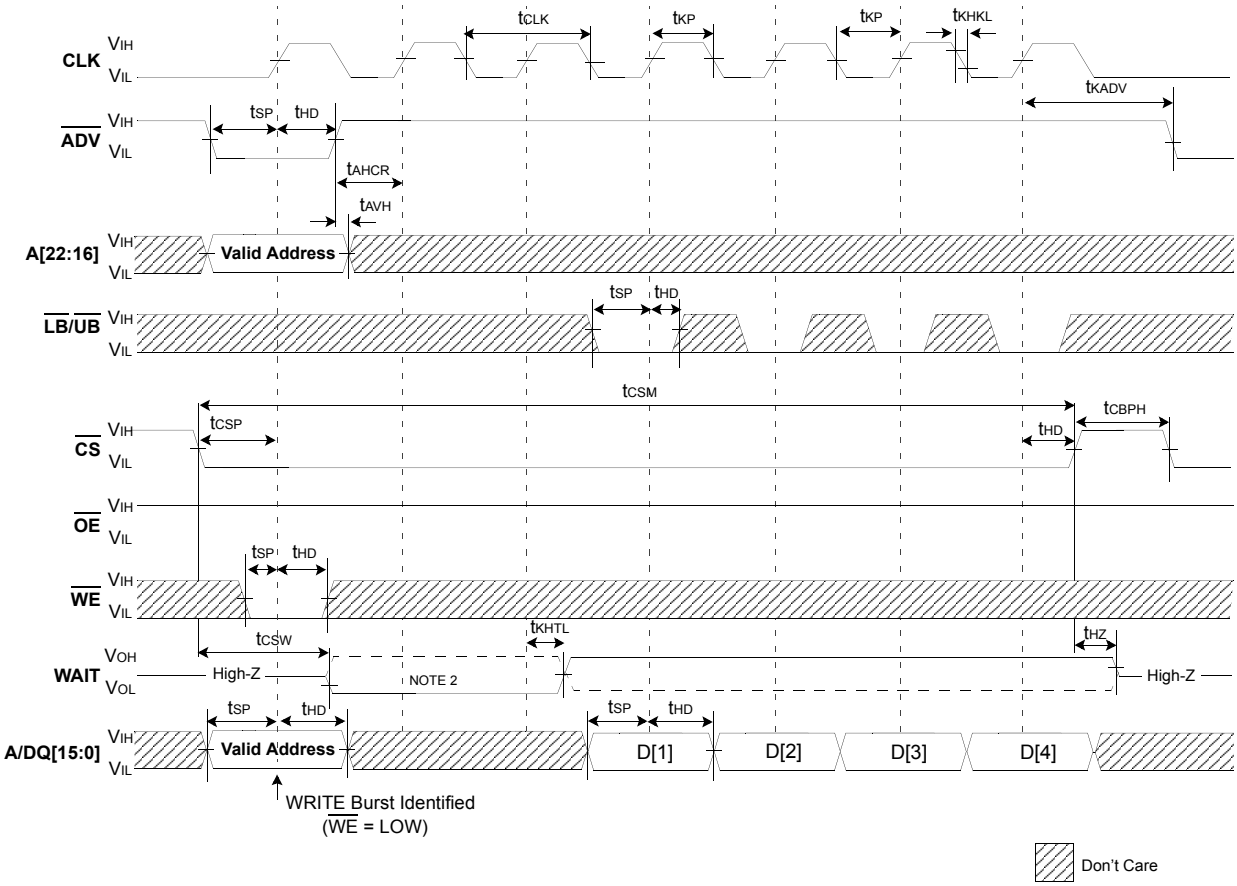


11.17 Burst WRITE Operation—Variable Latency Mode



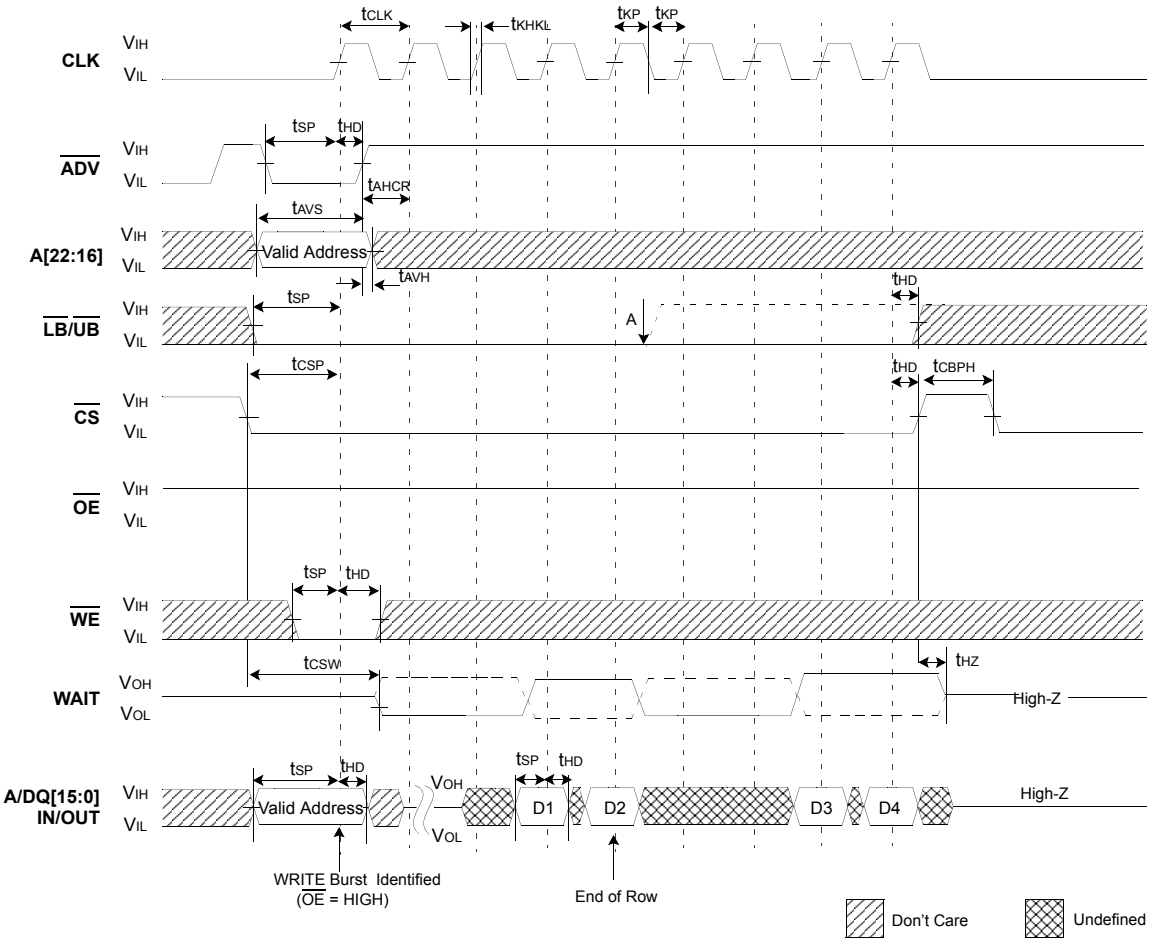
NOTE :
1) Non-default BCR settings for burst WRITE operation in variable latency mode: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay; burst length four; burst wrap enabled.
2) WAIT asserts for LC cycles for both fixed and variable latency. LC = Latency Code (BCR[13:11]).
3) Don't care must be in VIL or VIH.

11.18 Burst WRITE Operation—Fixed Latency Mode



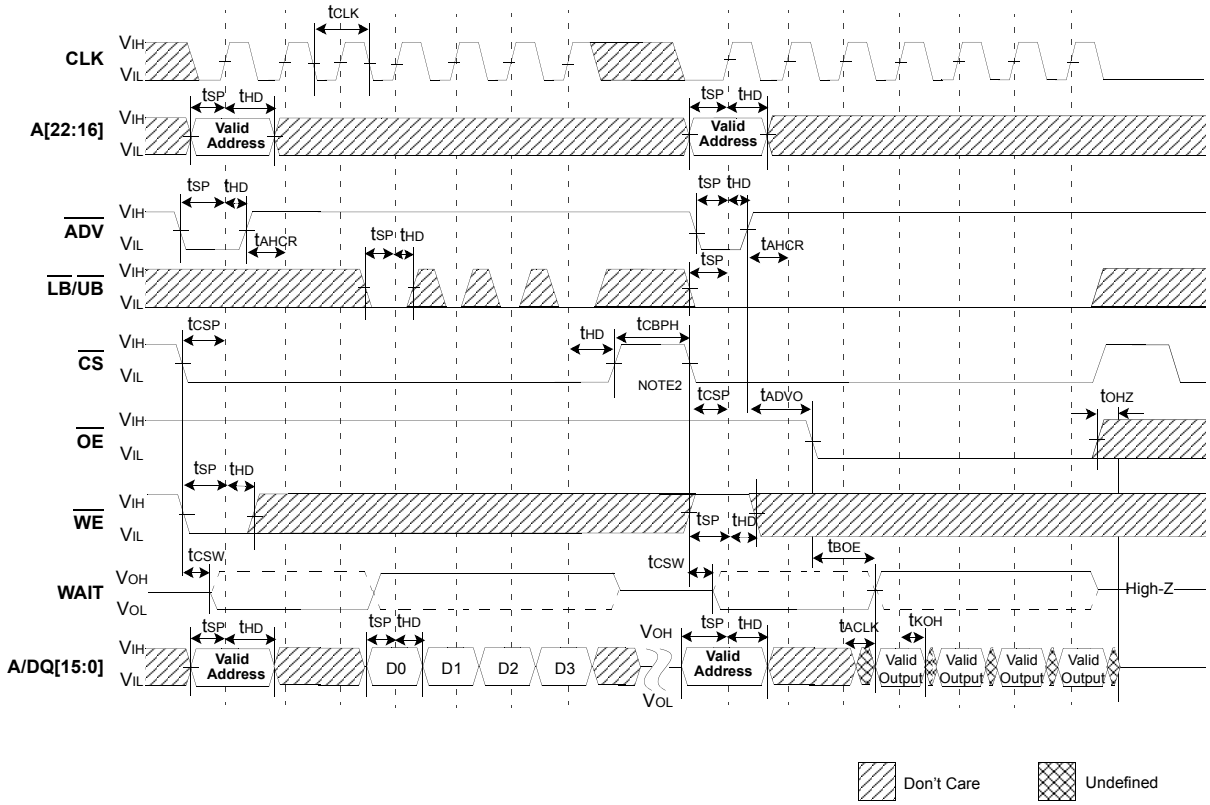
NOTE :
1) Non-default BCR settings for burst WRITE operation in fixed latency mode: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay; burst length four; burst wrap enabled.
2) WAIT asserts for LC cycles for both fixed and variable latency. LC = Latency Code (BCR[13:11]).
3) Don't care must be in VIL or VIH.

11.19 4-Word Burst WRITE Operation - Row Boundary Crossing



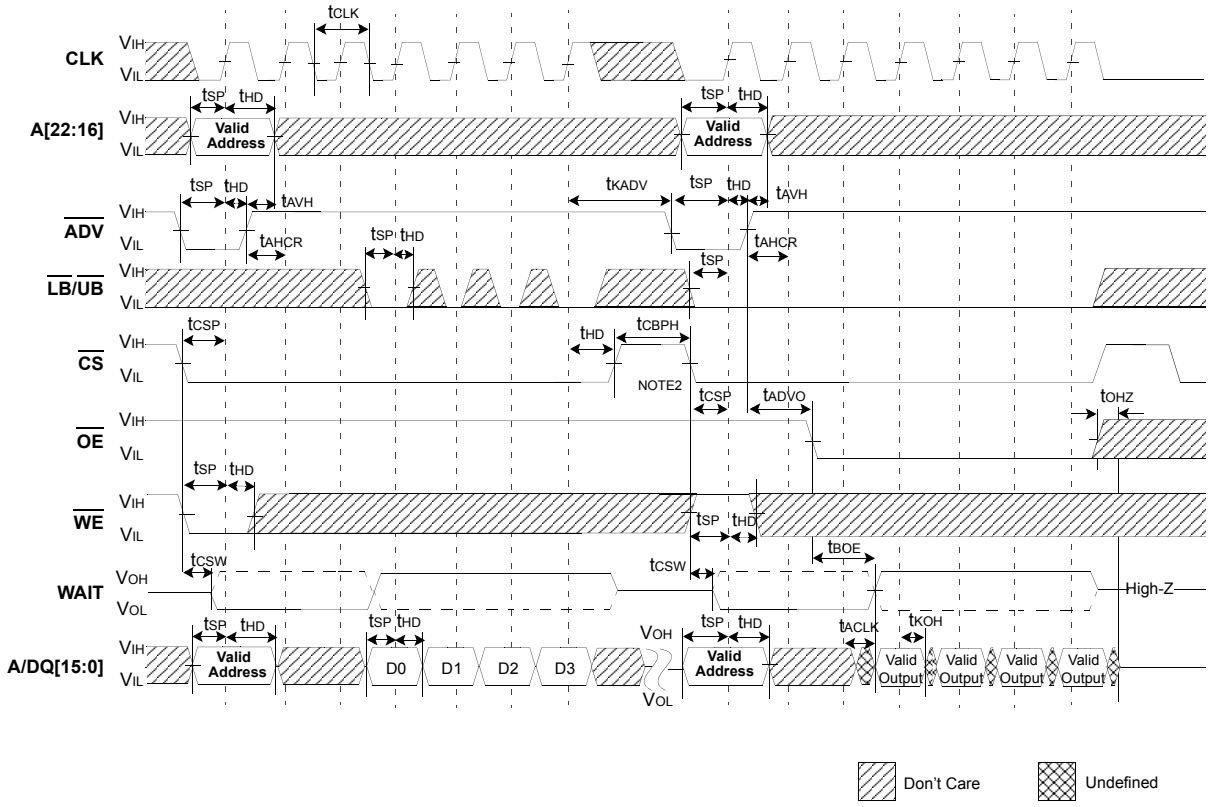
NOTE :
1) Non-default BCR settings: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2) Don't care must be in VIL or VIH.
3) D2 can be written when CS goes high at Point A.
4) There is no limitation for CS high time during Row Boundary Crossing.
6) There is no ADV low during Row Boundary Crossing.

11.20 Burst WRITE Followed by Burst READ, Variable Latency



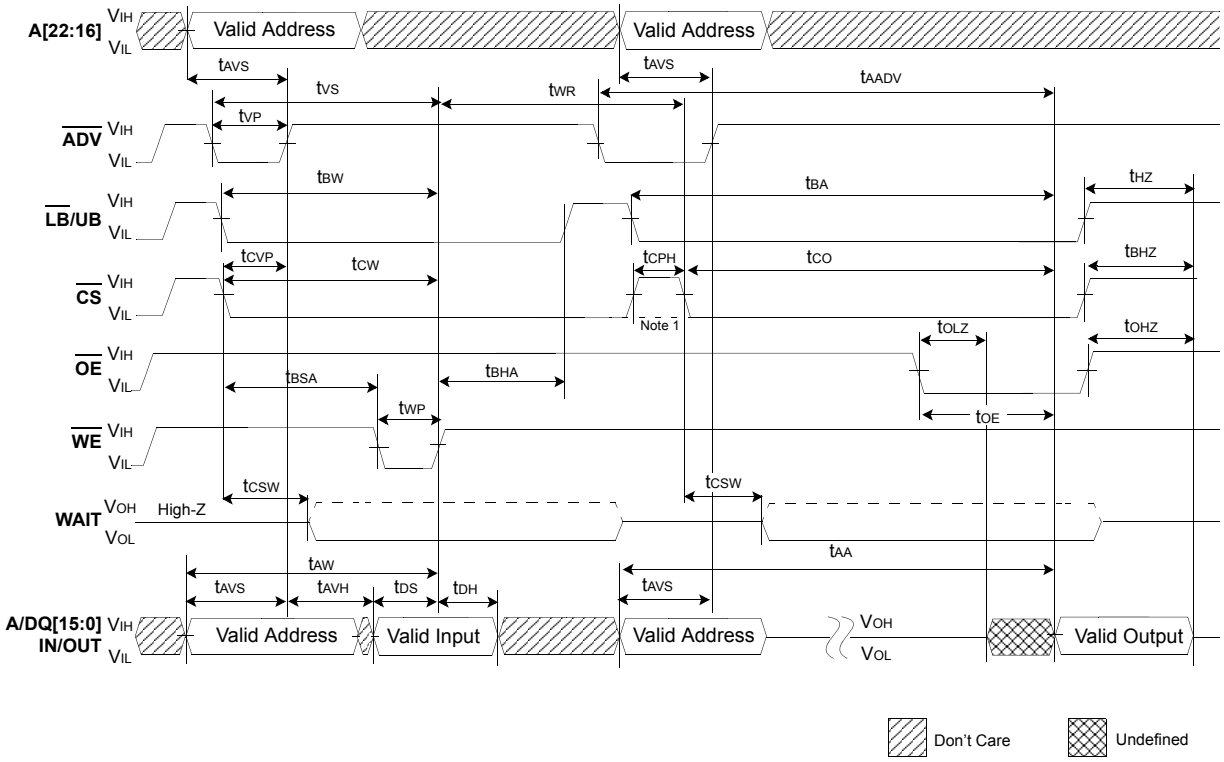
NOTE :
1) Non-default BCR settings for burst WRITE followed by burst READ: Variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2) A refresh opportunity must be provided every tCSM by taking $\overline{CS}$ HIGH.
3) Don't care must be in VIL or VIH.

11.21 Burst WRITE Followed by Burst READ, Fixed Latency



NOTE :
1) Non-default BCR settings for burst WRITE followed by burst READ: fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asseted during delay.
2) A refresh opportunity must be provided every tCSM by taking $\overline{CS}$ HIGH.
3) Don't care must be in VIL or VIH.

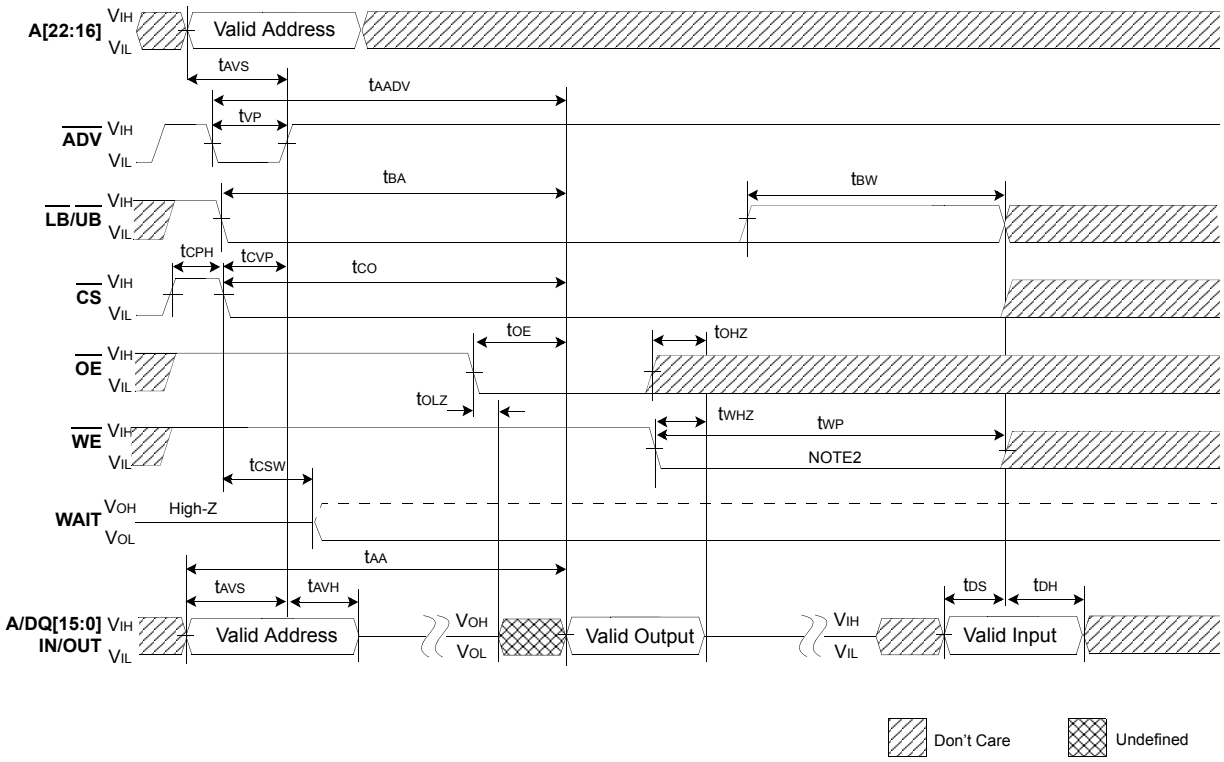
11.22 Asynchronous WRITE Followed by Asynchronous READ



NOTE :

1) $\overline{CS}$ can stay LOW when transitioning between asynchronous operations. If $\overline{CS}$ goes HIGH, it must remain HIGH for at least tCPH to schedule the appropriate internal refresh operation.
2) Don't care must be in V_{IL} or V_{IH}.

11.23 Asynchronous READ Followed by WRITE at the Same Address



NOTE :
1) The end of the WRITE cycle is controlled by $\overline{CS}$, $\overline{LB}$/$\overline{UB}$, or $\overline{WE}$, whichever de-asserts first.
2) $\overline{WE}$ must not remain LOW longer than 2.5μs (tCSM) while the device is selected ($\overline{CS}$ LOW).
3) Don't care must be in VIL or VIH.