



K60 Sub-Family Data Sheet

Supports the following:

MK60N256VLL100, MK60X256VLL100,
MK60N512VLL100, MK60N256V? L100,
MK60X256V? L100, MK60N512V? L100

Features

- Operating Characteristics
 - Voltage range: 1.71 to 3.6 V
 - Flash write voltage range: 1.71 to 3.6 V
 - Temperature range (ambient): -40 to 105°C
- Performance
 - Up to 100 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz
- Memories and memory interfaces
 - Up to 512 KB program flash memory on non-FlexMemory devices
 - Up to 256 KB program flash memory on FlexMemory devices
 - Up to 256 KB FlexNVM on FlexMemory devices
 - 4 KB FlexRAM on FlexMemory devices
 - Up to 128 KB RAM
 - Serial programming interface (EzPort)
 - FlexBus external bus interface
- Clocks
 - 1 to 32 MHz crystal oscillator
 - 32 kHz crystal oscillator
 - Multi-purpose clock generator
- System peripherals
 - 10 low-power modes to provide power optimization based on application requirements
 - Memory protection unit with multi-master protection
 - 16-channel DMA controller, supporting up to 64 request sources
 - External watchdog monitor
 - Software watchdog
 - Low-leakage wakeup unit
- Security and integrity modules
 - Hardware CRC module to support fast cyclic redundancy checks
 - Hardware random-number generator
 - Hardware encryption supporting DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
 - 128-bit unique identification (ID) number per chip
- Human-machine interface
 - Low-power hardware touch sensor interface (TSI)
 - General-purpose input/output
- Analog modules
 - 16-bit SAR ADC with PGA (x64)
 - 12-bit DAC
 - Analog comparator (CMP) containing a 6-bit DAC and programmable reference input
 - Voltage reference
- Timers
 - Programmable delay block
 - Eight-channel motor control/general purpose/PWM timers
 - Two-channel quadrature decoder/general purpose timers
 - IEEE 1588 timers
 - Periodic interrupt timers
 - 16-bit low-power timer
 - Carrier modulator transmitter
 - Real-time clock

www.DataSheet4U.com



This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

© 2010–2010 Freescale Semiconductor, Inc.

Preliminary

- Communication interfaces
 - Ethernet controller with MII and RMII interface to external PHY and hardware IEEE 1588 capability
 - USB full-/low-speed On-the-Go controller with on-chip transceiver
 - Controller Area Network (CAN) module
 - SPI modules
 - I2C modules
 - UART modules
 - Secure Digital host controller (SDHC)
 - I2S

Preliminary

Table of Contents

| | | | | | |
|---------|--|----|---------|--|----|
| 1 | Ordering parts..... | 5 | 6 | Peripheral operating requirements and behaviors..... | 20 |
| 1.1 | Determining valid orderable parts..... | 5 | 6.1 | Core modules..... | 20 |
| 2 | Part identification..... | 5 | 6.1.1 | Debug trace timing specifications..... | 20 |
| 2.1 | Description..... | 5 | 6.1.2 | JTAG electricals..... | 21 |
| 2.2 | Format..... | 5 | 6.2 | System modules..... | 24 |
| 2.3 | Fields..... | 5 | 6.3 | Clock modules..... | 24 |
| 2.4 | Example..... | 6 | 6.3.1 | MCG Specifications..... | 24 |
| 3 | Terminology and guidelines..... | 6 | 6.3.2 | Oscillator Electrical Characteristics..... | 26 |
| 3.1 | Definition: Operating requirement..... | 6 | 6.3.2.1 | Oscillator DC Electrical Specifications..... | 26 |
| 3.2 | Definition: Operating behavior..... | 7 | 6.3.2.2 | Oscillator frequency specifications..... | 27 |
| 3.3 | Definition: Attribute..... | 7 | 6.3.3 | 32kHz Oscillator Electrical Characteristics..... | 28 |
| 3.4 | Definition: Rating..... | 8 | 6.3.3.1 | 32kHz Oscillator DC Electrical Specifications..... | 28 |
| 3.5 | Result of exceeding a rating..... | 8 | 6.3.3.2 | 32kHz Oscillator Frequency Specifications..... | 28 |
| 3.6 | Relationship between ratings and operating requirements..... | 8 | 6.4 | Memories and memory interfaces..... | 29 |
| 3.7 | Guidelines for ratings and operating requirements..... | 9 | 6.4.1 | Flash (FTFL) Electrical Characteristics..... | 29 |
| 3.8 | Definition: Typical value..... | 9 | 6.4.1.1 | Flash Timing Parameters — Program and Erase..... | 29 |
| 3.9 | Typical Value Conditions..... | 10 | 6.4.1.2 | Flash Timing Parameters — Commands..... | 29 |
| 4 | Ratings..... | 10 | 6.4.1.3 | Flash (FTFL) Current and Power Parameters..... | 31 |
| 4.1 | Thermal handling ratings..... | 10 | 6.4.1.4 | Reliability Characteristics..... | 31 |
| 4.2 | Moisture handling ratings..... | 11 | 6.4.1.5 | Write Endurance to FlexRAM for EEPROM..... | 32 |
| 4.3 | ESD handling ratings..... | 11 | 6.4.2 | EzPort Switching Specifications..... | 33 |
| 4.4 | Voltage and current operating ratings..... | 11 | 6.4.3 | Flexbus Switching Specifications..... | 34 |
| 5 | General..... | 12 | 6.5 | Security and integrity modules..... | 36 |
| 5.1 | Nonswitching electrical specifications..... | 12 | 6.6 | Analog..... | 36 |
| 5.1.1 | Voltage and Current Operating Requirements..... | 12 | 6.6.1 | ADC electrical specifications..... | 36 |
| 5.1.2 | LVD and POR operating requirements..... | 13 | 6.6.1.1 | 16-bit ADC operating conditions..... | 37 |
| 5.1.3 | Voltage and current operating behaviors..... | 14 | 6.6.1.2 | 16-bit ADC electrical characteristics..... | 39 |
| 5.1.4 | Power mode transition operating behaviors..... | 14 | 6.6.1.3 | 16-bit ADC with PGA operating conditions..... | 42 |
| 5.1.5 | Power consumption operating behaviors..... | 15 | 6.6.1.4 | 16-bit ADC with PGA characteristics..... | 43 |
| 5.1.5.1 | Diagram: Typical IDD_RUN operating behavior..... | 17 | 6.6.2 | CMP and 6-bit DAC electrical specifications..... | 44 |
| 5.1.6 | EMC radiated emissions operating behaviors..... | 18 | 6.6.3 | 12-bit DAC electrical characteristics..... | 45 |
| 5.1.7 | Designing with radiated emissions in mind..... | 19 | 6.6.3.1 | 12-bit DAC operating requirements..... | 45 |
| 5.1.8 | Capacitance attributes..... | 19 | | | |
| 5.2 | Switching electrical specifications..... | 19 | | | |
| 5.3 | Thermal specifications..... | 19 | | | |
| 5.3.1 | Thermal operating requirements..... | 20 | | | |
| 5.3.2 | Thermal attributes..... | 20 | | | |

| | | | | | |
|---------|---|----|-------|--|----|
| 6.6.3.2 | 12-bit DAC operating behaviors..... | 46 | 6.8.7 | SDHC Specifications..... | 56 |
| 6.6.4 | Voltage Reference Electrical Specifications..... | 48 | 6.8.8 | I2S Switching Specifications..... | 57 |
| 6.7 | Timers..... | 49 | 6.9 | Human-machine interfaces (HMI)..... | 59 |
| 6.8 | Communication interfaces..... | 49 | 6.9.1 | General Switching Specifications..... | 59 |
| 6.8.1 | Ethernet Switching Specifications..... | 50 | 6.9.2 | TSI Electrical Specifications..... | 59 |
| 6.8.2 | USB electrical specifications..... | 51 | 7 | Dimensions..... | 60 |
| 6.8.3 | USB DCD Electrical Specifications..... | 51 | 7.1 | Obtaining package dimensions..... | 60 |
| 6.8.4 | USB Voltage Regulator Electrical Specifications. .52 | | 8 | Pinout..... | 61 |
| 6.8.5 | DSPI Switching Specifications for Low-speed Operation..... | 52 | 8.1 | K60 Signal Multiplexing and Pin Assignments..... | 61 |
| 6.8.6 | DSPI Switching Specifications (High-speed mode)..... | 54 | 8.2 | K60 Pinouts..... | 64 |
| | | | 9 | Revision History..... | 65 |

Preliminary

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: PK60 and MK60.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## M FFF T PP CCC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|-------|----------------------|--|
| Q | Qualification status | <ul style="list-style-type: none"> M = Fully qualified, general market flow P = Prequalification |
| K## | Kinetis family | <ul style="list-style-type: none"> K60 |
| M | Flash memory type | <ul style="list-style-type: none"> N = Program flash only X = Program flash and FlexMemory |

Table continues on the next page...

Terminology and guidelines

| Field | Description | Values |
|-------|-----------------------------|---|
| FFF | Program flash memory size | <ul style="list-style-type: none">• 32 = 32 KB• 64 = 64 KB• 128 = 128 KB• 256 = 256 KB• 512 = 512 KB• 1M0 = 1 MB |
| T | Temperature range (°C) | <ul style="list-style-type: none">• V = -40 to 105 |
| PP | Package identifier | <ul style="list-style-type: none">• FM = 32 QFN (5 mm x 5 mm)• FT = 48 QFN (7 mm x 7 mm)• LF = 48 LQFP (7 mm x 7 mm)• FX = 64 QFN (9 mm x 9 mm)• LH = 64 LQFP (10 mm x 10 mm)• LK = 80 LQFP (12 mm x 12 mm)• MB = 81 MAPBGA (8 mm x 8 mm)• LL = 100 LQFP (14 mm x 14 mm)• ML = 104 MAPBGA (8 mm x 8 mm)• LQ = 144 LQFP (20 mm x 20 mm)• MD = 144 MAPBGA (13 mm x 13 mm)• MF = 196 MAPBGA (15 mm x 15 mm)• MJ = 256 MAPBGA (17 mm x 17 mm) |
| CCC | Maximum CPU frequency (MHz) | <ul style="list-style-type: none">• 50 = 50 MHz• 72 = 72 MHz• 100 = 100 MHz• 120 = 120 MHz• 150 = 150 MHz |
| N | Packaging type | <ul style="list-style-type: none">• R = Tape and reel• (Blank) = Trays |

2.4 Example

This is an example part number:

MK60N512VMD100

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | 0.9 | 1.1 | V |

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|--|------|------|------|
| I _{WP} | Digital I/O weak pullup/pulldown current | 10 | 130 | μA |

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

www.DataSheet4U.com

| Symbol | Description | Min. | Max. | Unit |
|--------|---------------------------------|------|------|------|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

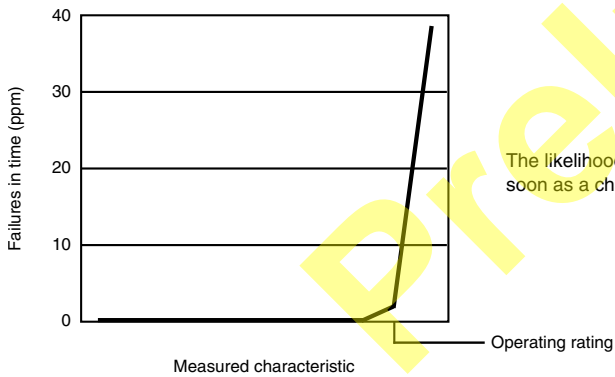
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | -0.3 | 1.2 | V |

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

3.6 Relationship between ratings and operating requirements

| | | | | | | | |
|-------------------------------------|---|---|---|------------------------------|--|-------------------------------------|--|
| Operating or handling rating (min.) | | Operating requirement (min.) | | Operating requirement (max.) | | Operating or handling rating (max.) | |
| Fatal range | Limited operating range | Normal operating range | Limited operating range | Fatal range | | | |
| - Probable permanent failure | - No permanent failure - Possible decreased life - Possible incorrect operation | - No permanent failure - Correct operation | - No permanent failure - Possible decreased life - Possible incorrect operation | - Probable permanent failure | | | |
| Handling range | | | | | | | |
| - No permanent failure | | | | | | | |

3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

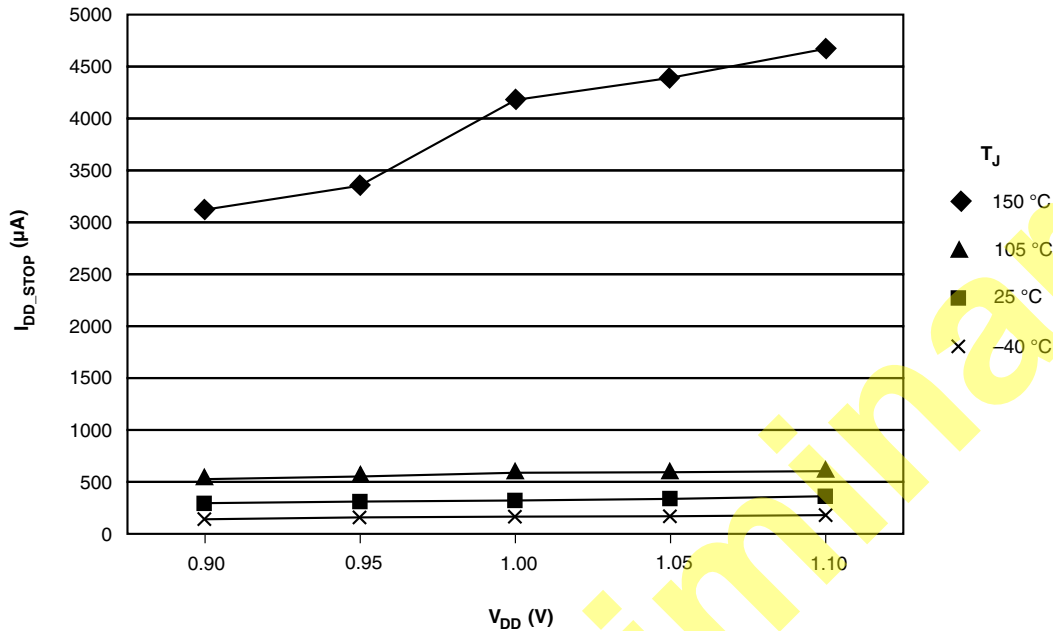
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------------|--|------|------|------|------|
| I _{WP} | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | μA |

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|-----------------|----------------------|-------|------|
| T _A | Ambient temperature | 25 | °C |
| V _{DD} | 3.3 V supply voltage | 3.3 | V |

4 Ratings

4.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|------|-------|
| T _{STG} | Storage temperature | -55 | 150 | °C | 1 |
| T _{SDR} | Solder temperature, lead-free | — | 260 | °C | 2 |
| | Solder temperature, leaded | — | 245 | | |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|-------|-------|------|-------|
| V _{HBM} | Electrostatic discharge voltage, human body model | -2000 | +2000 | V | 1 |
| V _{CDM} | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| I _{LAT} | Latch-up current at ambient temperature of 85°C | -100 | +100 | mA | |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|------------------|---|------|-----------------------|------|
| V _{DD} | Digital supply voltage | -0.3 | 3.8 | V |
| I _{DD} | Digital supply current | — | 185 | mA |
| V _{DIO} | Digital input voltage (except RESET, EXTAL, and XTAL) | -0.3 | 5.5 | V |
| V _{AIO} | Analog, RESET, EXTAL, and XTAL input voltage | -0.3 | V _{DD} + 0.3 | V |

Table continues on the next page...

General

| Symbol | Description | Min. | Max. | Unit |
|---------------|---|----------------|----------------|------|
| I_D | Instantaneous maximum current single pin limit (applies to all port pins) | -25 | 25 | mA |
| V_{DDA} | Analog supply voltage | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V |
| I_{DDA} | Analog supply current ¹ | TBD | TBD | mA |
| V_{USB_DP} | USB_DP input voltage | -0.3 | 3.63 | V |
| V_{USB_DM} | USB_DM input voltage | -0.3 | 3.63 | V |
| VREGIN | USB regulator input | -0.3 | 6.0 | V |
| V_{BAT} | RTC battery supply voltage | -0.3 | 3.8 | V |
| V_{RAM} | V_{DD} voltage required to retain RAM | 1.2 | — | V |
| V_{RFVBAT} | V_{BAT} voltage required to retain the VBAT register file | TBD | — | V |

- The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.

5 General

5.1 Nonswitching electrical specifications

5.1.1 Voltage and Current Operating Requirements

Table 1. Voltage and current operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------------------|---|----------------------|----------------------|------|-------|
| V_{DD} | Supply voltage | 1.71 | 3.6 | V | |
| V_{DDA} | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} - V_{DDA}$ | V_{DD} -to- V_{DDA} differential voltage | -0.1 | 0.1 | V | |
| $V_{SS} - V_{SSA}$ | V_{SS} -to- V_{SSA} differential voltage | -0.1 | 0.1 | V | |
| V_{IH} | Input high voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ | $0.7 \times V_{DD}$ | — | V | |
| | | $0.75 \times V_{DD}$ | — | V | |
| V_{IL} | Input low voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ | — | $0.35 \times V_{DD}$ | V | |
| | | — | $0.3 \times V_{DD}$ | V | |
| V_{HYS} | Input hysteresis | $0.06 \times V_{DD}$ | — | V | |

Table continues on the next page...

Table 1. Voltage and current operating requirements (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|----------|--|------|------|------|-------|
| I_{IC} | DC injection current — single pin | | | | 1 |
| | <ul style="list-style-type: none"> $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$ | 0 | 2 | mA | |
| | DC injection current — total MCU limit, includes sum of all stressed pins | | | | 1 |
| | <ul style="list-style-type: none"> $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$ | 0 | 25 | mA | |
| | | 0 | -5 | mA | |

1. All functional non-supply pins are internally clamped to VSS and VDD. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values. Power supply must maintain regulation within operating VDD range during instantaneous and operating maximum current conditions. If positive injection current ($V_{IN} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of VDD and could result in external power supply going out of regulation. Ensure external VDD load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

5.1.2 LVD and POR operating requirements

Table 2. LVD and POR operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------|---|------|------|------|------|-------|
| V_{POR} | Falling VDD POR detect voltage | TBD | 1.1 | TBD | V | |
| V_{LVDH} | Falling low-voltage detect threshold — high range (LVDV=01) | TBD | 2.56 | TBD | V | |
| | Low-voltage warning thresholds — high range | | | | | 1 |
| V_{LVW1} | <ul style="list-style-type: none"> Level 1 falling (LVWV=00) | TBD | 2.70 | TBD | V | |
| V_{LVW2} | <ul style="list-style-type: none"> Level 2 falling (LVWV=01) | TBD | 2.80 | TBD | V | |
| V_{LVW3} | <ul style="list-style-type: none"> Level 3 falling (LVWV=10) | TBD | 2.90 | TBD | V | |
| V_{LVW4} | <ul style="list-style-type: none"> Level 4 falling (LVWV=11) | TBD | 3.00 | TBD | V | |
| V_{HYS} | Low-voltage inhibit reset/recover hysteresis — high range | | 60 | | mV | |
| V_{LVDL} | Falling low-voltage detect threshold — low range (LVDV=00) | TBD | TBD | TBD | V | |
| | Low-voltage warning thresholds — low range | | | | | 1 |
| V_{LVW1} | <ul style="list-style-type: none"> Level 1 falling (LVWV=00) | TBD | 1.80 | TBD | V | |
| V_{LVW2} | <ul style="list-style-type: none"> Level 2 falling (LVWV=01) | TBD | 1.90 | TBD | V | |
| V_{LVW3} | <ul style="list-style-type: none"> Level 3 falling (LVWV=10) | TBD | 2.00 | TBD | V | |
| V_{LVW4} | <ul style="list-style-type: none"> Level 4 falling (LVWV=11) | TBD | 2.10 | TBD | V | |

Table continues on the next page...

Table 2. LVD and POR operating requirements (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------|--|------|------|------|---------|-------|
| V_{HYS} | Low-voltage inhibit reset/recover hysteresis — low range | | 40 | | mV | |
| V_{BG} | Bandgap voltage reference | TBD | 1.00 | TBD | V | |
| t_{LPO} | Internal low power oscillator period factory trimmed | TBD | 1000 | TBD | μ s | |

1. Rising thresholds are falling threshold + V_{HYS}

5.1.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------------------|--|----------------|------|------------|-------|
| V_{OH} | Output high voltage — high drive strength | | | | |
| | • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -10\text{mA}$ | $V_{DD} - 0.5$ | — | V | |
| | • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -3\text{mA}$ | $V_{DD} - 0.5$ | — | V | |
| | Output high voltage — low drive strength | | | | |
| V_{OL} | • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = -2\text{mA}$ | $V_{DD} - 0.5$ | — | V | |
| | • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = -0.6\text{mA}$ | $V_{DD} - 0.5$ | — | V | |
| I_{OHT} | Output high current total for all ports | — | 100 | mA | |
| V_{OL} | Output low voltage — high drive strength | | | | |
| | • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 10\text{mA}$ | — | 0.5 | V | |
| | • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 3\text{mA}$ | — | 0.5 | V | |
| | Output low voltage — low drive strength | | | | |
| I_{OLT} | • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 2\text{mA}$ | — | 0.5 | V | |
| | • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 0.6\text{mA}$ | — | 0.5 | V | |
| I_{OLT} | Output low current total for all ports | — | 100 | mA | |
| I_{IN} | Input leakage current (per pin) | — | 1 | μ A | |
| I_{OZ} | Hi-Z (off-state) leakage current (per pin) | — | 1 | μ A | |
| R_{PU} and R_{PD} | Internal weak pullup and pulldown resistors | 30 | 50 | k Ω | 1 |

1. Measured at V_{IL} max and V_{DD} min

5.1.4 Power mode transition operating behaviors

In the table below, all specifications except t_{POR} , assume the following clock configuration:

- CPU and system clocks = 100MHz
- Bus and FlexBus clocks = 50 MHz
- Flash clock = 25 MHz

Table 4. Power mode transition operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|--|------|-------|---------|-------|
| t_{POR} | After a POR event, amount of time from the point V_{DD} reaches 1.8V to execution of the first instruction across the operating temperature range of the chip. | — | 300 | μs | 1 |
| | RUN \rightarrow VLLS1 \rightarrow RUN | | | | |
| | • RUN \rightarrow VLLS1 | — | 4.1 | μs | |
| | • VLLS1 \rightarrow RUN | — | 123.8 | μs | |
| | RUN \rightarrow VLLS2 \rightarrow RUN | | | | |
| | • RUN \rightarrow VLLS2 | — | 4.1 | μs | |
| | • VLLS2 \rightarrow RUN | — | 49.3 | μs | |
| | RUN \rightarrow VLLS3 \rightarrow RUN | | | | |
| | • RUN \rightarrow VLLS3 | — | 4.1 | μs | |
| | • VLLS3 \rightarrow RUN | — | 49.2 | μs | |
| | RUN \rightarrow LLS \rightarrow RUN | | | | |
| | • RUN \rightarrow LLS | — | 4.1 | μs | |
| | • LLS \rightarrow RUN | — | 5.9 | μs | |
| | RUN \rightarrow STOP \rightarrow RUN | | | | |
| | • RUN \rightarrow STOP | — | 4.1 | μs | |
| | • STOP \rightarrow RUN | — | 4.2 | μs | |
| | RUN \rightarrow VLPS \rightarrow RUN | | | | |
| | • RUN \rightarrow VLPS | — | 4.1 | μs | |
| | • VLPS \rightarrow RUN | — | 5.8 | μs | |

1. Normal boot (FTFL_OPT[LPBOOT]=1)

www.DataSheet4U.com

5.1.5 Power consumption operating behaviors

Table 5. Power consumption operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------------|--|------|------|------|------|-------|
| I _{DD_RUN} | Run mode current — all peripheral clocks disabled, code executing from flash <ul style="list-style-type: none"> @ 1.8V @ 3.0V | — | 40 | TBD | mA | 1 |
| | | — | 42 | TBD | mA | |
| I _{DD_RUN} | Run mode current — all peripheral clocks enabled, code executing from flash <ul style="list-style-type: none"> @ 1.8V @ 3.0V | — | 55 | TBD | mA | 2 |
| | | — | 56 | TBD | mA | |
| I _{DD_RUN_M} AX | Run mode current — all peripheral clocks enabled and peripherals active, code executing from flash <ul style="list-style-type: none"> @ 1.8V @ 3.0V | — | 85 | TBD | mA | 3 |
| | | — | 85 | TBD | mA | |
| I _{DD_WAIT} | Wait mode current at 3.0 V — all peripheral clocks disabled | — | 15 | TBD | mA | 4 |
| I _{DD_STOP} | Stop mode current at 3.0 V | — | 1.4 | TBD | mA | |
| I _{DD_VLPR} | Very-low-power run mode current at 3.0 V — all peripheral clocks disabled | — | 1.25 | TBD | mA | 5 |
| I _{DD_VLPR} | Very-low-power run mode current at 3.0 V — all peripheral clocks enabled | — | TBD | TBD | mA | 6 |
| I _{DD_VLPW} | Very-low-power wait mode current at 3.0 V | — | 1.05 | TBD | mA | 7 |
| I _{DD_VLPS} | Very-low-power stop mode current at 3.0 V | — | 30 | TBD | μA | |
| I _{DD_LLS} | Low leakage stop mode current at 3.0 V | — | 12 | TBD | μA | |
| I _{DD_VLLS3} | Very low-leakage stop mode 3 current at 3.0 V <ul style="list-style-type: none"> 128KB RAM devices 64KB RAM devices | — | 8 | TBD | μA | |
| | | — | 6 | TBD | μA | |
| I _{DD_VLLS2} | Very low-leakage stop mode 2 current at 3.0 V | — | 4 | TBD | μA | |
| I _{DD_VLLS1} | Very low-leakage stop mode 1 current at 3.0 V | — | 2 | TBD | μA | |
| I _{DD_VBAT} | Average current when CPU is not accessing RTC registers at 3.0 V | — | 550 | TBD | nA | |

- 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
- 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, but peripherals are not in active operation.
- 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
- 25MHz core and system clock, 25MHz bus clock, and 12.5MHz FlexBus and flash clock. MCG configured for FEI mode.
- 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for fast IRCLK mode. All peripheral clocks disabled. Code executing from flash.

6. 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for fast IRCLK mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
7. 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for fast IRCLK mode. All peripheral clocks disabled.

5.1.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FEI mode (39.0625 kHz IRC), except for 1 MHz core (FBE)
- All peripheral clocks disabled except FTFLL
- LVD disabled, USB regulator disabled
- No GPIOs toggled
- Code execution from flash

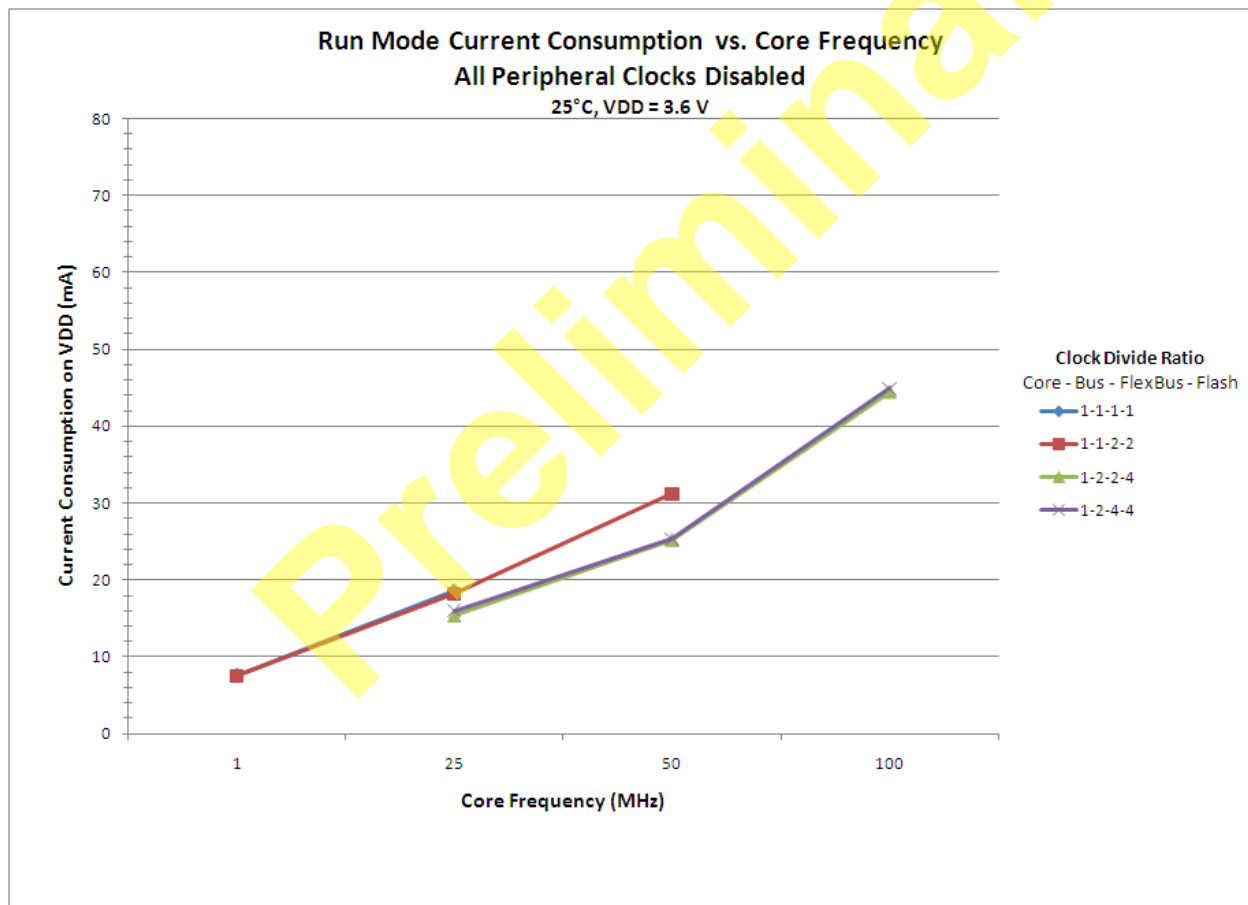


Figure 1. Run mode supply current vs. core frequency — all peripheral clocks disabled

www.DataSheet4U.com

The following data was measured under these conditions:

- MCG in FEI mode (39.0625 kHz IRC), except for 1 MHz core (FBE)
- All peripheral clocks enabled but peripherals are not in active operation
- LVD disabled, USB regulator disabled

General

- No GPIOs toggled
- Code execution from flash

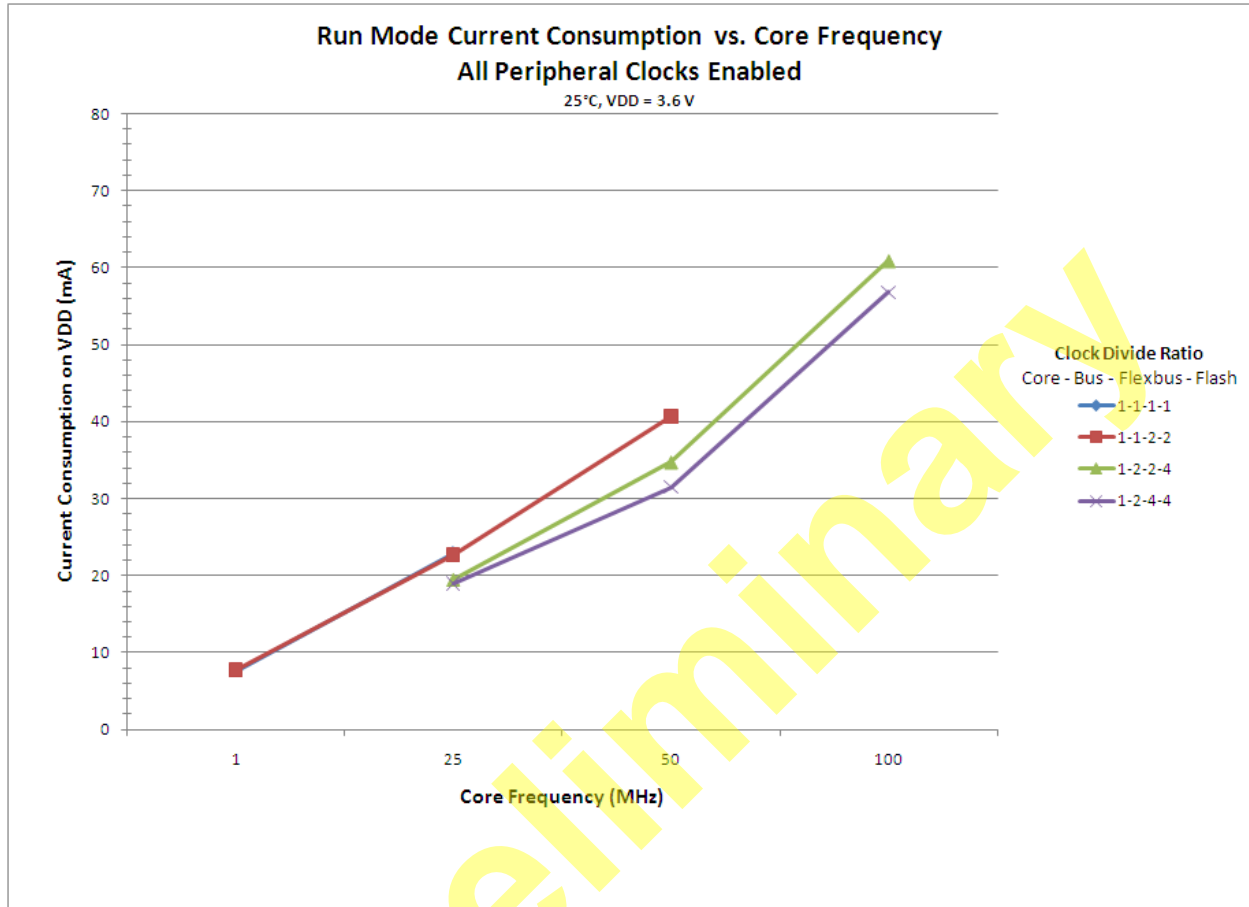


Figure 2. Run mode supply current vs. core frequency — all peripheral clocks enabled

5.1.6 EMC radiated emissions operating behaviors

Table 6. EMC radiated emissions operating behaviors

| Symbol | Description | Frequency band (MHz) | Typ. | Unit | Notes |
|-------------------------|------------------------------------|----------------------|------|------|-------|
| V _{RE1} | Radiated emissions voltage, band 1 | 0.15–50 | TBD | dBμV | 1, 2 |
| V _{RE2} | Radiated emissions voltage, band 2 | 50–150 | TBD | | |
| V _{RE3} | Radiated emissions voltage, band 3 | 150–500 | TBD | | |
| V _{RE4} | Radiated emissions voltage, band 4 | 500–1000 | TBD | | |
| V _{RE_IEC_SAE} | IEC and SAE level | 0.15–1000 | TBD | — | 2, 3 |

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions*, IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*, and SAE Standard J1752-3, *Measurement of Radiated Emissions from Integrated Circuits—TEM/ Wideband TEM (GTEM) Cell Method*.

2. $V_{DD} = 3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $f_{OSC} = 16\text{ MHz}$ (crystal), $f_{BUS} = 20\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*, and Appendix D of SAE Standard J1752-3, *Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method*.

5.1.7 Designing with radiated emissions in mind

1. To find application notes that provide guidance on designing your system to minimize interference from radiated emissions, go to www.freescale.com and perform a keyword search for “EMC design.”

5.1.8 Capacitance attributes

Table 7. Capacitance attributes

| Symbol | Description | Min. | Max. | Unit |
|-------------|---------------------------------|------|------|------|
| C_{IN_A} | Input capacitance: analog pins | — | 7 | pF |
| C_{IN_D} | Input capacitance: digital pins | — | 7 | pF |

5.2 Switching electrical specifications

Table 8. Device clock specifications

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------------|-----------------------|------|------|------|-------|
| Normal run mode | | | | | |
| f_{SYS} | System and core clock | — | 100 | MHz | |
| f_{BUS} | Bus clock | — | 50 | MHz | |
| FB_CLK | FlexBus clock | — | 50 | MHz | |
| f_{FLASH} | Flash clock | — | 25 | MHz | |
| VLPR mode | | | | | |
| f_{SYS} | System and core clock | — | 2 | MHz | |
| f_{BUS} | Bus clock | — | 2 | MHz | |
| FB_CLK | FlexBus clock | — | 2 | MHz | |
| f_{FLASH} | Flash clock | — | 1 | MHz | |

5.3 Thermal specifications

5.3.1 Thermal operating requirements

Table 9. Thermal operating requirements

| Symbol | Description | Min. | Max. | Unit |
|--------|--------------------------|------|------|------|
| T_J | Die junction temperature | -40 | 125 | °C |
| T_A | Ambient temperature | -40 | 105 | °C |

5.3.2 Thermal attributes

| Board type | Symbol | Description | 104 MABGA | 100 LQFP | Unit | Notes |
|-------------------|------------------|---|-----------|----------|------|-------|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | TBD | TBD | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | TBD | TBD | °C/W | 1 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | TBD | TBD | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | TBD | TBD | °C/W | 1 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | TBD | TBD | °C/W | 2 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | TBD | TBD | °C/W | 3 |
| — | Ψ_{JT} | Thermal characterization parameter, junction to package top outside center (natural convection) | TBD | TBD | °C/W | 4 |

6 Peripheral operating requirements and behaviors

6.1 Core modules

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6.1.1 Debug trace timing specifications

Table 10. Debug trace operating behaviors

| Symbol | Description | Min. | Max. | Unit |
|-----------|--------------------------|---------------------|------|------|
| T_{cyc} | Clock period | Frequency dependent | | MHz |
| T_{wl} | Low pulse width | 2 | — | ns |
| T_{wh} | High pulse width | 2 | — | ns |
| T_r | Clock and data rise time | — | 3 | ns |
| T_f | Clock and data fall time | — | 3 | ns |
| T_s | Data setup | 3 | — | ns |
| T_h | Data hold | 2 | — | ns |

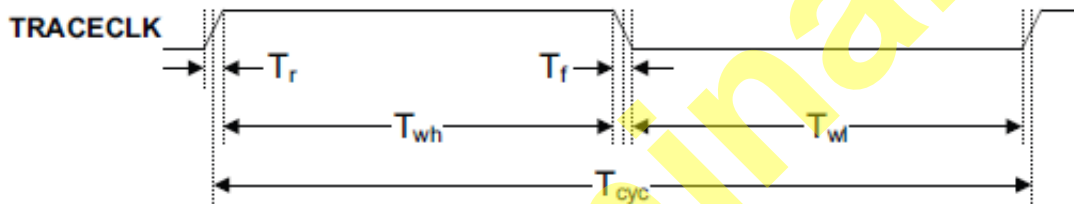


Figure 3. TRACE_CLKOUT specifications

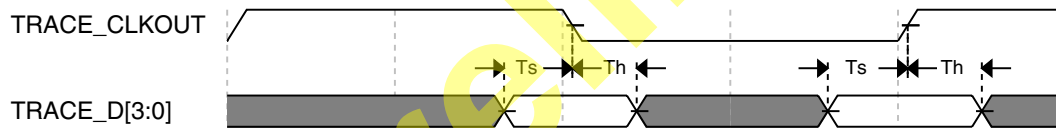


Figure 4. Trace data specifications

6.1.2 JTAG electricals

Table 11. JTAG electricals

| Symbol | Description | Min. | Max. | Unit |
|--------|---|------|------|------|
| | Operating voltage | 2.7 | 3.6 | V |
| J1 | TCLK frequency of operation <ul style="list-style-type: none"> JTAG and CJTAG Serial Wire Debug | 0 | 25 | MHz |
| J2 | TCLK cycle period | 1/J1 | — | ns |

Table continues on the next page...

Table 11. JTAG electricals (continued)

| Symbol | Description | Min. | Max. | Unit |
|--------|--|------|------|------|
| J3 | TCLK clock pulse width <ul style="list-style-type: none"> JTAG and CJTAG Serial Wire Debug | 20 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 0 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 30 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 30 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 16 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1 | — | ns |
| J11 | TCLK low to TDO data valid | — | 4 | ns |
| J12 | TCLK low to TDO high-Z | — | 4 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | 8 | — | ns |

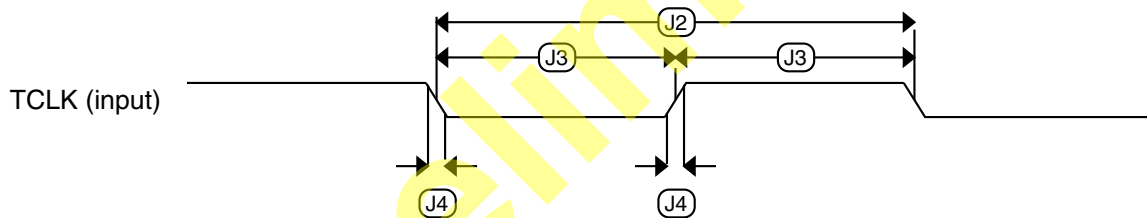


Figure 5. Test clock input timing

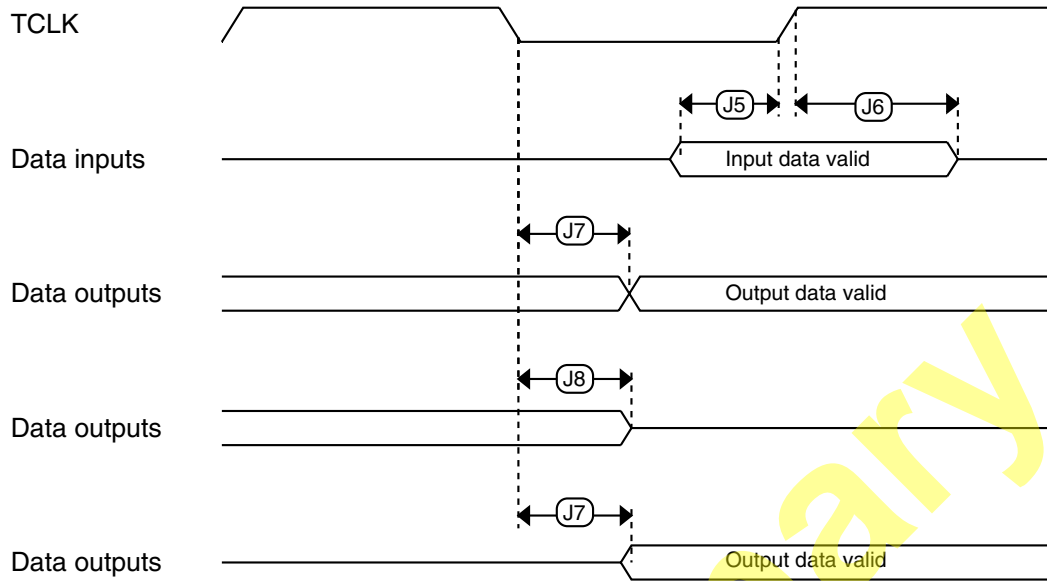


Figure 6. Boundary scan (JTAG) timing

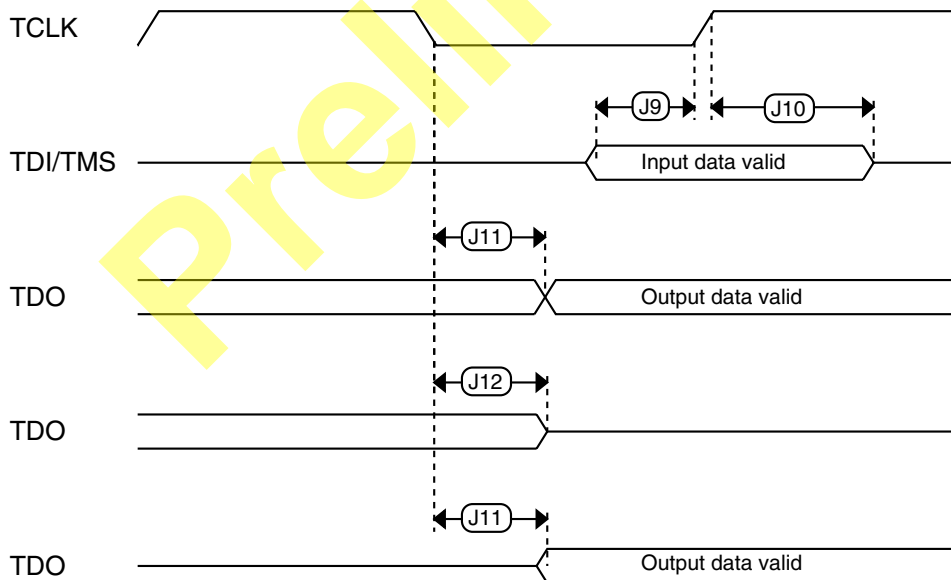


Figure 7. Test Access Port timing

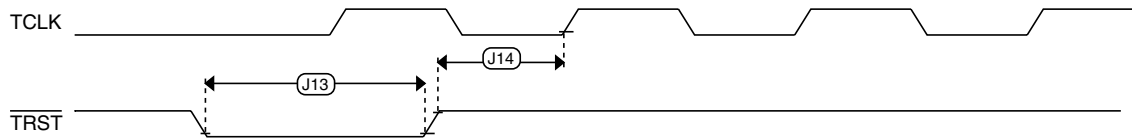


Figure 8. TRST timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.3.1 MCG Specifications

Table 12. MCG specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------------|--|-------|----------------|-----------|-------------|-------|
| f_{ints_ft} | Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25°C | — | 32.768 | — | kHz | |
| f_{ints_t} | Internal reference frequency (slow clock) — user trimmed | 31.25 | — | 39.0625 | kHz | |
| $t_{irefsts}$ | Internal reference (slow clock) startup time | — | TBD | 4 | μ s | |
| $\Delta f_{dco_res_t}$ | Resolution of trimmed DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | — | ± 0.1 | ± 0.3 | % f_{dco} | |
| $\Delta f_{dco_res_t}$ | Resolution of trimmed DCO output frequency at fixed voltage and temperature — using SCTRIM only | — | ± 0.2 | ± 0.5 | % f_{dco} | |
| Δf_{dco_t} | Total deviation of trimmed DCO output frequency over voltage and temperature | — | + 0.5 - 1.0 | ± 3.5 | % f_{dco} | |
| Δf_{dco_t} | Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0–70°C | — | ± 0.5 | \pm TBD | % f_{dco} | |
| f_{intf_ft} | Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C | 3.875 | 4 | 4.125 | MHz | |
| f_{intf_t} | Internal reference frequency (fast clock) — user trimmed | 3 | — | 5 | MHz | |

Table continues on the next page...

Table 12. MCG specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes | |
|------------------------------|---|---|------|--------------------------------------|---------------|-------|------|
| t_{irefstf} | Internal reference startup time (fast clock) | — | TBD | TBD | μs | | |
| $f_{\text{loc_low}}$ | Loss of external clock minimum frequency — RANGE = 00 | $(3/5) \times f_{\text{ints_t}}$ | — | — | kHz | | |
| $f_{\text{loc_high}}$ | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | $(16/5) \times f_{\text{ints_t}}$ | — | — | kHz | | |
| FLL | | | | | | | |
| $f_{\text{dco_t}}$ | DCO output frequency range — user trimmed and DMX32=0 | Low range (DRS=00) $640 \times f_{\text{ints_t}}$ | 20 | 20.97 | 25 | MHz | 1, 2 |
| | | Mid range (DRS=01) $1280 \times f_{\text{ints_t}}$ | 40 | 41.94 | 50 | MHz | |
| | | Mid-high range (DRS=10) $1920 \times f_{\text{ints_t}}$ | 60 | 62.91 | 75 | MHz | |
| | | High range (DRS=11) $2560 \times f_{\text{ints_t}}$ | 80 | 83.89 | 100 | MHz | |
| $f_{\text{dco_t_DMX32}}_2$ | DCO output frequency range — reference = 32,768Hz and DMX32=1 | Low range (DRS=00) $732 \times f_{\text{ints_t}}$ | — | 23.99 | — | MHz | 3 |
| | | Mid range (DRS=01) $1464 \times f_{\text{ints_t}}$ | — | 47.97 | — | MHz | |
| | | Mid-high range (DRS=10) $2197 \times f_{\text{ints_t}}$ | — | 71.99 | — | MHz | |
| | | High range (DRS=11) $2929 \times f_{\text{ints_t}}$ | — | 95.98 | — | MHz | |
| $J_{\text{cyc_fll}}$ | FLL period jitter | — | TBD | TBD | ps | 4 | |
| $J_{\text{acc_fll}}$ | FLL accumulated jitter of DCO output over a 1 μs time window | — | TBD | TBD | ps | | |
| $t_{\text{fll_acquire}}$ | FLL target frequency acquisition time | — | — | 1 | ms | 5 | |
| PLL | | | | | | | |
| f_{vco} | VCO operating frequency | 48.0 | — | 100 | MHz | | |
| $f_{\text{pll_ref}}$ | PLL reference frequency range | 2.0 | — | 4.0 | MHz | | |
| $J_{\text{cyc_pll}}$ | PLL period jitter | — | 400 | — | ps | 6, 7 | |
| $J_{\text{acc_pll}}$ | PLL accumulated jitter over 1 μs window | — | TBD | — | ps | 6, 7 | |
| D_{lock} | Lock entry frequency tolerance | ± 1.49 | — | ± 2.98 | % | | |
| D_{unl} | Lock exit frequency tolerance | ± 4.47 | — | ± 5.97 | % | | |
| $t_{\text{pll_lock}}$ | Lock detector detection time | — | — | $0.15 + 1075(1/f_{\text{pll_ref}})$ | ms | 8 | |

1. The resulting system clock frequencies should not exceed their maximum specified values.

Peripheral operating requirements and behaviors

2. This specification includes the 2% precision of the internal reference frequency (slow clock).
3. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
4. This specification was obtained at TBD frequency.
5. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
6. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
7. This specification was obtained at internal frequency of TBD.
8. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator Electrical Characteristics

This section provides the electrical characteristics of the module.

6.3.2.1 Oscillator DC Electrical Specifications

Table 13. Oscillator DC electrical specifications, ($V_{SSOSC} = 0 V_{DC}$) ($T_A = T_L$ to T_H)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---------------|---|------|------|------|---------|-------|
| $V_{DD33OSC}$ | 3.3 V supply voltage | 1.71 | — | 3.6 | V | |
| I_{DDOSC} | Supply current — low-power mode <ul style="list-style-type: none"> • 32 kHz • 1 MHz • 4 MHz • 8 MHz • 16 MHz • 24 MHz • 32 MHz | — | 500 | — | nA | 1 |
| | | — | 100 | — | μ A | |
| | | — | 200 | — | μ A | |
| | | — | 300 | — | μ A | |
| | | — | 700 | — | μ A | |
| | | — | 1.2 | — | mA | |
| | | — | 1.5 | — | mA | |
| I_{DDOSC} | Supply current — high gain mode <ul style="list-style-type: none"> • 32 kHz • 1 MHz • 4 MHz • 8 MHz • 16 MHz • 24 MHz • 32 MHz | — | 25 | — | μ A | 1 |
| | | — | 200 | — | μ A | |
| | | — | 400 | — | μ A | |
| | | — | 800 | — | μ A | |
| | | — | 1.5 | — | mA | |
| | | — | 3 | — | mA | |
| | | — | 4 | — | mA | |
| C_x | EXTAL load capacitance | — | — | — | | 2, 3 |
| C_y | XTAL load capacitance | — | — | — | | 2, 3 |

Table continues on the next page...

Table 13. Oscillator DC electrical specifications, ($V_{SSOSC} = 0 V_{DC}$) ($T_A = T_L$ to T_H) (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------|--|---------------------------|---------------|------------|------------|-------|
| R_F | Feedback resistor — low-frequency, low-power mode | — | — | — | M Ω | 2, 3 |
| | Feedback resistor — low-frequency, high-gain mode | — | 10 | — | M Ω | |
| | Feedback resistor — high-frequency, low-power mode (1 – 8 MHz, 8 – 32 MHz) | — | — | — | M Ω | |
| | Feedback resistor — high-frequency, high-gain mode (1 – 8 MHz, 8 – 32 MHz) | — | 1 | — | M Ω | |
| R_S | Series resistor — low-frequency, low-power mode | — | — | — | k Ω | |
| | Series resistor — low-frequency, high-gain mode | — | 200 | — | k Ω | |
| | Series resistor — high-frequency, low-power mode | — | — | — | k Ω | |
| | Series resistor — high-frequency, high-gain mode | | | | | |
| | • 1 MHz resonator | — | 6.6 | — | k Ω | |
| | • 2 MHz resonator | — | 3.3 | — | k Ω | |
| | • 4 MHz resonator | — | 0 | — | k Ω | |
| | • 8 MHz resonator | — | 0 | — | k Ω | |
| • 16 MHz resonator | — | 0 | — | k Ω | | |
| • 20 MHz resonator | — | 0 | — | k Ω | | |
| • 32 MHz resonator | — | 0 | — | k Ω | | |
| V_{pp} | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode | $0.75 \times V_{DD33OSC}$ | $V_{DD33OSC}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode | $0.75 \times V_{DD33OSC}$ | $V_{DD33OSC}$ | — | V | |

- $V_{DD33OSC} = 3.3$ V, Temperature = 27 °C, $C_x/C_y = 20$ pF
- See crystal or resonator manufacturer's recommendation
- R_F and C_x, C_y are integrated in low-frequency, low-power mode and must not be attached externally

6.3.2.2 Oscillator frequency specifications

Table 14. Oscillator frequency specifications, ($V_{DD33OSC} = V_{DD33OSC} (min)$ to $V_{DD33OSC} (max)$, $T_A = T_L$ to T_H)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|--|------|------|------|------|---------|
| f_{osc_lo} | Oscillator crystal or resonator frequency — low frequency mode | 32 | — | 40 | kHz | |
| $f_{osc_hi_1}$ | Oscillator crystal or resonator frequency — high frequency mode (low range) | 1 | — | 8 | MHz | |
| $f_{osc_hi_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) | 8 | — | 32 | MHz | |
| t_{dc_extal} | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| t_{cst} | Crystal start-up time — 32 kHz low-frequency, low-power mode | — | TBD | — | ms | 1, 2, 3 |
| | Crystal start-up time — 32 kHz low-frequency, high-gain mode | — | 800 | — | ms | |
| | Crystal start-up time — 8 MHz high-frequency, low-power mode | — | 4 | — | ms | |
| | Crystal start-up time — 8 MHz high-frequency, high-gain mode | — | 3 | — | ms | |

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.
3. Crystal start up time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

6.3.3 32kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

6.3.3.1 32kHz Oscillator DC Electrical Specifications

Table 15. 32kHz Oscillator Module DC Electrical Specifications ($V_{SSOSC} = 0 V_{DC}$) ($T_A = T_L$ to T_H)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|------------|---|------|------|------|------------|
| V_{BAT} | Supply voltage | 1.71 | — | 3.6 | V |
| R_F | Internal feedback resistor | — | 100 | — | M Ω |
| C_{para} | Parasitical capacitance of EXTAL32 and XTAL32 | — | 2.5 | — | pF |
| C_{load} | Internal load capacitance (programmable) | — | 15 | — | pF |
| V_{pp} | Peak-to-peak amplitude of oscillation | — | 0.6 | — | V |

6.3.3.2 32kHz Oscillator Frequency Specifications

Table 16. 32kHz oscillator frequency specifications ($V_{DD33OSC} = V_{DD33OSC}(\text{min})$ to $V_{DD33OSC}(\text{max})$, $T_A = T_L$ to T_H)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---------------|-----------------------|------|------|------|------|-------|
| f_{osc_lo} | Oscillator crystal | — | 32 | — | kHz | |
| t_{start} | Crystal start-up time | — | 1000 | — | ms | 1, 2 |

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

6.4 Memories and memory interfaces

6.4.1 Flash (FTFL) Electrical Characteristics

This section describes the electrical characteristics of the FTFL module.

6.4.1.1 Flash Timing Parameters — Program and Erase

The following characteristics represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 17. NVM program/erase timing characteristics

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------------|------------------------------------|------|------|------|---------------|-------|
| t_{hvpgm4} | Longword Program high-voltage time | — | 20 | TBD | μs | |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 20 | 100 | ms | 1 |
| $t_{hversblk}$ | Erase Block high-voltage time | — | 160 | 800 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash Timing Parameters — Commands

Table 18. Flash command timing characteristics

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------------|--|------|------|------|---------------|-------|
| t_{rd1blk} | Read 1s Block execution time | — | — | 1.4 | ms | |
| $t_{rd1sec2k}$ | Read 1s Section execution time (2 KB flash sector) | — | — | 40 | μs | |
| t_{pgmchk} | Program Check execution time | — | — | 35 | μs | |

Table continues on the next page...

Table 18. Flash command timing characteristics (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--|---|------|------|------|---------|-------|
| t_{rdsrc} | Read Resource execution time | — | — | 35 | μ s | 1 |
| t_{pgm4} | Program Longword execution time | — | 50 | TBD | μ s | |
| t_{ersblk} | Erase Flash Block execution time | — | 160 | 800 | ms | 2 |
| t_{ersscr} | Erase Flash Sector execution time | — | 20 | 100 | ms | 2 |
| $t_{pgmsec2k}$ | Program Section execution time (2 KB flash sector) | — | TBD | TBD | ms | |
| t_{rd1all} | Read 1s All Blocks execution time | — | — | 2.8 | ms | |
| t_{rdonce} | Read Once execution time | — | — | 35 | μ s | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 50 | TBD | μ s | |
| t_{ersall} | Erase All Blocks execution time | — | 320 | 1600 | ms | 2 |
| t_{vfykey} | Verify Backdoor Access Key execution time | — | — | 35 | μ s | 1 |
| $t_{pgmpart}$ | Program Partition for EEPROM execution time | — | 175 | TBD | ms | |
| $t_{setram32k}$ | Set FlexRAM Function execution time for 32 KB of EEPROM backup | — | TBD | TBD | ms | |
| $t_{setram256k}$ | Set FlexRAM Function execution time for 256 KB of EEPROM backup | — | TBD | TBD | ms | |
| Byte-write to FlexRAM for EEPROM operation | | | | | | |
| $t_{eewr8bers}$ | Byte-write to erased FlexRAM location execution time | — | 100 | TBD | μ s | 3 |
| $t_{eewr8b32k}$ | Byte-write to FlexRAM execution time (32 KB EEPROM backup) | — | TBD | TBD | ms | |
| $t_{eewr8b64k}$ | Byte-write to FlexRAM execution time (64 KB EEPROM backup) | — | TBD | 1.5 | ms | |
| $t_{eewr8b128k}$ | Byte-write to FlexRAM execution time (128 KB EEPROM backup) | — | TBD | TBD | ms | |
| $t_{eewr8b256k}$ | Byte-write to FlexRAM execution time (256 KB EEPROM backup) | — | TBD | 2.5 | ms | |
| Word-write to FlexRAM for EEPROM operation | | | | | | |
| $t_{eewr16bers}$ | Word-write to erased FlexRAM location execution time | — | 100 | TBD | μ s | |
| $t_{eewr16b32k}$ | Word-write to FlexRAM execution time (32 KB EEPROM backup) | — | TBD | TBD | ms | |
| $t_{eewr16b64k}$ | Word-write to FlexRAM execution time (64 KB EEPROM backup) | — | TBD | 1.5 | ms | |
| $t_{eewr16b128k}$ | Word-write to FlexRAM execution time (128 KB EEPROM backup) | — | TBD | TBD | ms | |
| $t_{eewr16b256k}$ | Word-write to FlexRAM execution time (256 KB EEPROM backup) | — | TBD | 2.5 | ms | |
| Longword-write to FlexRAM for EEPROM operation | | | | | | |

Table continues on the next page...

Table 18. Flash command timing characteristics (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------------|---|------|------|------|---------------|-------|
| $t_{\text{eevr32bers}}$ | Longword-write to erased FlexRAM location execution time | — | 200 | TBD | μs | |
| $t_{\text{eevr16b32k}}$ | Longword-write to FlexRAM execution time (32 KB EEPROM backup) | — | TBD | TBD | ms | |
| $t_{\text{eevr16b64k}}$ | Longword-write to FlexRAM execution time (64 KB EEPROM backup) | — | TBD | 2.7 | ms | |
| $t_{\text{eevr32b128k}}$ | Longword-write to FlexRAM execution time (128 KB EEPROM backup) | — | TBD | TBD | ms | |
| $t_{\text{eevr32b256k}}$ | Longword-write to FlexRAM execution time (256 KB EEPROM backup) | — | TBD | 3.7 | ms | |

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash (FTFL) Current and Power Parameters

Table 19. Flash (FTFL) current and power parameters

| Symbol | Description | Typ. | Unit |
|----------------------|---|------|------|
| $I_{\text{DD_PGM}}$ | Worst case programming current in program flash | 10 | mA |

6.4.1.4 Reliability Characteristics

Table 20. NVM reliability characteristics

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|----------------------------|--|------|-------------------|------|--------|-------|
| Program Flash | | | | | | |
| $t_{\text{nvmpretp10k}}$ | Data retention after up to 10 K cycles | 5 | TBD | — | years | 2 |
| $t_{\text{nvmpretp1k}}$ | Data retention after up to 1 K cycles | 10 | TBD | — | years | 2 |
| $t_{\text{nvmpretp100}}$ | Data retention after up to 100 cycles | 15 | TBD | — | years | 2 |
| n_{nvmcycp} | Cycling endurance | 10 K | TBD | — | cycles | 3 |
| Data Flash | | | | | | |
| $t_{\text{nvmpretd10k}}$ | Data retention after up to 10 K cycles | 5 | TBD | — | years | 2 |
| $t_{\text{nvmpretd1k}}$ | Data retention after up to 1 K cycles | 10 | TBD | — | years | 2 |
| $t_{\text{nvmpretd100}}$ | Data retention after up to 100 cycles | 15 | TBD | — | years | 2 |
| n_{nvmcycd} | Cycling endurance | 10 K | TBD | — | cycles | 3 |
| FlexRAM as EEPROM | | | | | | |
| $t_{\text{nvmpreteee100}}$ | Data retention up to 100% of write endurance | 5 | TBD | — | years | 2 |

Table continues on the next page...

Table 20. NVM reliability characteristics (continued)

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|-------------------------|--|--------|-------------------|------|--------|-------|
| $t_{\text{nmwretee10}}$ | Data retention up to 10% of write endurance | 10 | TBD | — | years | 2 |
| $t_{\text{nmwretee1}}$ | Data retention up to 1% of write endurance | 15 | TBD | — | years | 2 |
| n_{nmwree16} | Write endurance with an EEPROM backup to FlexRAM ratio of 16 | 35 K | TBD | — | writes | 4 |
| $n_{\text{nmwree128}}$ | Write endurance with an EEPROM backup to FlexRAM ratio of 128 | 315 K | TBD | — | writes | 4 |
| $n_{\text{nmwree512}}$ | Write endurance with an EEPROM backup to FlexRAM ratio of 512 | 1.27 M | TBD | — | writes | 4 |
| n_{nmwree4k} | Write endurance with an EEPROM backup to FlexRAM ratio of 4096 | 10 M | TBD | — | writes | 4 |
| $n_{\text{nmwree32k}}$ | Write endurance with an EEPROM backup to FlexRAM ratio of 32,768 | 80 M | TBD | — | writes | 4 |

1. Typical data retention values are based on intrinsic capability of the technology measured at high temperature derated to 25°C. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618.
2. Data retention is based on $T_{\text{javg}} = 55^\circ\text{C}$ (temperature profile over the lifetime of the application).
3. Cycling endurance represents number of program/erase cycles at $-40^\circ\text{C} \leq T_j \leq 125^\circ\text{C}$
4. Write endurance represents the number of writes to FlexRAM at $-40^\circ\text{C} \leq T_j \leq 125^\circ\text{C}$ influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum value assumes all byte-writes to FlexRAM.

6.4.1.5 Write Endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFL to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size are used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes}_{\text{subsystem}} = \frac{\text{EEPROM} - 2 \times \text{EESPLIT} \times \text{EESIZE}}{\text{EESPLIT} \times \text{EESIZE}} \times \text{Write}_{\text{efficiency}} \times n_{\text{nmwcyd}}$$

where

- $\text{Writes}_{\text{subsystem}}$ — minimum writes to FlexRAM for subsystem (each subsystem can have different endurance)

- EEPROM — allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with Program Partition command
- EEESPLIT — FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE — total allocated FlexRAM based on DEPART; entered with Program Partition command
- Write_efficiency —
 - 0.25 for 8-bit writes to FlexRAM
 - 0.50 for 16-bit or 32-bit writes to FlexRAM
- n_{nvmcycd} — data flash cycling endurance

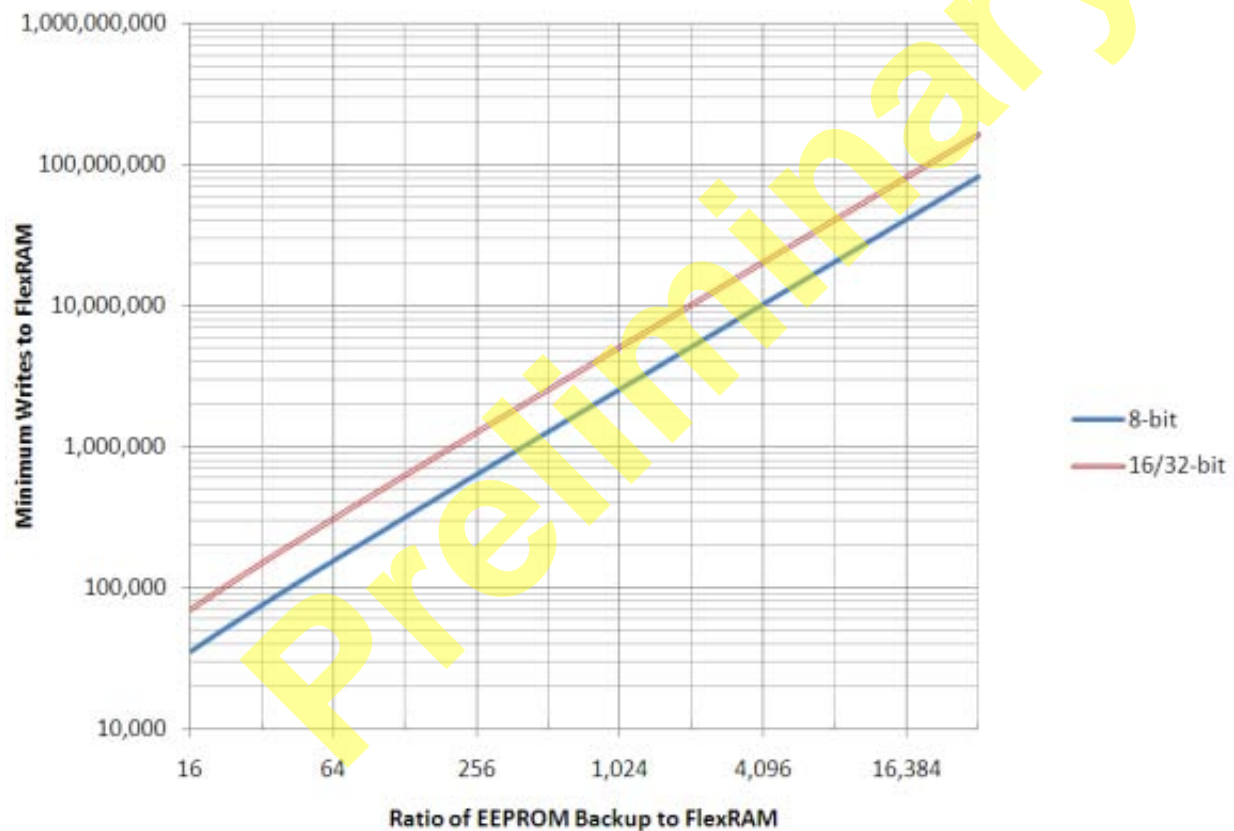


Figure 9. EEPROM backup writes to FlexRAM

6.4.2 EzPort Switching Specifications

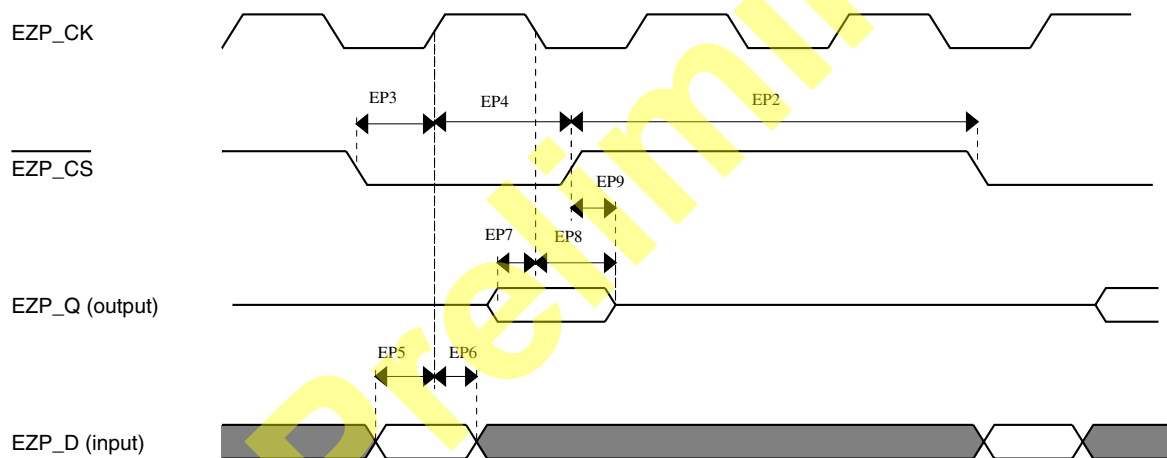
Table 21. EzPort switching specifications

| Num | Description | Min. | Max. | Unit |
|-----|-------------------|------|------|------|
| | Operating voltage | 2.7 | 3.6 | V |

Table continues on the next page...

Table 21. EzPort switching specifications (continued)

| Num | Description | Min. | Max. | Unit |
|------|--|-------------------------------|-------------|------|
| EP1 | EZP_CK frequency of operation (all commands except READ) | — | $f_{SYS}/2$ | MHz |
| EP1a | EZP_CK frequency of operation (READ command) | — | $f_{SYS}/8$ | MHz |
| EP2 | $\overline{\text{EZP_CS}}$ negation to next $\overline{\text{EZP_CS}}$ assertion | $2 \times t_{\text{EZP_CK}}$ | — | ns |
| EP3 | $\overline{\text{EZP_CS}}$ input valid to EZP_CK high (setup) | 5 | — | ns |
| EP4 | EZP_CK high to $\overline{\text{EZP_CS}}$ input invalid (hold) | 5 | — | ns |
| EP5 | EZP_D input valid to EZP_CK high (setup) | 2 | — | ns |
| EP6 | EZP_CK high to EZP_D input invalid (hold) | 5 | — | ns |
| EP7 | EZP_CK low to EZP_Q output valid (setup) | — | 12 | ns |
| EP8 | EZP_CK low to EZP_Q output invalid (hold) | 0 | — | ns |
| EP9 | $\overline{\text{EZP_CS}}$ negation to EZP_Q tri-state | — | 12 | ns |

**Figure 10. EzPort Timing Diagram**

6.4.3 Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 22. Flexbus switching specifications

| Num | Description | Min. | Max. | Unit | Notes |
|-----|---|------|------|------|-------|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | 50 | Mhz | |
| FB1 | Clock period | 20 | — | ns | |
| FB2 | Address, data, and control output valid | TBD | 11.5 | ns | 1 |
| FB3 | Address, data, and control output hold | 0 | — | ns | 1 |
| FB4 | Data and $\overline{\text{FB_TA}}$ input setup | 8.5 | — | ns | 2 |
| FB5 | Data and $\overline{\text{FB_TA}}$ input hold | 0.5 | — | ns | 2 |

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}n}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, $\overline{\text{FB_R/W}}$, $\overline{\text{FB_TBST}}$, $\overline{\text{FB_TSIZ}}[1:0]$, and $\overline{\text{FB_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

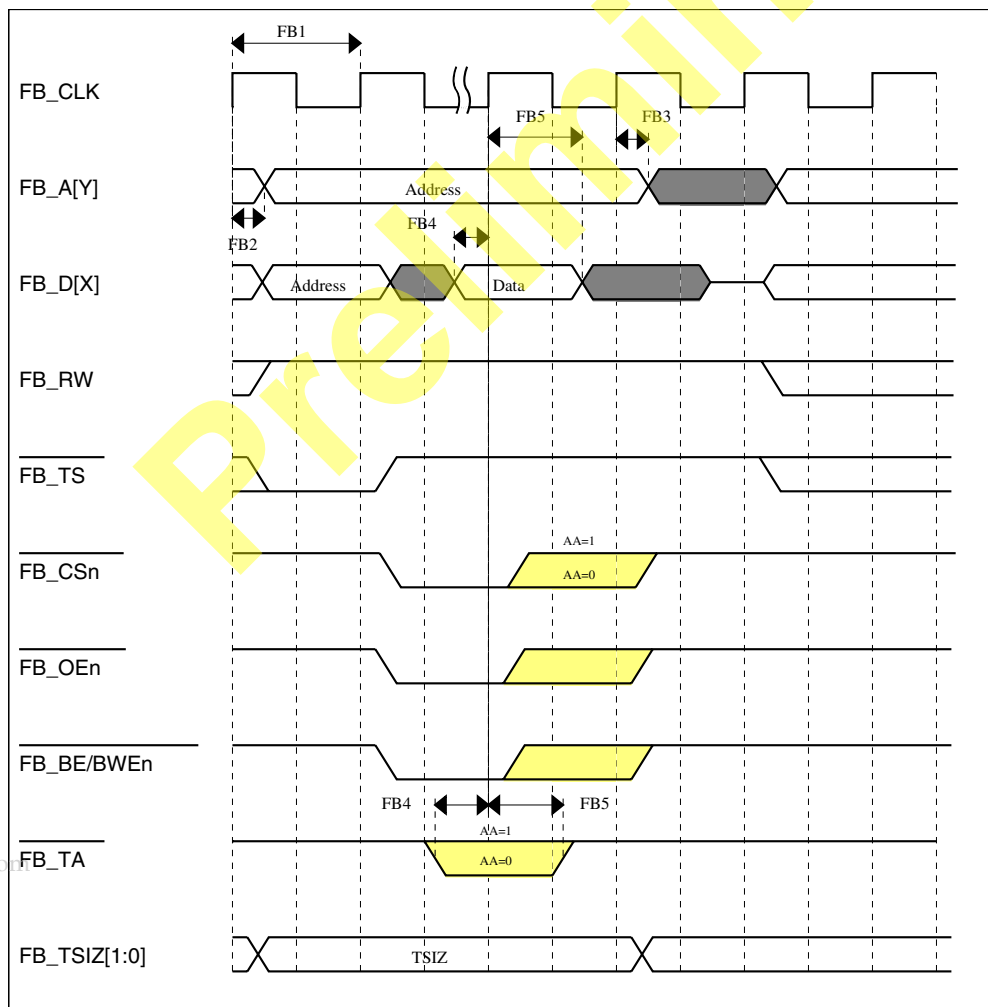


Figure 11. FlexBus read timing diagram

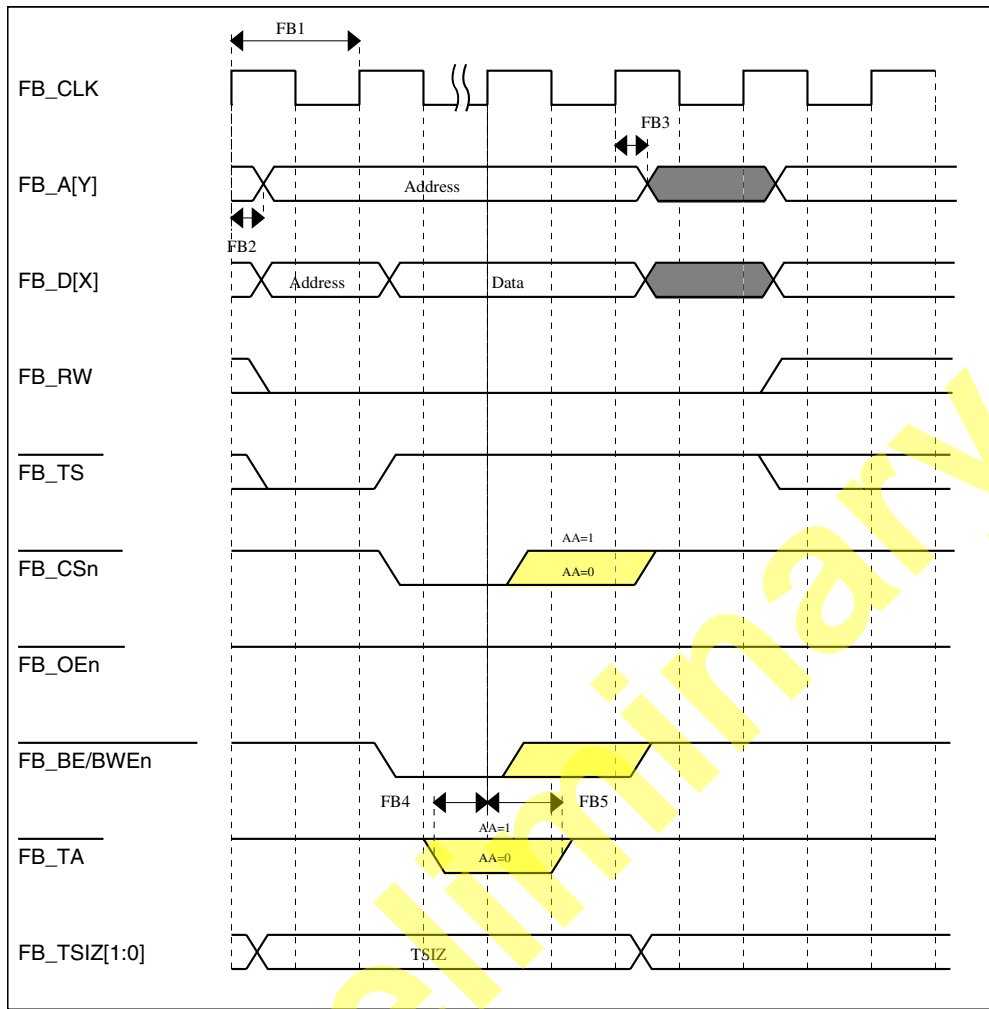


Figure 12. FlexBus write timing diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.6 Analog

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 23](#) and [Table 24](#) are achievable on the differential pins (ADCx_DP0, ADCx_DM0, ADCx_DP1, ADCx_DM1, ADCx_DP3, and ADCx_DM3). The ADCx_DP2 and ADCx_DM2 ADC inputs are used

as the PGA inputs and are not direct device pins. Accuracy specifications for these pins are defined in [Table 25](#) and [Table 26](#). All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

6.6.1.1 16-bit ADC operating conditions

Table 23. 16-bit ADC operating conditions

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|------------------|----------------------------|---|------------|-------------------|------------|------------|-------|
| V_{DDA} | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| ΔV_{DDA} | Supply voltage | Delta to V_{DD} ($V_{DD} - V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| ΔV_{SSA} | Ground voltage | Delta to V_{SS} ($V_{SS} - V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| V_{REFH} | ADC reference voltage high | | 1.13 | V_{DDA} | V_{DDA} | V | |
| V_{REFL} | Reference voltage low | | V_{SSA} | V_{SSA} | V_{SSA} | V | |
| V_{ADIN} | Input voltage | | V_{REFL} | — | V_{REFH} | V | |
| C_{ADIN} | Input capacitance | <ul style="list-style-type: none"> 16 bit modes 8/10/12 bit modes | — | 8 4 | 10 5 | pF | |
| R_{ADIN} | Input resistance | | — | 2 | 5 | k Ω | |

Table continues on the next page...

Table 23. 16-bit ADC operating conditions (continued)

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes | |
|----------------------------|--------------------------------|------------------------------|------|-------------------|------|------|--|--|
| R _{AS} | Analog source resistance | 16 bit modes | | | | | External to MCU Assumes ADLSMP=0 | |
| | | • f _{ADCK} > 8MHz | — | — | 0.5 | kΩ | | |
| | | • f _{ADCK} = 4–8MHz | — | — | 1 | kΩ | | |
| | | • f _{ADCK} < 4MHz | — | — | 2 | kΩ | | |
| | | 13/12 bit modes | | | | | | |
| | | • f _{ADCK} > 16MHz | — | — | 0.5 | kΩ | | |
| | | • f _{ADCK} > 8MHz | — | — | 1 | kΩ | | |
| | | • f _{ADCK} = 4–8MHz | — | — | 2 | kΩ | | |
| | | • f _{ADCK} < 4MHz | — | — | 5 | kΩ | | |
| | | 11/10 bit modes | | | | | | |
| | | • f _{ADCK} > 8MHz | — | — | 2 | kΩ | | |
| | | • f _{ADCK} = 4–8MHz | — | — | 5 | kΩ | | |
| | | • f _{ADCK} < 4MHz | — | — | 10 | kΩ | | |
| 9/8 bit modes | | | | | | | | |
| • f _{ADCK} > 8MHz | — | — | 5 | kΩ | | | | |
| • f _{ADCK} < 8MHz | — | — | 10 | kΩ | | | | |
| f _{ADCK} | ADC conversion clock frequency | ADLPC=0, ADHSC=1 | | | | | | |
| | | • 16 bit modes | 1.0 | — | TBD | MHz | | |
| | | • ≤13 bit modes | 1.0 | — | TBD | MHz | | |
| | | ADLPC=0, ADHSC=0 | | | | | | |
| | | • 16 bit modes | 1.0 | — | 8.0 | MHz | | |
| | | • ≤13 bit modes | 1.0 | — | 12.0 | MHz | | |
| | | ADLPC=1, ADHSC=1 | | | | | | |
| | | • 16 bit modes | 1.0 | — | 5.0 | MHz | | |
| | | • ≤13 bit modes | 1.0 | — | 8.0 | MHz | | |
| | | ADLPC=1, ADHSC=0 | | | | | | |
| | | • 16 bit modes | 1.0 | — | 2.5 | MHz | | |
| | | • ≤13 bit modes | 1.0 | — | 5.0 | MHz | | |

www.DataSheet4U.com

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

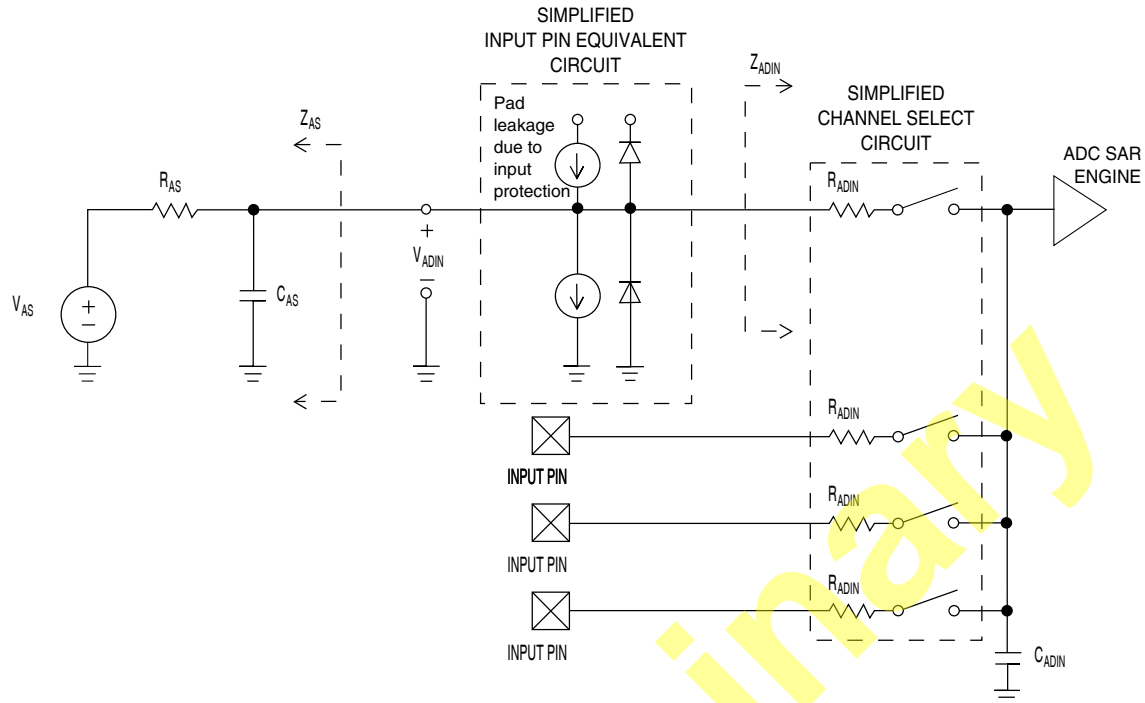


Figure 13. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics

Table 24. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|-------------|-------------------------------|--|------|-------------------|------|---------------|---------------------------|
| I_{DDA} | Supply current | <ul style="list-style-type: none"> ADLPC=1, ADHSC=0 ADLPC=1, ADHSC=1 ADLPC=0, ADHSC=0 ADLPC=0, ADHSC=1 | — | 215 | — | μA | ADLSMP=0 ADCO=1 |
| | Supply current | • Stop, reset, module off | — | 0.01 | 0.8 | μA | |
| f_{ADACK} | ADC asynchronous clock source | • ADLPC=1, ADHSC=0 | TBD | 2.4 | TBD | MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | | • ADLPC=1, ADHSC=1 | TBD | 4.0 | TBD | MHz | |
| | | • ADLPC=0, ADHSC=0 | TBD | 5.2 | TBD | MHz | |
| | | • ADLPC=0, ADHSC=1 | TBD | 6.2 | TBD | MHz | |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| | Conversion Time | See Reference Manual chapter for conversion times | | | | | |

Table continues on the next page...

Table 24. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|--------|----------------------------|--|------|-------------------|------|------------------|--|
| TUE | Total unadjusted error | <ul style="list-style-type: none"> 16 bit differential 16 bit single-ended 13 bit differential 12 bit single-ended 11 bit differential 10 bit single-ended 9 bit differential 8 bit single-ended | — | ±14.0 | ±TBD | LSB ³ | Max hardware averaging (AVGE = %1, AVGS = %11) |
| DNL | Differential non-linearity | <ul style="list-style-type: none"> 16 bit differential 16 bit single-ended 13 bit differential 12 bit single-ended 11 bit differential 10 bit single-ended 9 bit differential 8 bit single-ended | — | ±2.5 | ±TBD | LSB ³ | Max hardware averaging (AVGE = %1, AVGS = %11) |
| INL | Integral non-linearity | <ul style="list-style-type: none"> 16 bit differential 16 bit single-ended 13 bit differential 12 bit single-ended 11 bit differential 10 bit single-ended 9 bit differential 8 bit single-ended | — | -6 to +2.5 | — | LSB ³ | Max averaging |
| Ezs | Zero-scale error | <ul style="list-style-type: none"> 16 bit differential 16 bit single-ended 13 bit differential 12 bit single-ended 11 bit differential 10 bit single-ended 9 bit differential 8 bit single-ended | — | ±4.0 | — | LSB ³ | $V_{ADIN} = V_{SSA}$ |

Table continues on the next page...

Table 24. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|----------|---------------------------------|---|--------------------|-------------------|------|------------------|----------------------|
| E_{FS} | Full-scale error | <ul style="list-style-type: none"> 16 bit differential 16 bit single-ended 13 bit differential 12 bit single-ended 11 bit differential 10 bit single-ended 9 bit differential 8 bit single-ended | — | 0 to +10 | — | LSB ³ | $V_{ADIN} = V_{DDA}$ |
| E_Q | Quantization error | <ul style="list-style-type: none"> 16 bit modes ≤13 bit modes | — | -1 to 0 | — | LSB ³ | |
| ENOB | Effective number of bits | 16 bit differential mode <ul style="list-style-type: none"> Avg=32 Avg=16 Avg=8 Avg=4 Avg=1 16 bit single-ended mode <ul style="list-style-type: none"> Avg=32 Avg=16 Avg=8 Avg=4 Avg=1 | TBD | 13.6 | TBD | bits | 4 |
| SINAD | Signal-to-noise plus distortion | See ENOB | 6.02 × ENOB + 1.76 | | | dB | |
| THD | Total harmonic distortion | 16 bit differential mode <ul style="list-style-type: none"> Avg=32 16 bit single-ended mode <ul style="list-style-type: none"> Avg=32 | — | -94 | TBD | dB | 4 |
| SFDR | Spurious free dynamic range | 16 bit differential mode <ul style="list-style-type: none"> Avg=32 16 bit single-ended mode <ul style="list-style-type: none"> Avg=32 | TBD | 95 | — | dB | 4 |

Table continues on the next page...

Table 24. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|--------------|---------------------|--|------------------------|-------------------|------|-------|--|
| E_{IL} | Input leakage error | | $I_{in} \times R_{AS}$ | | | mV | I_{in} = leakage current (refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | <ul style="list-style-type: none"> -40°C to 25°C 25°C to 105°C | — | TBD | — | mV/°C | |
| V_{TEMP25} | Temp sensor voltage | 25°C | — | TBD | — | mV | |

- All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
- Typical values assume $V_{DDA} = 3.0$ V, Temp = 25°C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
- Input data is 1 kHz sine wave.

6.6.1.3 16-bit ADC with PGA operating conditions

Table 25. 16-bit ADC with PGA operating conditions

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|--------------|------------------------------|---|-------------------|-------------------|-------------------|------|------------|
| V_{DDA} | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| V_{REFPGA} | PGA ref voltage | | VREFOUT | VREFOUT | VREFOUT | V | 2, 3 |
| V_{ADIN} | Input voltage | | V_{SSA} | — | V_{DDA} | V | |
| R_{PGA} | Input impedance | Gain = 1, 2, 4, 8 Gain = 16, 32 Gain = 64 | TBD TBD TBD | 64 32 16 | TBD TBD TBD | kΩ | |
| R_{PGAD} | Differential input impedance | Gain = 1, 2, 4, 8 Gain = 16, 32 Gain = 64 | TBD TBD TBD | 128 64 32 | TBD TBD TBD | kΩ | IN+ to IN- |
| R_{AS} | Analog source resistance | Gain = 16, 32 | — | 100 | — | Ω | 4 |
| T_S | ADC sampling time | Gain = 64 | 1.25 | — | — | μs | 5 |

- Typical values assume $V_{DDA} = 3.0$ V, Temp = 25°C, $f_{ADCK} = 6$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- ADC must be configured to use the internal voltage reference (VREFOUT)
- PGA reference connected to the VREFOUT pin. If the user wishes to drive VREFOUT with a voltage other than the output of the VREF module, the VREF module must be disabled.

- The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
- The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of $1.25\mu\text{s}$ time should be allowed for $F_{in}=4\text{ kHz}$ at 16-bit differential mode. Recommended ADC setting is: $ADLSMP=1$, $ADLSTS=2$ at 8 MHz ADC clock. The $ADLSTS$ bits can be adjusted for different ADC clock frequency

6.6.1.4 16-bit ADC with PGA characteristics

Table 26. 16-bit ADC with PGA characteristics

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|-----------------|--------------------------------|--|------|-------------------|-----------|-------------------------|---|
| I_{DDA_PGA} | Supply current | | TBD | 590 | TBD | μA | |
| I_{LKG} | Leakage current | PGA disabled | — | < 1 | TBD | μA | |
| G | Gain ² | <ul style="list-style-type: none"> PGAG=0 PGAG=1 PGAG=2 PGAG=3 PGAG=4 PGAG=5 PGAG=6 | TBD | 1 | TBD | dB | $R_{AS} < 100\Omega$ |
| | | | TBD | 2 | TBD | dB | |
| | | | TBD | 3.9 | TBD | dB | |
| | | | TBD | TBD | TBD | dB | |
| | | | TBD | TBD | TBD | dB | |
| | | | TBD | 29.9 | TBD | dB | |
| | | | TBD | TBD | TBD | dB | |
| G_A | Gain error | | — | — | ± 0.5 | dB | $R_{AS} < 100\Omega$ |
| BW | Input signal bandwidth | <ul style="list-style-type: none"> 16-bit modes < 16-bit modes | — | — | 4 | kHz | |
| | | | — | — | 40 | kHz | |
| PSRR | Power supply rejection ration | Gain=1 | TBD | TBD | — | dB | $V_{DDA}=3\text{V}$ $\pm 100\text{mV}$, $f_{VDDA}=50\text{Hz}$, 60Hz |
| CMRR | Common mode rejection ratio | <ul style="list-style-type: none"> Gain=1 Gain=64 | TBD | TBD | — | dB | $V_{CM}=500\text{mVpp}$, $f_{VCM}=50\text{Hz}$, 100Hz |
| | | | TBD | TBD | — | dB | |
| V_{OFS} | Input offset voltage | | — | 0.2 | TBD | mV | Gain=1, ADC Averaging=32 |
| T_{GSW} | Gain switching settling time | | — | TBD | 10 | μs | 3 |
| dG/dT | Gain drift over temperature | <ul style="list-style-type: none"> Gain=1 Gain=64 | — | TBD | TBD | ppm/ $^{\circ}\text{C}$ | 0 to 50°C |
| | | | — | TBD | TBD | ppm/ $^{\circ}\text{C}$ | |
| d V_{OFS} /dT | Offset drift over temperature | Gain=1 | — | TBD | TBD | ppm/ $^{\circ}\text{C}$ | 0 to 50°C , ADC Averaging=32 |
| dG/d V_{DDA} | Gain drift over supply voltage | <ul style="list-style-type: none"> Gain=1 Gain=64 | — | TBD | TBD | %/V | V_{DDA} from 1.71 to 3.6V |
| | | | — | TBD | TBD | %/V | |

Table continues on the next page...

Table 26. 16-bit ADC with PGA characteristics (continued)

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|---------------|---|--|---|-------------------|------|------|--|
| E_{IL} | Input leakage error | All modes | $I_{in} \times R_{AS}$ | | | mV | I_{in} = leakage current (refer to the MCU's voltage and current operating ratings) |
| $V_{PP,DIFF}$ | Maximum differential input signal swing | | $[(V_{REFPGA} \times 2.33) - 0.2] / (2 \times \text{Gain})$ | | | V | 4 |
| SNR | Signal-to-noise ratio | <ul style="list-style-type: none"> Gain=1 Gain=64 | TBD | 8.3 | — | dB | Average=32 |
| | | | TBD | 57.7 | — | dB | |
| THD | Total harmonic distortion | <ul style="list-style-type: none"> Gain=1 Gain=64 | TBD | 87.3 | — | dB | Average=32, $f_{in}=100\text{Hz}$ |
| | | | TBD | 85.3 | — | dB | |
| SFDR | Spurious free dynamic range | <ul style="list-style-type: none"> Gain=1 Gain=64 | TBD | 92.42 | — | dB | Average=32, $f_{in}=100\text{Hz}$ |
| | | | TBD | 92.54 | — | dB | |
| ENOB | Effective number of bits | <ul style="list-style-type: none"> Gain=1, Average=4 | TBD | 12.3 | — | bits | |
| | | <ul style="list-style-type: none"> Gain=1, Average=8 | TBD | 12.7 | — | bits | |
| | | <ul style="list-style-type: none"> Gain=64, Average=4 | TBD | 8.4 | — | bits | |
| | | <ul style="list-style-type: none"> Gain=64, Average=8 | TBD | 8.7 | — | bits | |
| | | <ul style="list-style-type: none"> Gain=1, Average=32 | TBD | 13.4 | — | bits | |
| | | <ul style="list-style-type: none"> Gain=2, Average=32 | TBD | 13.1 | — | bits | |
| | | <ul style="list-style-type: none"> Gain=4, Average=32 | TBD | 12.6 | — | bits | |
| | | <ul style="list-style-type: none"> Gain=8, Average=32 | TBD | 11.8 | — | bits | |
| | | <ul style="list-style-type: none"> Gain=16, Average=32 | TBD | 11.1 | — | bits | |
| | | <ul style="list-style-type: none"> Gain=32, Average=32 Gain=64, Average=32 | TBD | 10.2 | — | bits | |
| SINAD | Signal-to-noise plus distortion ratio | See ENOB | $6.02 \times \text{ENOB} + 1.76$ | | | dB | |

1. Typical values assume $V_{DDA} = 3.0\text{V}$, $\text{Temp} = 25^\circ\text{C}$, $f_{ADCK} = 6\text{MHz}$ unless otherwise stated.
2. $\text{Gain} = 2^{\text{PGAGx}}$
3. When the PGA gain is changed, it takes some time to settle the output for the ADC to work properly. During a gain switching, a few ADC outputs should be discarded (minimum two data samples, may be more depending on ADC sampling rate and time of the switching).
4. Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

6.6.2 CMP and 6-bit DAC electrical specifications

Table 27. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------------------|---|-----------------------|---------------------|-----------------|----------------------|
| V _{DD} | Supply voltage | 1.71 | — | 3.6 | V |
| I _{DDHS} | Supply current, High-speed mode (EN=1, PMODE=1, VDDA >= V _{LVI_trip}) | — | — | 200 | μA |
| I _{DDL} | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | μA |
| I _{DDOFF} | Supply current, OFF Mode (EN=0,) | — | — | 100 | nA |
| V _{AIN} | Analog input voltage | V _{SS} – 0.3 | — | V _{DD} | V |
| V _{AIO} | Analog input offset voltage | — | — | 20 | mV |
| V _H | Analog comparator hysteresis <ul style="list-style-type: none"> • HYSTCTR = 00 • HYSTCTR = 01 • HYSTCTR = 10 • HYSTCTR = 11 | — | 5 10 20 30 | — | mV mV mV mV |
| V _{CMPOH} | Output high | V _{DD} – 0.5 | — | — | V |
| V _{CMPOI} | Output low | — | — | 0.5 | V |
| t _{DHS} | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 120 | ns |
| t _{DLS} | Propagation delay, low-speed mode (EN=1, PMODE=1) | 120 | 250 | 420 | ns |
| | Analog comparator initialization delay | — | — | TBD | ns |
| I _{DAC6b} | 6-bit DAC current adder (enabled) | — | — | 8 | μA |
| INL | 6-bit DAC integral non-Linearity | –0.5 | — | 0.5 | LSB ¹ |
| DNL | 6-bit DAC differential non-linearity | –0.3 | — | 0.3 | LSB |

1. 1 LSB = V_{reference}/64

6.6.3 12-bit DAC electrical characteristics

6.6.3.1 12-bit DAC operating requirements

Table 28. 12-bit DAC operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|-------------------|-------------------|------|------|------|-------|
| V _{DDA} | Supply voltage | 1.71 | 3.6 | V | |
| V _{DACR} | Reference voltage | 1.15 | 3.6 | V | 1 |
| T _A | Temperature | –40 | 105 | °C | |

Table continues on the next page...

Table 28. 12-bit DAC operating requirements (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------------------|------|------|------|-------|
| C_L | Output load capacitance | — | 100 | pF | 2 |
| I_L | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be VDDA or the voltage output of the VREF module (VREFO)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

6.6.3.2 12-bit DAC operating behaviors

Table 29. 12-bit DAC operating behaviors

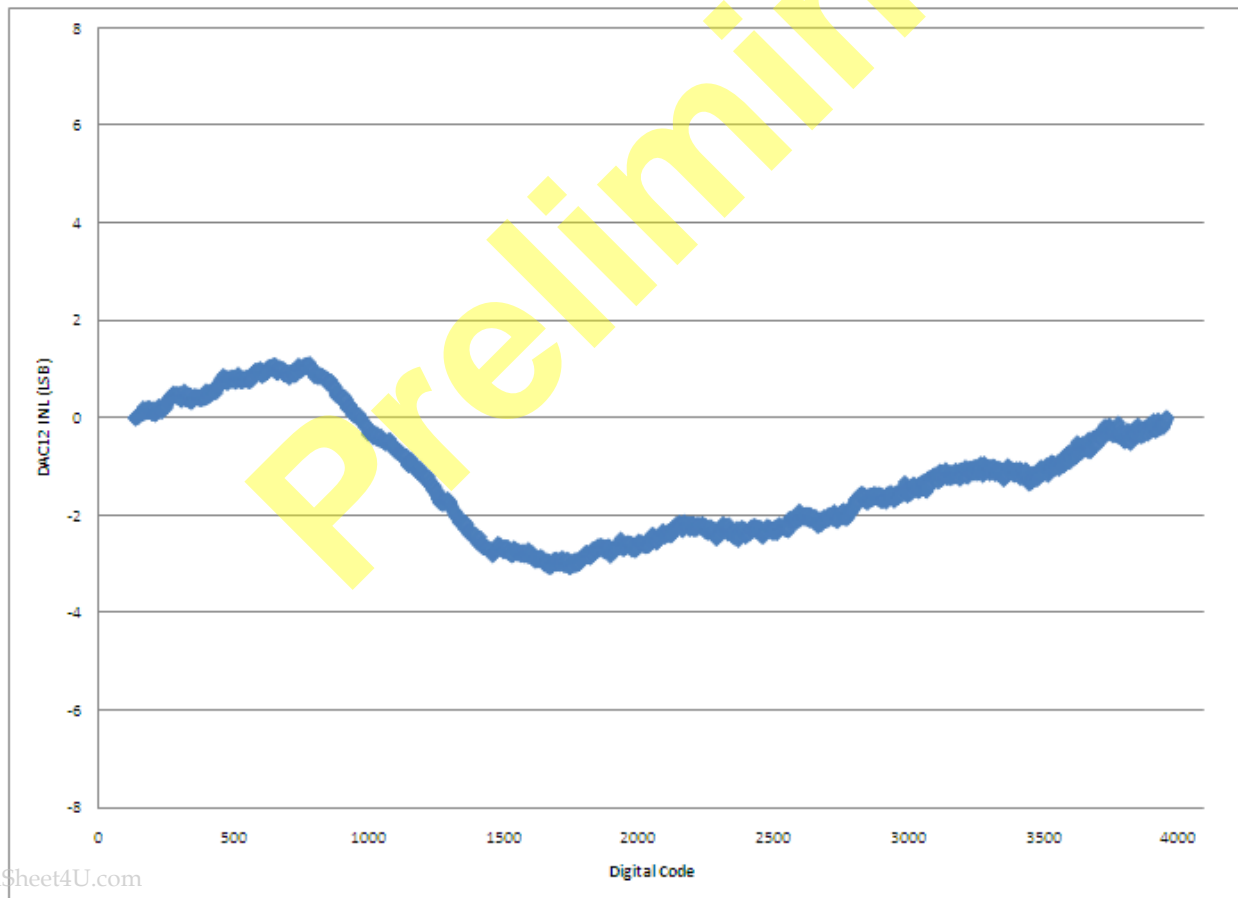
| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|--|--------------------|------|------------|--------------|-------|
| n | Resolution | 12 | — | 12 | b | |
| I_{DDA_DACLP} | Supply current — low-power mode | — | — | 150 | μ A | |
| I_{DDA_DACHP} | Supply current — high-speed mode | — | — | 700 | μ A | |
| t_{DACLP} | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | μ s | 1 |
| t_{DACHP} | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | μ s | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode | — | — | 5 | μ s | 1 |
| $t_{CCDACHP}$ | Code-to-code settling time (0xBF8 to 0xC08) — high-speed mode | 1 | TBD | — | μ s | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | 0 | 100 | — | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF | V_{DACR} -100 | — | V_{DACR} | mV | |
| INL | Integral non-linearity error — high speed mode | ± 3 | — | ± 8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR} > 2$ V | ± 0.5 | — | ± 1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR} = VREFO$ (1.15 V) | ± 0.5 | — | ± 1 | LSB | 4 |
| V_{OFFSET} | Offset error | ± 0.4 | — | ± 0.8 | %FSR | 5 |
| E_G | Gain error | ± 0.1 | — | ± 0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA} \geq 2.4$ V | 60 | — | 90 | dB | |
| T_{CO} | Temperature coefficient offset voltage | — | TBD | — | μ V/C | |
| T_{GE} | Temperature coefficient gain error | — | TBD | — | ppm of FSR/C | |
| A_C | Offset aging coefficient | — | — | TBD | μ V/yr | |
| R_{op} | Output resistance load = 3 k Ω | — | — | 250 | Ω | |

Table continues on the next page...

Table 29. 12-bit DAC operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|---|-------------|-------------|--------|------|-------|
| SR | Slew rate -80h→ F7Fh→ 80h <ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) | 1.2 0.05 | 1.7 0.12 | — — | V/μs | |
| CT | Channel to channel cross talk | — | — | -80 | dB | |
| BW | 3dB bandwidth <ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) | 550 40 | — — | — — | kHz | |

1. Settling within ± 1 LSB
2. The INL is measured for 0+100mV to VD_{ACR}-100 mV
3. The DNL is measured for 0+100 mV to V_{D_{ACR}}-100 mV
4. The DNL is measured for 0+100mV to V_{D_{ACR}}-100 mV with V_{D_{DDA}} > 2.4V
5. Calculated by a best fit curve from V_{SS}+100 mV to V_{REF}-100 mV

**Figure 14. Typical INL error vs. digital code**

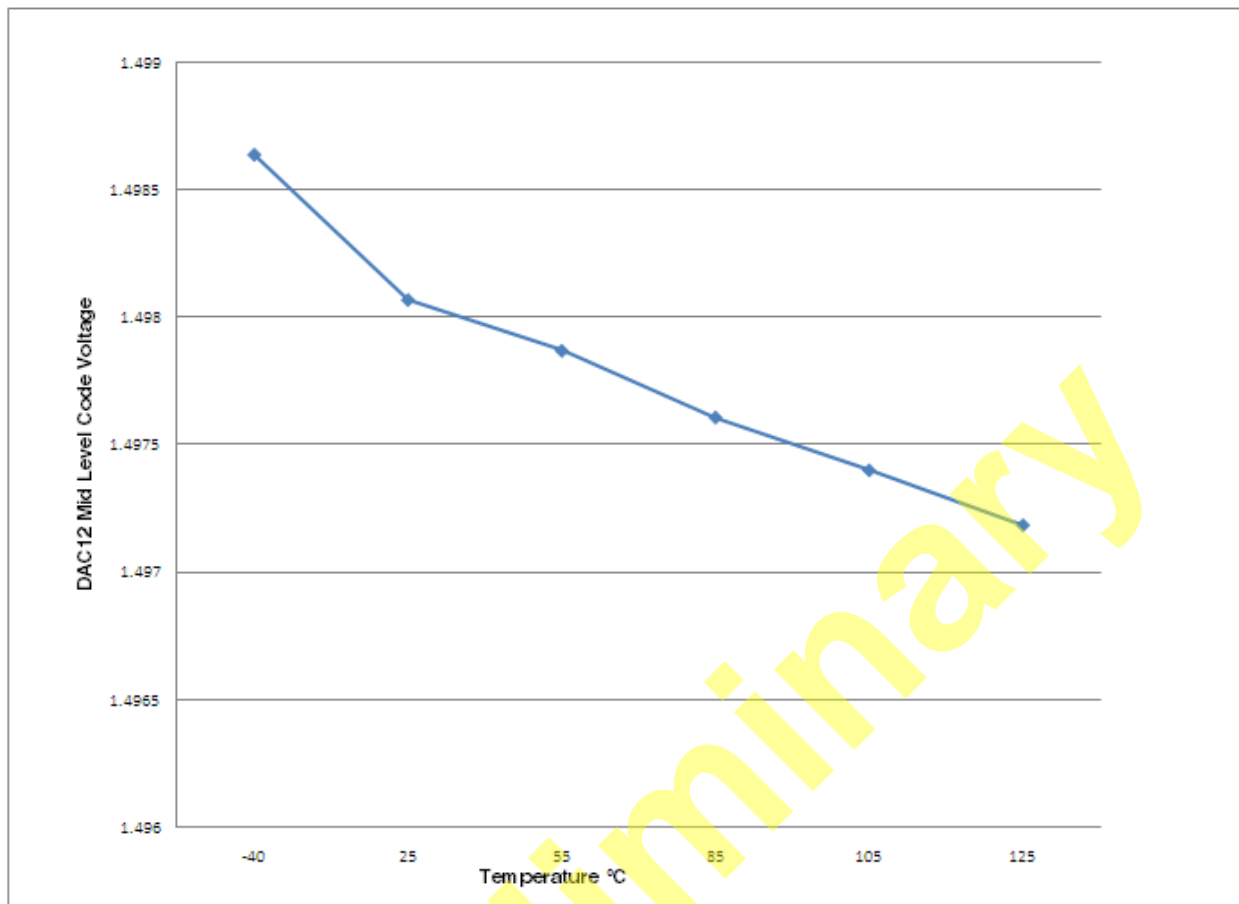


Figure 15. Offset at half scale vs. temperature

6.6.4 Voltage Reference Electrical Specifications

Table 30. VREF full-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|-------------------------|------|------|------|-------|
| V_{DDA} | Supply voltage | 1.71 | 3.6 | V | |
| T_A | Temperature | -40 | 105 | °C | |
| C_L | Output load capacitance | — | 100 | nF | |

Table 31. VREF full-range operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------|--|------|------|------|------|---------------|
| V_{out} | Voltage reference output with factory trim | TBD | 1.2 | TBD | V | |
| V_{out} | Voltage reference output without factory trim | 1.15 | — | 1.24 | V | |
| V_{drift} | Temperature drift ($V_{max} - V_{min}$ across the full temperature range) | — | — | 7 | mV | See Figure 16 |

Table continues on the next page...

Table 31. VREF full-range operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------|---|------|------|------|----------|-------|
| T_c | Temperature coefficient | — | — | TBD | ppm/°C | |
| A_c | Aging coefficient | — | — | TBD | ppm/year | |
| I_{off} | Powered down current (off mode, VREFEN = 0, VRSTEN = 0) | — | — | 0.10 | μA | |
| I_{bg} | Bandgap only (MODE_LV = 00) current | — | TBD | 75 | μA | |
| I_{tr} | Tight-regulation buffer (MODE_LV = 10) current | — | — | 1.1 | mA | |
| | Load regulation (MODE_LV = 10) current | — | — | 100 | μV/mA | |
| T_{stup} | Buffer startup time | 100 | — | TBD | μs | |
| DC | Line regulation (power supply rejection) | — | — | TBD | mV | |
| | | -60 | — | TBD | dB | |

Table 32. VREF limited-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| T_A | Temperature | 0 | 50 | °C | |

Table 33. VREF limited-range operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|--|------|------|------|-------|
| V_{out} | Voltage reference output with factory trim | TBD | TBD | μA | |

TBD

Figure 16. Typical output vs. temperature

TBD

Figure 17. Typical output vs. VDD

6.7 Timers

See [General Switching Specifications](#).

6.8 Communication interfaces

6.8.1 Ethernet Switching Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.8.1.1 MII Signal Switching Specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 34. Ethernet MII mode signal timing

| Symbol | Description | Min. | Max. | Unit |
|--------|---------------------------------------|------|------|--------------|
| — | RXCLK frequency | — | 25 | MHz |
| MII1 | RXCLK pulse width high | 35% | 65% | RXCLK period |
| MII2 | RXCLK pulse width low | 35% | 65% | RXCLK period |
| MII3 | RXD[3:0], RXDV, RXER to RXCLK setup | 5 | — | ns |
| MII4 | RXCLK to RXD[3:0], RXDV, RXER hold | 5 | — | ns |
| — | TXCLK frequency | — | 25 | MHz |
| MII5 | TXCLK pulse width high | 35% | 65% | TXCLK period |
| MII6 | TXCLK pulse width low | 35% | 65% | TXCLK period |
| MII7 | TXCLK to TXD[3:0], TXEN, TXER invalid | 2 | — | ns |
| MII8 | TXCLK to TXD[3:0], TXEN, TXER valid | — | 25 | ns |

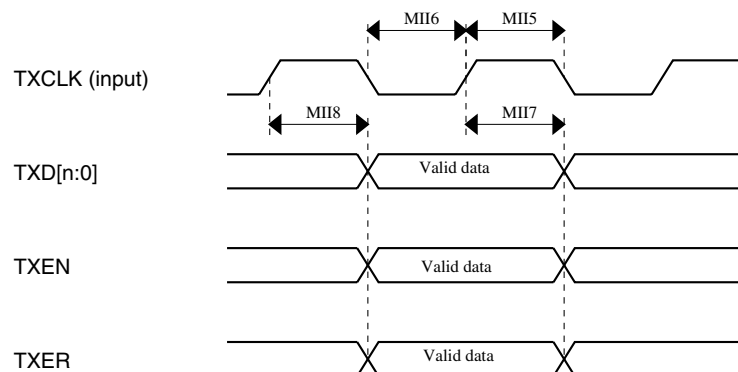


Figure 18. MII transmit signal timing diagram

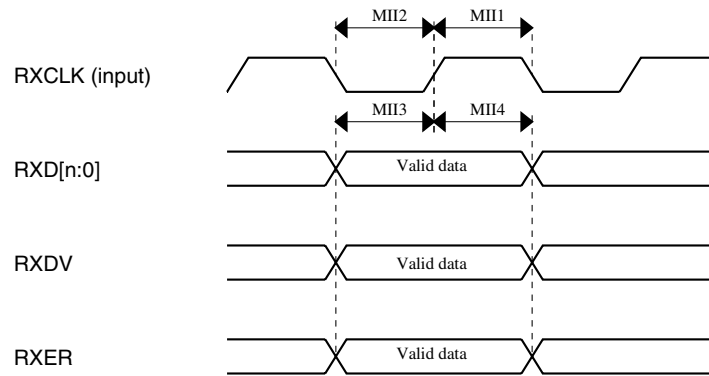


Figure 19. MII receive signal timing diagram

6.8.1.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 35. Ethernet RMII mode signal timing

| Num | Description | Min. | Max. | Unit |
|-------|---|------|------|-----------------|
| — | EXTAL frequency (RMII input clock RMII_CLK) | — | 50 | MHz |
| RMII1 | RMII_CLK pulse width high | 35% | 65% | RMII_CLK period |
| RMII2 | RMII_CLK pulse width low | 35% | 65% | RMII_CLK period |
| RMII3 | RXD[1:0], CRS_DV, RXER to RMII_CLK setup | 4 | — | ns |
| RMII4 | RMII_CLK to RXD[1:0], CRS_DV, RXER hold | 2 | — | ns |
| RMII7 | RMII_CLK to TXD[1:0], TXEN invalid | 4 | — | ns |
| RMII8 | RMII_CLK to TXD[1:0], TXEN valid | — | 15 | ns |

6.8.2 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit <http://www.usb.org>.

www.DataSheet4U.com

6.8.3 USB DCD Electrical Specifications

Table 36. USB DCD specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|----------------------|--|-------|------|------|------------|
| V _{DP_SRC} | USB_DP source voltage (up to 250 μ A) | TBD | TBD | TBD | V |
| V _{LGC} | Threshold voltage for logic high | 0.8 | — | 2.0 | V |
| I _{DP_SRC} | USB_DP source current | 7 | 10 | 13 | μ A |
| I _{DM_SINK} | USB_DM sink current | 50 | 100 | 150 | μ A |
| R _{DM_DWN} | D- pulldown resistance for data pin contact detect | 14.25 | — | 24.8 | k Ω |
| V _{DAT_REF} | Data detect voltage | 0.25 | TBD | 0.4 | V |

6.8.4 USB Voltage Regulator Electrical Specifications

Table 37. USB voltage regulator electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|---|-----------------|-----------------|-------------------|-------------|-------|
| V _{REGIN} | Input supply voltage | 2.7 | — | 5.5 | V | |
| I _{DDon} | Quiescent current — Run mode, load current equal zero | — | 120 | — | μ A | |
| I _{DDstby} | Quiescent current — Standby mode, load current equal zero | — | TBD | — | μ A | |
| I _{DDoff} | Quiescent current — Shutdown mode | — | — | 500 | nA | |
| I _{LOADrun} | Maximum load current — Run mode | — | — | 120 | mA | |
| I _{LOADstby} | Maximum load current — Standby mode | — | — | TBD | mA | |
| V _{Reg33out} | Regulator output voltage — Input supply (V _{REGIN}) > 3.6 V <ul style="list-style-type: none"> • Run mode • Standby mode • Pass-through mode | 3 TBD 2.3 | 3.3 TBD — | 3.6 TBD 3.6 | V V V | 1 |
| C _{OUT} | External output capacitor | 1.76 | 2.2 | 8.16 | μ F | |
| ESR | External output capacitor equivalent series resistance | 1 | — | 100 | m Ω | |
| I _{LIM} | Current limitation threshold | 185 | 290 | 395 | mA | |

1. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

6.8.5 DSPI Switching Specifications for Low-speed Operation

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 38. Master Mode DSPI Timing (Low-speed mode)

| Num | Description | Min. | Max. | Unit | Notes |
|-----|--|---------------------|-------------------|------|-------|
| | Operating voltage | 1.71 | 3.6 | V | 1 |
| | Frequency of operation | — | 12.5 | MHz | |
| DS1 | DSPI_SCK output cycle time | $4 \times t_{BCLK}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 4$ | $(t_{SCK}/2) + 4$ | ns | |
| DS3 | DSPI_PCS _n to DSPI_SCK output valid | $(t_{SCK}/2) - 4$ | — | ns | |
| DS4 | DSPI_SCK to DSPI_PCS _n output hold | $(t_{SCK}/2) - 4$ | — | ns | |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 10 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -2 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 15 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

- The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.

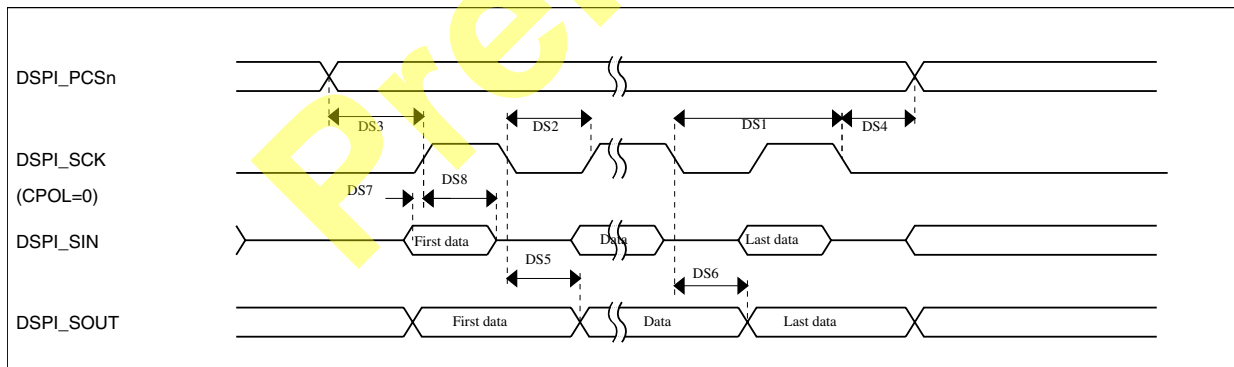


Figure 20. DSPI Classic SPI Timing — Master Mode

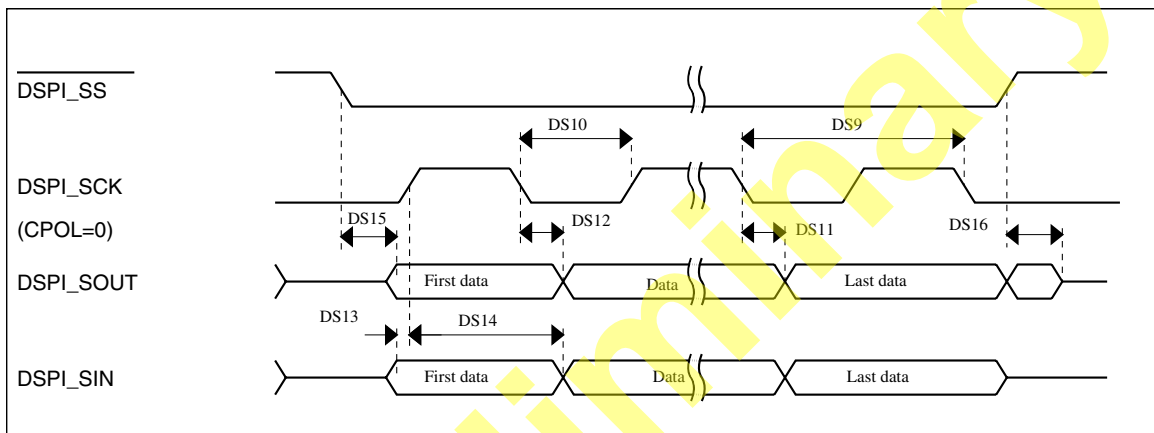
Table 39. Slave Mode DSPI Timing (Low-speed Mode)

| Num | Description | Min. | Max. | Unit |
|-----|---------------------------|---------------------|------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| | Frequency of operation | — | 6.25 | MHz |
| DS9 | DSPI_SCK input cycle time | $8 \times t_{BCLK}$ | — | ns |

Table continues on the next page...

Table 39. Slave Mode DSPI Timing (Low-speed Mode) (continued)

| Num | Description | Min. | Max. | Unit |
|------|---|-------------------|-------------------|------|
| DS10 | DSPI_SCK input high/low time | $(t_{SCK/2}) - 4$ | $(t_{SCK/2}) + 4$ | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 20 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 5 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 15 | — | ns |
| DS15 | $\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven | — | 15 | ns |
| DS16 | $\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven | — | 15 | ns |

**Figure 21. DSPI Classic SPI Timing — Slave Mode**

6.8.6 DSPI Switching Specifications (High-speed mode)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

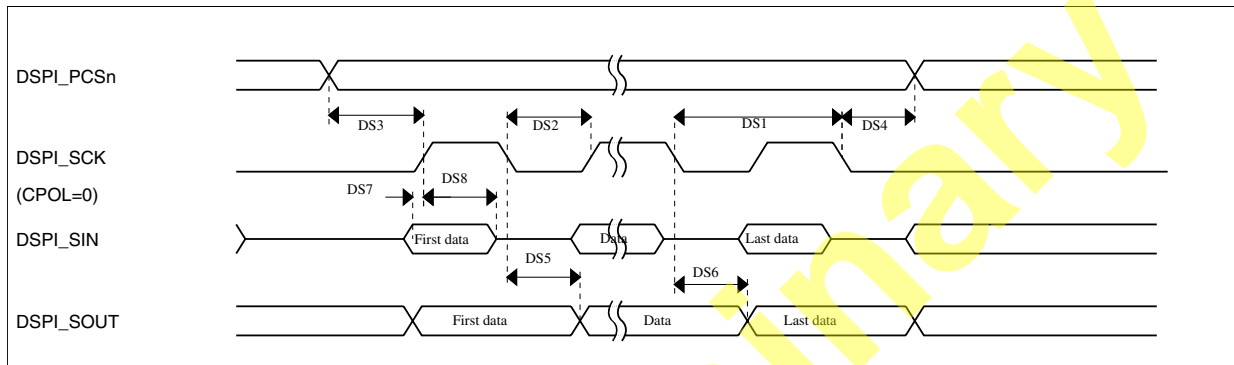
Table 40. Master Mode DSPI Timing (High-speed mode)

| Num | Description | Min. | Max. | Unit |
|-----|--|---------------------|-------------------|------|
| | Operating voltage | 2.7 | 3.6 | V |
| | Frequency of operation | — | 25 | MHz |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{BCLK}$ | — | ns |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK/2}) - 2$ | $(t_{SCK/2}) + 2$ | ns |
| DS3 | DSPI_PCS _n to DSPI_SCK output valid | $(t_{SCK/2}) - 2$ | — | ns |

Table continues on the next page...

Table 40. Master Mode DSPI Timing (High-speed mode) (continued)

| Num | Description | Min. | Max. | Unit |
|-----|-----------------------------------|-------------------|------|------|
| DS4 | DSPI_SCK to DSPI_PCSn output hold | $(t_{SCK}/2) - 2$ | — | ns |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 8.5 | ns |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -2 | — | ns |
| DS7 | DSPI_SIN to DSPI_SCK input setup | TBD | — | ns |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns |

**Figure 22. DSPI Classic SPI Timing — Master Mode****Table 41. Slave Mode DSPI Timing (High-speed mode)**

| Num | Description | Min. | Max. | Unit |
|------|--|---------------------|-------------------|------|
| | Operating voltage | 2.7 | 3.6 | V |
| | Frequency of operation | | 12.5 | MHz |
| DS9 | DSPI_SCK input cycle time | $4 \times t_{BCLK}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK}/2) - 2$ | $(t_{SCK}/2) + 2$ | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | TBD | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns |
| DS15 | $\overline{DSPI_SS}$ active to DSPI_SOUT driven | — | 14 | ns |
| DS16 | $\overline{DSPI_SS}$ inactive to DSPI_SOUT not driven | — | 14 | ns |

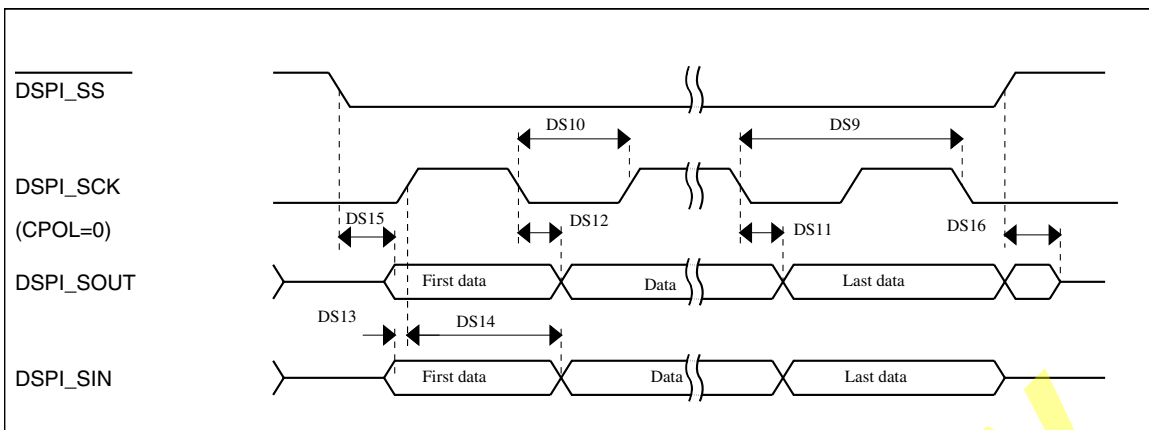


Figure 23. DSPI Classic SPI Timing — Slave Mode

6.8.7 SDHC Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 42. SDHC switching specifications

| Num | Symbol | Description | Min. | Max. | Unit |
|---|------------------|---------------------------------------|------|------|------|
| Card input clock | | | | | |
| SD1 | fpp | Clock frequency (low speed) | 0 | 400 | kHz |
| | fpp | Clock frequency (SD\SDIO full speed) | 0 | 25 | MHz |
| | fpp | Clock frequency (MMC full speed) | 0 | 20 | MHz |
| | f _{OD} | Clock frequency (identification mode) | 0 | 400 | kHz |
| SD2 | t _{WL} | Clock low time | 7 | — | ns |
| SD3 | t _{WH} | Clock high time | 7 | — | ns |
| SD4 | t _{TLH} | Clock rise time | — | 3 | ns |
| SD5 | t _{THL} | Clock fall time | — | 3 | ns |
| SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK) | | | | | |
| SD6 | t _{OD} | SDHC output delay (output valid) | -5 | 6.5 | ns |
| SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK) | | | | | |
| SD7 | t _{THL} | SDHC input setup time | 5 | — | ns |
| SD8 | t _{THL} | SDHC input hold time | 0 | — | ns |

www.DataSheet4U.com

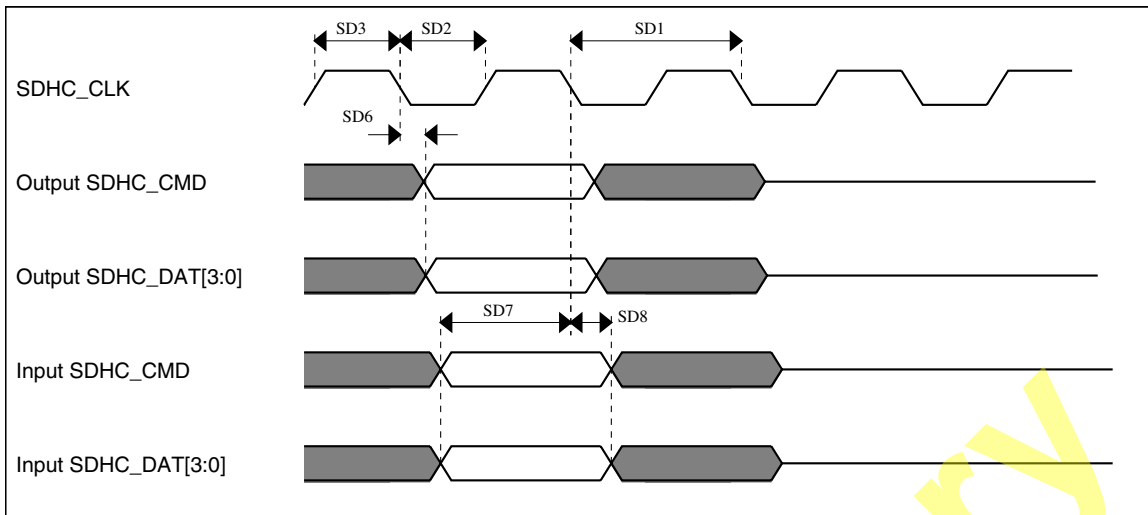


Figure 24. SDHC timing

6.8.8 I²S Switching Specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 43. I²S master mode timing

| Num | Description | Min. | Max. | Unit |
|-----|--|----------------------|------|-------------|
| | Operating voltage | 2.7 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 2 x t _{sys} | | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_BCLK cycle time | 5 x t _{sys} | — | ns |
| S4 | I2S_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_BCLK to I2S_FS output valid | — | 15 | ns |
| S6 | I2S_BCLK to I2S_FS output invalid | -2.5 | — | ns |
| S7 | I2S_BCLK to I2S_TXD valid | — | 15 | ns |
| S8 | I2S_BCLK to I2S_TXD invalid | -3 | — | ns |
| S9 | I2S_RXD/I2S_FS input setup before I2S_BCLK | 20 | — | ns |
| S10 | I2S_RXD/I2S_FS input hold after I2S_BCLK | 0 | — | ns |

Peripheral operating requirements and behaviors

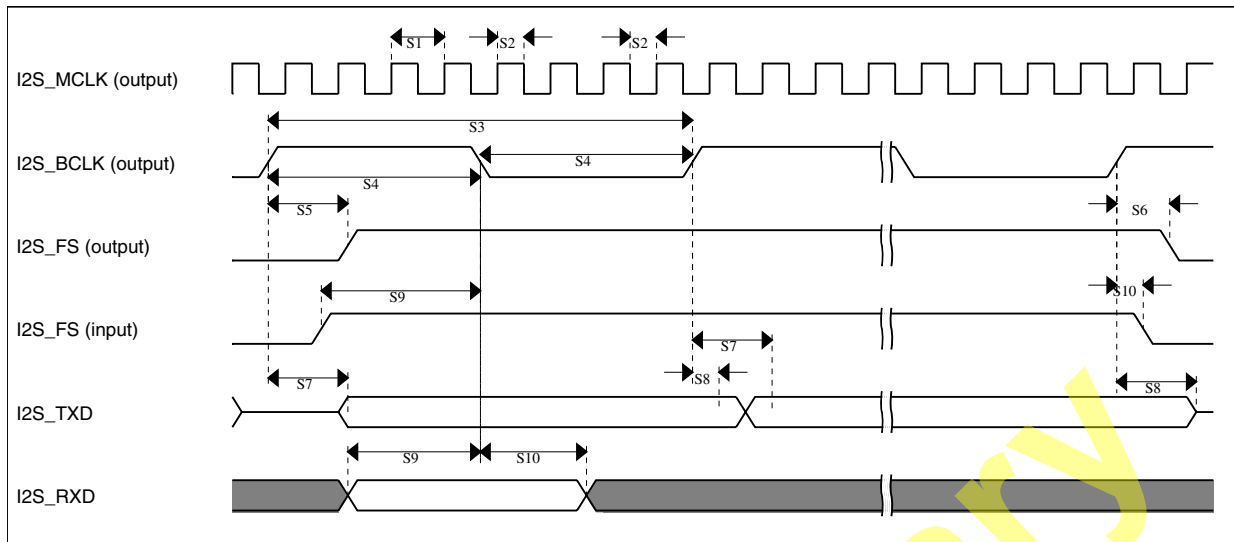


Figure 25. I²S timing — master mode

Table 44. I²S slave mode timing

| Num | Description | Min. | Max. | Unit |
|-----|---|----------------------|------|-------------|
| | Operating voltage | 2.7 | 3.6 | V |
| S11 | I2S_BCLK cycle time (input) | 8 x t _{SYS} | — | ns |
| S12 | I2S_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_FS input setup before I2S_BCLK | 10 | — | ns |
| S14 | I2S_FS input hold after I2S_BCLK | 3 | — | ns |
| S15 | I2S_BCLK to I2S_TXD/I2S_FS output valid | — | 20 | ns |
| S16 | I2S_BCLK to I2S_TXD/I2S_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_BCLK | 10 | — | ns |
| S18 | I2S_RXD hold after I2S_BCLK | 2 | — | ns |

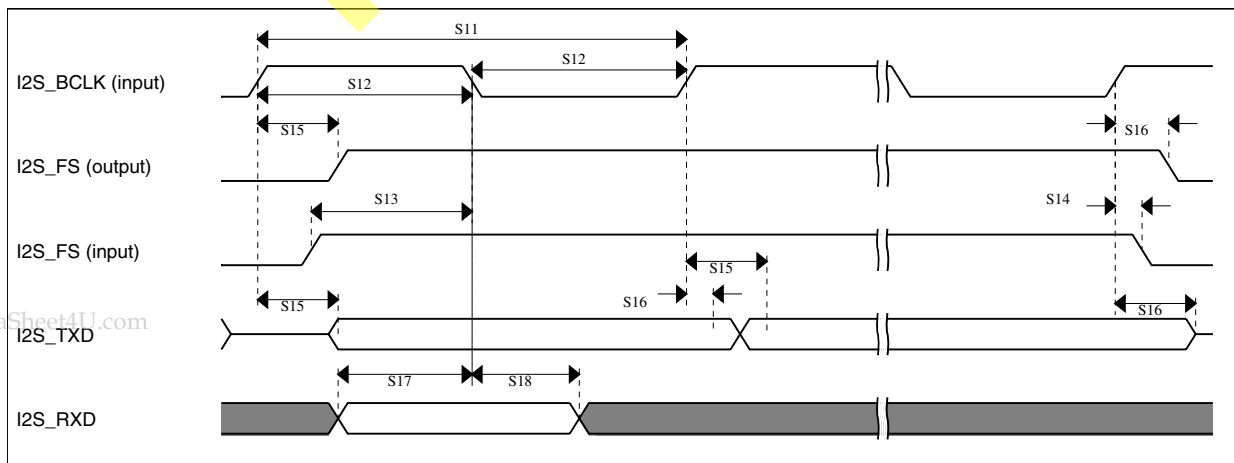


Figure 26. I²S timing — slave modes

6.9 Human-machine interfaces (HMI)

6.9.1 General Switching Specifications

These general purpose specifications apply to all signals configured for GPIO, SCI, FlexCAN, CMT, IEEE 1588 timer, and I²C signals.

Table 45. General switching specifications

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|---|------|------|------------------|-------|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path | 100 | — | ns | 2 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path | 16 | — | ns | 2 |
| | External reset pulse width (digital glitch filter disabled) | TBD | — | | |
| | Mode select ($\overline{\text{EZP_CS}}$) hold time after reset deassertion | 2 | — | Bus clock cycles | |
| | Port rise and fall time (high drive strength) | | | | 3 |
| | • Slew disabled | — | 12 | ns | |
| | • Slew enabled | — | 36 | ns | |
| | Port rise and fall time (low drive strength) | | | | 4 |
| | • Slew disabled | — | 32 | ns | |
| | • Slew enabled | — | 36 | ns | |

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75pF load
4. 15pF load

6.9.2 TSI Electrical Specifications

Table 46. Touch Sensing Input module specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---------------------|------------------------------------|------|------|------|------|-------|
| V _{DDTSI} | Operating voltage | 1.71 | — | 3.6 | V | |
| C _{ELE} | Target electrode capacitance range | 1 | 20 | 500 | pF | 1 |
| f _{REFmax} | Reference oscillator frequency | — | 5.5 | TBD | MHz | |

Table continues on the next page...

Table 46. Touch Sensing Input module specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|--|-------|-------|------|---------------|-------|
| f_{ELEmax} | Electrode oscillator frequency | — | 0.5 | TBD | MHz | |
| C_{REF} | Internal reference capacitor | TBD | 1 | TBD | pF | |
| V_{DELTA} | Oscillator delta voltage | TBD | 600 | TBD | mV | |
| I_{REF} | Reference oscillator current source base current | TBD | 1 | TBD | μA | 2 |
| I_{ELE} | Electrode oscillator current source base current | TBD | 1 | TBD | μA | 3 |
| Pres5 | Electrode capacitance measurement precision | — | TBD | TBD | % | 4 |
| Pres20 | Electrode capacitance measurement precision | — | TBD | TBD | % | 5 |
| Pres100 | Electrode capacitance measurement precision | — | TBD | TBD | % | 6 |
| Max-Sens20 | Max sensitivity @ 20pF electrode | 0.15 | 0.326 | 600 | fF | 7 |
| MaxSens | Maximum sensitivity | 0.006 | 0.326 | 24 | fF | 8 |
| Res | Resolution | — | — | 16 | bits | |
| T_{Con20} | Response time @ 20pF | — | 30 | — | μs | 9 |
| $I_{\text{TSL_RUN}}$ | Current added in run mode | — | TBD | — | μA | |
| $I_{\text{TSL_LP}}$ | Low power mode current adder | — | 1 | TBD | μA | |

1. The TSI module is functional with capacitance values outside of this range. However, optimal performance is not guaranteed.
2. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current
3. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current
4. Measured with a 5pF electrode, reference oscillator frequency of 10MHz, PS = 128, NCSC = 8; Iext = 16
5. Measured with a 20pF electrode, reference oscillator frequency of 10MHz, PS = 128, NCSC = 2; Iext = 16
6. Measured with a 20pF electrode, reference oscillator frequency of 10MHz, PS = 16, NCSC = 3; Iext = 16
7. 6.2ms scan time
8. 1pF electrode capacitance with 4.96ms scan time
9. Time that takes to do one complete measurement of the electrode. Sensitivity resolution of 0.0133pF

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|--|-------------------------------|
| 100-pin LQFP | 98ASS23308W |
| 104-pin MAPBGA | 98ARH98267A |

8 Pinout

8.1 K60 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 100 QFP | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---------|-----------------------------------|-----------------------------------|------|-----------|-------------|------------|------|------------|------|--------|
| 1 | ADC1_SE4a | ADC1_SE4a | PTE0 | SPI1_PCS1 | UART1_TX | SDHC0_D1 | | I2C1_SDA | | |
| 2 | ADC1_SE5a | ADC1_SE5a | PTE1 | SPI1_SOUT | UART1_RX | SDHC0_D0 | | I2C1_SCL | | |
| 3 | ADC1_SE6a | ADC1_SE6a | PTE2 | SPI1_SCK | UART1_CTS_b | SDHC0_DCLK | | | | |
| 4 | ADC1_SE7a | ADC1_SE7a | PTE3 | SPI1_SIN | UART1_RTS_b | SDHC0_CMD | | | | |
| 5 | DISABLED | | PTE4 | SPI1_PCS0 | UART3_TX | SDHC0_D3 | | | | |
| 6 | DISABLED | | PTE5 | SPI1_PCS2 | UART3_RX | SDHC0_D2 | | | | |
| 7 | DISABLED | | PTE6 | SPI1_PCS3 | UART3_CTS_b | I2S0_MCLK | | I2S0_CLKIN | | |
| 8 | VDD | VDD | | | | | | | | |
| 9 | VSS | VSS | | | | | | | | |
| 10 | USB0_DP | USB0_DP | | | | | | | | |
| 11 | USB0_DM | USB0_DM | | | | | | | | |
| 12 | VOUT33 | VOUT33 | | | | | | | | |
| 13 | VREGIN | VREGIN | | | | | | | | |
| 14 | ADC0_DP1 | ADC0_DP1 | | | | | | | | |
| 15 | ADC0_DM1 | ADC0_DM1 | | | | | | | | |
| 16 | ADC1_DP1 | ADC1_DP1 | | | | | | | | |
| 17 | ADC1_DM1 | ADC1_DM1 | | | | | | | | |
| 18 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | | | | | | | | |
| 19 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | | | | | | | | |
| 20 | PGA1_DP/ ADC1_DP0/ ADC0_DP3 | PGA1_DP/ ADC1_DP0/ ADC0_DP3 | | | | | | | | |
| 21 | PGA1_DM/ ADC1_DM0/ ADC0_DM3 | PGA1_DM/ ADC1_DM0/ ADC0_DM3 | | | | | | | | |
| 22 | VDDA | VDDA | | | | | | | | |
| 23 | VREFH | VREFH | | | | | | | | |

Pinout

| 100 QFP | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---------|-----------------------------------|-----------|-------|-------------|-------------|----------------------------|----------|--------------|------------------------|----------|
| 24 | VREFL | VREFL | | | | | | | | |
| 25 | VSSA | VSSA | | | | | | | | |
| 26 | VREF_OUT | VREF_OUT | | | | | | | | |
| 27 | DAC0_OUT | DAC0_OUT | | | | | | | | |
| 28 | XTAL32 | XTAL32 | | | | | | | | |
| 29 | EXTAL32 | EXTAL32 | | | | | | | | |
| 30 | VBAT | VBAT | | | | | | | | |
| 31 | ADC0_SE17 | ADC0_SE17 | PTE24 | CAN1_TX | UART4_TX | | | EWM_OUT_b | | |
| 32 | ADC0_SE18 | ADC0_SE18 | PTE25 | CAN1_RX | UART4_RX | | | EWM_IN | | |
| 33 | DISABLED | | PTE26 | | UART4_CTS_b | ENET_1588_CLKIN | | RTC_CLKOUT | USB_CLKIN | |
| 34 | JTAG_TCLK/ SWD_CLK/ EZP_CLK | TSI0_CH1 | PTA0 | UART0_CTS_b | FTM0_CH5 | | | | JTAG_TCLK/ SWD_CLK | EZP_CLK |
| 35 | JTAG_TDI/ EZP_DI | TSI0_CH2 | PTA1 | UART0_RX | FTM0_CH6 | | | | JTAG_TDI | EZP_DI |
| 36 | JTAG_TDO/ TRACE_SWO/ EZP_DO | TSI0_CH3 | PTA2 | UART0_TX | FTM0_CH7 | | | | JTAG_TDO/ TRACE_SWO | EZP_DO |
| 37 | JTAG_TMS/ SWD_DIO | TSI0_CH4 | PTA3 | UART0_RTS_b | FTM0_CH0 | | | | JTAG_TMS/ SWD_DIO | |
| 38 | NMI_b/ EZP_CS_b | TSI0_CH5 | PTA4 | | FTM0_CH1 | | | | NMI_b | EZP_CS_b |
| 39 | JTAG_TRST | | PTA5 | | FTM0_CH2 | RMII0_RXER/ MII0_RXER | CMP2_OUT | I2S0_RX_BCLK | JTAG_TRST | |
| 40 | VDD | VDD | | | | | | | | |
| 41 | VSS | VSS | | | | | | | | |
| 42 | CMP2_IN0 | CMP2_IN0 | PTA12 | CAN0_TX | FTM1_CH0 | RMII0_RXD1/ MII0_RXD1 | | I2S0_TXD | FTM1_QD_PHA | |
| 43 | CMP2_IN1 | CMP2_IN1 | PTA13 | CAN0_RX | FTM1_CH1 | RMII0_RXD0/ MII0_RXD0 | | I2S0_TX_FS | FTM1_QD_PHB | |
| 44 | DISABLED | | PTA14 | SPI0_PCS0 | UART0_TX | RMII0_CRS_DV/ MII0_RXDV | | I2S0_TX_BCLK | | |
| 45 | DISABLED | | PTA15 | SPI0_SCK | UART0_RX | RMII0_TXEN/ MII0_TXEN | | I2S0_RXD | | |
| 46 | DISABLED | | PTA16 | SPI0_SOUT | UART0_CTS_b | RMII0_TXD0/ MII0_TXD0 | | I2S0_RX_FS | | |
| 47 | ADC1_SE17 | ADC1_SE17 | PTA17 | SPI0_SIN | UART0_RTS_b | RMII0_TXD1/ MII0_TXD1 | | I2S0_MCLK | I2S0_CLKIN | |
| 48 | VDD | VDD | | | | | | | | |
| 49 | VSS | VSS | | | | | | | | |
| 50 | EXTAL | EXTAL | PTA18 | | FTM0_FLT2 | FTM_CLKIN0 | | | | |
| 51 | XTAL | XTAL | PTA19 | | FTM1_FLT0 | FTM_CLKIN1 | | LPT0_ALT1 | | |
| 52 | RESET_b | RESET_b | | | | | | | | |

| 100 QFP | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---------|--------------------------------------|--------------------------------------|-------|-----------|-----------------|--------------------------|-----------|-----------------|------|--------|
| 53 | ADC0_SE8/ ADC1_SE8/ TSI0_CH0 | ADC0_SE8/ ADC1_SE8/ TSI0_CH0 | PTB0 | I2C0_SCL | FTM1_CH0 | RMII0_MDIO/ MII0_MDIO | | FTM1_QD_PH A | | |
| 54 | ADC0_SE9/ ADC1_SE9/ TSI0_CH6 | ADC0_SE9/ ADC1_SE9/ TSI0_CH6 | PTB1 | I2C0_SDA | FTM1_CH1 | RMII0_MDC/ MII0_MDC | | FTM1_QD_PH B | | |
| 55 | ADC0_SE12/ TSI0_CH7 | ADC0_SE12/ TSI0_CH7 | PTB2 | I2C0_SCL | UART0_RTS_ b | ENET0_1588_ TMR0 | | FTM0_FLT3 | | |
| 56 | ADC0_SE13/ TSI0_CH8 | ADC0_SE13/ TSI0_CH8 | PTB3 | I2C0_SDA | UART0_CTS_ b | ENET0_1588_ TMR1 | | FTM0_FLT0 | | |
| 57 | DISABLED | | PTB9 | SPI1_PCS1 | UART3_CTS_ b | | FB_AD20 | | | |
| 58 | ADC1_SE14 | ADC1_SE14 | PTB10 | SPI1_PCS0 | UART3_RX | | FB_AD19 | FTM0_FLT1 | | |
| 59 | ADC1_SE15 | ADC1_SE15 | PTB11 | SPI1_SCK | UART3_TX | | FB_AD18 | FTM0_FLT2 | | |
| 60 | VSS | VSS | | | | | | | | |
| 61 | VDD | VDD | | | | | | | | |
| 62 | TSI0_CH9 | TSI0_CH9 | PTB16 | SPI1_SOUT | UART0_RX | | FB_AD17 | EWM_IN | | |
| 63 | TSI0_CH10 | TSI0_CH10 | PTB17 | SPI1_SIN | UART0_TX | | FB_AD16 | EWM_OUT_b | | |
| 64 | TSI0_CH11 | TSI0_CH11 | PTB18 | CAN0_TX | FTM2_CH0 | I2S0_TX_BCL K | FB_AD15 | FTM2_QD_PH A | | |
| 65 | TSI0_CH12 | TSI0_CH12 | PTB19 | CAN0_RX | FTM2_CH1 | I2S0_TX_FS | FB_OE_b | FTM2_QD_PH B | | |
| 66 | DISABLED | | PTB20 | SPI2_PCS0 | | | FB_AD31 | CMP0_OUT | | |
| 67 | DISABLED | | PTB21 | SPI2_SCK | | | FB_AD30 | CMP1_OUT | | |
| 68 | DISABLED | | PTB22 | SPI2_SOUT | | | FB_AD29 | CMP2_OUT | | |
| 69 | DISABLED | | PTB23 | SPI2_SIN | SPI0_PCS5 | | FB_AD28 | | | |
| 70 | ADC0_SE14/ TSI0_CH13 | ADC0_SE14/ TSI0_CH13 | PTC0 | SPI0_PCS4 | PDB0_EXTRG | I2S0_TXD | FB_AD14 | | | |
| 71 | ADC0_SE15/ TSI0_CH14 | ADC0_SE15/ TSI0_CH14 | PTC1 | SPI0_PCS3 | UART1_RTS_ b | FTM0_CH0 | FB_AD13 | | | |
| 72 | ADC0_SE4b/ CMP1_IN0/ TSI0_CH15 | ADC0_SE4b/ CMP1_IN0/ TSI0_CH15 | PTC2 | SPI0_PCS2 | UART1_CTS_ b | FTM0_CH1 | FB_AD12 | | | |
| 73 | CMP1_IN1 | CMP1_IN1 | PTC3 | SPI0_PCS1 | UART1_RX | FTM0_CH2 | FB_CLKOUT | | | |
| 74 | VSS | VSS | | | | | | | | |
| 75 | VDD | VDD | | | | | | | | |
| 76 | DISABLED | | PTC4 | SPI0_PCS0 | UART1_TX | FTM0_CH3 | FB_AD11 | CMP1_OUT | | |
| 77 | DISABLED | | PTC5 | SPI0_SCK | | LPT0_ALT2 | FB_AD10 | CMP0_OUT | | |
| 78 | CMP0_IN0 | CMP0_IN0 | PTC6 | SPI0_SOUT | PDB0_EXTRG | | FB_AD9 | | | |
| 79 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_SIN | | | FB_AD8 | | | |
| 80 | ADC1_SE4b/ CMP0_IN2 | ADC1_SE4b/ CMP0_IN2 | PTC8 | | I2S0_MCLK | I2S0_CLKIN | FB_AD7 | | | |
| 81 | ADC1_SE5b/ CMP0_IN3 | ADC1_SE5b/ CMP0_IN3 | PTC9 | | | I2S0_RX_BCL K | FB_AD6 | FTM2_FLT0 | | |
| 82 | ADC1_SE6b/ CMP0_IN4 | ADC1_SE6b/ CMP0_IN4 | PTC10 | I2C1_SCL | | I2S0_RX_FS | FB_AD5 | | | |

Pinout

| 100 QFP | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---------|-----------|-----------|-------|-----------|-------------|-----------------|---|-----------|------|--------|
| 83 | ADC1_SE7b | ADC1_SE7b | PTC11 | I2C1_SDA | | I2S0_RXD | FB_RW_b | | | |
| 84 | DISABLED | | PTC12 | | UART4_RTS_b | | FB_AD27 | | | |
| 85 | DISABLED | | PTC13 | | UART4_CTS_b | | FB_AD26 | | | |
| 86 | DISABLED | | PTC14 | | UART4_RX | | FB_AD25 | | | |
| 87 | DISABLED | | PTC15 | | UART4_TX | | FB_AD24 | | | |
| 88 | VSS | VSS | | | | | | | | |
| 89 | VDD | VDD | | | | | | | | |
| 90 | DISABLED | | PTC16 | CAN1_RX | UART3_RX | ENET0_1588_TMR0 | FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_ BLS15_8_b | | | |
| 91 | DISABLED | | PTC17 | CAN1_TX | UART3_TX | ENET0_1588_TMR1 | FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_ BLS7_0_b | | | |
| 92 | DISABLED | | PTC18 | | UART3_RTS_b | ENET0_1588_TMR2 | FB_TBST_b/ FB_CS2_b/ FB_BE15_8_B LS23_16_b | | | |
| 93 | DISABLED | | PTD0 | SPI0_PCS0 | UART2_RTS_b | | FB_ALE/ FB_CS1_b/ FB_TS_b | | | |
| 94 | ADC0_SE5b | ADC0_SE5b | PTD1 | SPI0_SCK | UART2_CTS_b | | FB_CS0_b | | | |
| 95 | DISABLED | | PTD2 | SPI0_SOUT | UART2_RX | | FB_AD4 | | | |
| 96 | DISABLED | | PTD3 | SPI0_SIN | UART2_TX | | FB_AD3 | | | |
| 97 | DISABLED | | PTD4 | SPI0_PCS1 | UART0_RTS_b | FTM0_CH4 | FB_AD2 | EWM_IN | | |
| 98 | ADC0_SE6b | ADC0_SE6b | PTD5 | SPI0_PCS2 | UART0_CTS_b | FTM0_CH5 | FB_AD1 | EWM_OUT_b | | |
| 99 | ADC0_SE7b | ADC0_SE7b | PTD6 | SPI0_PCS3 | UART0_RX | FTM0_CH6 | FB_AD0 | FTM0_FLT0 | | |
| 100 | DISABLED | | PTD7 | CMT_IRO | UART0_TX | FTM0_CH7 | | FTM0_FLT1 | | |

8.2 K60 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

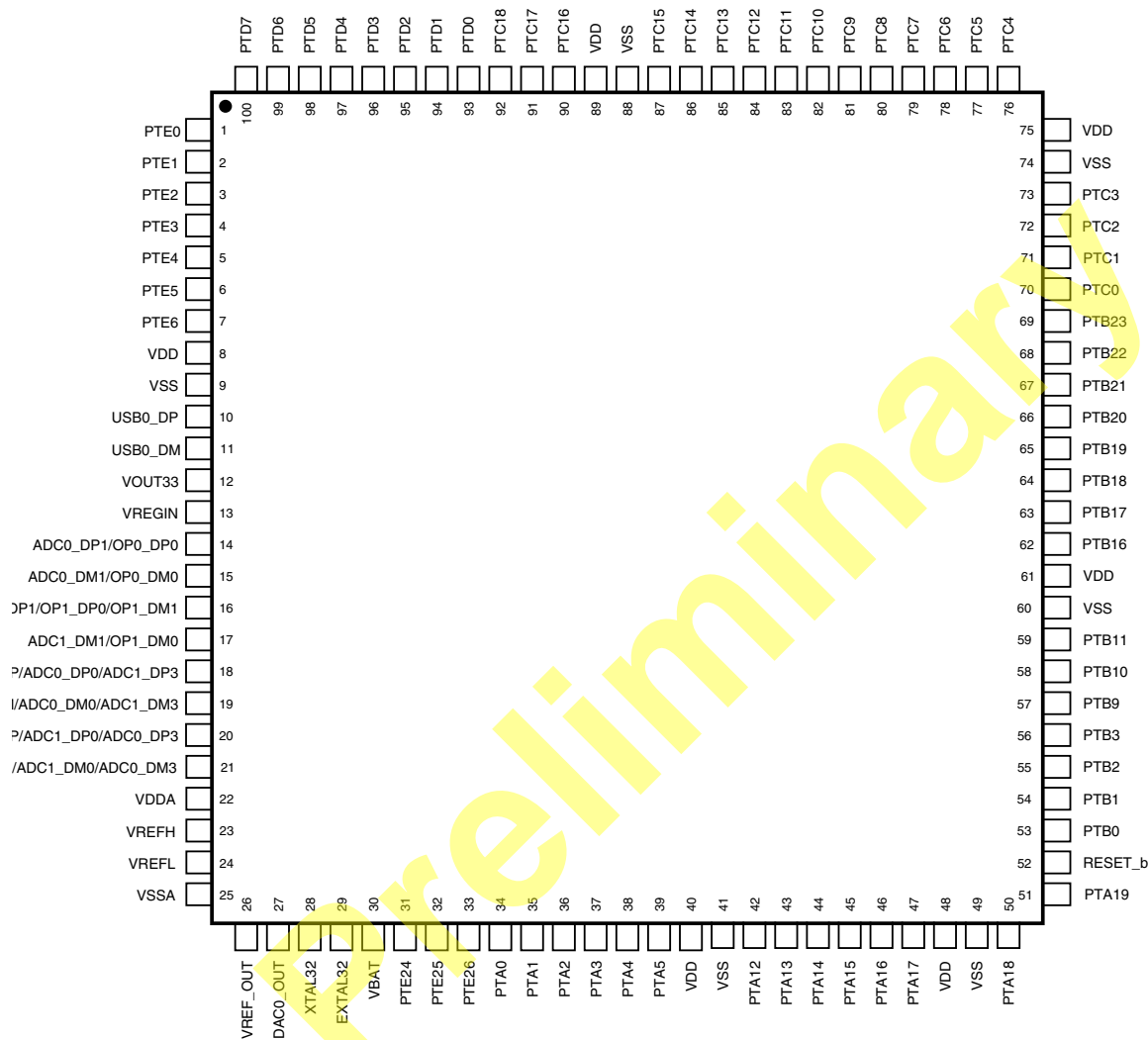


Figure 27. K60 100 LQFP Pinout Diagram

9 Revision History

The following table provides a revision history for this document.

Table 47. Revision History

| Rev. No. | Date | Substantial Changes |
|----------|---------|-------------------------|
| 1 | 11/2010 | Initial public revision |

Preliminary

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd. Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. ARM is the registered trademark of ARM Limited. ARM Cortex-M4 is the trademark of ARM Limited. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2010. All rights reserved.

K60P104M100SF2

Rev. 1
11/2010

