

## Document Title

512K x8 bit Super Low Power and Low Voltage Full CMOS Static RAM

## Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial Draft	October 25, 2000	Preliminary
1.0	Finalize	March 12, 2001	Final

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## 512K x 8 bit Super Low Power and Low Voltage Full CMOS Static RAM

### FEATURES

- Process Technology: Full CMOS
- Organization: 512K x8 bit
- Power Supply Voltage: 2.7~3.3V
- Low Data Retention Voltage: 1.5V(Min)
- Three State Outputs
- Package Type: 48(36)-TBGA-6.00x7.00

### GENERAL DESCRIPTION

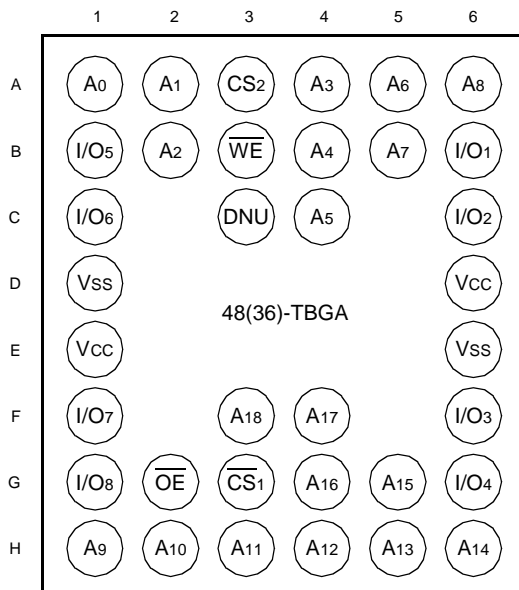
The K6F4008U2E families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>sb1</sub> , Typ.)	Operating (I <sub>cc1</sub> , Max)	
K6F4008U2E-F	Industrial(-40~85°C)	2.7~3.3V	55 <sup>1)</sup> /70ns	1.0μA <sup>2)</sup>	2mA	48(36)-TBGA-6.00x7.00

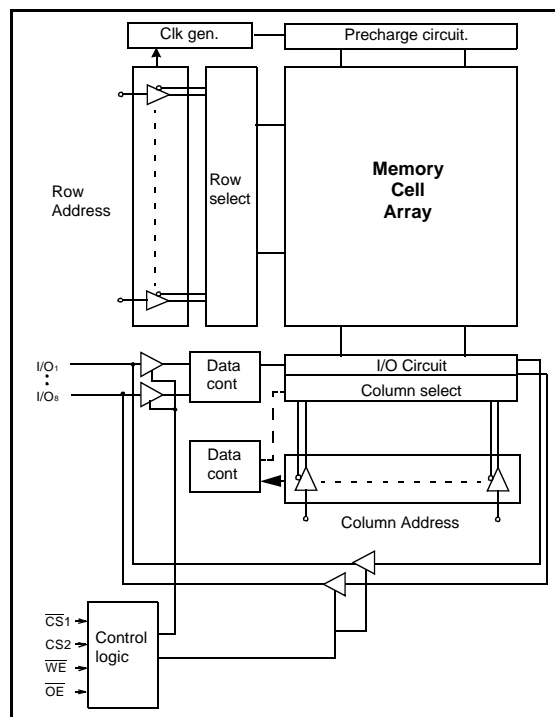
1. The parameter is measured with 30pF test load.
2. Typical value are at V<sub>cc</sub>=3.0V, T<sub>A</sub>=25°C and not 100% tested.

### PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS1}$ , $\overline{CS2}$	Chip Select Inputs	I/O1~I/O8	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
A0~A18	Address Inputs	DNU	Do Not Use

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
K6F4008U2E-EF55	48(36)-TBGA, 55ns, 3.0V
K6F4008U2E-EF70	48(36)-TBGA, 70ns, 3.0V

## FUNCTIONAL DESCRIPTION

CS <sub>1</sub>	CS <sub>2</sub>	OE	WE	I/O	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care (Must be in low or high state)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V <sub>ss</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.3V(Max. 3.6V)	V
Voltage on V <sub>CC</sub> supply relative to V <sub>ss</sub>	V <sub>CC</sub>	-0.3 to 3.6	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	T <sub>A</sub>	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.3	V
Ground	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.3 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.3 <sup>3)</sup>	-	0.6	V

Note:

1. T<sub>A</sub>=-40 to 85°C, otherwise specified.
2. Overshoot: V<sub>CC</sub>+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

## DC AND OPERATING CHARACTERISTICS

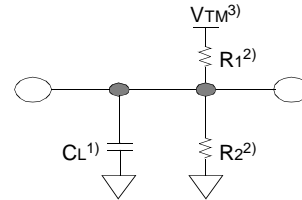
Item	Symbol	Test Conditions	Min	Typ <sup>1)</sup>	Max	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CS}_1=V_{IH}$ , CS <sub>2</sub> =V <sub>IL</sub> or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100%duty, I <sub>IO</sub> =0mA, $\overline{CS}_1 \leq 0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	-	-	2	mA	
			I <sub>CC2</sub>	Cycle time=Min, I <sub>IO</sub> =0mA, 100% duty, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	70ns		-
			55ns	-	-	20	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA	-	-	0.4	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4	-	-	V	
Standby Current (CMOS)	I <sub>SB1</sub>	$\overline{CS}_1 \geq V_{CC}-0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V( $\overline{CS}_1$ controlled) or 0V≤CS <sub>2</sub> ≤0.2V(CS <sub>2</sub> controlled), Other inputs=0-V <sub>CC</sub>	-	1	12	μA	

1. Typical value are measured at V<sub>CC</sub>=3.0V, T<sub>A</sub>=25°C, and not 100% tested.

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V  
 Input rising and falling time: 5ns  
 Input and output reference voltage: 1.5V  
 Output load (See right):  $C_L = 100\text{pF} + 1\text{TTL}$   
 $C_L = 30\text{pF} + 1\text{TTL}$



1. Including scope and jig capacitance
2.  $R_1 = 3070\Omega$ ,  $R_2 = 3150\Omega$
3.  $V_{TM} = 2.8\text{V}$

## AC CHARACTERISTICS ( $V_{CC} = 2.7 \sim 3.3\text{V}$ , Industrial product: $T_A = -40$ to $85^\circ\text{C}$ )

Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	t <sub>RC</sub>	55	-	70	-	ns
	Address Access Time	t <sub>AA</sub>	-	55	-	70	ns
	Chip Select to Output	t <sub>CO</sub>	-	55	-	70	ns
	Output Enable to Valid Output	t <sub>OE</sub>	-	25	-	35	ns
	Chip Select to Low-Z Output	t <sub>LZ</sub>	10	-	10	-	ns
	Output Enable to Low-Z Output	t <sub>OLZ</sub>	5	-	5	-	ns
	Chip Disable to High-Z Output	t <sub>HZ</sub>	0	20	0	25	ns
	Output Disable to High-Z Output	t <sub>OHZ</sub>	0	20	0	25	ns
	Output Hold from Address Change	t <sub>OH</sub>	10	-	10	-	ns
Write	Write Cycle Time	t <sub>WC</sub>	55	-	70	-	ns
	Chip Select to End of Write	t <sub>CW</sub>	45	-	60	-	ns
	Address Set-up Time	t <sub>AS</sub>	0	-	0	-	ns
	Address Valid to End of Write	t <sub>AW</sub>	45	-	60	-	ns
	Write Pulse Width	t <sub>WP</sub>	40	-	50	-	ns
	Write Recovery Time	t <sub>WR</sub>	0	-	0	-	ns
	Write to Output High-Z	t <sub>WHZ</sub>	0	20	0	20	ns
	Data to Write Time Overlap	t <sub>DW</sub>	25	-	30	-	ns
	Data Hold from Write Time	t <sub>DH</sub>	0	-	0	-	ns
End Write to Output Low-Z	t <sub>OW</sub>	5	-	5	-	ns	

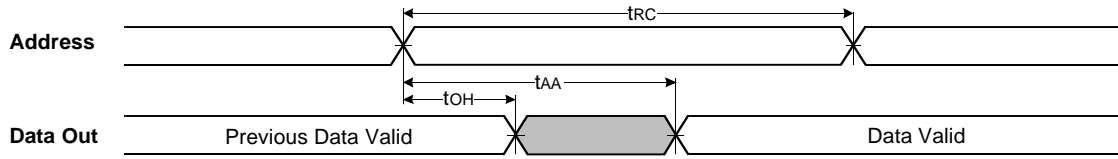
## DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{CS}_1 \geq V_{CC} - 0.2\text{V}^{(1)}$	1.5	-	3.3	V
Data retention current	I <sub>DR</sub>	$V_{CC} = 1.5\text{V}$ , $\overline{CS}_1 \geq V_{CC} - 0.2\text{V}^{(1)}$ , $V_{IN} \geq 0\text{V}$	-	0.5 <sup>(2)</sup>	3	$\mu\text{A}$
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ns
Recovery time	t <sub>RDR</sub>		t <sub>RC</sub>	-	-	

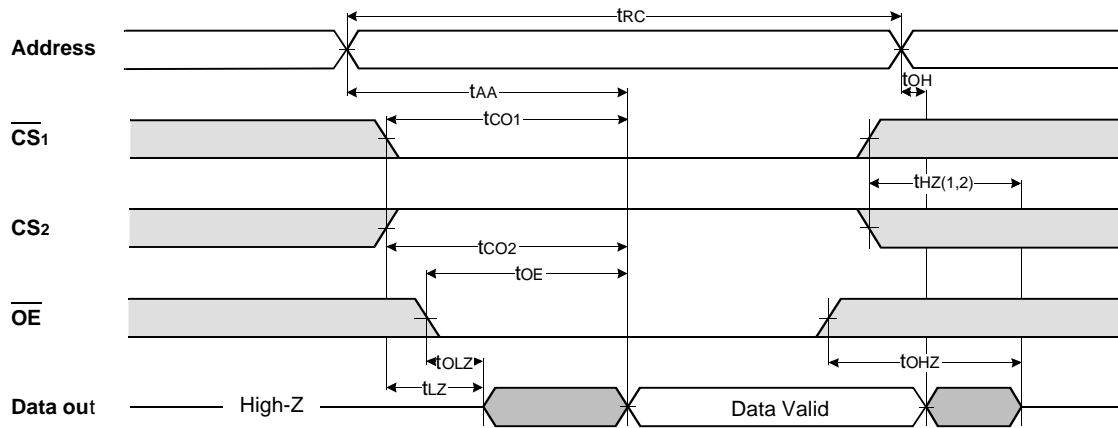
1.  $\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$ ,  $\overline{CS}_2 \geq V_{CC} - 0.2\text{V}$  ( $\overline{CS}_1$  controlled) or  $0 \leq \overline{CS}_2 \leq 0.2\text{V}$  ( $\overline{CS}_2$  controlled).
2. Typical value are measured at  $T_A = 25^\circ\text{C}$  and not 100% tested.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS}_1=\overline{OE}=V_{IL}$ ,  $CS_2=\overline{WE}=V_{IH}$ )



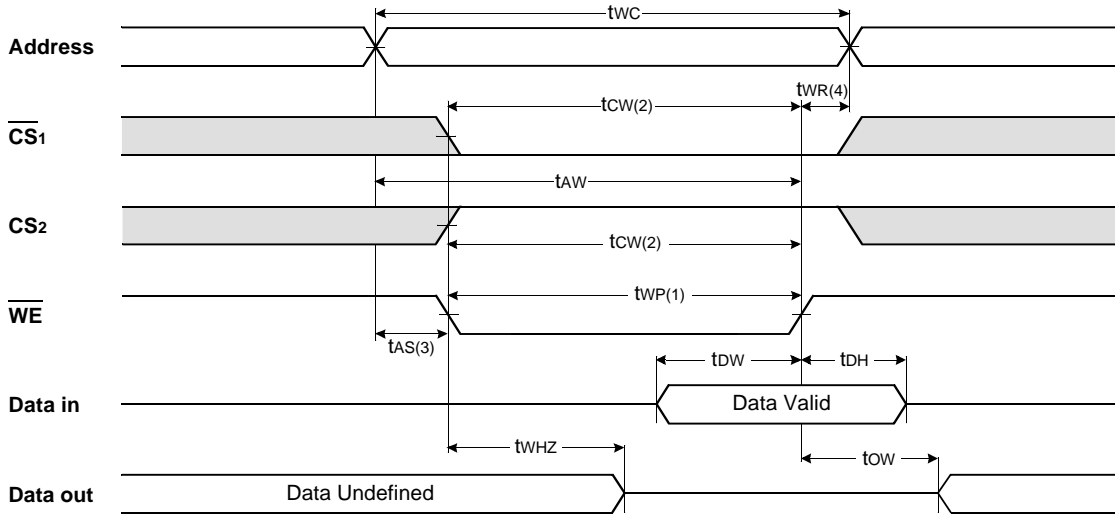
TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )



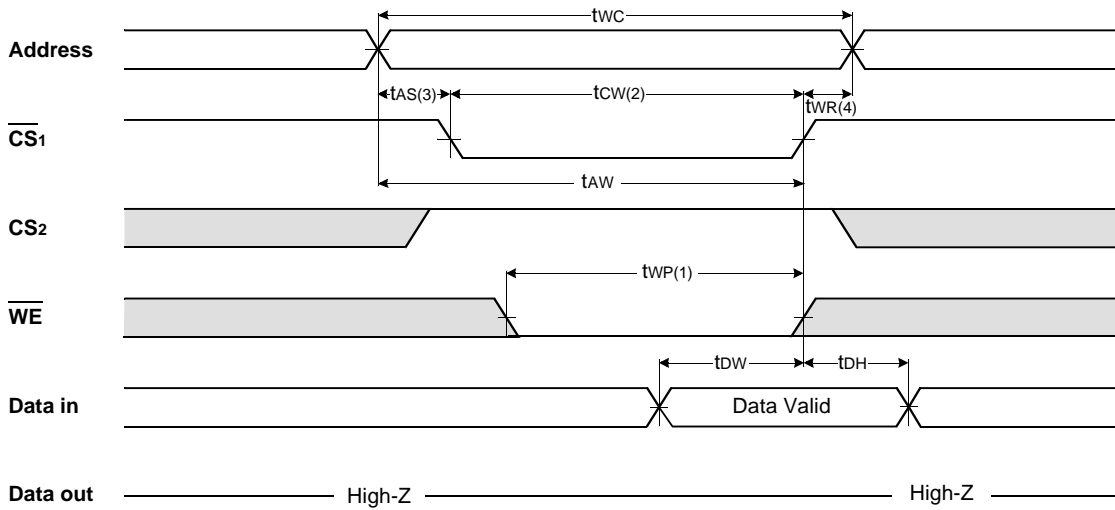
NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

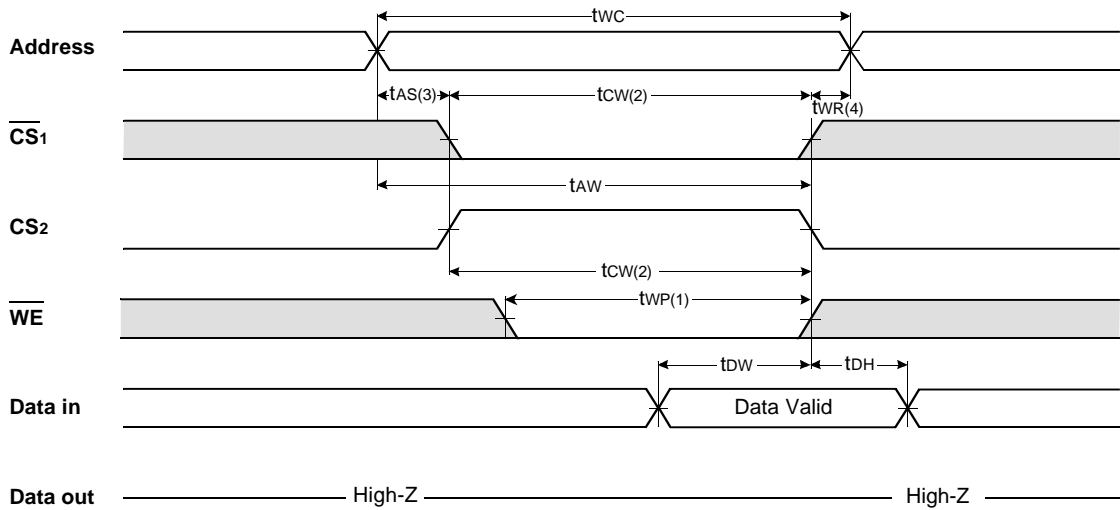
TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS1}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS<sub>2</sub> Controlled)

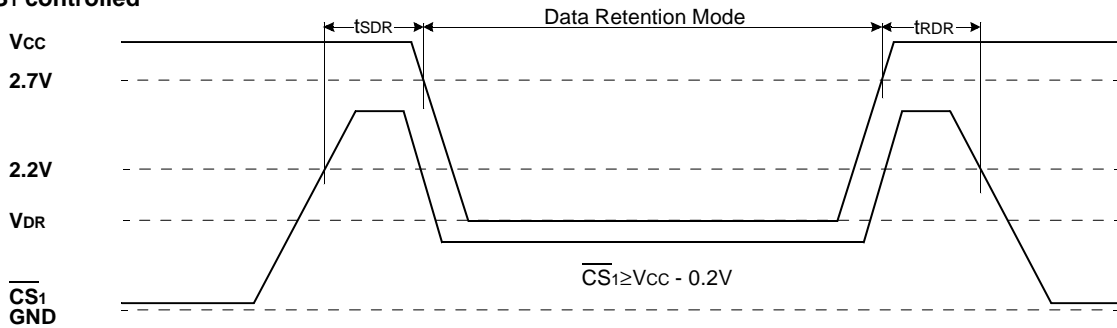


NOTES (WRITE CYCLE)

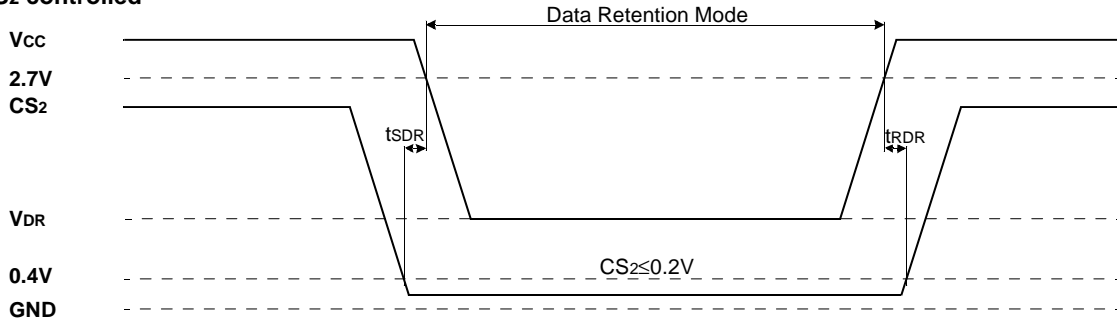
1. A write occurs during the overlap of a low  $\overline{CS}_1$ , a high  $CS_2$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}_1$  goes low,  $CS_2$  going high and  $\overline{WE}$  going low: A write end at the earliest transition among  $CS_1$  going high,  $CS_2$  going low and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $CS_1$  going low or  $CS_2$  going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR1}$  applied in case a write ends as  $\overline{CS}_1$  or  $\overline{WE}$  going high  $t_{WR2}$  applied in case a write ends as  $CS_2$  going to low.

DATA RETENTION WAVE FORM

$\overline{CS}_1$  controlled



$CS_2$  controlled

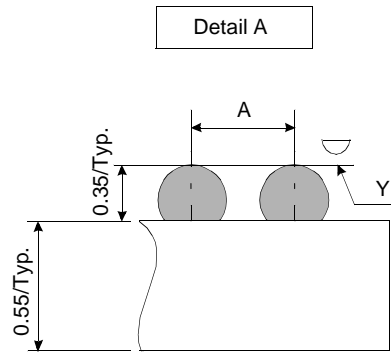
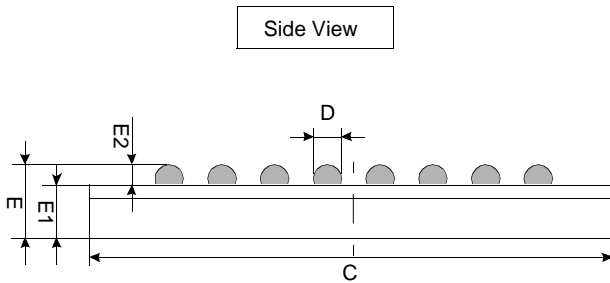
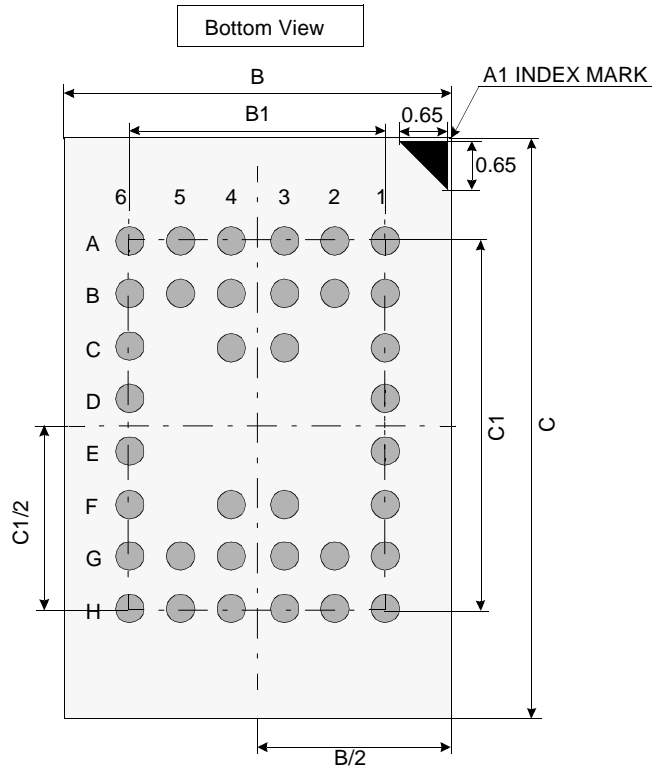
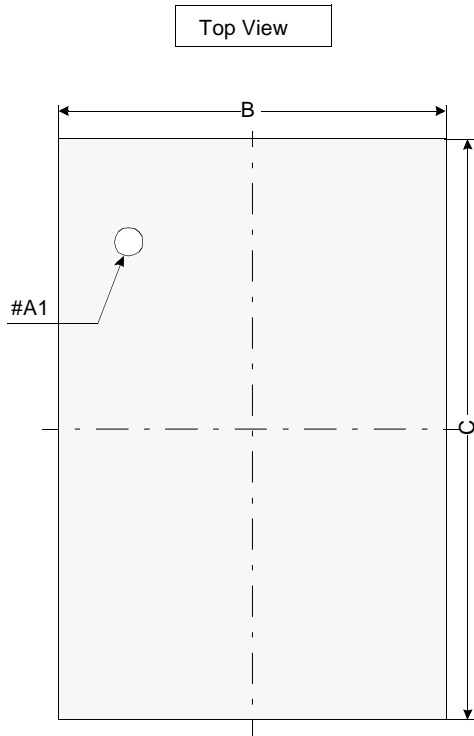




PACKAGE DIMENSIONS

Units: millimeters

48(36) TAPE BALL GRID ARRAY(0.75mm ball pitch)



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	6.90	7.00	7.10
C1	-	5.25	-
D	0.40	0.45	0.50
E	0.80	0.90	1.00
E1	-	0.55	-
E2	0.30	0.35	0.40
Y	-	-	0.08

Notes.

1. Bump counts: 48(8 row x 6 column)
2. Bump pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ: Typical
5. Y is coplanarity: 0.08(Max)