

K6R4008V1C-C/C-L, K6R4008V1C-I/C-P**CMOS SRAM****3 Document Title**

**512Kx8 Bit High Speed Static RAM(3.3V Operating).
Operated at Commercial and Industrial Temperature Ranges.**

Revision History

RevNo.	History	Draft Data	Remark																													
Rev. 0.0	Initial release with Preliminary.	Feb. 12. 1999	Preliminary																													
Rev. 1.0	1.1 Removed Low power Version. 1.2 Removed Data Retention Characteristics. 1.3 Changed Isb1 to 20mA	Mar. 29. 1999	Preliminary																													
Rev. 2.0	Relax D.C parameters.	Aug. 19. 1999	Preliminary																													
	<table border="1"> <thead> <tr> <th>Item</th> <th>Previous</th> <th>Current</th> </tr> </thead> <tbody> <tr> <td rowspan="3">Icc</td> <td>12ns</td> <td>160mA</td> </tr> <tr> <td>15ns</td> <td>155mA</td> </tr> <tr> <td>20ns</td> <td>150mA</td> </tr> </tbody> </table>	Item	Previous	Current	Icc	12ns	160mA	15ns	155mA	20ns	150mA																					
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Rev. 3.0	3.1 Delete Preliminary 3.2 Update D.C parameters and 10ns part.	Mar. 27. 2000	Final																													
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Rev. 4.0	Add Low Power-Ver.	Apr. 24. 2000	Final																													
Rev. 5.0	Delete 20ns speed bin	Sep. 24. 2001	Final																													

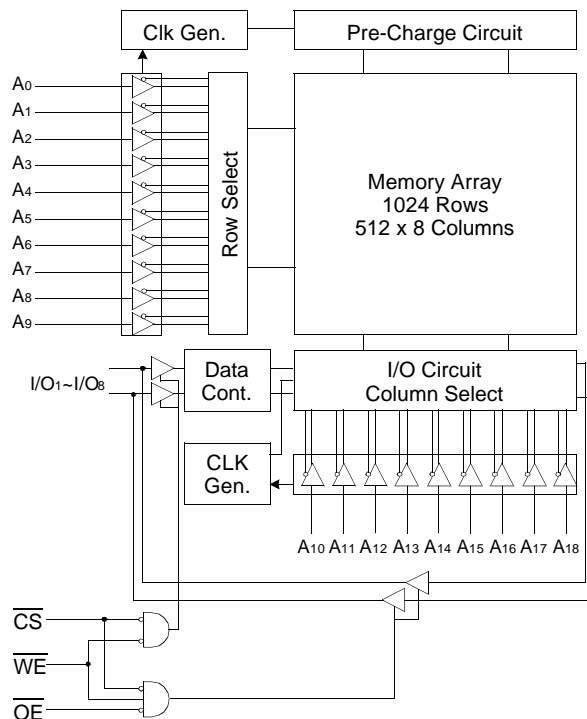
The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

K6R4008V1C-C/C-L, K6R4008V1C-I/C-P**CMOS SRAM****512K x 8 Bit High-Speed CMOS Static RAM****FEATURES**

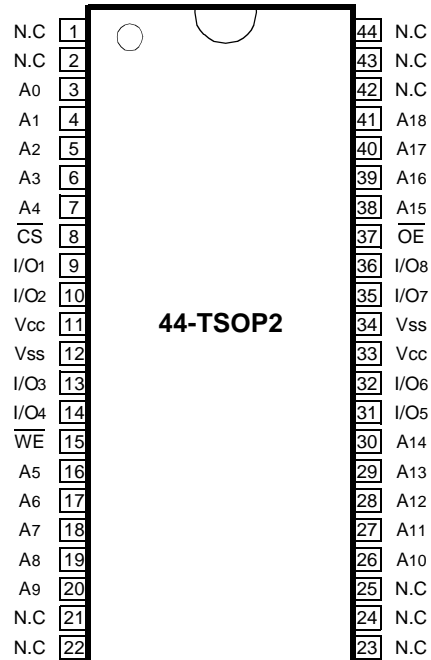
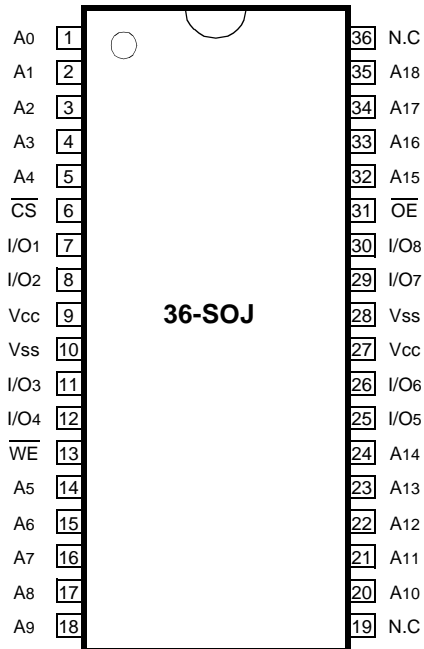
- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 60mA(Max.)
 - (CMOS) : 10mA(Max.)
 - 1.2mA(Max.) L-Ver. only
- Operating K6R4008V1C-10 : 155mA(Max.)
- K6R4008V1C-12 : 145mA(Max.)
- K6R4008V1C-15 : 135mA(Max.)
- Single 3.3±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention : L-Ver. only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
 - K6R4008V1C-J : 36-SOJ-400
 - K6R4008V1C-T : 44-TSOP2-400BF

GENERAL DESCRIPTION

The K6R4008V1C is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The K6R4008V1C uses 8 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R4008V1C is packaged in a 400 mil 36-pin plastic SOJ and 44-pin plastic TSOP type II.

FUNCTIONAL BLOCK DIAGRAM**ORDERING INFORMATION**

K6R4008V1C-C10/C12/C15	Commercial Temp.
K6R4008V1C-I10/I12/I15	Industrial Temp.

K6R4008V1C-C/C-L, K6R4008V1C-I/C-P**CMOS SRAM****PIN CONFIGURATION** (Top View)**PIN FUNCTION**

Pin Name	Pin Function
A0 - A18	Address Inputs
\overline{WE}	Write Enable
\overline{CS}	Chip Select
\overline{OE}	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit	
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 to 4.6	V	
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5 to 4.6	V	
Power Dissipation	P _D	1.0	W	
Storage Temperature	T _{STG}	-65 to 150	°C	
Operating Temperature	Commercial	T _A	0 to 70	°C
	Industrial	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

K6R4008V1C-C/C-L, K6R4008V1C-I/C-P**CMOS SRAM****RECOMMENDED DC OPERATING CONDITIONS***($T_A=0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3***	V
Input Low Voltage	V _{IL}	-0.3**	-	0.8	V

* The above parameters are also guaranteed at industrial temperature range.

** V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.

*** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS*($T_A=0$ to 70°C , V_{CC}=3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit		
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-2	2	μA		
Output Leakage Current	I _{LO}	$\overline{\text{CS}}=\text{V}_{\text{IH}}$ or $\overline{\text{OE}}=\text{V}_{\text{IH}}$ or $\overline{\text{WE}}=\text{V}_{\text{IL}}$ V _{OUT} =V _{SS} to V _{CC}	-2	2	μA		
Operating Current	I _{CC}	Min. Cycle, 100% Duty $\overline{\text{CS}}=\text{V}_{\text{IL}}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	Com.	10ns	-	155	mA
				12ns	-	145	
				15ns	-	135	
			Ind.	10ns	-	170	
				12ns	-	160	
				15ns	-	150	
Standby Current	I _{SB}	Min. Cycle, $\overline{\text{CS}}=\text{V}_{\text{IH}}$	Normal	-	60	mA	
				I _{SB1}	f=0MHz, $\overline{\text{CS}}\geq\text{V}_{\text{CC}}-0.2\text{V}$, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V		-
			L-Ver.	-	1.2		
Output Low Voltage Level	V _{OL}	I _{OL} =8mA	-	0.4	V		
Output High Voltage Level	V _{OH}	I _{OH} =-4mA	2.4	-	V		

* The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*($T_A=25^\circ\text{C}$, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	7	pF

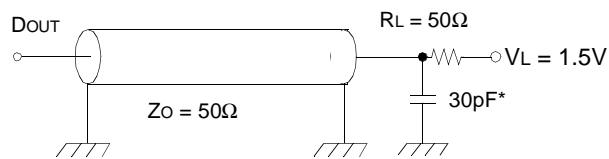
* Capacitance is sampled and not 100% tested.

K6R4008V1C-C/C-L, K6R4008V1C-I/C-P**CMOS SRAM****AC CHARACTERISTICS**($T_A=0$ to 70°C , $V_{CC}=3.3\pm 0.3\text{V}$, unless otherwise noted.)**TEST CONDITIONS***

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

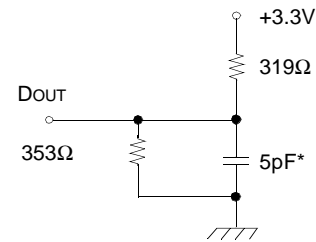
*The above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE*

Parameter	Symbol	K6R4008V1C-10		K6R4008V1C-12		K6R4008V1C-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	10	-	12	-	15	-	ns
Address Access Time	t _{AA}	-	10	-	12	-	15	ns
Chip Select to Output	t _{CO}	-	10	-	12	-	15	ns
Output Enable to Valid Output	t _{OE}	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	t _{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t _{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t _{HZ}	0	5	0	6	0	7	ns
Output Disable to High-Z Output	t _{OHZ}	0	5	0	6	0	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t _{PU}	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t _{PD}	-	10	-	12	-	15	ns

* The above parameters are also guaranteed at industrial temperature range.

K6R4008V1C-C/C-L, K6R4008V1C-I/C-P

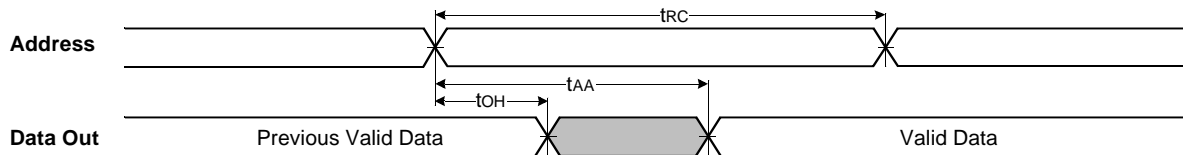
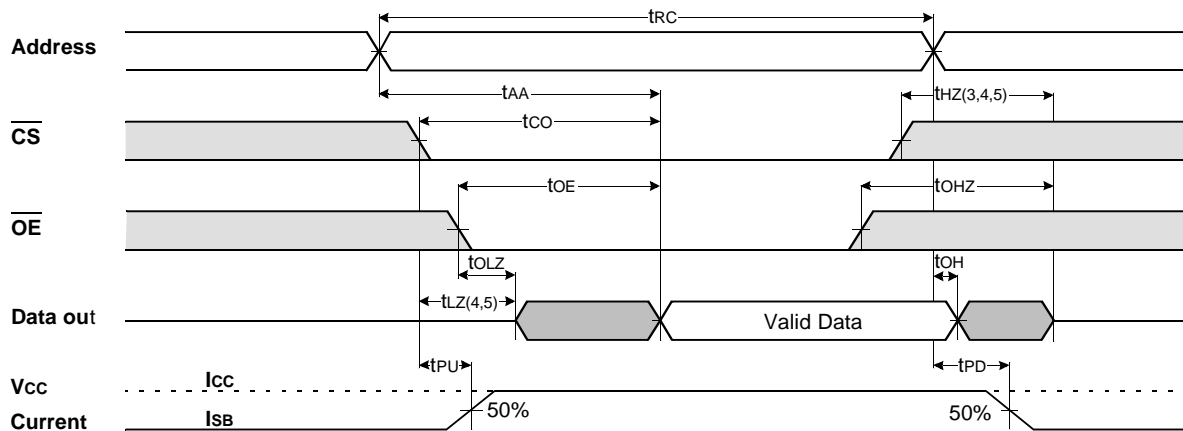
CMOS SRAM

WRITE CYCLE*

Parameter	Symbol	K6R4008V1C-10		K6R4008V1C-12		K6R4008V1C-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	10	-	12	-	15	-	ns
Chip Select to End of Write	tcw	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	7	-	8	-	10	-	ns
Write Pulse Width(\overline{OE} High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width(\overline{OE} Low)	tWP1	10	-	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	5	0	6	0	7	ns
Data to Write Time Overlap	tdw	5	-	6	-	7	-	ns
Data Hold from Write Time	tdH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tow	3	-	3	-	3	-	ns

* The above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)

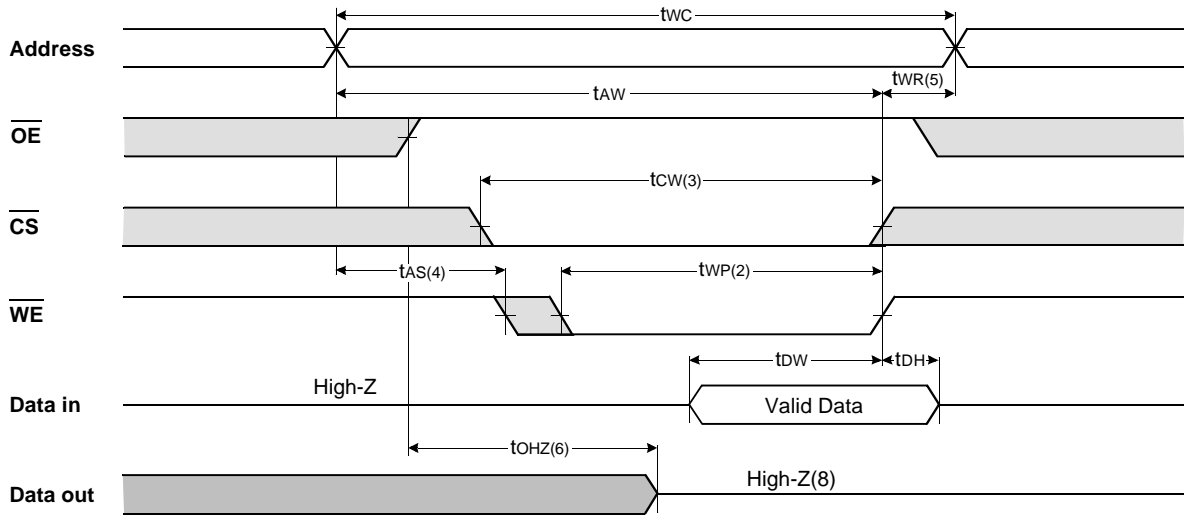
NOTES(WRITE CYCLE)

- \overline{WE} is high for read cycle.
- All read cycle timing is referenced from the last valid address to the first transition address.
- tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
- At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device.
- Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- Device is continuously selected with $\overline{CS}=V_{IL}$.
- Address valid prior to coincident with \overline{CS} transition low.
- For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

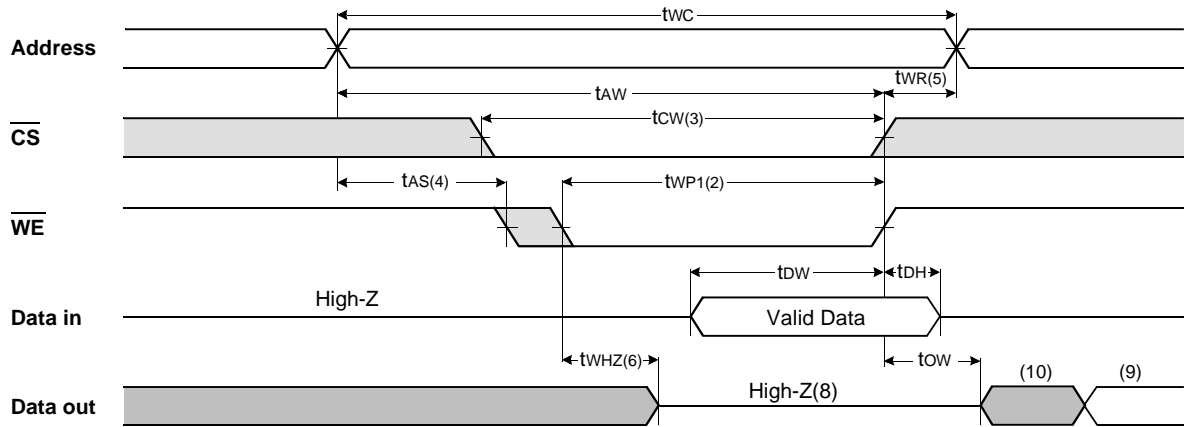
K6R4008V1C-C/C-L, K6R4008V1C-I/C-P

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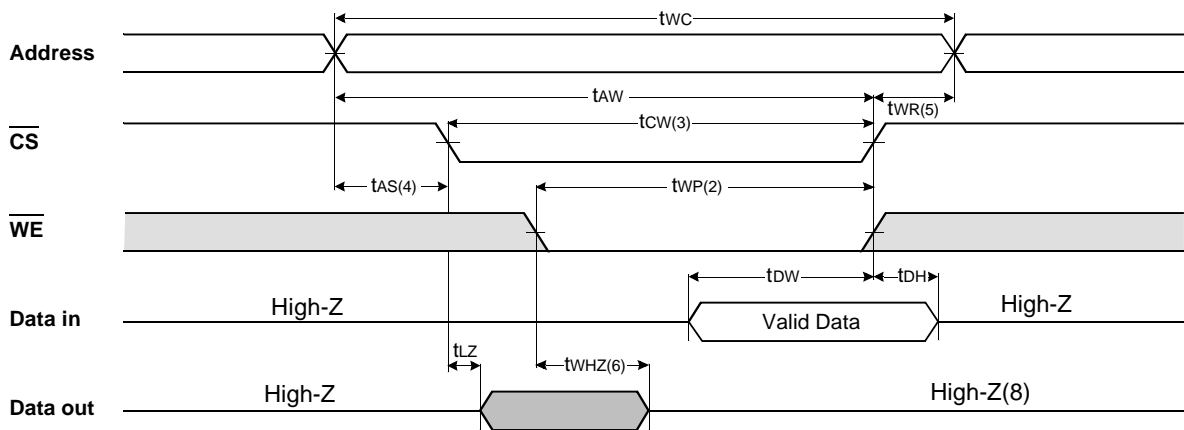
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{OE} = Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{OE} =Low Fixed)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{CS} = Controlled)



K6R4008V1C-C/C-L, K6R4008V1C-I/C-P

CMOS SRAM

NOTES(WRITE CYCLE)

- All write cycle timing is referenced from the last valid address to the first transition address.
- A write occurs during the overlap of a low CS and WE. A write begins at the latest transition CS going low and WE going low ; A write ends at the earliest transition CS going high or WE going high. t_{w} is measured from the beginning of write to the end of write.
- t_{cw} is measured from the later of CS going low to end of write.
- t_{as} is measured from the address valid to the beginning of write.
- t_{wr} is measured from the end of write to the address change. t_{wr} applied in case a write ends as CS or WE going high.
- If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
- Dout is the read data of the new address.
- When CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

CS	WE	OE	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	ISB, ISB1
L	H	H	Output Disable	High-Z	I _{cc}
L	H	L	Read	DOUT	I _{cc}
L	L	X	Write	DIN	I _{cc}

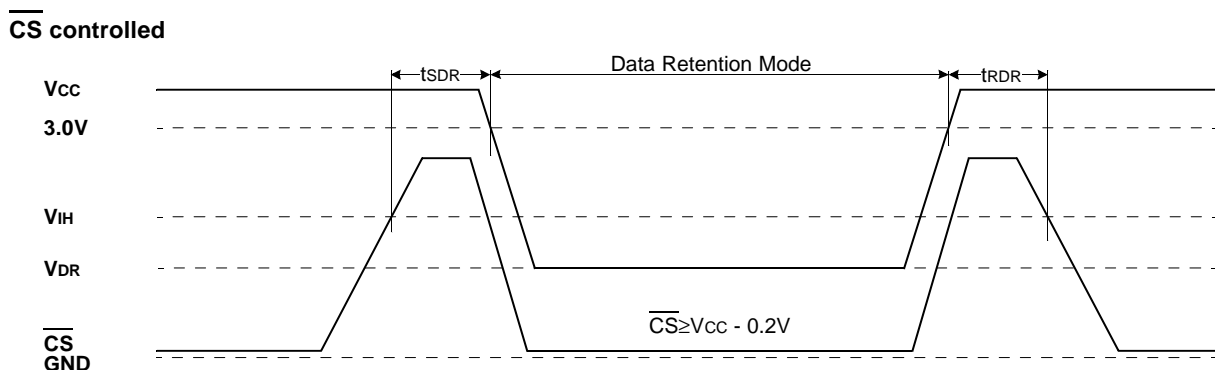
* X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A=0 to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V _{cc} for Data Retention	VDR	$\overline{CS} \geq V_{cc} - 0.2V$	2.0	-	3.6	V
Data Retention Current	I _{DR}	$V_{cc}=3.0V, \overline{CS} \geq V_{cc} - 0.2V$ $V_{IN} \geq V_{cc} - 0.2V$ or $V_{IN} \leq 0.2V$	-	-	1.0	mA
		$V_{cc}=2.0V, \overline{CS} \geq V_{cc} - 0.2V$ $V_{IN} \geq V_{cc} - 0.2V$ or $V_{IN} \leq 0.2V$	-	-	0.7	
Data Retention Set-Up Time	t _{SDR}	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	t _{RDR}		5	-	-	ms

* The above parameters are also guaranteed at industrial temperature range.
Data Retention Characteristic is for L-ver only.

DATA RETENTION WAVE FORM



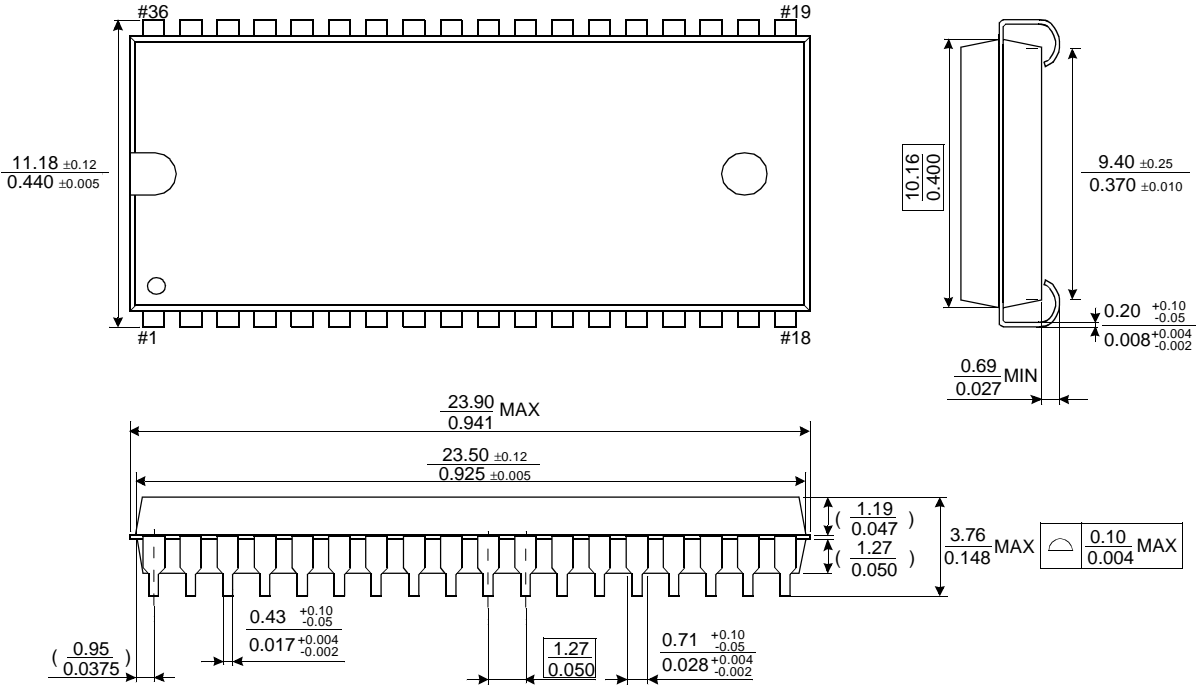
K6R4008V1C-C/C-L, K6R4008V1C-I/C-P

CMOS SRAM

PACKAGE DIMENSIONS

Units: millimeters/Inches

36-SOJ-400



44-TSOP2-400BF

Units: millimeters/Inches

