

Document Title**256Kx8 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	April 27, 1998	Preliminary

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K6T2008S2A Family

256Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 256Kx8
- Power Supply Voltage: 2.3 ~ 2.7V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-TSOP1-0813.4F,
48(36)-FBGA-6.00x7.00

GENERAL DESCRIPTION

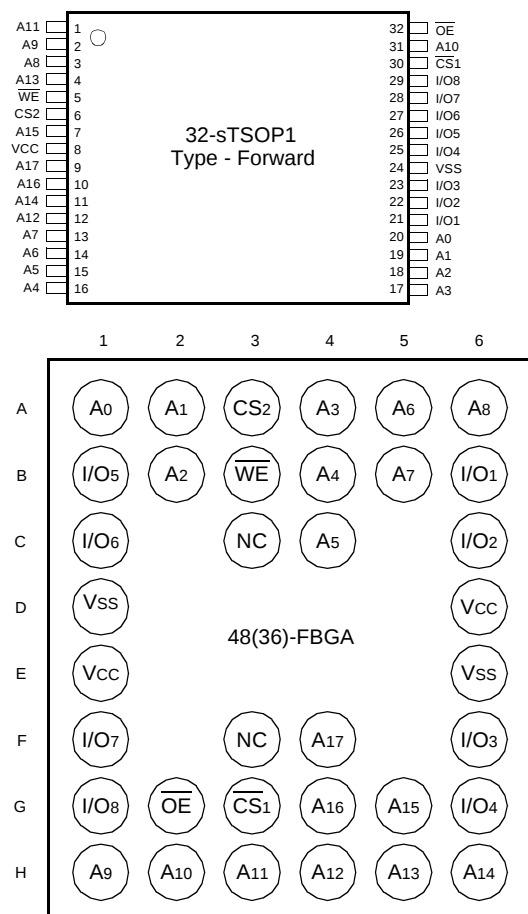
The K6T2008S2A families are fabricated by SAMSUNG's advanced CMOS process technology. The families support industrial temperature ranges and have small package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

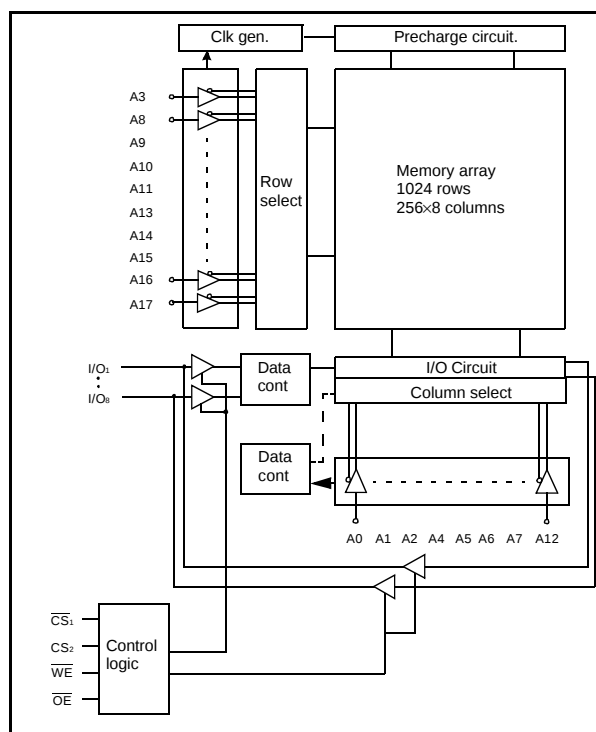
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
K6T2008S2A-F	Industrial(-40~85°C)	2.3~2.7V	85 ¹⁾ /100ns	10μA	15mA	32-TSOP1-0813.4F 48(36)-FBGA

1. The parameter is tested with 30pF test load.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
CS1, CS2	Chip Select Inputs	I/O1~I/O8	Data Inputs/Outputs
OE	Output Enable Input	Vcc	Power
WE	Write Enable Input	Vss	Ground
A0~A17	Address Inputs	N.C.	No Connection

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K6T2008S2A Family**Preliminary
CMOS SRAM****PRODUCT LIST**

Industrial Temperature Products(-40~85°C)	
Part Name	Function
K6T2008S2A-YF85 K6T2008S2A-YF10	32-sTSOP1 F, 85ns, 2.5V, LL 32-sTSOP1 F, 100ns, 2.5V, LL
K6T2008S2A-FF85 K6T2008S2A-FF10	48(36)-FBGA, 85ns, 2.5V, LL 48(36)-FBGA, 100ns, 2.5V, LL

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to 3.0V	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 3.6V	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-55 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.3	2.5	2.7	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.0	-	V _{CC} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.6	V

Note:

1. Industrial Product: T_A=-40 to 85°C, otherwise specified
2. Overshoot: V_{CC} + 1.0 V in case of pulse width ≤ 20ns
3. Undershoot: -1.0 V in case of pulse width ≤ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾(f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

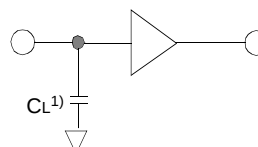
Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS_1}$ =V _{IH} or CS ₂ =V _{IL} or $\overline{OE}$ =V _{IH} or $\overline{WE}$ =V _{IL} , V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS_1}$ =V _{IL} , CS ₂ =V _{IH} , $\overline{WE}$ =V _{IH} , V _{IN} =V _{IH} or V _{IL}	-	-	1	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS_1}$ ≤0.2V, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	2	mA
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS_1}$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL}	-	-	15	mA
Output low voltage	V _{OL}	I _{OL} =0.5mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-0.5mA	2.0	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS_1}$ =V _{IH} , CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL}	-	-	0.3	mA
Standby Current(CMOS)	I _{SB1}	$\overline{CS_1}$ ≥V _{CC} -0.2V, CS ₂ ≥V _{CC} -0.2V or CS ₂ ≤0.2V, Other inputs=0~V _{CC}	-	-	10	μA

AC OPERATING CONDITIONS**TEST CONDITIONS**(Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V

Input rising and falling time : 5ns

Input and output reference voltage :1.1V

Output load(see right) : $C_L=100\text{pF}+1\text{TTL}$ $C_L=30\text{pF}+1\text{TTL}$ 

1. Including scope and jig capacitance

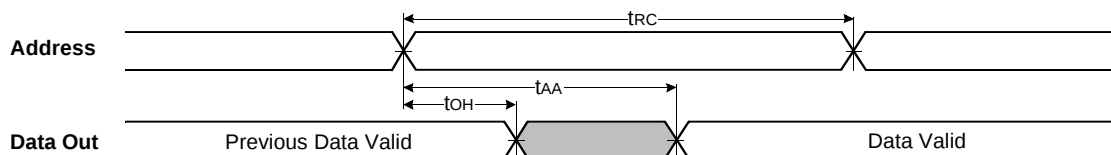
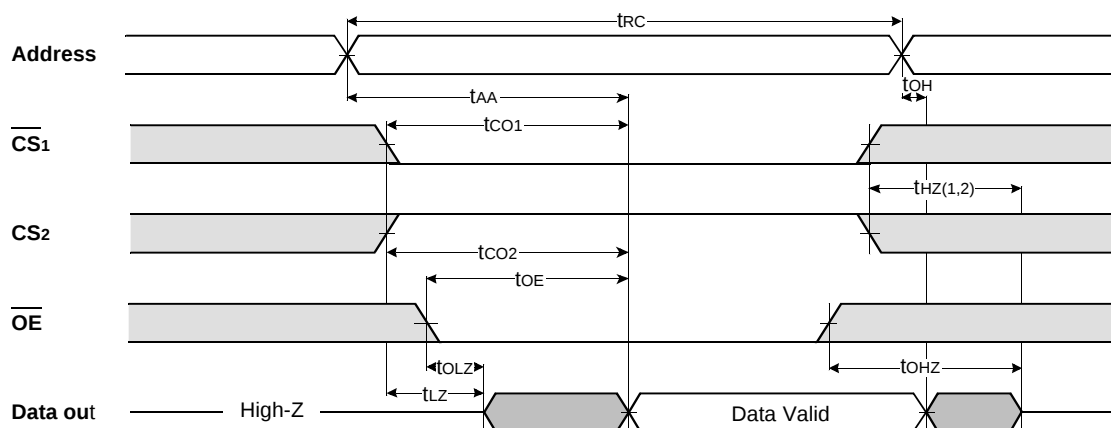
AC CHARACTERISTICS($V_{CC}=2.3\sim 2.7\text{V}$, $T_A=-40$ to 85°C)

Parameter List		Symbol	Speed Bins				Units
			85ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	85	-	100	-	ns
	Address access time	t _{AA}	-	85	-	100	ns
	Chip select to output	t _{CO1} , t _{CO2}	-	85	-	100	ns
	Output enable to valid output	t _{OE}	-	40	-	50	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	25	0	30	ns
	Output disable to high-Z output	t _{OHZ}	0	25	0	30	ns
	Output hold from address change	t _{OH}	10	-	15	-	ns
Write	Write cycle time	t _{WC}	85	-	100	-	ns
	Chip select to end of write	t _{CW}	70	-	80	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	70	-	80	-	ns
	Write pulse width	t _{WP}	55	-	70	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	30	ns
	Data to write time overlap	t _{DW}	35	-	40	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	ns

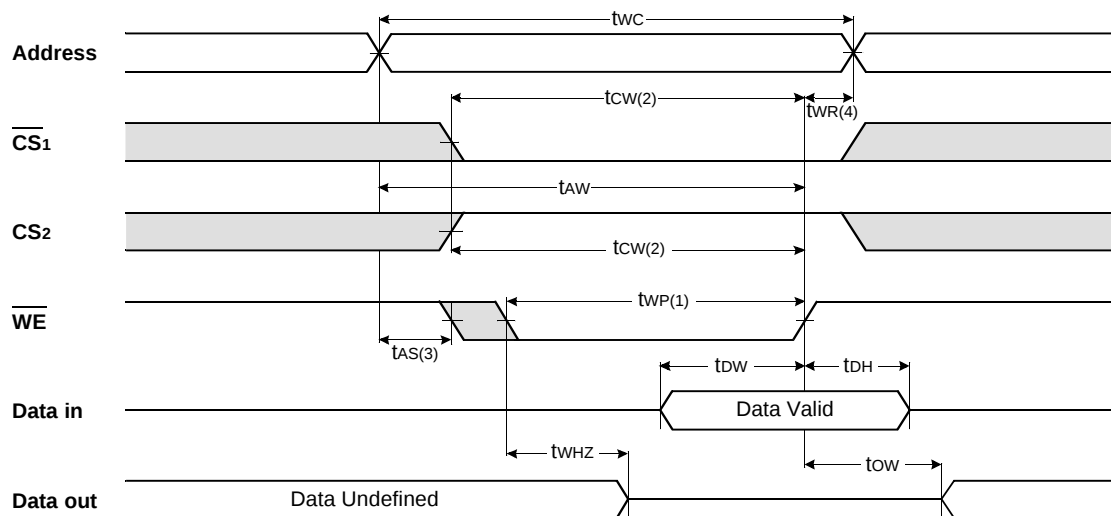
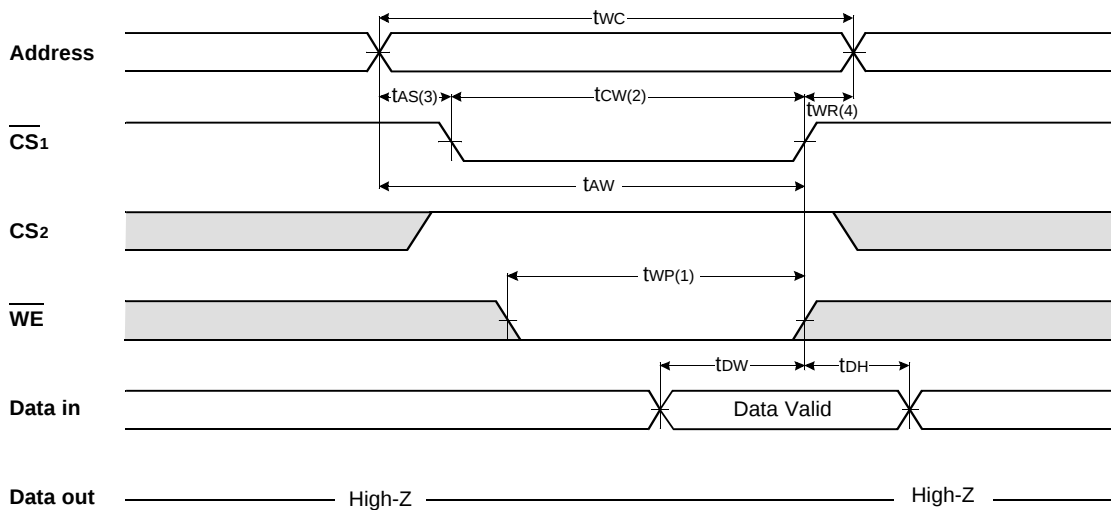
DATA RETENTION CHARACTERISTICS

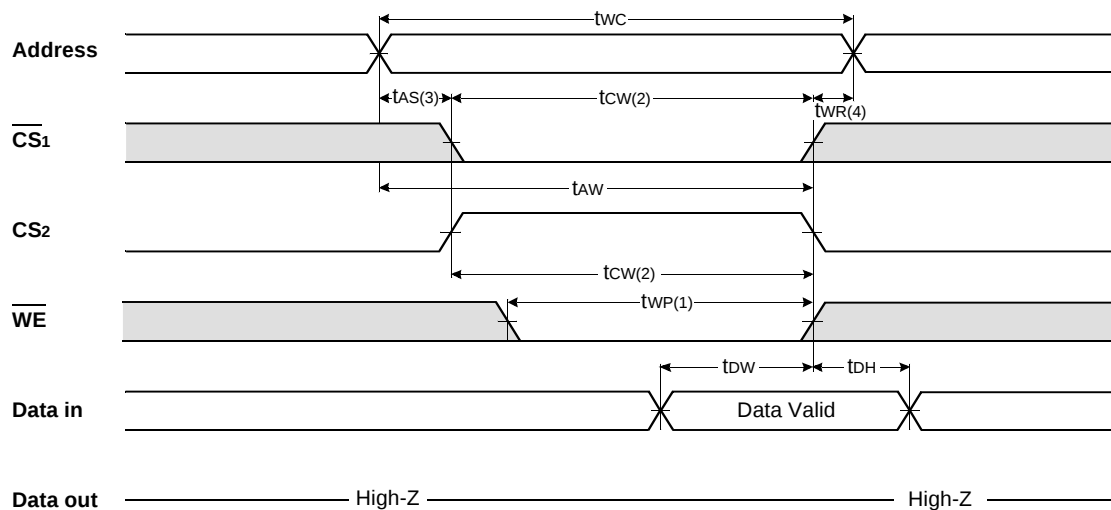
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{(1)}$	2.0	-	2.7	V
Data retention current	I _{DR}	$V_{CC}=2.5\text{V}$, $\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{(1)}$	-	-	10	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

1. $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$, $\overline{CS}_2 \geq V_{CC}-0.2\text{V}$ ($\overline{CS}_1$ controlled) or $\overline{CS}_2 \leq 0.2\text{V}$ ($\overline{CS}_2$ controlled)

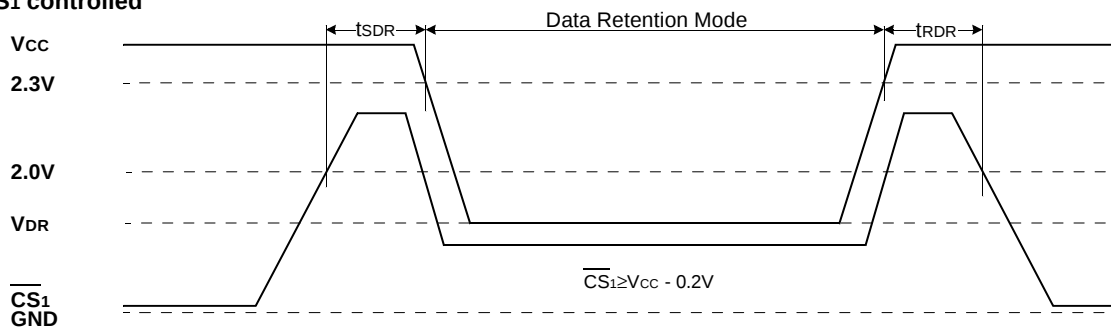
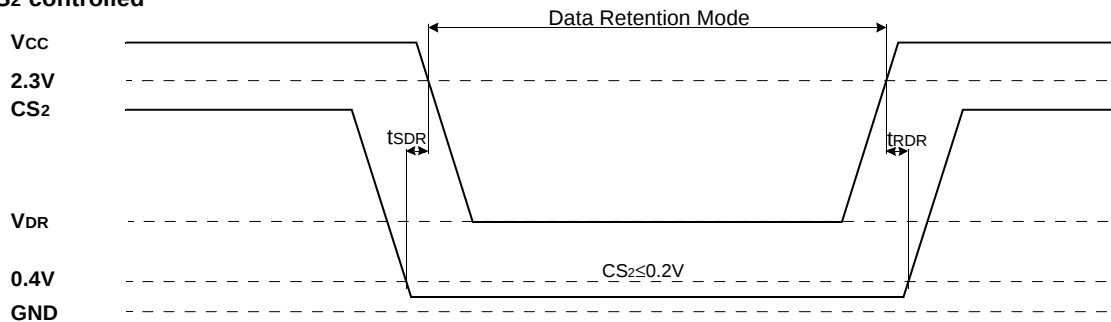
TIMMING DIAGRAMS**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)**TIMING WAVEFORM OF READ CYCLE(2)** ($\overline{WE}=V_{IH}$)**NOTES (READ CYCLE)**

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{\text{WE}}$ Controlled)**TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{CS1}}$ Controlled)**

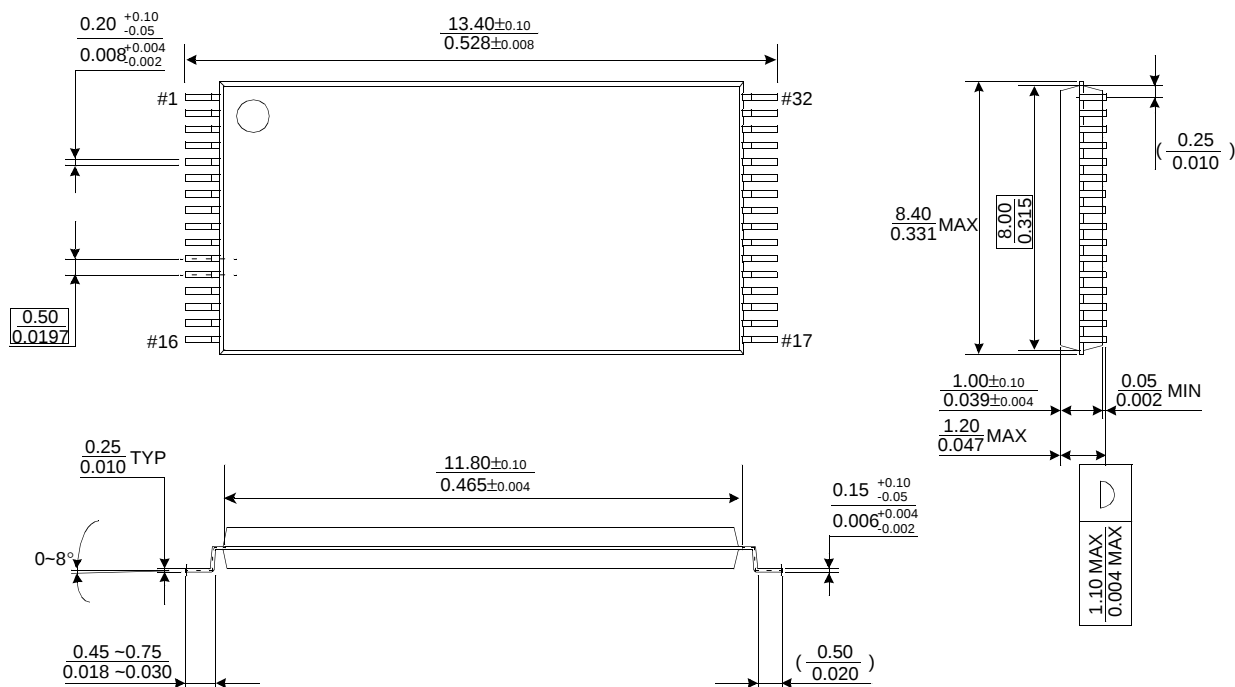
TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)**NOTES (WRITE CYCLE)**

1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS₂ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS₂ going high and WE going low : A write end at the earliest transition among CS₁ going high, CS₂ going low and WE going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the CS₁ going low or CS₂ going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high t_{WR2} applied in case a write ends as CS₂ going to low.

DATA RETENTION WAVE FORM**CS₁ controlled****CS₂ controlled**

K6T2008S2A Family**Preliminary**
CMOS SRAM**PACKAGE DIMENSIONS**

Units: millimeters(inches)

32 PIN SMALLER THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)

PACKAGE DIMENSIONS

Units: millimeters

