

Document Title

128Kx36 & 128Kx32-Bit Synchronous Pipelined Burst SRAM

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	1. Initial draft	May. 15. 2001	Preliminary
0.1	1. Changed DC parameters Icc ; from 350mA to 290mA at -16, from 330mA to 270mA at -15, from 300mA to 250mA at -14, ISB1 ; from 100mA to 80mA	June. 12. 2001	Preliminary
0.2	1 Delete Pass-Through	June. 25. 2001	Preliminary
0.3	1. Add x32 org and industrial temperature	Agu. 11. 2001	Preliminary

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4Mb SB/SPB Synchronous SRAM Ordering Information

Org.	Part Number	Mode	VDD	Speed FT ; Access Time(ns) Pipelined ; Cycle Time(MHz)	PKG	Temp
256Kx18	K7B401825B-QC(I)65/75/80	SB	3.3	6.5/7.5/8.0 ns	Q (100TQFP)	C (Commercial Temperature Range) I: (Industrial Temperature Range)
	K7A401800B-QC(I)16/14	SPB(2E1D)	3.3	167/138 MHz		
	K7A401809B-QC(I)30/27/25/22/20	SPB(2E1D)	3.3	300/275/250/225/200 MHz		
128Kx32	K7B403225B-QC(I)65/75/80	SB	3.3	6.5/7.5/8.0 ns		
	K7A403200B-QC(I)16/14	SPB(2E1D)	3.3	167/138 MHz		
	K7A403209B-QC(I)30/27/25/22/20	SPB(2E1D)	3.3	300/275/250/225/200 MHz		
	K7A403201B-QC(I)16/14	SPB(2E2D)	3.3	167/138/ MHz		
128Kx36	K7B403625B-QC(I)65/75/80	SB	3.3	6.5/7.5/8.0 ns		
	K7A403600B-QC(I)16/14	SPB(2E1D)	3.3	167/138 MHz		
	K7A403609B-QC(I)30/27/25/22/20	SPB(2E1D)	3.3	300/275/250/225/200 MHz		
	K7A403601B-QC(I)16/14	SPB(2E2D)	3.3	167/138 MHz		

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FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- $V_{DD} = 3.3V + 0.3V / -0.165V$ Power Supply.
- V_{DDQ} Supply Voltage $3.3V + 0.3V / -0.165V$ for 3.3V I/O or $2.5V + 0.4V / -0.125V$ for 2.5V I/O
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- \overline{LBO} Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2cycle Enable, 2cycle Disable.
- Asynchronous Output Enable Control.
- \overline{ADSP} , \overline{ADSC} , \overline{ADV} Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A
- Operating in commercial and industrial temperature range.

FAST ACCESS TIMES

PARAMETER	Symbol	-16	-14	Unit
Cycle Time	t _{CYC}	6.0	7.2	ns
Clock Access Time	t _{CD}	3.5	4.0	ns
Output Enable Access Time	t _{OE}	3.5	4.0	ns

GENERAL DESCRIPTION

The K7A403601B and K7A403201B are a 4,718,592-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 128K words of 36bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; \overline{GW} , \overline{BW} , \overline{LBO} , ZZ. Write cycles are internally self-timed and synchronous.

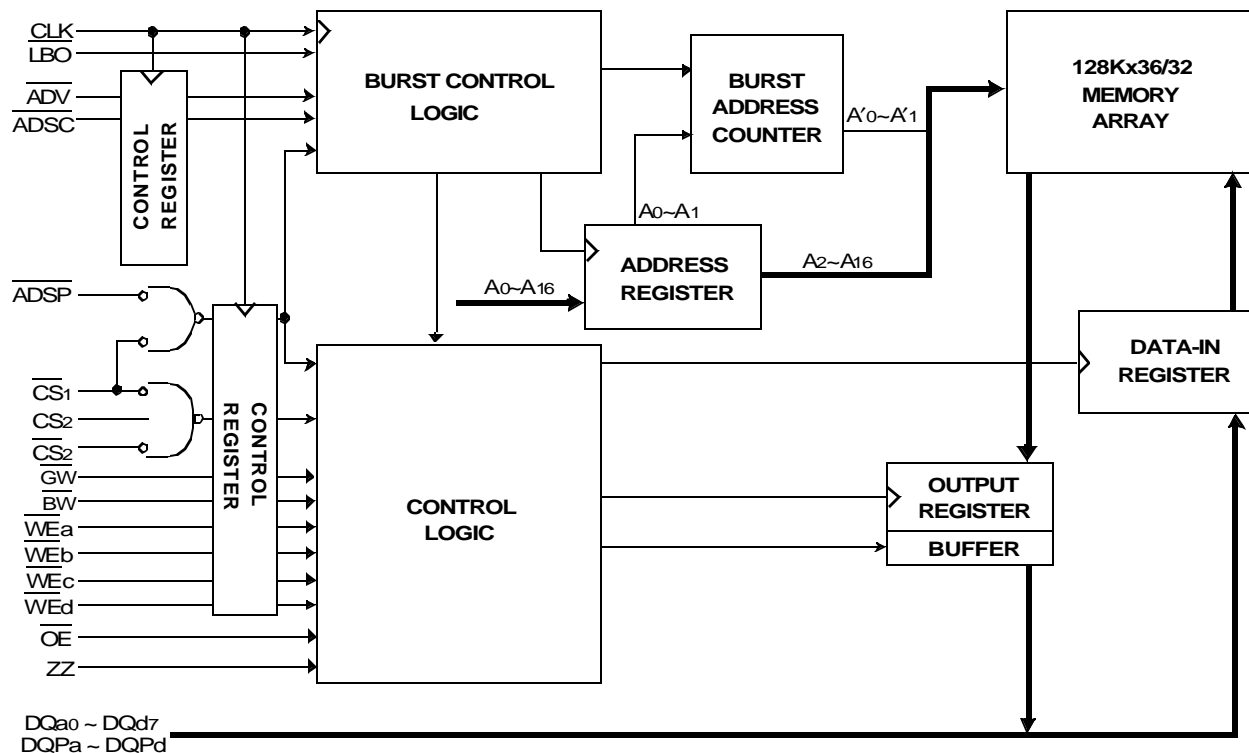
Full bus-width write is done by \overline{GW} , and each byte write is performed by the combination of \overline{WEx} and \overline{BW} when \overline{GW} is high. And with $\overline{CS1}$ high, \overline{ADSP} is blocked to control signals. Burst cycle can be initiated with either the address status processor(\overline{ADSP}) or address status cache controller(\overline{ADSC}) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(\overline{ADV}) input.

\overline{LBO} pin is DC operated and determines burst sequence(linear or interleaved).

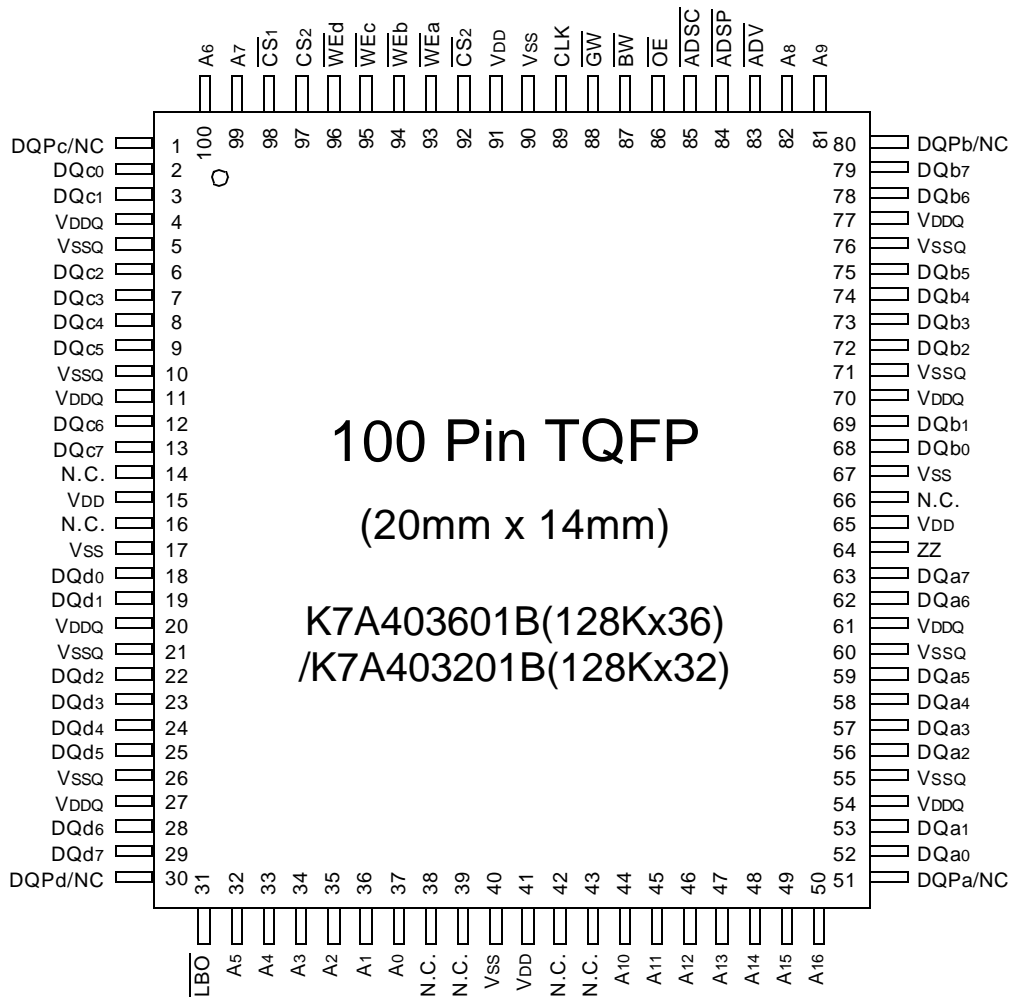
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7A403601B and K7A403201B are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A16	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,50,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	14,16,38,39,42,43,66
$\overline{\text{ADV}}$	Burst Address Advance	83	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{\text{ADSP}}$	Address Status Processor	84	DQb0~b7		68,69,72,73,74,75,78,79
$\overline{\text{ADSC}}$	Address Status Controller	85	DQc0~c7		2,3,6,7,8,9,12,13
CLK	Clock	89	DQd0~d7		18,19,22,23,24,25,28,29
$\overline{\text{CS}}_1$	Chip Select	98	DQPa~Pd		51,80,1,30
$\overline{\text{CS}}_2$	Chip Select	97	/NC		
$\overline{\text{CS}}_2$	Chip Select	92	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
$\overline{\text{WE}}_x$	Byte Write Inputs	93,94,95,96	VSSQ	Output Ground	5,10,21,26,55,60,71,76
OE	Output Enable	86			
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

FUNCTION DESCRIPTION

The K7A4036/3201B are synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of \overline{OE} , \overline{LBO} and \overline{ZZ}) are sampled on rising clock edges. The start and duration of the burst access is controlled by \overline{ADSC} , \overline{ADSP} and \overline{ADV} and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with \overline{ADV} .

When \overline{ZZ} is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When \overline{ZZ} returns to low, the SRAM normally operates after 2cycles of wake up time. \overline{ZZ} pin is pulled down internally.

Read cycles are initiated with \overline{ADSP} (regardless of \overline{WEx} and \overline{ADSC})using the new external address clocked into the on-chip address register whenever \overline{ADSP} is sampled low, the chip selects are sampled active, and the output buffer is enabled with \overline{OE} . In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of \overline{CLK} , are carried to the Data-out buffer by the next positive edge of \overline{CLK} . The data, registered in the Data-out buffer, are projected to the output pins. \overline{ADV} is ignored on the clock edge that samples \overline{ADSP} asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when \overline{WEx} are sampled High and \overline{ADV} is sampled low. And \overline{ADSP} is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by \overline{GW} (regardless of \overline{BW} and \overline{WEx}), and each byte write is performed by the combination of \overline{BW} and \overline{WEx} when \overline{GW} is high.

Write cycles are performed by disabling the output buffers with \overline{OE} and asserting \overline{WEx} . \overline{WEx} are ignored on the clock edge that samples \overline{ADSP} low, but are sampled on the subsequent clock edges. The output buffers are disabled when \overline{WEx} are sampled Low(regardless of \overline{OE}). Data is clocked into the data input register when \overline{WEx} sampled Low. The address increases internally to the next address of burst, if both \overline{WEx} and \overline{ADV} are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals(\overline{WEa} , \overline{WEb} , \overline{WEc} or \overline{WEd}) sampled low. The \overline{WEa} control $\overline{DQa0} \sim \overline{DQa7}$ and \overline{DQPd} , \overline{WEb} controls $\overline{DQb0} \sim \overline{DQb7}$ and \overline{DQPa} , \overline{WEc} controls $\overline{DQc0} \sim \overline{DQc7}$ and \overline{DQPc} , and \overline{WEd} control $\overline{DQd0} \sim \overline{DQd7}$ and \overline{DQPd} . Read or write cycle may also be initiated with \overline{ADSC} , instead of \overline{ADSP} . The differences between cycles initiated with \overline{ADSC} and \overline{ADSP} as are follows;

\overline{ADSP} must be sampled high when \overline{ADSC} is sampled low to initiate a cycle with \overline{ADSC} .
 \overline{WEx} are sampled on the same clock edge that sampled \overline{ADSC} low(and \overline{ADSP} high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the \overline{LBO} pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

\overline{LBO} PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

\overline{LBO} PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

Note : 1. \overline{LBO} pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

\overline{CS}_1	CS_2	\overline{CS}_2	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	\overline{WRITE}	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

- Notes :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.
 3. $\overline{WRITE} = L$ means Write operation in WRITE TRUTH TABLE.
 $\overline{WRITE} = H$ means Read operation in WRITE TRUTH TABLE.
 4. Operation finally depends on status of asynchronous input pins(ZZ and \overline{OE}).

WRITE TRUTH TABLE

\overline{GW}	\overline{BW}	\overline{WE}_a	\overline{WE}_b	\overline{WE}_c	\overline{WE}_d	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

- Notes :** 1. X means "Don't Care".
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

OPERATION	ZZ	\overline{OE}	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Voltage on VDD Supply Relative to VSS		VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to VSS		VDDQ	VDD	V
Voltage on Input Pin Relative to VSS		VIN	-0.3 to VDD+0.3	V
Voltage on I/O Pin Relative to VSS		VIO	-0.3 to VDDQ+0.3	V
Power Dissipation		PD	2.2	W
Storage Temperature		TSTG	-65 to 150	°C
Operating Temperature	Commercial	TOPR	0 to 70	°C
	Industrial	TOPR	-40 to 85	°C
Storage Temperature Range Under Bias		TBIAS	-10 to 85	°C

*Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.6	V
	VDDQ	3.135	3.3	3.6	V
Ground	VSS	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O (0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.6	V
	VDDQ	2.375	2.5	2.9	V
Ground	VSS	0	0	0	V

CAPACITANCE*(TA=25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	COUT	VOUT=0V	-	7	pF

*NOTE: Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS($T_A=0$ to 70°C , $V_{DD}=3.3\text{V}+0.3\text{V}/-0.165\text{V}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	
Input Leakage Current(except ZZ)	IIL	$V_{DD} = \text{Max}$; $V_{IN}=V_{SS}$ to V_{DD}	-2	+2	μA	
Output Leakage Current	IOL	Output Disabled, $V_{OUT}=V_{SS}$ to V_{DDQ}	-2	+2	μA	
Operating Current	ICC	Device Selected, $I_{OUT}=0\text{mA}$, $ZZ \leq V_{IL}$, All Inputs= V_{IL} or V_{IH}	-16	-	290	mA
			-14	-	250	
Standby Current	ISB	Device deselected, $I_{OUT}=0\text{mA}$, $ZZ \leq V_{IL}$, $f=\text{Max}$, All Inputs $\leq 0.2\text{V}$ or $\geq V_{DD}-0.2\text{V}$	-16	-	140	mA
			-14	-	120	
	ISB1	Device deselected, $I_{OUT}=0\text{mA}$, $ZZ \leq 0.2\text{V}$, $f = 0$, All Inputs=fixed ($V_{DD}-0.2\text{V}$ or 0.2V)	-	-	80	mA
	ISB2	Device deselected, $I_{OUT}=0\text{mA}$, $ZZ \geq V_{DD}-0.2\text{V}$, $f=\text{Max}$, All Inputs $\leq V_{IL}$ or $\geq V_{IH}$	-	-	50	mA
Output Low Voltage(3.3V I/O)	VOL	$I_{OL} = 8.0\text{mA}$	-	0.4	V	
Output High Voltage(3.3V I/O)	VOH	$I_{OH} = -4.0\text{mA}$	2.4	-	V	
Output Low Voltage(2.5V I/O)	VOL	$I_{OL} = 1.0\text{mA}$	-	0.4	V	
Output High Voltage(2.5V I/O)	VOH	$I_{OH} = -1.0\text{mA}$	2.0	-	V	
Input Low Voltage(3.3V I/O)	VIL		-0.5*	0.8	V	
Input High Voltage(3.3V I/O)	VIH		2.0	$V_{DD}+0.3^{**}$	V	
Input Low Voltage(2.5V I/O)	VIL		-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	VIH		1.7	$V_{DD}+0.3^{**}$	V	

* $V_{L}(\text{Min})=-2.0(\text{Pulse Width} \leq t_{CYC}/2)$

** $V_{H}(\text{Max})=4.6(\text{Pulse Width} \leq t_{CYC}/2)$

** In Case of I/O Pins, the Max. $V_{IH}=V_{DDQ}+0.3\text{V}$

TEST CONDITIONS

($V_{DD}=3.3\text{V}+0.3\text{V}/-0.165\text{V}$, $V_{DDQ}=3.3\text{V}+0.3\text{V}/-0.165\text{V}$ or $V_{DD}=3.3\text{V}+0.3\text{V}/-0.165\text{V}$, $V_{DDQ}=2.5\text{V}+0.4\text{V}/-0.125\text{V}$, $T_A=0$ to 70°C)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O)	1ns
Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O)	1ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	$V_{DDQ}/2$
Output Load	See Fig. 1

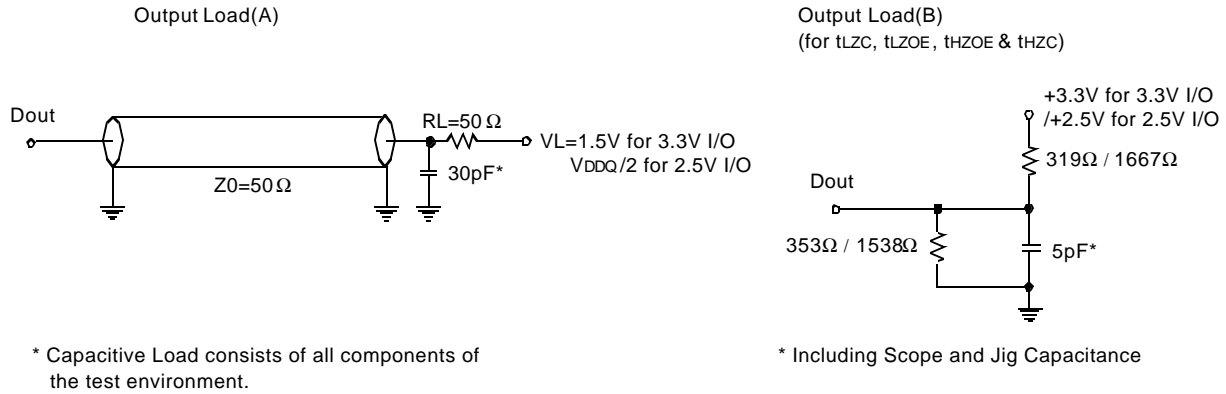


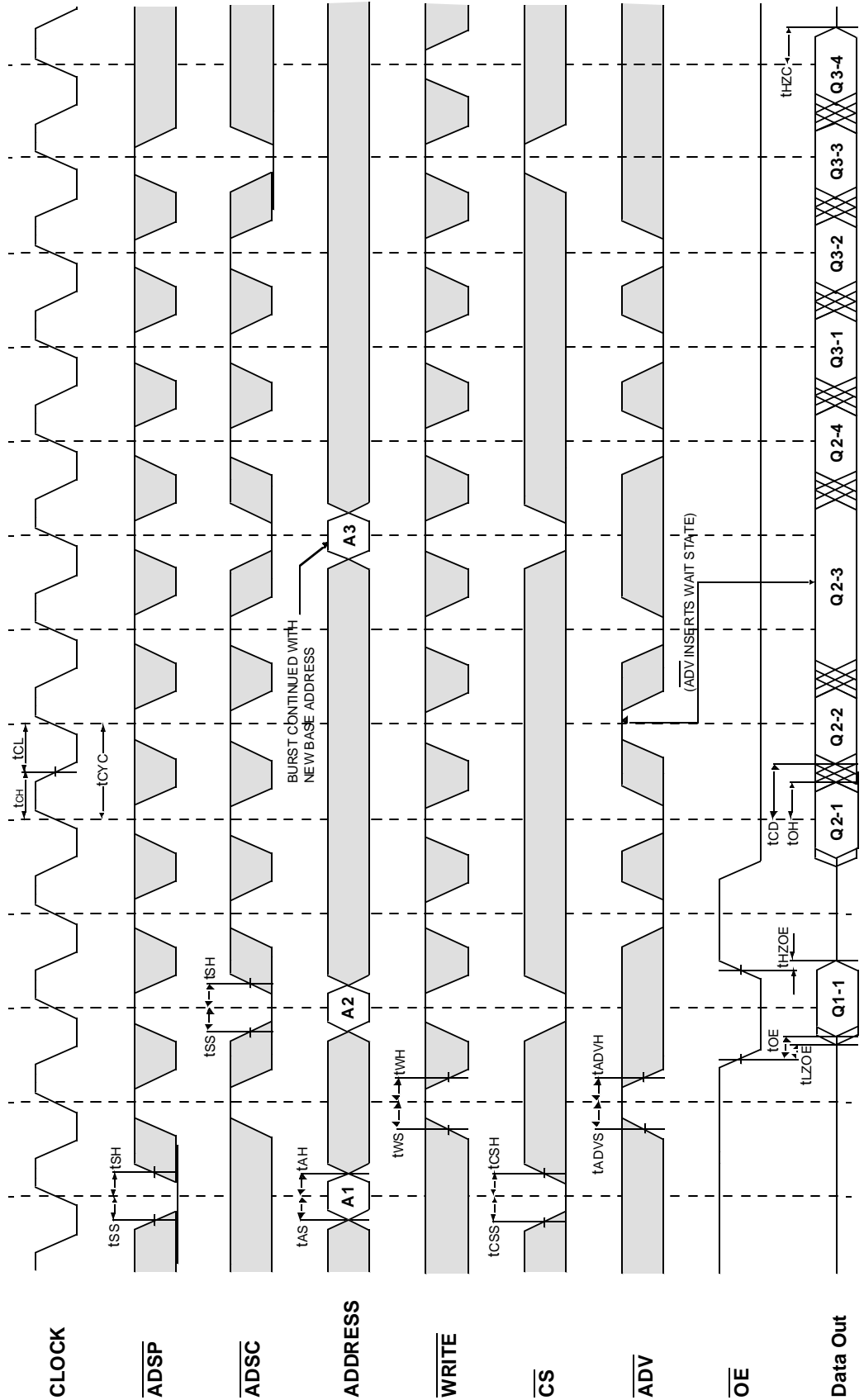
Fig. 1

AC TIMING CHARACTERISTICS($T_A=0$ to 70°C , $V_{DD}=3.3\text{V}+0.3\text{V}/-0.165\text{V}$)

Parameter	Symbol	-16		-14		Unit
		Min	Max	Min	Max	
Cycle Time	t _{CYC}	6.0	-	7.2	-	ns
Clock Access Time	t _{CD}	-	3.5	-	4.0	ns
Output Enable to Data Valid	t _{OE}	-	3.5	-	4.0	ns
Clock High to Output Low-Z	t _{TLZC}	0	-	0	-	ns
Output Hold from Clock High	t _{OH}	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	t _{tlZOE}	0	-	0	-	ns
Output Enable High to Output High-Z	t _{thZOE}	-	3.5	-	4.0	ns
Clock High to Output High-Z	t _{thZC}	1.5	3.5	1.5	4.0	ns
Clock High Pulse Width	t _{CH}	2.4	-	2.8	-	ns
Clock Low Pulse Width	t _{CL}	2.4	-	2.8	-	ns
Address Setup to Clock High	t _{AS}	1.5	-	1.5	-	ns
Address Status Setup to Clock High	t _{SS}	1.5	-	1.5	-	ns
Data Setup to Clock High	t _{DS}	1.5	-	1.5	-	ns
Write Setup to Clock High ($\overline{\text{GW}}$, $\overline{\text{BW}}$, $\overline{\text{WEx}}$)	t _{WS}	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	t _{ADVS}	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	t _{CSS}	1.5	-	1.5	-	ns
Address Hold from Clock High	t _{AH}	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t _{SH}	0.5	-	0.5	-	ns
Data Hold from Clock High	t _{DH}	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{\text{GW}}$, $\overline{\text{BW}}$, $\overline{\text{WEx}}$)	t _{WH}	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t _{ADVH}	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t _{CSh}	0.5	-	0.5	-	ns
ZZ High to Power Down	t _{PDs}	2	-	2	-	cycle
ZZ Low to Power Up	t _{PUS}	2	-	2	-	cycle

- Notes :**
1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{\text{ADSC}}$ and/or $\overline{\text{ADSP}}$ is sampled low and $\overline{\text{CS}}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
 2. Both chip selects must be active whenever $\overline{\text{ADSC}}$ or $\overline{\text{ADSP}}$ is sampled low in order for the this device to remain enabled.
 3. $\overline{\text{ADSC}}$ or $\overline{\text{ADSP}}$ must not be asserted for at least 2 Clock after leaving ZZ state.
 4. At any given voltage and temperature, t_{thZC} is less than t_{tlZC}

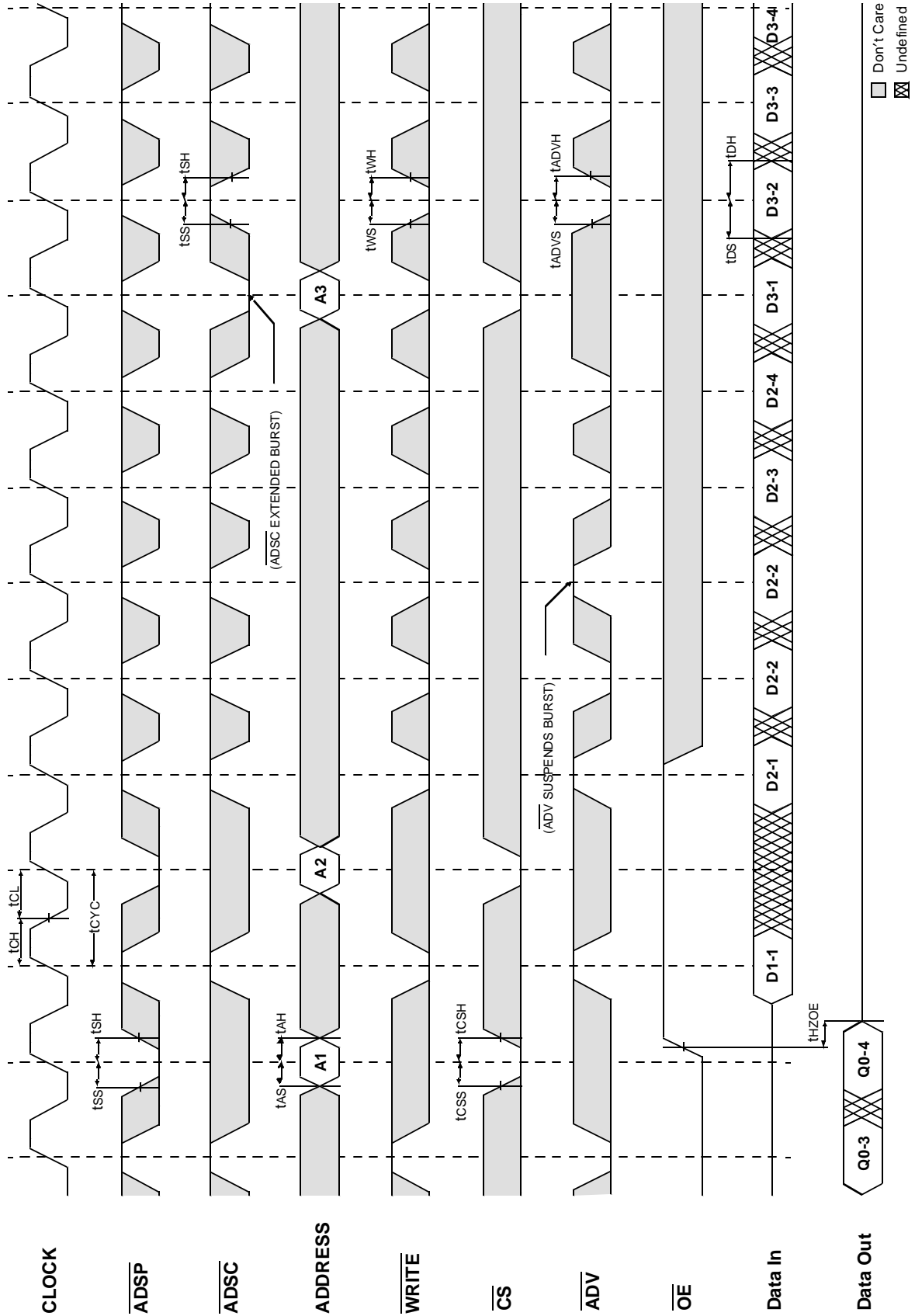
TIMING WAVEFORM OF READ CYCLE



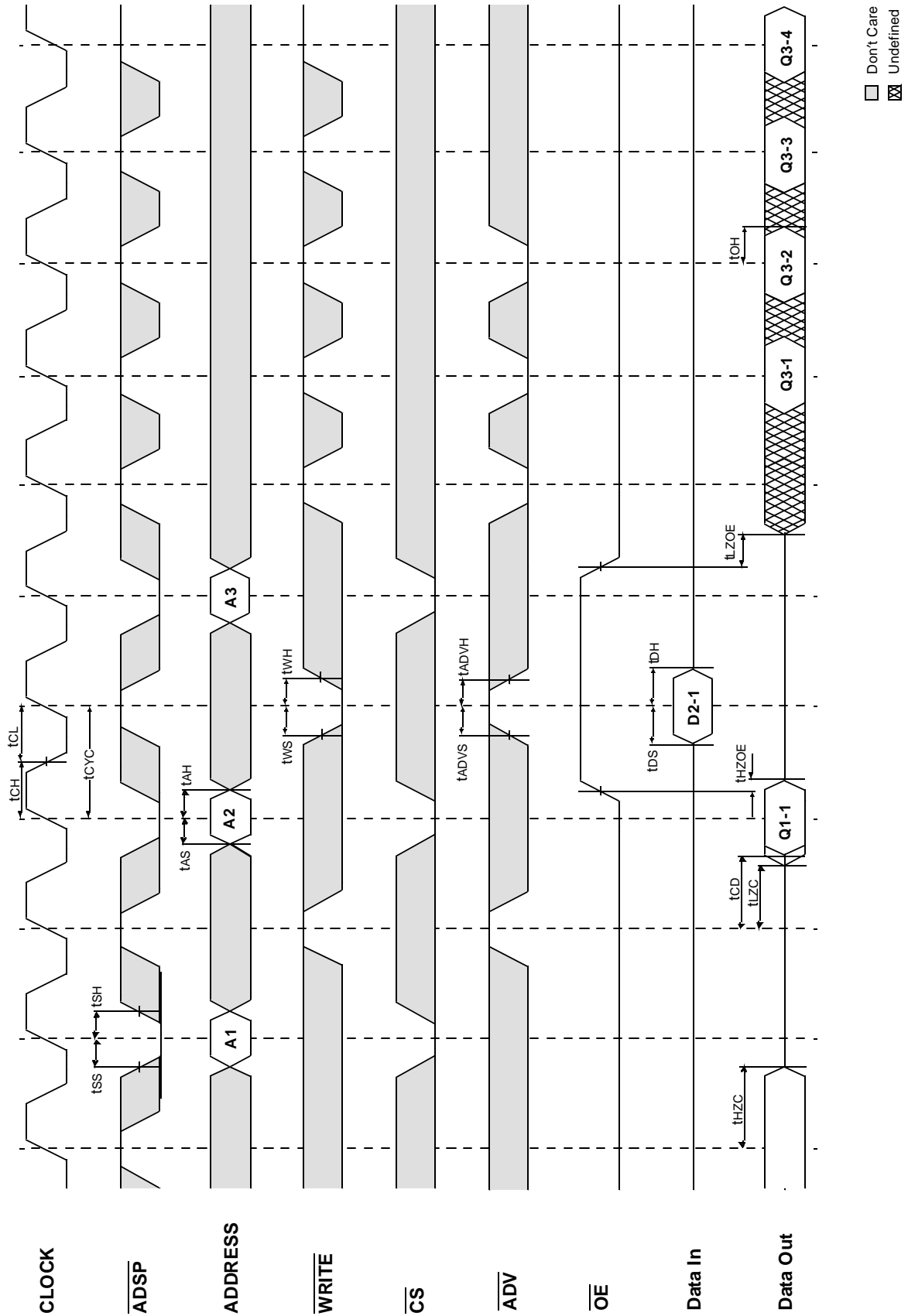
□ Don't Care
⊗ Undefined

NOTES : $\overline{WRITE} = L$ means $\overline{GW} = L$, or $\overline{GW} = H$, $\overline{BW} = L$, $\overline{WE} = L$
 $\overline{CS}_1 = L$ means $\overline{CS}_1 = L$, $\overline{CS}_2 = H$ and $\overline{CS}_2 = L$
 $\overline{CS} = H$ means $\overline{CS}_1 = H$, or $\overline{CS}_1 = L$ and $\overline{CS}_2 = H$, or $\overline{CS}_1 = L$, and $\overline{CS}_2 = L$

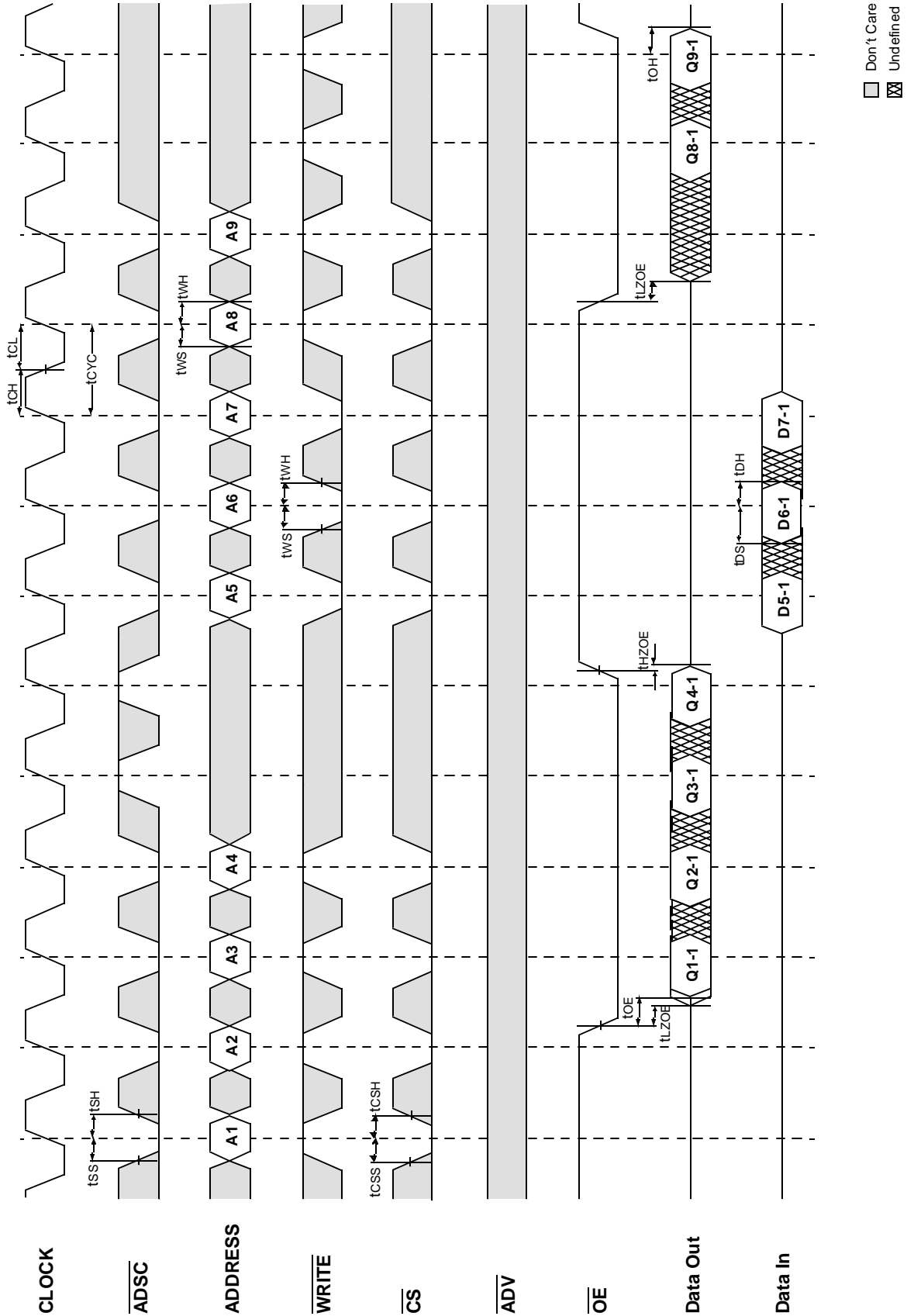
TIMING WAVEFORM OF WRTE CYCLE



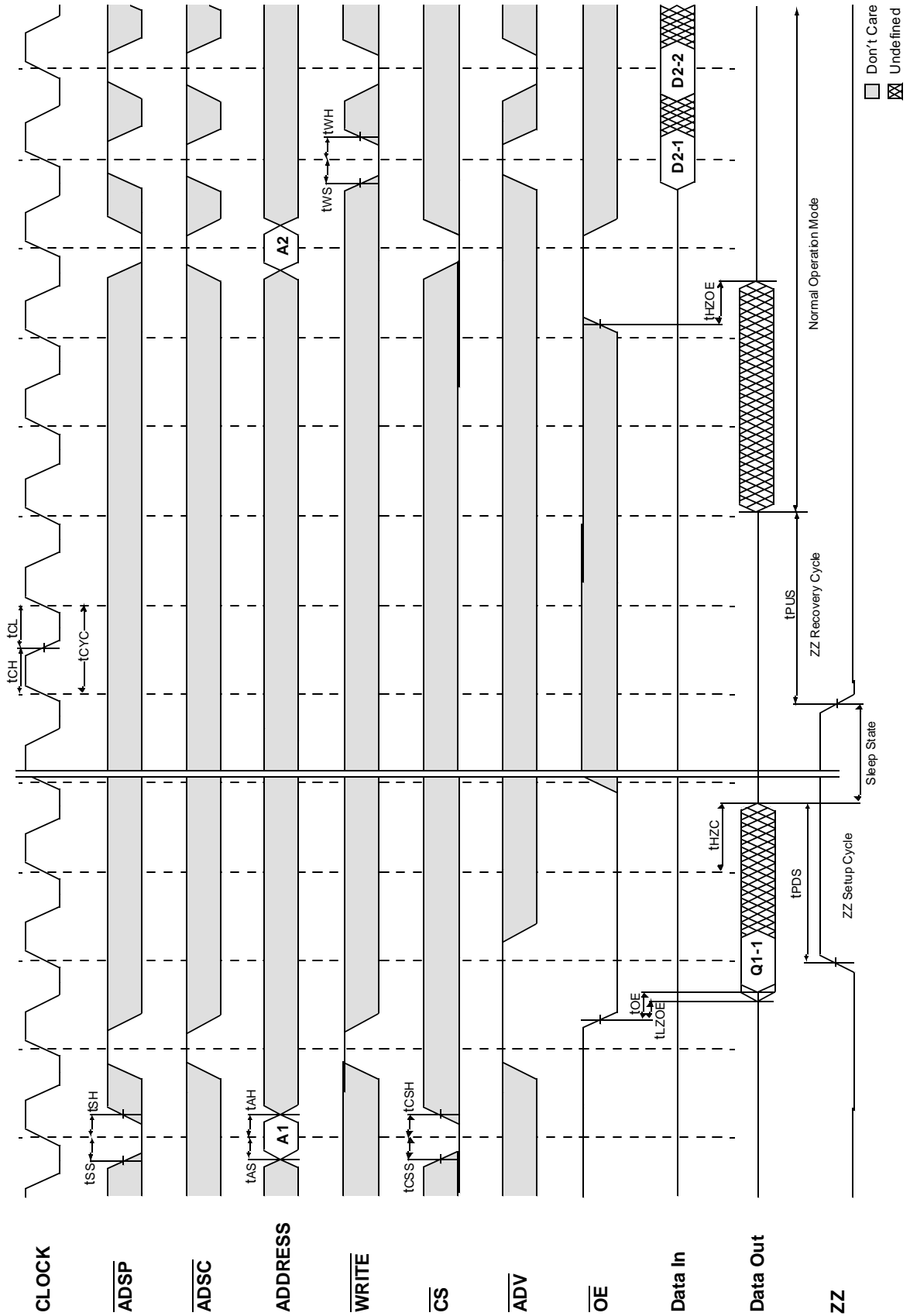
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED, $\overline{\text{ADSC}}=\text{HIGH}$)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED, $\overline{\text{ADSP}}=\text{HIGH}$)



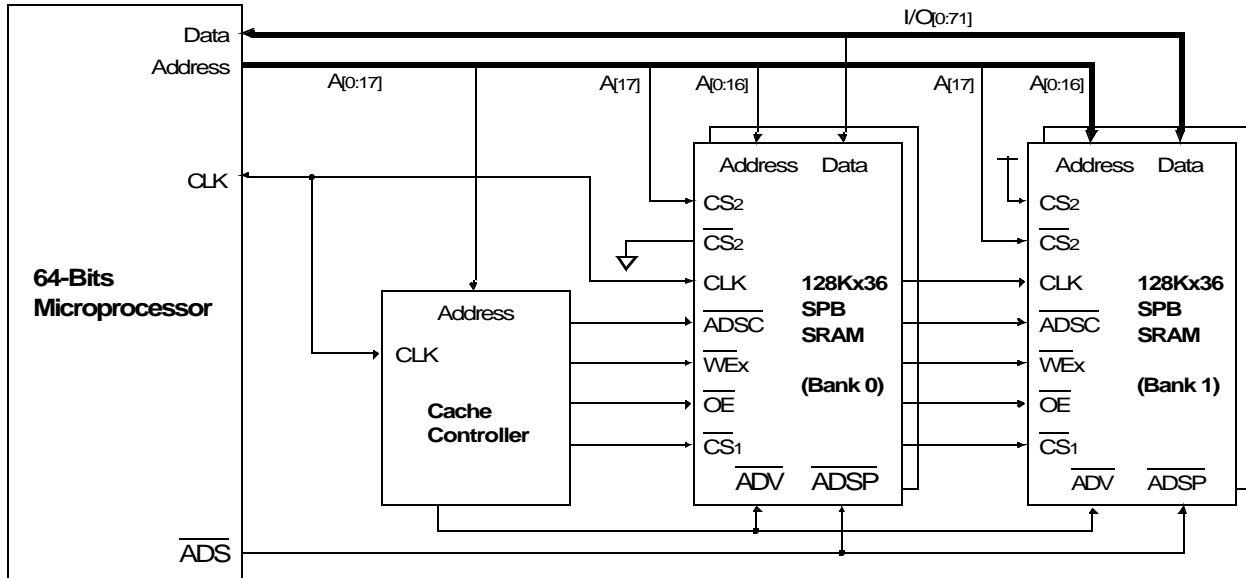
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

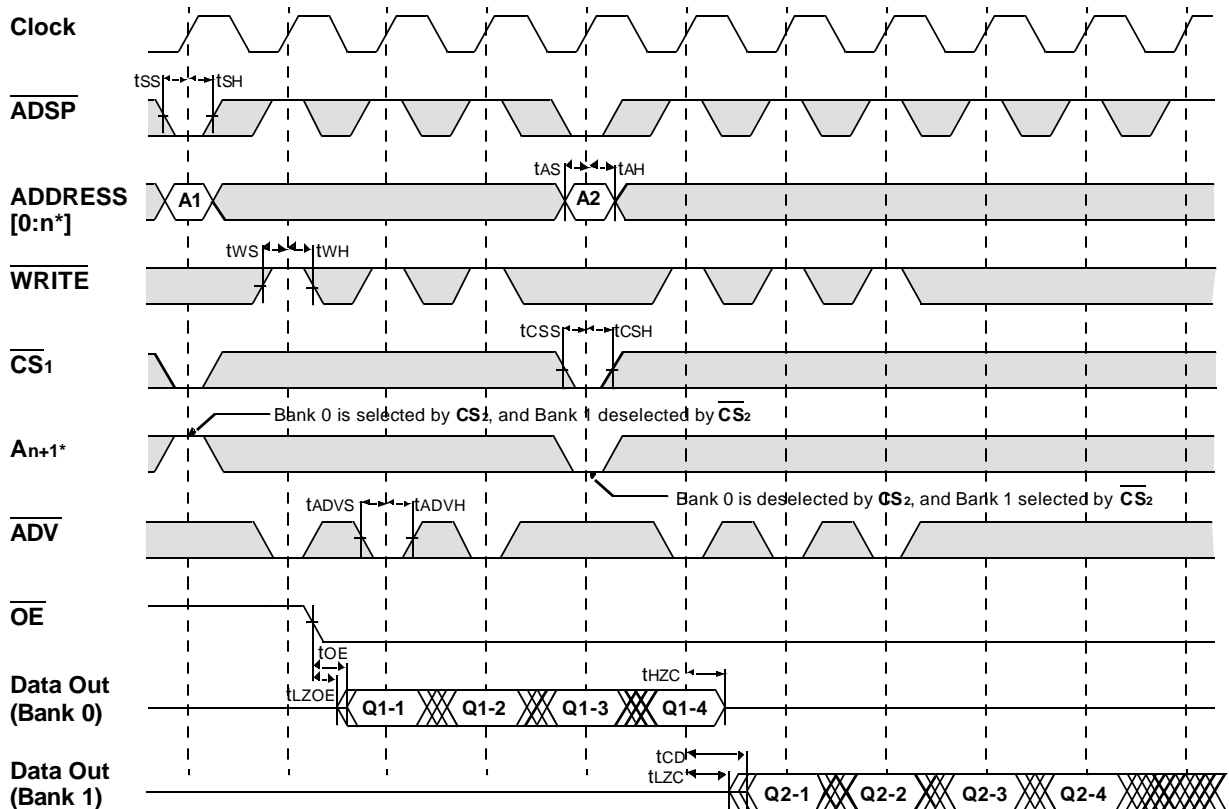
DEPTH EXPANSION

The Samsung 128Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED, ADSC=HIGH)



*Notes : n = 14 32K depth, 15 64K depth, 16 128K depth, 17 256K depth

□ Don't Care ⊗ Undefined

PACKAGE DIMENSIONS

100-TQFP-1420A

Units: millimeters/inches

