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**Document Title**

**128Kx36 & 256Kx18 Synchronous Pipelined SRAM**

**Revision History**

<b><u>Rev.No.</u></b>	<b><u>History</u></b>	<b><u>DraftDate</u></b>	<b><u>Remark</u></b>
Rev. 0.0	- Preliminary specification release	Oct. 2002	Preliminary
Rev. 0.1	- Update DC CHARACTERISTICS x36 : IDD6 : TBD -> 300, IDD65 -> 290, IDD7 -> 280. x18 : IDD6 : TBD -> 290, IDD65 -> 280, IDD7 -> 270.	Jan. 2003	Preliminary
Rev. 0.2	- Change symbol in DC CHARACTERISTICS IDD6, IDD65, IDD7 -> IDD65, IDD70, IDD75	Feb. 2003	Preliminary
Rev. 1.0	- Final Version	Jun. 2003	Final
Rev. 1.1	- Add Single ended differential clock on clock comment.	Jun. 2003	Final

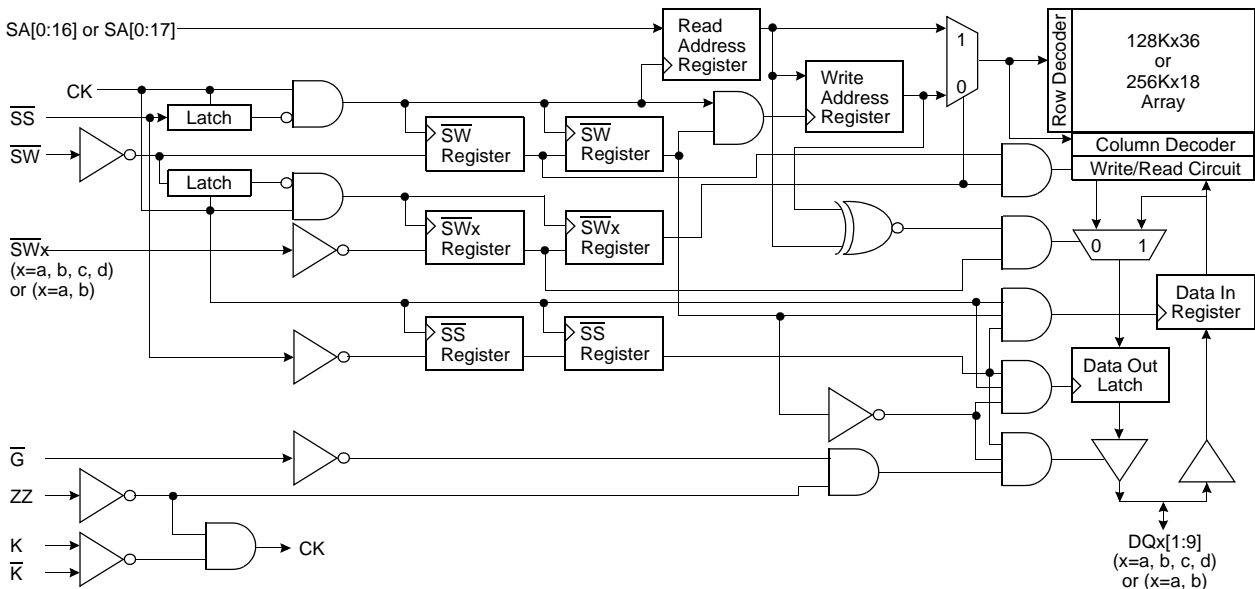
**128Kx36 & 256Kx18 Synchronous Pipelined SRAM**

**FEATURES**

- 128Kx36 or 256Kx18 Organizations.
- 3.3V V<sub>DD</sub>, 2.5/3.3V V<sub>DDQ</sub>.
- LVTTTL 2.5/3.3V Input and Output Levels.
- Differential, PECL clock / Single ended or differential LVTTTL clock Inputs
- Synchronous Read and Write Operation
- Registered Input and Latched Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9 bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- JTAG 1149.1 Compatible Test Access port.
- 119(7x17) Pin Ball Grid Array Package(14mmx22mm).

Organiza-tion	Part Number	Cycle Time	Access Time
128Kx36	K7P403623B-H65	6	6.5
	K7P403623B-H70	6.5	7.0
	K7P403623B-H75	7	7.5
256Kx18	K7P401823B-H65	6	6.5
	K7P401823B-H70	6.5	7.0
	K7P401823B-H75	7	7.5

**FUNCTIONAL BLOCK DIAGRAM**



**PIN DESCRIPTION**

Pin Name	Pin Description	Pin Name	Pin Description
K, $\bar{K}$	Differential Clocks(PECL or LVTTTL Level)	V <sub>DDQ</sub>	Output Power Supply
SAn	Synchronous Address Input	M <sub>1</sub> , M <sub>2</sub>	Read Protocol Mode Pins ( M <sub>1</sub> =V <sub>DD</sub> , M <sub>2</sub> =V <sub>SS</sub> )
DQn	Bi-directional Data Bus	$\bar{G}$	Asynchronous Output Enable
$\bar{SW}$	Synchronous Global Write Enable	$\bar{SS}$	Synchronous Select
$\bar{SW}_a$	Synchronous Byte a Write Enable	TCK	JTAG Test Clock
$\bar{SW}_b$	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
$\bar{SW}_c$	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
$\bar{SW}_d$	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
ZZ	Asynchronous Power Down	V <sub>SS</sub>	GND
V <sub>DD</sub>	Core Power Supply	NC	No Connection

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**PACKAGE PIN CONFIGURATIONS(TOP VIEW)**

**K7P403623B(128Kx36)**

	1	2	3	4	5	6	7
<b>A</b>	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
<b>B</b>	NC	NC	SA9	NC	SA8	NC	NC
<b>C</b>	NC	SA12	SA11	VDD	SA6	SA5	NC
<b>D</b>	DQc8	DQc9	VSS	NC*	VSS	DQb9	DQb8
<b>E</b>	DQc6	DQc7	VSS	$\overline{SS}$	VSS	DQb7	DQb6
<b>F</b>	VDDQ	DQc5	VSS	$\overline{G}$	VSS	DQb5	VDDQ
<b>G</b>	DQc3	DQc4	$\overline{SWc}$	NC*	$\overline{SWb}$	DQb4	DQb3
<b>H</b>	DQc1	DQc2	VSS	NC*	VSS	DQb2	DQb1
<b>J</b>	VDDQ	VbD	NC***	VDD	NC***	VDD	VDDQ
<b>K</b>	DQd1	DQd2	VSS	K	VSS	DQa2	DQa1
<b>L</b>	DQd3	DQd4	$\overline{SWd}$	$\overline{K}$	$\overline{SWa}$	DQa4	DQa3
<b>M</b>	VDDQ	DQd5	VSS	$\overline{SW}$	VSS	DQa5	VDDQ
<b>N</b>	DQd6	DQd7	VSS	SA16	VSS	DQa7	DQa6
<b>P</b>	DQd8	DQd9	VSS	SA0	VSS	DQa9	DQa8
<b>R</b>	NC	SA15	M1	VDD	M2	SA2	NC
<b>T</b>	NC	NC	SA14	SA1	SA3	NC	ZZ
<b>U</b>	VDDQ	TMS	TDI	TCK	TDO	NC**	VDDQ

**NOTE :** 1. NC\* is used for the Boundary Scan.  
2. NC\*\* is reserved for TRST input.  
3. NC\*\*\* is reserved for HSTL interface.

**KM718FV4022(256Kx18)**

	1	2	3	4	5	6	7
<b>A</b>	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
<b>B</b>	NC	NC	SA9	NC	SA8	NC	NC
<b>C</b>	NC	SA12	SA11	VDD	SA6	SA5	NC
<b>D</b>	DQb1	NC	VSS	NC*	VSS	DQa9	NC
<b>E</b>	NC	DQb2	VSS	$\overline{SS}$	VSS	NC	DQa8
<b>F</b>	VDDQ	NC	VSS	$\overline{G}$	VSS	DQa7	VDDQ
<b>G</b>	NC	DQb3	$\overline{SWb}$	NC*	NC	NC	DQa6
<b>H</b>	DQb4	NC	VSS	NC*	VSS	DQa5	NC
<b>J</b>	VDDQ	VbD	NC***	VDD	NC***	VbD	VDDQ
<b>K</b>	NC	DQb5	VSS	K	VSS	NC	DQa4
<b>L</b>	DQb6	NC	NC	$\overline{K}$	$\overline{SWa}$	DQa3	NC
<b>M</b>	VDDQ	DQb7	VSS	$\overline{SW}$	VSS	NC	VDDQ
<b>N</b>	DQb8	NC	VSS	SA16	VSS	DQa2	NC
<b>P</b>	NC	DQb9	VSS	SA1	VSS	NC	DQa1
<b>R</b>	NC	SA15	M1	VDD	M2	SA2	NC
<b>T</b>	NC	SA17	SA14	NC	SA3	SA0	ZZ
<b>U</b>	VDDQ	TMS	TDI	TCK	TDO	NC**	VDDQ

**NOTE :** 1. NC\* is used for the Boundary Scan.  
2. NC\*\* is reserved for TRST input.  
3. NC\*\*\* is reserved for HSTL interface.

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**FUNCTION DESCRIPTION**

The K7P403623B and K7P401823B are 4,718,592 bit Synchronous SRAM. It is organized as 131,072 words of 36 bits(or 262,144 words of 18 bits) and is implemented in SAMSUNG's advanced CMOS technology.

Single differential PECL level K clocks or single ended or differential LVCMOS/LVTTL clock are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses, Write Enables, Synchronous Select and Data Ins are registered internally. Data outputs are updated from output latches of the falling edge of K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

**Read Operation**

During reads, the address is registered during the clock rising edge and the internal array is read. The data is driven to the CPU in the following cycle.  $\overline{SS}$  is driven low during this cycle, signaling that the SRAM should drive out the data.

During consecutive read cycles where the address is the same, the data output must be held constantly without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

**Write(Store) Operation**

All addresses and  $\overline{SW}$  are both sampled on the clock rising edge.  $\overline{SW}$  is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and  $\overline{SW}$  have been sampled by the SRAM.  $\overline{SS}$  will be driven low during the same cycle that the Address,  $\overline{SW}$  and  $\overline{SW}[a:d]$  are valid to signal that a valid operations is on the Address and Control Input.

Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals  $\overline{SW}[a:d]$  signal which 9-bit bytes will be written. Timing of  $\overline{SW}[a:d]$  is the same as the  $\overline{SW}$  signal.

**Bypass Read Operation**

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

**Low Power Dissipation Mode**

During normal operation, asynchronous signal ZZ must be pulled low. Low Power Mode is enabled by switching ZZ high. When the SRAM is in Power Down Mode, the outputs will go to a Hi-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time(tzr) is required before the SRAM resumes to normal operation.

**TRUTH TABLE**

K	ZZ	$\overline{G}$	$\overline{SS}$	$\overline{SW}$	$\overline{SWa}$	$\overline{SWb}$	$\overline{SWc}$	$\overline{SWd}$	DQa	DQb	DQc	DQd	Operation
X	H	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
X	L	H	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	H	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	L	H	X	X	X	X	DOUT	DOUT	DOUT	DOUT	Read Cycle
↑	L	X	L	L	H	H	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
↑	L	X	L	L	L	H	H	H	DIN	Hi-Z	Hi-Z	Hi-Z	Write first byte
↑	L	X	L	L	H	L	H	H	Hi-Z	DIN	Hi-Z	Hi-Z	Write second byte
↑	L	X	L	L	H	H	L	H	Hi-Z	Hi-Z	DIN	Hi-Z	Write third byte
↑	L	X	L	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z	DIN	Write fourth byte
↑	L	X	L	L	L	L	L	L	DIN	DIN	DIN	DIN	Write all byte

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	V <sub>DD</sub>	-0.3 to 4.6	V
Output Supply Voltage Relative to Vss	V <sub>DDQ</sub>	V <sub>DD</sub>	V
Voltage on any I/O pin Relative to Vss	V <sub>TERM</sub>	-0.3 to V <sub>DD</sub> +0.3	V
Maximum Power Dissipation	P <sub>D</sub>	1.5	W
Output Short-Circuit Current	I <sub>OUT</sub>	25	mA
Operating Temperature	T <sub>OPR</sub>	0 to 70	°C
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C

**NOTE :** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	V <sub>DD</sub>	3.15	3.3	3.45	V	
Output Power Supply Voltage (for 2.5V I/O)	V <sub>DDQ</sub>	2.375	2.5	2.9	V	
Output Power Supply Voltage (for 3.3V I/O)	V <sub>DDQ</sub>	3.135	3.3	3.6	V	
Input High Level (for 2.5V I/O)	V <sub>IH</sub>	1.7	-	V <sub>DD</sub> +0.3	V	
Input Low Level (for 2.5V I/O)	V <sub>IL</sub>	-0.3	-	0.7	V	
Input High Level (for 3.3V I/O)	V <sub>IH</sub>	2.0	-	V <sub>DD</sub> +0.3	V	
Input Low Level (for 3.3V I/O)	V <sub>IL</sub>	-0.3	-	0.8	V	
PECL Clock Input High Level	V <sub>IH-PECL</sub>	2.135	-	2.420	V	1
PECL Clock Input Low Level	V <sub>IL-PECL</sub>	1.490	-	1.825	V	1
Clock Input Signal Voltage	V <sub>IN</sub>	-0.3	-	3.45	V	2
Clock Input Differential Voltage	V <sub>DIF-CLK</sub>	0.2	-	V <sub>DD</sub> +0.6	V	2
Clock Input Common Mode Voltage	V <sub>CM-CLK</sub>	1.1	-	2.1	V	2
Operating Junction Temperature	T <sub>J</sub>	10	-	110	°C	

**NOTE**

1. For operation with differential PECL clock inputs.
2. For operation with single ended or differential LVCMOS / LVTTTL clock input.

**DC CHARACTERISTICS**

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 ( $V_{IN}=V_{IH}$ or $V_{IL}$ , $ZZ$ & $SS=V_{IL}$ )	$I_{DD65}$ $I_{DD70}$ $I_{DD75}$	-	300 290 280	mA	1, 2
Average Power Supply Operating Current-x18 ( $V_{IN}=V_{IH}$ or $V_{IL}$ , $ZZ$ & $SS=V_{IL}$ )	$I_{DD65}$ $I_{DD70}$ $I_{DD75}$	-	290 280 270	mA	1, 2
Power Supply Standby Current ( $V_{IN}=V_{IH}$ or $V_{IL}$ , $ZZ=V_{IH}$ )	$I_{SB}$	-	120	mA	1
Input Leakage Current ( $V_{IN}=V_{SS}$ or $V_{DDQ}$ )	$I_{LI}$	-1	1	$\mu A$	
Output Leakage Current ( $V_{OUT}=V_{SS}$ or $V_{DDQ}$ , $ZZ=V_{IH}$ , $\bar{G}=V_{IH}$ )	$I_{LO}$	-1	1	$\mu A$	
Output High Voltage( $I_{OH}=-4mA$ ) for $V_{DDQ}=3.3V$ Output High Voltage( $I_{OH}=-4mA$ ) for $V_{DDQ}=2.5V$	$V_{OH1}$ $V_{OH2}$	2.4 2.0	$V_{DDQ}$	V	
Output Low Voltage( $I_{OL}=4mA$ )	$V_{OL}$	$V_{SS}$	0.4	V	

**NOTE** :1. Minimum cycle.  $I_{OUT}=0mA$ .  
 2. 50% read cycles.

**PIN CAPACITANCE**

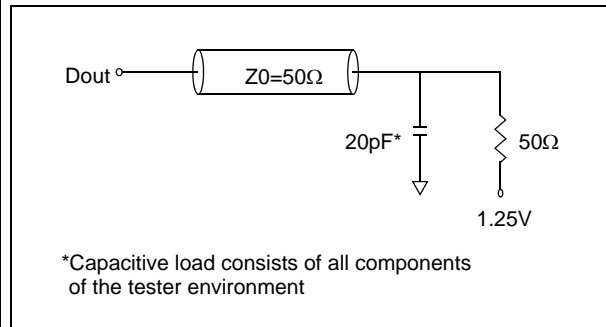
Parameter	Symbol	Typ	Max	Unit
Input Capacitance	$C_{IN}$	-	5	pF
Output Capacitance	$C_{OUT}$	-	7	pF

**NOTE** : Periodically sampled and not 100% tested. ( $dV=0V$ ,  $f=1MHz$ )

**AC TEST CONDITIONS**

Parameter	Symbol	Value	Unit
Core Power Supply Voltage	V <sub>DD</sub>	3.15~3.45	V
Output Power Supply Voltage	V <sub>DDQ</sub>	2.4~2.6	V
Input High/Low Level	V <sub>IH</sub> /V <sub>IL</sub>	1.7/0.7	V
Clock Input High/Low Level(PECL)	V <sub>IH</sub> /V <sub>IL</sub>	2.4/1.5	V
Input Rise/Fall Time	T <sub>R</sub> /T <sub>F</sub>	1.0/1.0	ns
Clock Input Rise/Fall Time(PECL)	T <sub>R</sub> /T <sub>F</sub>	1.0/1.0	ns
Input and Out Timing Reference Level		1.25	V
Clock Input Timing Reference Level		Cross Point	V

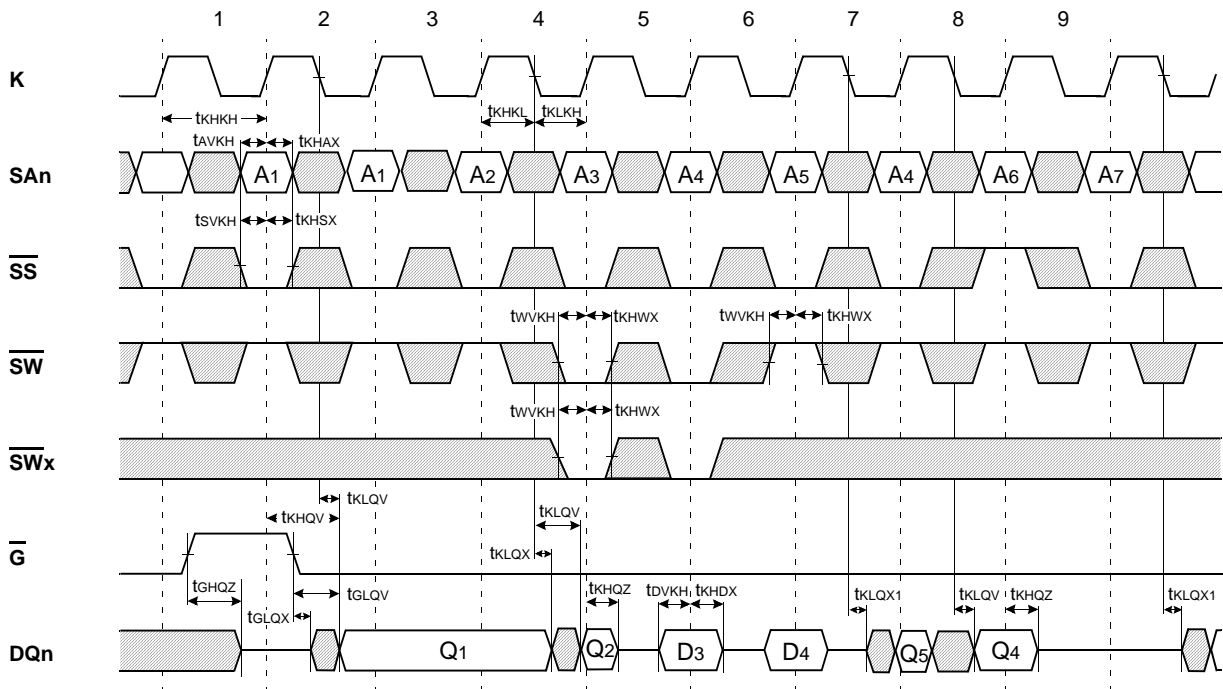
**AC TEST OUTPUT LOAD**



**AC CHARACTERISTICS**

Parameter	Symbol	-65		-70		-75		Unit	Note
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	t <sub>KHKH</sub>	6.0	-	6.5	-	7.0	-	ns	
Clock High Pulse Width	t <sub>KHKL</sub>	2.0	-	2.0	-	2.0	-	ns	
Clock Low Pulse Width	t <sub>KLKH</sub>	2.0	-	2.0	-	2.0	-	ns	
Clock High to Output Valid	t <sub>KHQV</sub>	-	6.5	-	7.0	-	7.5	ns	
Clock Low to Output Valid	t <sub>KLQV</sub>	-	2.5	-	2.5	-	3.0	ns	
Clock Low to Output Hold	t <sub>KLQX</sub>	0.5	-	0.5	-	0.5	-	ns	
Address Setup Time	t <sub>AVKH</sub>	0.5	-	0.5	-	0.5	-	ns	
Address Hold Time	t <sub>KHAX</sub>	1.0	-	1.0	-	1.0	-	ns	
Write Data Setup Time	t <sub>DVKH</sub>	0.5	-	0.5	-	0.5	-	ns	
Write Data Hold Time	t <sub>KHDX</sub>	1.0	-	1.0	-	1.0	-	ns	
$\overline{SW}$ , $\overline{SW}$ [a:d] Setup Time	t <sub>WVKH</sub>	0.5	-	0.5	-	0.5	-	ns	
$\overline{SW}$ , $\overline{SW}$ [a:d] Hold Time	t <sub>KHWX</sub>	1.0	-	1.0	-	1.0	-	ns	
$\overline{SS}$ Setup Time	t <sub>SVKH</sub>	0.5	-	0.5	-	0.5	-	ns	
$\overline{SS}$ Hold Time	t <sub>KHSX</sub>	1.0	-	1.0	-	1.0	-	ns	
Clock High to Output Hi-Z	t <sub>KHQZ</sub>	-	2.5	-	3.0	-	3.5	ns	
Clock Low to Output Low-Z	t <sub>KLQX1</sub>	0.5	-	0.5	-	0.5	-	ns	
$\overline{G}$ High to Output High-Z	t <sub>GHQZ</sub>	-	2.5	-	3.0	-	3.5	ns	
$\overline{G}$ Low to Output Low-Z	t <sub>GLQX</sub>	0.5	-	0.5	-	0.5	-	ns	
$\overline{G}$ Low to Output Valid	t <sub>GLQV</sub>	-	2.5	-	3.0	-	3.5	ns	
ZZ High to Power Down(Sleep Time)	t <sub>ZZE</sub>	-	15	-	15	-	15	ns	
ZZ Low to Recovery(Wake-up Time)	t <sub>ZZR</sub>	-	20	-	20	-	20	ns	

TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES

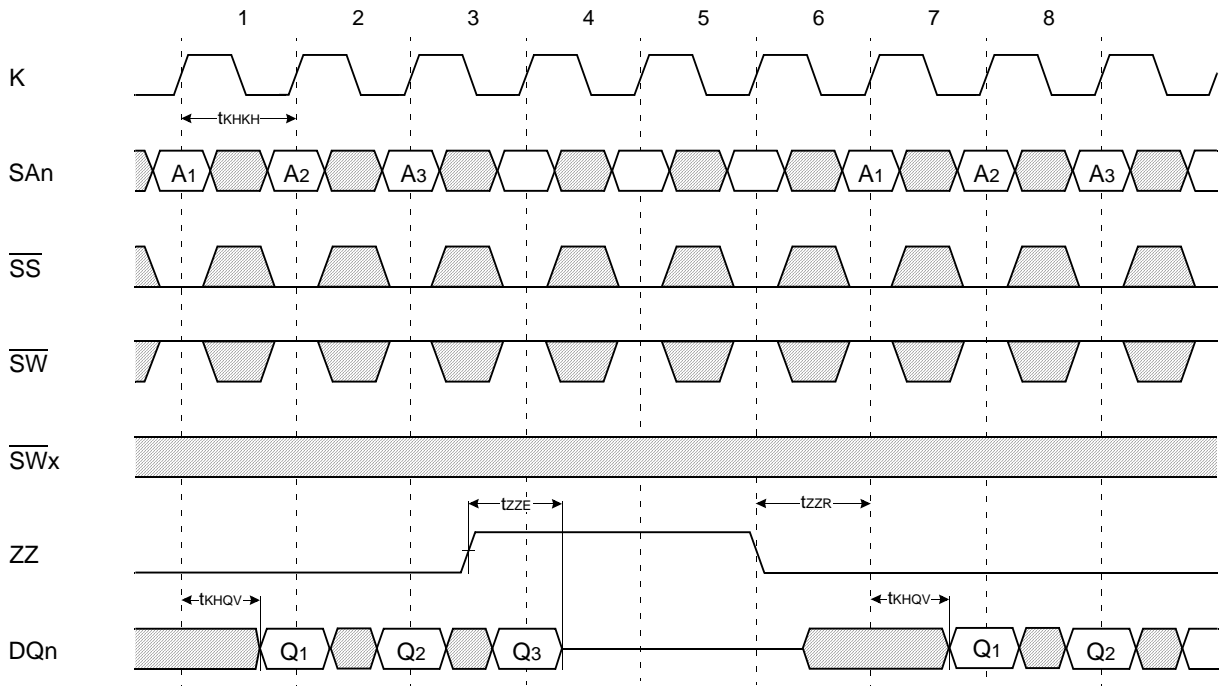


NOTE

1. D3 is the input data written in memory location A3.
2. Q4 is the output data read from the write data buffer(not from the cell array), as a result of address A4 being a match from the last write cycle address.
3. Data is valid at the output at the later of  $t_{KHQV}$  following the rising clock edge, or  $t_{KLQV}$  following the following clock edge.
4. When  $\overline{SS}$  is sampled high or  $\overline{SW}$  is sampled low on the rising edge of clock, the outputs go into Hi-Z state no later than  $t_{KHQZ}$  following the rising clock edge.
5. When  $\overline{SS}$  is low and  $\overline{SW}$  is high on the rising edge of clock, the outputs go into Low-Z state (being driven) no earlier than  $t_{KLQX1}$  following the next falling edge of clock.
6. When the SRAM is deselected, the output goes Hi-Z at  $t_{KHQZ}$  following the rising clock edge. On the next read cycle, note that the SRAM output do not leave the Hi-Z state until  $t_{KLQX1}$  after the falling clock edge.



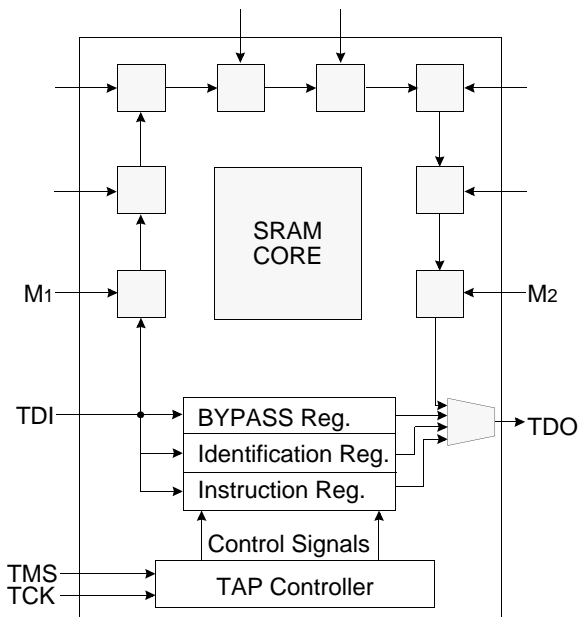
TIMING WAVEFORMS OF STANDBY CYCLES



**IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG**

This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

**JTAG Block Diagram**



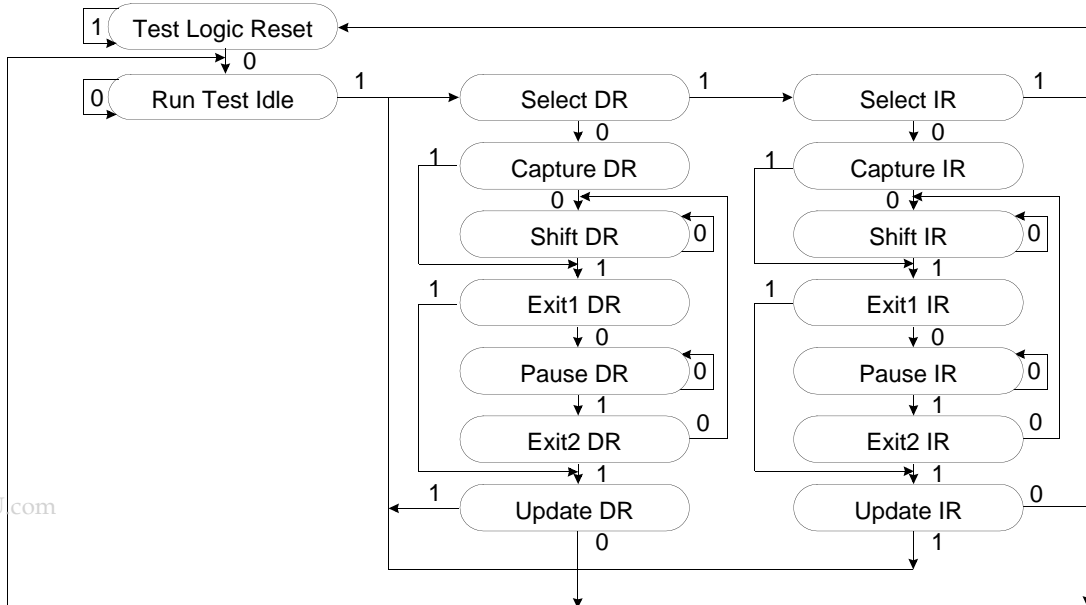
**JTAG Instruction Coding**

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

**NOTE**

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to VSS when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

**TAP Controller State Diagram**



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**SCAN REGISTER DEFINITION**

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	70 bits
256Kx18	3 bits	1 bits	32 bits	51 bits

**ID REGISTER DEFINITION**

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
128Kx36	0000	00101 00100	xxxxxx	00001001110	1
256Kx18	0000	00110 00011	xxxxxx	00001001110	1

**BOUNDARY SCAN EXIT ORDER(x36)**

36	3B	SA9	SA8	5B	35
37	2B	NC	NC	6B	34
38	3A	SA10	SA7	5A	33
39	3C	SA11	SA6	5C	32
40	2C	SA12	SA5	6C	31
41	2A	SA13	SA4	6A	30
42	2D	DQc9	DQb9	6D	29
43	1D	DQc8	DQb8	7D	28
44	2E	DQc7	DQb7	6E	27
45	1E	DQc6	DQb6	7E	26
46	2F	DQc5	DQb5	6F	25
47	2G	DQc4	DQb4	6G	24
48	1G	DQc3	DQb3	7G	23
49	2H	DQc2	DQb2	6H	22
50	1H	DQc1	DQb1	7H	21
51	3G	$\overline{SW}c$	$\overline{SW}b$	5G	20
52	4D	NC	$\overline{G}$	4F	19
53	4E	$\overline{SS}$	K	4K	18
54	4G	NC	$\overline{K}$	4L	17
55	4H	NC	$\overline{SW}a$	5L	16
56	4M	$\overline{SW}$	DQa1	7K	15
57	3L	$\overline{SW}d$	DQa2	6K	14
58	1K	DQd1	DQa3	7L	13
59	2K	DQd2	DQa4	6L	12
60	1L	DQd3	DQa5	6M	11
61	2L	DQd4	DQa6	7N	10
62	2M	DQd5	DQa7	6N	9
63	1N	DQd6	DQa8	7P	8
64	2N	DQd7	DQa9	6P	7
65	1P	DQd8	ZZ	7T	6
66	2P	DQd9	SA3	5T	5
67	3T	SA14	SA2	6R	4
68	2R	SA15	SA1	4T	3
69	4N	SA16	SA0	4P	2
70	3R	M1	M2	5R	1

**BOUNDARY SCAN EXIT ORDER(x18)**

26	3B	SA9	SA8	5B	25
27	2B	NC	NC	6B	24
28	3A	SA10	SA7	5A	23
29	3C	SA11	SA6	5C	22
30	2C	SA12	SA5	6C	21
31	2A	SA13	SA4	6A	20
			DQa9	6D	19
32	1D	DQb1			
33	2E	DQb2			
			DQa8	7E	18
			DQa7	6F	17
34	2G	DQb3			
			DQa6	7G	16
			DQa5	6H	15
35	1H	DQb4			
36	3G	$\overline{SW}b$			
37	4D	NC	$\overline{G}$	4F	14
38	4E	$\overline{SS}$	K	4K	13
39	4G	NC	$\overline{K}$	4L	12
40	4H	NC	$\overline{SW}a$	5L	11
41	4M	$\overline{SW}$	DQa4	7K	10
42	2K	DQb5	DQa3	6L	9
43	1L	DQb6			
44	2M	DQb7	DQa2	6N	8
45	1N	DQb8	DQa1	7P	7
			ZZ	7T	6
46	2P	DQb9	SA3	5T	5
47	3T	SA14	SA2	6R	4
48	2R	SA15			
49	4N	SA16	SA1	4P	3
50	2T	SA17	SA0	6T	2
51	3R	M1	M2	5R	1

**NOTE :** 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 16M part and the scanned data are fixed to "0" for this 4M parts.

**JTAG DC OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V <sub>DD</sub>	3.15	3.3	3.45	V	
Input High Level	V <sub>IH</sub>	1.7	-	V <sub>DD</sub> +0.3	V	
Input Low Level	V <sub>IL</sub>	-0.3	-	0.8	V	
Output High Voltage(I <sub>OH</sub> =-2mA)	V <sub>OH</sub>	2.1	-	V <sub>DD</sub>	V	
Output Low Voltage(I <sub>OL</sub> =2mA)	V <sub>OL</sub>	V <sub>SS</sub>	-	0.2	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

**JTAG AC TEST CONDITIONS**

Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V <sub>IH</sub> /V <sub>IL</sub>	2.5/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		1.5	V	1

NOTE : 1. See SRAM AC test output load.

**JTAG AC Characteristics**

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t <sub>CHCH</sub>	50	-	ns	
TCK High Pulse Width	t <sub>CHCL</sub>	20	-	ns	
TCK Low Pulse Width	t <sub>CLCH</sub>	20	-	ns	
TMS Input Setup Time	t <sub>MVCH</sub>	5	-	ns	
TMS Input Hold Time	t <sub>CHMX</sub>	5	-	ns	
TDI Input Setup Time	t <sub>DVCH</sub>	5	-	ns	
TDI Input Hold Time	t <sub>CHDX</sub>	5	-	ns	
SRAM Input Setup Time	t <sub>SVCH</sub>	5	-	ns	
SRAM Input Hold Time	t <sub>CHSX</sub>	5	-	ns	
Clock Low to Output Valid	t <sub>CLQV</sub>	0	10	ns	

**JTAG TIMING DIAGRAM**

