

Document Title

1Mx36-bit, 2Mx18-bit, 4Mx8-bit QDR™ II b4 SRAM

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	1. Initial document.	June 30, 2001	Advance
0.1	1. Package dimension modify. P.20 from 13mmx15mm to 15mmx17mm	Oct. 20, 2001	Advance
0.2	1. Pin name change from $\overline{DLL}$ to $\overline{Doff}$ . 2. Vddq range change from 1.5V to 1.5V~1.8V. 3. Update JTAG test conditions. 4. Reserved pin for high density name change from NC to Vss/SA 5. Delete AC test condition about Clock Input timing Reference Level 6. Delete clock description on page 2 and add HSTL I/O comment	Dec. 5, 2001	Preliminary
0.3	1. Update current characteristics in DC electrical characteristics 2. Change AC timing characteristics 3. Update JTAG instruction coding and diagrams	July, 29. 2002	Preliminary
0.4	1. Add -FC25 part(AC Characteristics) 2. Add AC electrical characteristics. 3. Change AC timing characteristics 4. Change DC electrical characteristics(Isb1)	Sep. 6. 2002	Preliminary
0.5	1. Change the data Setup/Hold time. 2. Change the Access Time.(tCHQV, tCHQX, etc.) 3. Change the Clock Cycle Time.(MAX value of tKHKH) 4. Change the JTAG instruction coding.	Oct. 7. 2002	Preliminary
0.6	1. Change the Boundary scan exit order. 2. Change the AC timing characteristics(-25, -20) 3. Correct the Overshoot and Undershoot timing diagrams.	Dec. 16, 2002	Preliminary
0.7	1. Change the JTAG Block diagram	Dec. 26, 2002	Preliminary
0.8	1. Correct the JTAG ID register definition 2. Correct the AC timing parameter (delete the tKHKH Max value) 3. Change the Isb1 current	Mar. 20, 2003	Preliminary
0.9	1. Change the Maximum Clock cycle time. 2. Correct the 165FBGA package ball size.	April. 4, 2003	Preliminary

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

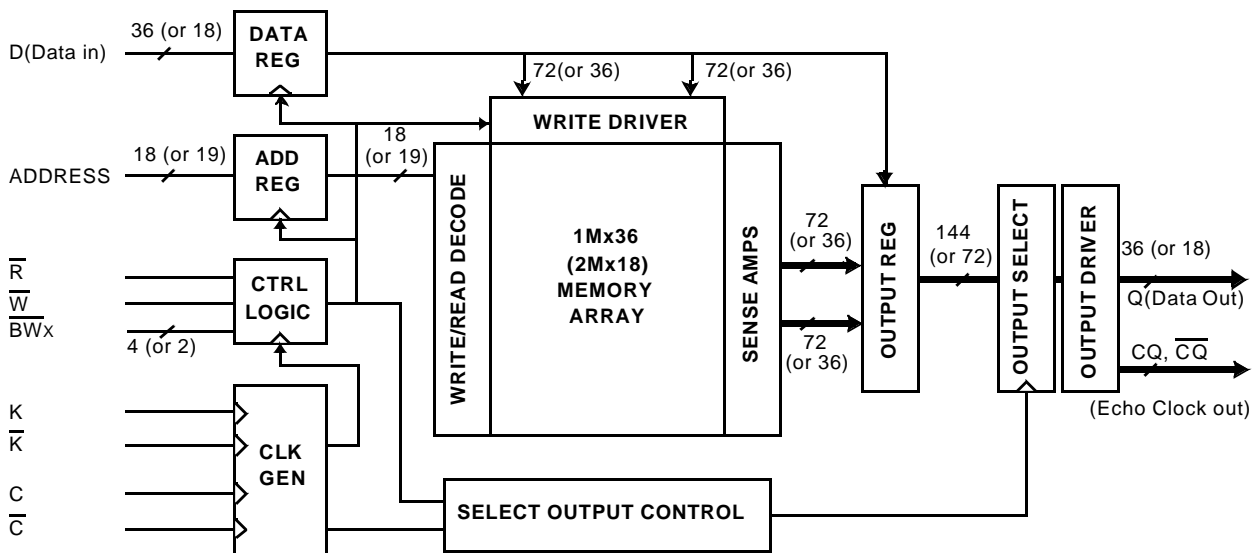
**1Mx36-bit, 2Mx18-bit, 4Mx8-bit QDR™ II b4 SRAM**

**FEATURES**

- 1.8V+0.1V/-0.1V Power Supply.
- DLL circuitry for wide output data valid window and future frequency scaling.
- I/O Supply Voltage 1.5V+0.1V/-0.1V for 1.5V I/O, 1.8V+0.1V/-0.1V for 1.8V I/O.
- Separate independent read and write data ports with concurrent read and write operation
- HSTL I/O
- Full data coherency, providing most current data .
- Synchronous pipeline read with self timed late write.
- Registered address, control and data input/output.
- DDR(Double Data Rate) Interface on read and write ports.
- Fixed 4-bit burst for both read and write operation.
- Clock-stop supports to reduce current.
- Two input clocks(K and  $\bar{K}$ ) for accurate DDR timing at clock rising edges only.
- Two input clocks for output data(C and  $\bar{C}$ ) to minimize clock-skew and flight-time mismatches.
- Two echo clocks (CQ and  $\bar{CQ}$ ) to enhance output data traceability.
- Single address bus.
- Byte write (x18, x36) and nybble(x8) write function.
- Sepatate read/write control pin( $\bar{R}$  and  $\bar{W}$ )
- Simple depth expansion with no data contention.
- Programmable output impenance.
- JTAG 1149.1 compatible test access port.
- 165FBGA(11x15 ball aray FBGA) with body size of 15x17mm

Organization	Part Number	Cycle Time	Access Time	Unit
X36	K7R323684M-FC25	4.0	0.45	ns
	K7R323684M-FC20	5.0	0.45	ns
	K7R323684M-FC16	6.0	0.50	ns
X18	K7R321884M-FC25	4.0	0.45	ns
	K7R321884M-FC20	5.0	0.45	ns
	K7R321884M-FC16	6.0	0.50	ns
X8	K7R320884M-FC25	4.0	0.45	ns
	K7R320884M-FC20	5.0	0.45	ns
	K7R320884M-FC16	6.0	0.50	ns

**FUNCTIONAL BLOCK DIAGRAM**



**Notes:** 1. Numbers in ( ) are for x18 device, x8 device also the same with appropriate adjustments of depth and width.

QDR SRAM and Quad Data Rate comprise a new family of products developed by Cypress, Hitachi, IDT, Micron, NEC and Samsung technology.

**K7R323684M**  
**K7R321884M**  
**K7R320884M**

*Preliminary*

**1Mx36 & 2Mx18 & 4Mx8 QDR™ II b4 SRAM**

**PIN CONFIGURATIONS(TOP VIEW) K7R323684M(1Mx36)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	$\overline{CQ}$	Vss/SA*	NC/SA*	$\overline{W}$	$\overline{BW}_2$	$\overline{K}$	$\overline{BW}_1$	$\overline{R}$	SA	Vss/SA*	CQ
<b>B</b>	Q27	Q18	D18	SA	$\overline{BW}_3$	K	$\overline{BW}_0$	SA	D17	Q17	Q8
<b>C</b>	D27	Q28	D19	Vss	SA	NC	SA	Vss	D16	Q7	D8
<b>D</b>	D28	D20	Q19	Vss	Vss	Vss	Vss	Vss	Q16	D15	D7
<b>E</b>	Q29	D29	Q20	VDDQ	Vss	Vss	Vss	VDDQ	Q15	D6	Q6
<b>F</b>	Q30	Q21	D21	VDDQ	VDD	Vss	VDD	VDDQ	D14	Q14	Q5
<b>G</b>	D30	D22	Q22	VDDQ	VDD	Vss	VDD	VDDQ	Q13	D13	D5
<b>H</b>	$\overline{Doff}$	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ
<b>J</b>	D31	Q31	D23	VDDQ	VDD	Vss	VDD	VDDQ	D12	Q4	D4
<b>K</b>	Q32	D32	Q23	VDDQ	VDD	Vss	VDD	VDDQ	Q12	D3	Q3
<b>L</b>	Q33	Q24	D24	VDDQ	Vss	Vss	Vss	VDDQ	D11	Q11	Q2
<b>M</b>	D33	Q34	D25	Vss	Vss	Vss	Vss	Vss	D10	Q1	D2
<b>N</b>	D34	D26	Q25	Vss	SA	SA	SA	Vss	Q10	D9	D1
<b>P</b>	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0
<b>R</b>	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

**Notes:** 1. \*,  $\overline{C}$ ,  $\overline{K}$  or  $\overline{K}$  pins are reserved for higher density address, i.e. 3A for 64Mb, 10A for 128Mb and 2A for 256Mb  
2.  $\overline{BW}_0$  controls write to D0:D8,  $\overline{BW}_1$  controls write to D9:D17,  $\overline{BW}_2$  controls write to D18:D26 and  $\overline{BW}_3$  controls write to D27:D35.

**PIN NAME**

SYMBOL	PIN NUMBERS	DESCRIPTION	NOTE
K, $\overline{K}$	6B, 6A	Input Clock	
C, $\overline{C}$	6P, 6R	Input Clock for Output Data	1
CQ, $\overline{CQ}$	11A, 1A	Output Echo Clock	
$\overline{Doff}$	1H	DLL Disable when low	
SA	9A,4B,8B,5C,7C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R	Address Inputs	
D0-35	10P,11N,11M,10K,11J,11G,10E,11D,11C,10N,9M,9L,9J,10G,9F,10D,9C,9B,3B,3C,2D,3F,2G,3J,3L,3M,2N,1C,1D,2E,1G,1J,2K,1M,1N,2P	Data Inputs	
Q0-35	11P,10M,11L,11K,10J,11F,11E,10C,11B,9P,9N,10L,9K,9G,10F,9E,9D,10B,2B,3D,3E,2F,3G,3K,2L,3N,3P,1B,2C,1E,1F,2J,1K,1L,2M,1P	Data Outputs	
$\overline{W}$	4A	Write Control Pin, active when low	
$\overline{R}$	8A	Read Control Pin, active when low	
$\overline{BW}_0, \overline{BW}_1, \overline{BW}_2, \overline{BW}_3$	7B,7A,5A,5B	Block Write Control Pin, active when low	
VREF	2H,10H	Input Reference Voltage	
ZQ	11H	Output Driver Impedance Control Input	2
VDD	5F,7F,5G,7G,5H,7H,5J,7J,5K,7K	Power Supply ( 1.8 V )	
VDDQ	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output Power Supply ( 1.5V or 1.8V )	
Vss	2A,10A,4C,8C,4D-8D,5E-7E,6F,6G,6H,6J,6K,5L-7L,4M,8M,4N,8N	Ground	
TMS	10R	JTAG Test Mode Select	
TDI	11R	JTAG Test Data Input	
TCK	2R	JTAG Test Clock	
TDO	1R	JTAG Test Data Output	
NC	3A,6C	No Connect	3

**Notes:** 1. C,  $\overline{C}$ , K or  $\overline{K}$  cannot be set to VREF voltage.  
2. When ZQ pin is directly connected to VDD output impedance is set to minimum value and it cannot be connected to ground or left unconnected.  
3. Not connected to chip pad internally.

**PIN CONFIGURATIONS(TOP VIEW) K7R321884M(2Mx18)**

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	Vss/SA*	SA	$\overline{W}$	$\overline{BW}_1$	$\overline{K}$	NC	$\overline{R}$	SA	Vss/SA*	CQ
B	NC	Q9	D9	SA	NC	K	$\overline{BW}_0$	SA	NC	NC	Q8
C	NC	NC	D10	Vss	SA	NC	SA	Vss	NC	Q7	D8
D	NC	D11	Q10	Vss	Vss	Vss	Vss	Vss	NC	NC	D7
E	NC	NC	Q11	VDDQ	Vss	Vss	Vss	VDDQ	NC	D6	Q6
F	NC	Q12	D12	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	Q5
G	NC	D13	Q13	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	D5
H	$\overline{Doff}$	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	D14	VDDQ	VDD	Vss	VDD	VDDQ	NC	Q4	D4
K	NC	NC	Q14	VDDQ	VDD	Vss	VDD	VDDQ	NC	D3	Q3
L	NC	Q15	D15	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	Q2
M	NC	NC	D16	Vss	Vss	Vss	Vss	Vss	NC	Q1	D2
N	NC	D17	Q16	Vss	SA	SA	SA	Vss	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

Notes: 1. \* Checked No Connect(NC) pins are reserved for higher density address, i.e. 10A for 64Mb and 2A for 128Mb.  
2.  $\overline{BW}_0$  controls write to D0:D8 and  $\overline{BW}_1$  controls write to D9:D17.

**PIN NAME**

SYMBOL	PIN NUMBERS	DESCRIPTION	NOTE
K, $\overline{K}$	6B, 6A	Input Clock	
C, $\overline{C}$	6P, 6R	Input Clock for Output Data	1
CQ, $\overline{CQ}$	11A, 1A	Output Echo Clock	
$\overline{Doff}$	1H	DLL Disable when low	
SA	3A,9A,4B,8B,5C,7C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R	Address Inputs	
D0-17	10P,11N,11M,10K,11J,11G,10E,11D,11C,3B,3C,2D 3F,2G,3J,3L,3M,2N	Data Inputs	
Q0-17	11P,10M,11L,11K,10J,11F,11E,10C,11B,2B,3D,3E 2F,3G,3K,2L,3N,3P	Data Outputs	
$\overline{W}$	4A	Write Control Pin,active when low	
$\overline{R}$	8A	Read Control Pin,active when low	
$\overline{BW}_0, \overline{BW}_1$	7B, 5A	Block Write Control Pin,active when low	
VREF	2H,10H	Input Reference Voltage	
ZQ	11H	Output Driver Impedance Control Input	2
VDD	5F,7F,5G,7G,5H,7H,5J,7J,5K,7K	Power Supply ( 1.8 V )	
VDDQ	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output Power Supply ( 1.5V or 1.8V )	
VSS	2A,10A,4C,8C,4D-8D,5E-7E,6F,6G,6H,6J,6K,5L-7L,4M-8M,4N,8N	Ground	
TMS	10R	JTAG Test Mode Select	
TDI	11R	JTAG Test Data Input	
TCK	2R	JTAG Test Clock	
TDO	1R	JTAG Test Data Output	
NC	7A,1B,5B,9B,10B,1C,2C,6C,9C,1D,9D,10D,1E,2E,9E,1F 9F,10F,1G,9G,10G,1J,2J,9J,1K,2K,9J,1L,9L,10L,1M 2M,9M,1N,9N,10N,1P,2P,9P	No Connect	3

Notes: 1. C,  $\overline{C}$ , K or  $\overline{K}$  cannot be set to VREF voltage.  
2. When ZQ pin is directly connected to VDD output impedance is set to minimum value and it cannot be connected to ground or left unconnected.  
3. Not connected to chip pad internally.

**PIN CONFIGURATIONS(TOP VIEW) K7R320884M(4Mx8)**

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	V <sub>SS</sub> /SA*	SA	$\overline{W}$	$\overline{NW}_1$	$\overline{K}$	NC	$\overline{R}$	SA	SA	CQ
B	NC	NC	NC	SA	NC	K	$\overline{NW}_0$	SA	NC	NC	Q3
C	NC	NC	NC	V <sub>SS</sub>	SA	NC	SA	V <sub>SS</sub>	NC	NC	D3
D	NC	D4	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	NC
E	NC	NC	Q4	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	D2	Q2
F	NC	NC	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	NC
G	NC	D5	Q5	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	NC
H	$\overline{Doff}$	V <sub>REF</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>REF</sub>	ZQ
J	NC	NC	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	Q1	D1
K	NC	NC	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	NC
L	NC	Q6	D6	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC	Q0
M	NC	NC	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	D0
N	NC	D7	NC	V <sub>SS</sub>	SA	SA	SA	V <sub>SS</sub>	NC	NC	NC
P	NC	NC	Q7	SA	SA	C	SA	SA	NC	NC	NC
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

Notes: 1. \* Checked No Connect(NC) pin is reserved for higher density address, i.e. 2A for 72Mb.  
2.  $\overline{NW}_0$  controls write to D0:D3 and  $\overline{NW}_1$  controls write to D4:D7.

**PIN NAME**

SYMBOL	PIN NUMBERS	DESCRIPTION	NOTE
K, $\overline{K}$	6B, 6A	Input Clock	
C, $\overline{C}$	6P, 6R	Input Clock for Output Data	1
CQ, $\overline{CQ}$	11A, 1A	Output Echo Clock	
$\overline{Doff}$	1H	DLL Disable when low	
SA	3A,9A,10A,4B,8B,5C,7C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R	Address Inputs	
D0-7	11M,11J,10E,11C,2D,2G,3L,2N	Data Inputs	
Q0-7	11L,10J,11E,11B,3E,3G,2L,3P	Data Outputs	
$\overline{W}$	4A	Write Control Pin,active when low	
$\overline{R}$	8A	Read Control Pin,active when low	
$\overline{NW}_0, \overline{NW}_1$	7B, 5A	Nybble Write Control Pin,active when low	
V <sub>REF</sub>	2H,10H	Input Reference Voltage	
ZQ	11H	Output Driver Impedance Control Input	2
V <sub>DD</sub>	5F,7F,5G,7G,5H,7H,5J,7J,5K,7K	Power Supply ( 1.8 V )	
V <sub>DDQ</sub>	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output Power Supply ( 1.5V or 1.8V )	
V <sub>SS</sub>	2A,4C,8C,4D-8D,5E-7E,6F,6G,6H,6J,6K,5L-7L,4M-8M,4N,8N	Ground	
TMS	10R	JTAG Test Mode Select	
TDI	11R	JTAG Test Data Input	
TCK	2R	JTAG Test Clock	
TDO	1R	JTAG Test Data Output	
NC	7A,1B,2B,3B,5B,9B,10B,1C,2C,3C,6C,9C,10C,1D,3D,9D,10D,11D,1E,2E,9E,1F,2F,3F,9F,11F,1G,9G,10G,11G,1J,2J,3J,9J,1K,2K,3K,10K,11K,9L,1L,9L,10L,1M,2M,3M,9M,10M,1N,3N,9N,10N,11N,1P,2P,9P,10P,11P	No Connect	3

Notes: 1. C,  $\overline{C}$ , K or  $\overline{K}$  cannot be set to V<sub>REF</sub> voltage.

2. When ZQ pin is directly connected to V<sub>DD</sub> output impedance is set to minimum value and it cannot be connected to ground or left unconnected.  
3. Not connected to chip pad internally.

## GENERAL DESCRIPTION

The K7R323684M, K7R321884M and K7R320884M are 37,748,736-bits QDR(Quad Data Rate) Synchronous Pipelined Burst SRAMs.

They are organized as 1,048,576 words by 36bits for K7R323684M, 2,097,152 words by 18 bits for K7R321884M and 4,194,304 words by 8bits for K7R320884M.

The QDR operation is possible by supporting DDR read and write operations through separate data output and input ports with the same cycle. Memory bandwidth is maximized as data can be transferred into sram on every rising edge of K and  $\overline{K}$ , and transferred out of sram on every rising edge of C and  $\overline{C}$ . And totally independent read and write ports eliminate the need for high speed bus turn around.

Address for read and write are latched on alternate rising edges of the input clock K. Data inputs, and all control signals are synchronized to the input clock ( K or  $\overline{K}$  ). Normally data outputs are synchronized to output clocks ( C and  $\overline{C}$  ), but when C and  $\overline{C}$  are tied high, the data outputs are synchronized to the input clocks ( K and  $\overline{K}$  ). Read data are referenced to echo clock ( CQ or  $\overline{CQ}$  ) outputs.

Common address bus is used to access address both for read and write operations.

The internal burst counter is fixed to 4-bit sequential for both read and write operations, requiring two full clock bus cycles. Any request that attempts to interrupt a burst operation in progress is ignored.

Synchronous pipeline read and late write enable high speed operations.

Simple depth expansion is accomplished by using  $\overline{R}$  and  $\overline{W}$  for port selection.

Byte write operation is supported with  $\overline{BW_0}$  and  $\overline{BW_1}$  (  $\overline{BW_2}$  and  $\overline{BW_3}$  ) pins.

Nybble write operation is supported with  $\overline{NW_0}$  and  $\overline{NW_1}$  pins for x8 device.

IEEE 1149.1 serial boundary scan (JTAG) simplifies monitoring package pads attachment status with system.

The K7R323684M, K7R321884M and K7R320884M are implemented with SAMSUNG's high performance 6T CMOS technology and is available in 165pin FBGA packages. Multiple power and ground pins minimize ground bounce.

## Read Operations

Read cycles are initiated by activating  $\overline{R}$  at the rising edge of the positive input clock K. Address is presented and stored in the read address register synchronized with K clock.

For 4-bit burst DDR operation, it will access four 36-bit or 18-bit or 8-bit data words with each read command.

The first pipelined data is transferred out of the device triggered by  $\overline{C}$  clock following next  $\overline{K}$  clock rising edge.

Next burst data is triggered by the rising edge of following C clock rising edge.

The process continues until all four data are transferred.

Continuous read operations are initiated with K clock rising edge.

And pipelined data are transferred out of device on every rising edge of both C and  $\overline{C}$  clocks.

In case C and  $\overline{C}$  tied to high, output data are triggered by K and  $\overline{K}$  instead of C and  $\overline{C}$ .

When the  $\overline{R}$  is disabled after a read operation, the K7R323684M, K7R321884M and K7R320884M will first complete burst read operation

before entering into deselect mode at the next K clock rising edge.

Then output drivers disabled automatically to high impedance state.

## Echo clock operation

To assure the output traceability, the SRAM provides the output Echo clock, pair of complement clock CQ and  $\overline{CQ}$ , which are synchronized with internal data output.

Echo clocks run free during normal operation.

The Echo clock is triggered by internal output clock signal, and transferred to external through same structures as output driver.

## Write Operations

Write cycles are initiated by activating  $\overline{W}$  at the rising edge of the positive input clock K. Address is presented and stored in the write address register synchronized with K clock.

For 4-bit burst DDR operation, it will write four 36-bit or 18-bit or 8-bit data words with each write command. The first "late" data is transferred and registered in to the device synchronous with next K clock rising edge. Next burst data is transferred and registered synchronous with following  $\overline{K}$  clock rising edge. The process continues until all four data are transferred and registered.

Continuous write operations are initiated with K rising edge. And "late written" data is presented to the device on every rising edge of both K and  $\overline{K}$  clocks.

The device disregards input data presented on the same cycle  $\overline{W}$  disabled. When the  $\overline{W}$  is disabled after a read operation, the K7R323684M, K7R321884M and K7R320884M will first complete burst read operation before entering into deselect mode at the next K clock rising edge.

The K7R323684M and K7R321884M support byte write operations. With activating  $\overline{BW}_0$  or  $\overline{BW}_1$  ( $\overline{BW}_2$  or  $\overline{BW}_3$ ) in write cycle, only one byte of input data is presented. In K7R321884M,  $\overline{BW}_0$  controls write operation to D0:D8,  $\overline{BW}_1$  controls write operation to D9:D17. And in K7R323684M  $\overline{BW}_2$  controls write operation to D18:D26,  $\overline{BW}_3$  controls write operation to D27:D35. The the K7R320884M support nybble write operations. In K7R320884M,  $\overline{NW}_0$  controls write operation to D0:D3,  $\overline{NW}_1$  controls write operation to D4:D7.

## Programmable Impedance Output Buffer Operation

The designer can program the SRAM's output buffer impedance by terminating the ZQ pin to V<sub>SS</sub> through a precision resistor(R<sub>Q</sub>). The value of R<sub>Q</sub> (within 15%) is five times the output impedance desired.

For example, 250Ω resistor will give an output impedance of 50Ω. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles. In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM.

There are no power up requirements for the SRAM. However, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

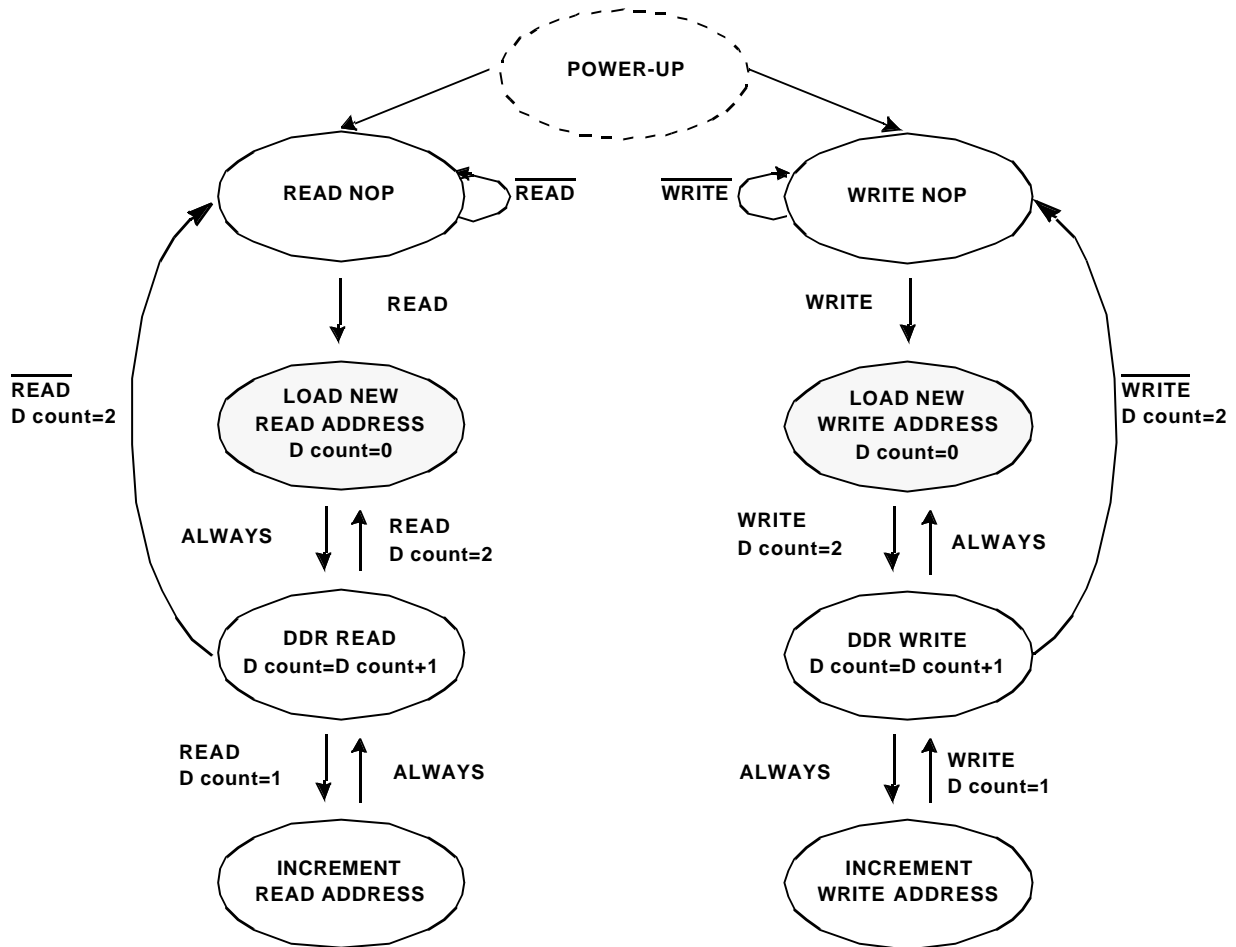
## Single Clock Mode

The K7R323684M, K7R321884M and K7R320884M can be operated with the single clock pair K and  $\overline{K}$ , instead of C or  $\overline{C}$  for output clocks. To operate these devices in single clock mode, C and  $\overline{C}$  must be tied high during power up and must be maintained high during operation. After power up, this device can't change to or from single clock mode. System flight time and clock skew could not be compensated in this mode.

## Depth Expansion

Separate input and output ports enables easy depth expansion. Each port can be selected and deselected independently and read and write operation do not affect each other. Before chip deselected, all read and write pending operations are completed.

STATE DIAGRAM



- Notes:**
1. Internal burst counter is fixed as 2-bit linear, i.e. when first address is A0+0, next internal burst address is A0+1.
  2. "READ" refers to read active status with  $\overline{R}$ =Low, " $\overline{\text{READ}}$ " refers to read inactive status with  $\overline{R}$ =high. "WRITE" and " $\overline{\text{WRITE}}$ " are the same case.
  3. Read and write state machine can be active simultaneously.
  4. State machine control timing sequence is controlled by K.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

K	$\bar{R}$	$\bar{W}$	D				Q				OPERATION
			D(A1)	D(A2)	D(A3)	D(A4)	Q(A1)	Q(A2)	Q(A3)	Q(A4)	
Stopped	X	X	Previous state	Previous state	Previous state	Previous state	Previous state	Previous state	Previous state	Previous state	Clock Stop
↑	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	No Operation
↑	L <sup>4</sup>	X	X	X	X	X	D <sub>OUT</sub> at $\bar{C}(t+1)$	D <sub>OUT</sub> at C(t+2)	D <sub>OUT</sub> at $\bar{C}(t+2)$	D <sub>OUT</sub> at C(t+3)	Read
↑	H <sup>5</sup>	L <sup>4</sup>	D <sub>in</sub> at K(t+1)	D <sub>in</sub> at $\bar{K}(t+1)$	D <sub>in</sub> at K(t+2)	D <sub>in</sub> at $\bar{K}(t+2)$	X	X	X	X	Write

Notes: 1. X means "Don't Care".

2. The rising edge of clock is symbolized by (↑).

3. Before enter into clock stop status, all pending read and write operations will be completed.

4. This signal was HIGH on previous K clock rising edge. Initiating consecutive READ or WRITE operations on consecutive K clock rising edges is not permitted. The device will ignore the second request.

5. If this signal was LOW to initiate the previous cycle, this signal becomes a don't care for this operation however it is strongly recommended that this signal is brought HIGH as shown in the truth table.

WRITE TRUTH TABLE<sub>(x18)</sub>

K	$\bar{K}$	$\bar{BW}_0$	$\bar{BW}_1$	OPERATION
↑		L	L	WRITE ALL BYTES (K↑)
	↑	L	L	WRITE ALL BYTES ( $\bar{K}$ ↑)
↑		L	H	WRITE BYTE 0 (K↑)
	↑	L	H	WRITE BYTE 0 ( $\bar{K}$ ↑)
↑		H	L	WRITE BYTE 1 (K↑)
	↑	H	L	WRITE BYTE 1 ( $\bar{K}$ ↑)
↑		H	H	WRITE NOTHING (K↑)
	↑	H	H	WRITE NOTHING ( $\bar{K}$ ↑)

Notes: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of input clock K or  $\bar{K}$  (↑).

3. Assumes a WRITE cycle was initiated.

4. This table illustrates operation for x18 devices. x8 device operation is similar except that  $\bar{NW}_0$  controls D0:D3 and  $\bar{NW}_1$  controls D4:D7.

WRITE TRUTH TABLE<sub>(x36)</sub>

K	$\bar{K}$	$\bar{BW}_0$	$\bar{BW}_1$	$\bar{BW}_2$	$\bar{BW}_3$	OPERATION
↑		L	L	L	L	WRITE ALL BYTES (K↑)
	↑	L	L	L	L	WRITE ALL BYTES ( $\bar{K}$ ↑)
↑		L	H	H	H	WRITE BYTE 0 (K↑)
	↑	L	H	H	H	WRITE BYTE 0 ( $\bar{K}$ ↑)
↑		H	L	H	H	WRITE BYTE 1 (K↑)
	↑	H	L	H	H	WRITE BYTE 1 ( $\bar{K}$ ↑)
↑		H	H	L	L	WRITE BYTE 2 and BYTE 3 (K↑)
	↑	H	H	L	L	WRITE BYTE 2 and BYTE 3 ( $\bar{K}$ ↑)
↑		H	H	H	H	WRITE NOTHING (K↑)
	↑	H	H	H	H	WRITE NOTHING ( $\bar{K}$ ↑)

Notes: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of input clock K or  $\bar{K}$  (↑).

3. Assumes a WRITE cycle was initiated.

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on VDD Supply Relative to VSS	VDD	-0.5 to 2.9	V
Voltage on VDDQ Supply Relative to VSS	VDDQ	-0.5 to VDD	V
Voltage on Input Pin Relative to VSS	VIN	-0.5 to VDD+0.3	V
Power Dissipation	Pd	TBD	W
Storage Temperature	TSTG	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

\*Note: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.  
2. VDDQ must not exceed VDD during normal operation.

**DC ELECTRICAL CHARACTERISTICS**(VDD=1.8V ±0.1V, TA=0°C to +70°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	NOTES	
Input Leakage Current	IIL	VDD=Max ; VIN=VSS to VDDQ	-2	+2	µA		
Output Leakage Current	IOL	Output Disabled,	-2	+2	µA		
Operating Current (x36): DDR	ICC	VDD=Max , IOUT=0mA Cycle Time ≥ tKHKH Min	-25	-	800	mA	1,5
			-20	-	700		
			-16	-	600		
Operating Current (x18): DDR	ICC	VDD=Max , IOUT=0mA Cycle Time ≥ tKHKH Min	-25	-	750	mA	1,5
			-20	-	650		
			-16	-	550		
Operating Current (x8): DDR	ICC	VDD=Max , IOUT=0mA Cycle Time ≥ tKHKH Min	-25	-	730	mA	1,5
			-20	-	630		
			-16	-	530		
Standby Current(NOP): DDR	ISB1	Device deselected, IOUT=0mA, f=Max, All Inputs ≤ 0.2V or ≥ VDD-0.2V	-25	-	330	mA	1,6
			-20	-	300		
			-16	-	270		
Output High Voltage	VOH1		VDDQ/2-0.12	VDDQ/2+0.12	V	2,7	
Output Low Voltage	VOL1		VDDQ/2-0.12	VDDQ/2+0.12	V	3,7	
Output High Voltage	VOH2	I <sub>OH</sub> =-1.0mA	VDDQ-0.2	VDDQ	V	4	
Output Low Voltage	VOL2	I <sub>OL</sub> =1.0mA	VSS	0.2	V	4	
Input Low Voltage	VIL		-0.3	VREF-0.1	V	8,9	
Input High Voltage	VIH		VREF+0.1	VDDQ+0.3	V	8,10	

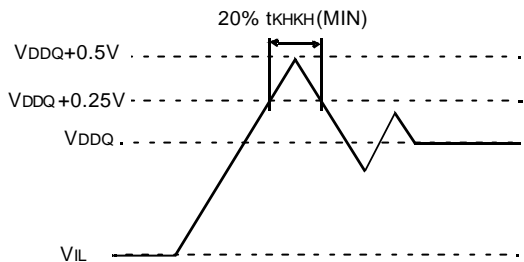
Notes: 1. Minimum cycle. IOUT=0mA.  
2. |I<sub>OH</sub>|=(VDDQ/2)/(RQ/5) for 175Ω ≤ RQ ≤ 350Ω.  
3. |I<sub>OL</sub>|=(VDDQ/2)/(RQ/5) for 175Ω ≤ RQ ≤ 350Ω.  
4. Minimum Impedance Mode when ZQ pin is connected to VDDQ.  
5. Operating current is calculated with 50% read cycles and 50% write cycles.  
6. Standby Current is only after all pending read and write burst operations are completed.  
7. Programmable Impedance Mode.  
8. These are DC test criteria. DC design criteria is VREF±50mV. The AC VIH/VIL levels are defined separately for measuring timing parameters.  
9. VIL (Min)DC=-0.3V, VIL (Min)AC=-1.5V(pulse width ≤ 3ns).  
10. VIH (Max)DC=VDDQ+0.3, VIH (Max)AC=VDDQ+0.85V(pulse width ≤ 3ns).

**AC ELECTRICAL CHARACTERISTICS** ( $V_{DD}=1.8V \pm 0.1V$ ,  $T_A=0^\circ C$  to  $+70^\circ C$ )

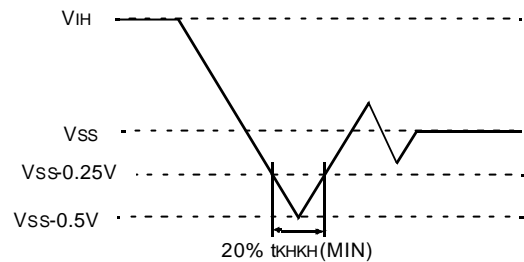
PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Input High Voltage	$V_{IH} (AC)$	$V_{REF} + 0.2$	-	V	1,2
Input Low Voltage	$V_{IL} (AC)$	-	$V_{REF} - 0.2$	V	1,2

- Notes:** 1. This condition is for AC function test only, not for AC parameter test.  
 2. To maintain a valid level, the transitioning edge of the input must :  
 a) Sustain a constant slew rate from the current AC level through the target AC level,  $V_{L(AC)}$  or  $V_{H(AC)}$   
 b) Reach at least the target AC level  
 c) After the AC target level is reached, continue to maintain at least the target DC level,  $V_{L(DC)}$  or  $V_{H(DC)}$

**Overshoot Timing**



**Undershoot Timing**



**Note:** For power-up,  $V_{IH} \leq V_{DDQ}+0.3V$  and  $V_{DD} \leq 1.7V$  and  $V_{DDQ} \leq 1.4V$   $t \leq 200ms$

**OPERATING CONDITIONS** ( $0^\circ C \leq T_A \leq 70^\circ C$ )

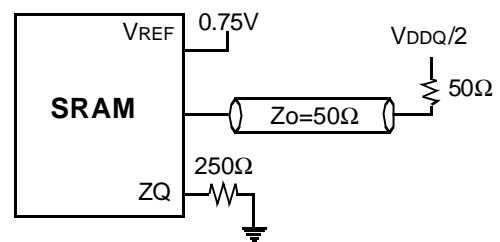
PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	VDD	1.7	1.9	V
	VDDQ	1.4	1.9	V
Reference Voltage	VREF	0.68	0.95	V
Ground	VSS	0	0	V

**AC TEST CONDITIONS**

Parameter	Symbol	Value	Unit
Core Power Supply Voltage	VDD	1.7~1.9	V
Output Power Supply Voltage	VDDQ	1.4~1.9	V
Input High/Low Level	$V_{IH}/V_{IL}$	1.25/0.25	V
Input Reference Level	VREF	0.75	V
Input Rise/Fall Time	$T_R/T_F$	0.3/0.3	ns
Output Timing Reference Level		$V_{DDQ}/2$	V

**Note:** Parameters are tested with  $R_Q=250\Omega$

**AC TEST OUTPUT LOAD**



AC TIMING CHARACTERISTICS (V<sub>DD</sub>=1.8V±0.1V, T<sub>A</sub>=0°C to +70°C)

PARAMETER	SYMBOL	-25		-20		-16		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
<b>Clock</b>									
Clock Cycle Time (K, $\bar{K}$ , C, $\bar{C}$ )	tkHKH	4.00	6.30	5.00	7.88	6.00	8.40	ns	
Clock Phase Jitter (K, $\bar{K}$ , C, $\bar{C}$ )	tkC var		0.20		0.20		0.20	ns	5
Clock High Time (K, $\bar{K}$ , C, $\bar{C}$ )	tkHKL	1.60		2.00		2.40		ns	
Clock Low Time (K, $\bar{K}$ , C, $\bar{C}$ )	tkLKH	1.60		2.00		2.40		ns	
Clock to $\bar{C}$ lock (K↑ → $\bar{K}$ ↑, C↑ → $\bar{C}$ ↑)	tkHKH	1.80		2.20		2.70		ns	
Clock to data clock (K↑ → C↑, $\bar{K}$ ↑ → $\bar{C}$ ↑)	tkHCH	0.00	1.80	0.00	2.30	0.00	2.80	ns	
DLL Lock Time (K, C)	tkC lock	1024		1024		1024		cycle	6
K Static to DLL reset	tkC reset	30		30		30		ns	
<b>Output Times</b>									
C, $\bar{C}$ High to Output Valid	tCHQV		0.45		0.45		0.50	ns	3
C, $\bar{C}$ High to Output Hold	tCHQX	-0.45		-0.45		-0.50		ns	3
C, $\bar{C}$ High to Echo Clock Valid	tCHCQV		0.45		0.45		0.50	ns	
C, $\bar{C}$ High to Echo Clock Hold	tCHCQX	-0.45		-0.45		-0.50		ns	
CQ, $\bar{CQ}$ High to Output Valid	tCQHQV		0.30		0.35		0.40	ns	7
CQ, $\bar{CQ}$ High to Output Hold	tCQHQX	-0.30		-0.35		-0.40		ns	7
C, High to Output High-Z	tCHQZ		0.45		0.45		0.50	ns	3
C, High to Output Low-Z	tCHQX1	-0.45		-0.45		-0.50		ns	3
<b>Setup Times</b>									
Address valid to K rising edge	tAVKH	0.50		0.60		0.70		ns	
Control inputs valid to K rising edge	tIVKH	0.50		0.60		0.70		ns	2
Data-in valid to K, $\bar{K}$ rising edge	tDVKH	0.35		0.40		0.50		ns	
<b>Hold Times</b>									
K rising edge to address hold	tkHAX	0.50		0.60		0.70		ns	
K rising edge to control inputs hold	tkHIX	0.50		0.60		0.70		ns	
K, $\bar{K}$ rising edge to data-in hold	tkHDX	0.35		0.40		0.50		ns	

- Notes:** 1. All address inputs must meet the specified setup and hold times for all latching clock edges.  
 2. Control signals are  $\bar{R}$ ,  $\bar{W}$ ,  $\bar{BW}_0$ ,  $\bar{BW}_1$  and ( $\bar{NW}_0$ ,  $\bar{NW}_1$ , for x8) and ( $\bar{BW}_2$ ,  $\bar{BW}_3$ , also for x36)  
 3. If C,  $\bar{C}$  are tied high, K,  $\bar{K}$  become the references for C,  $\bar{C}$  timing parameters.  
 4. To avoid bus contention, at a given voltage and temperature tCHQX1 is bigger than tCHQZ.  
 The specs as shown do not imply bus contention because tCHQX1 is a MIN parameter that is worst case at totally different test conditions (0°C, 1.9V) than tCHQZ, which is a MAX parameter (worst case at 70°C, 1.7V)  
 It is not possible for two SRAMs on the same board to be at such different voltage and temperature.  
 5. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.  
 6. V<sub>DD</sub> slew rate must be less than 0.1V DC per 50 ns for DLL lock retention. DLL lock time begins once V<sub>DD</sub> and input clock are stable.  
 7. Echo clock is very tightly controlled to data valid/data hold. By design, there is a ±0.1 ns variation from echo clock to data.  
 The data sheet parameters reflect tester guardbands and test setup variations.

PIN CAPACITANCE

PRMETER	SYMBOL	TESTCONDITION	TYP	MAX	Unit	NOTES
Address Control Input Capacitance	CIN	VIN=0V	4	5	pF	
Input and Output Capacitance	COUT	VOUT=0V	6	7	pF	
Clock Capacitance	CCLK	-	5	6	pF	

Note: 1. Parameters are tested with RQ=250Ω and VDDQ=1.5V.  
2. Periodically sampled and not 100% tested.

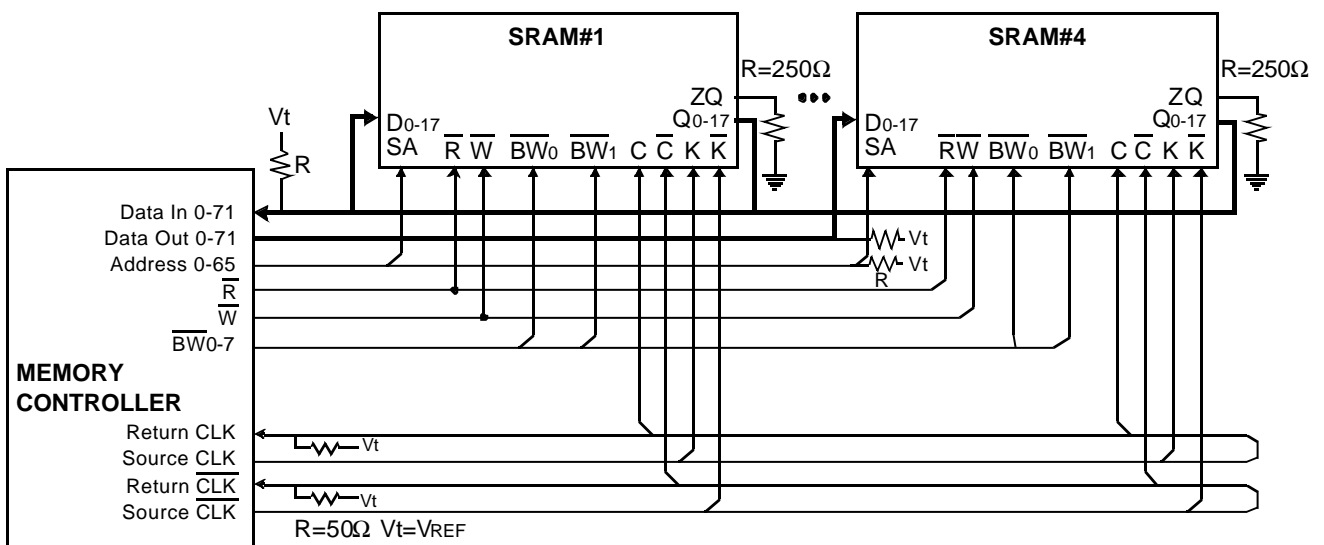
THERMAL RESISTANCE

PRMETER	SYMBOL	TYP	Unit	NOTES
Junction to Ambient	θJA	TBD	°C/W	
Junction to Case	θJC	TBD	°C/W	
Junction to Pins	θJB	TBD	°C/W	

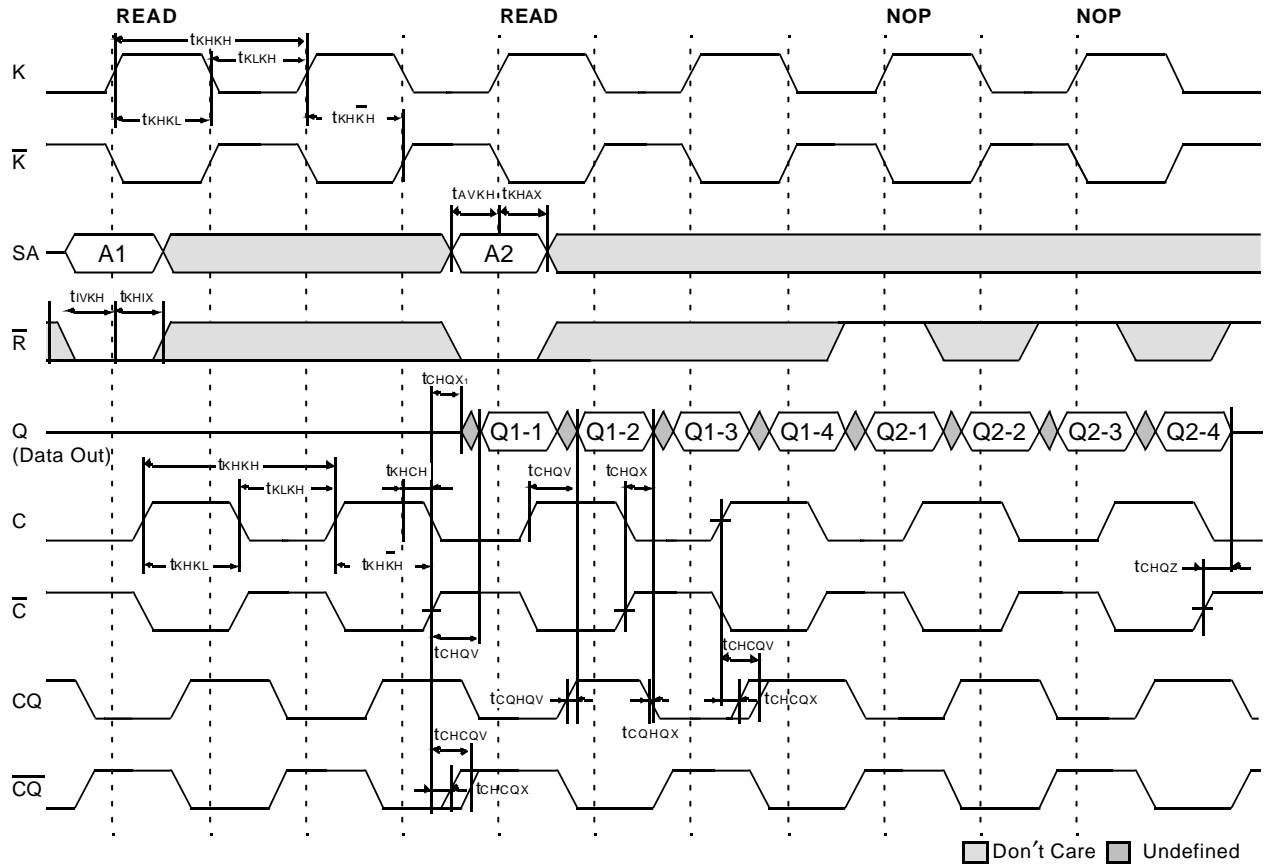
Note: Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance.  $T_J = T_A + P_D \times \theta_{JA}$

APPLICATION INFORMATION

2Mx18

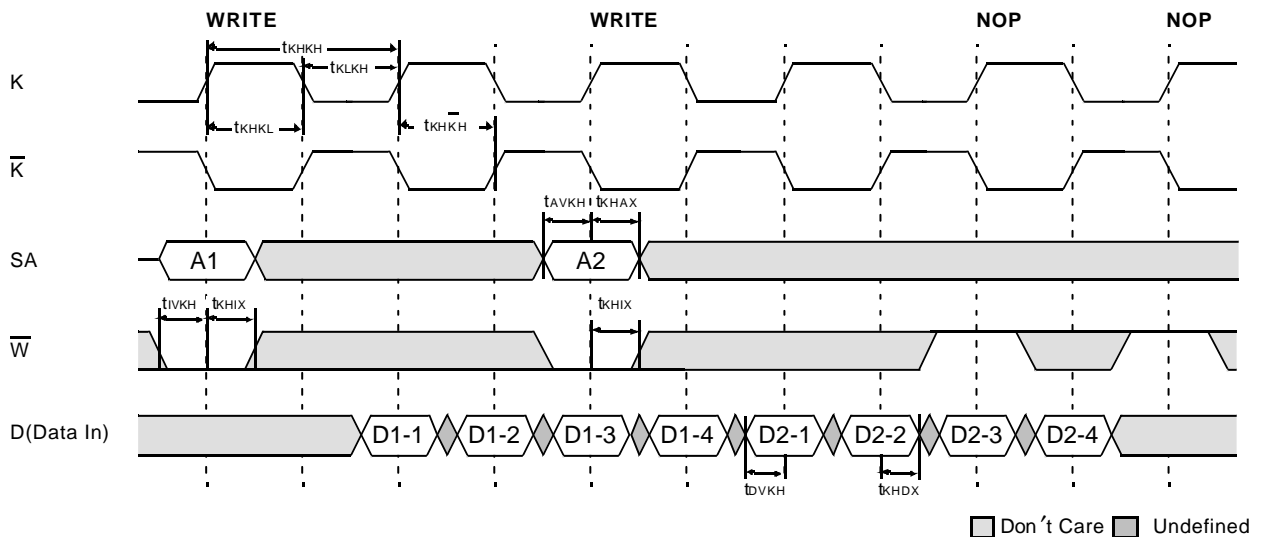


TIMING WAVE FORMS OF READ AND NOP



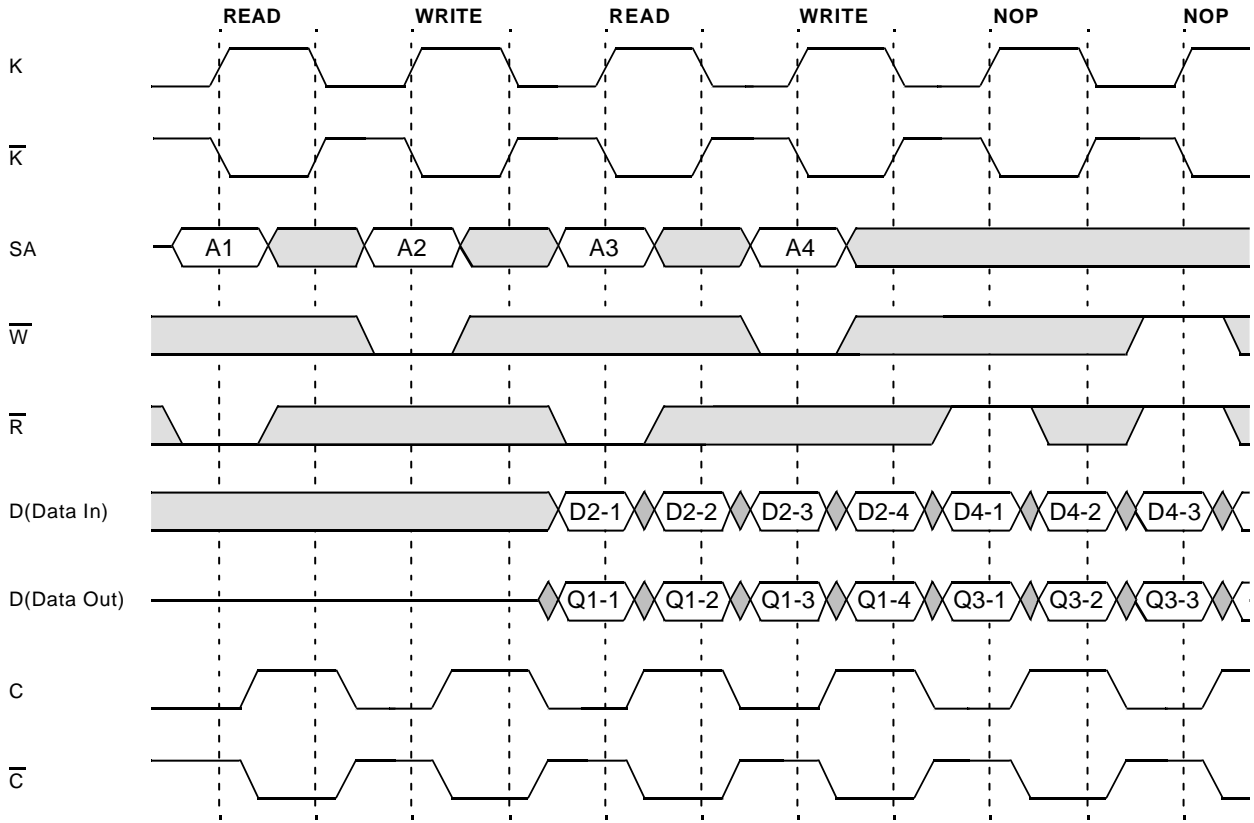
Note: 1. Q1-1 refers to output from address A1+0, Q1-2 refers to output from address A1+1 i.e. the next internal burst address following A1+0.  
 2. Outputs are disabled one cycle after a NOP.

TIMING WAVE FORMS OF WRITE AND NOP



Note: 1. D1-1 refers to input to address A1+0, D1-2 refers to input to address A1+1, i.e. the next internal burst address following A1+0.  
 2.  $\overline{BWx}$  ( $\overline{NWx}$ ) assumed active.

TIMING WAVE FORMS OF READ, WRITE AND NOP



**Note:** 1. If address A3=A2, data Q3-1=D2-1, data Q3-2=D2-2, data Q3-3=D2-3, data Q3-4=D2-4

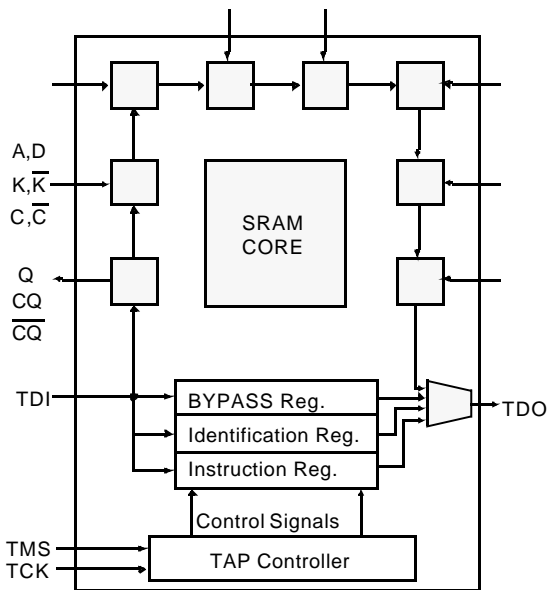
Write data is forwarded immediately as read results.

2.  $\bar{BWX}$  ( $\bar{NWX}$ ) assumed active.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



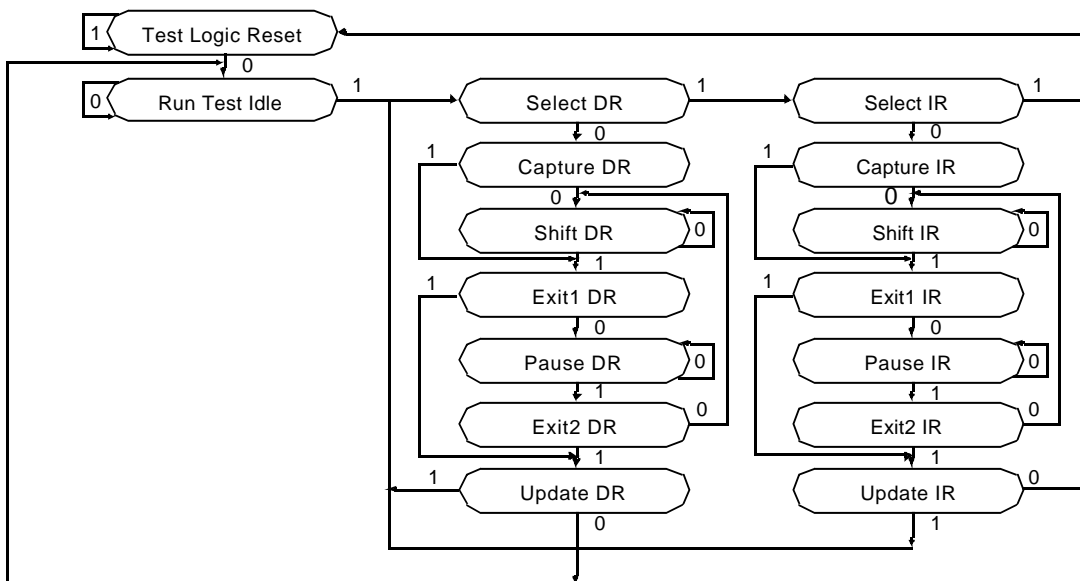
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	RESERVED	Do Not Use	6
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	RESERVED	Do Not Use	6
1	1	1	BYPASS	Bypass Register	4

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

TAP Controller State Diagram





**SCAN REGISTER DEFINITION**

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
1Mx36	3 bits	1 bit	32 bits	109 bits
2Mx18	3 bits	1 bit	32 bits	109 bits
4Mx8	3 bits	1 bit	32 bits	109 bits

**ID REGISTER DEFINITION**

Part	Revision Number (31:29)	Part Configuration (28:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
1Mx36	000	00def0wx0t0q0b0s0	00001001110	1
2Mx18	000	00def0wx0t0q0b0s0	00001001110	1
4Mx8	000	00def0wx0t0q0b0s0	00001001110	1

Note : Part Configuration

/def=010 for 36Mb, /wx=11 for x36, 10 for x18, 01 for x8

/t=1 for DLL Ver., 0 for non-DLL Ver. /q=1 for QDR, 0 for DDR /b=1 for 4Bit Burst, 0 for 2Bit Burst /s=1 for Separate I/O, 0 for Common I/O

**BOUNDARY SCAN EXIT ORDER**

ORDER	PIN ID
1	6R
2	6P
3	6N
4	7P
5	7N
6	7R
7	8R
8	8P
9	9R
10	11P
11	10P
12	10N
13	9P
14	10M
15	11N
16	9M
17	9N
18	11L
19	11M
20	9L
21	10L
22	11K
23	10K
24	9J
25	9K
26	10J
27	11J
28	11H
29	10G
30	9G
31	11F
32	11G
33	9F
34	10F
35	11E
36	10E

ORDER	PIN ID
37	10D
38	9E
39	10C
40	11D
41	9C
42	9D
43	11B
44	11C
45	9B
46	10B
47	11A
48	10A
49	9A
50	8B
51	7C
52	6C
53	8A
54	7A
55	7B
56	6B
57	6A
58	5B
59	5A
60	4A
61	5C
62	4B
63	3A
64	2A
65	1A
66	2B
67	3B
68	1C
69	1B
70	3D
71	3C
72	1D

ORDER	PIN ID
73	2C
74	3E
75	2D
76	2E
77	1E
78	2F
79	3F
80	1G
81	1F
82	3G
83	2G
84	1H
85	1J
86	2J
87	3K
88	3J
89	2K
90	1K
91	2L
92	3L
93	1M
94	1L
95	3N
96	3M
97	1N
98	2M
99	3P
100	2N
101	2P
102	1P
103	3R
104	4R
105	4P
106	5P
107	5N
108	5R
109	Internal

Note: 1. NC pins are read as "X" (i.e. don't care.)

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD	1.7	1.8	1.9	V	
Input High Level	VIH	1.3	-	VDD+0.3	V	
Input Low Level	VIL	-0.3	-	0.5	V	
Output High Voltage(IoH=-2mA)	VOH	1.4	-	VDD	V	
Output Low Voltage(IoL=2mA)	VOL	VSS	-	0.4	V	

Note: 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

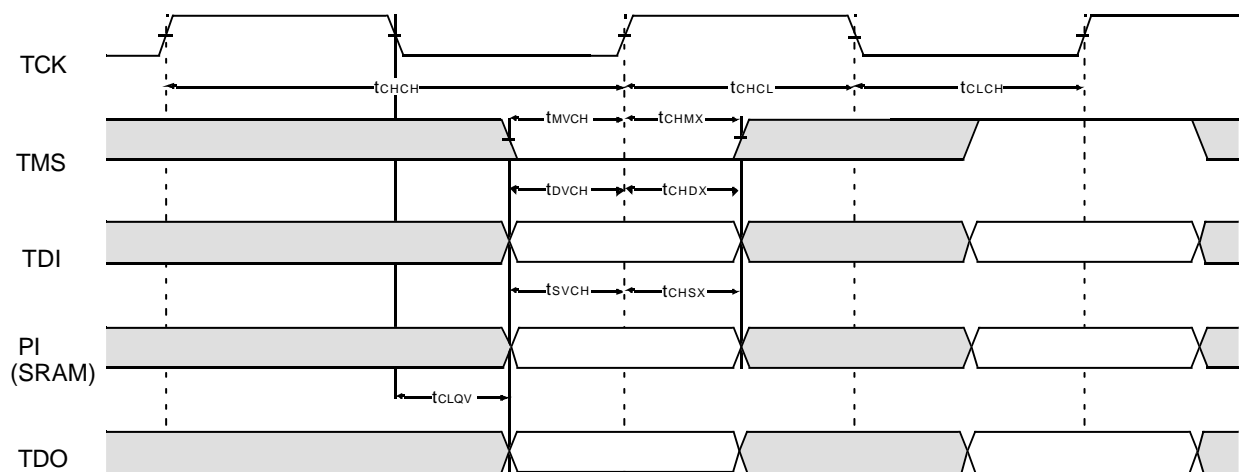
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	VIH/VIL	1.3/0.5	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		0.9	V	1

Note: 1. See SRAM AC test output load on page 11.

JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	tCHCH	50	-	ns	
TCK High Pulse Width	tCHCL	20	-	ns	
TCK Low Pulse Width	tCLCH	20	-	ns	
TMS Input Setup Time	tMVCH	5	-	ns	
TMS Input Hold Time	tCHMX	5	-	ns	
TDI Input Setup Time	tDVCH	5	-	ns	
TDI Input Hold Time	tCHDX	5	-	ns	
SRAM Input Setup Time	tSVCH	5	-	ns	
SRAM Input Hold Time	tCHSX	5	-	ns	
Clock Low to Output Valid	tCLQV	0	10	ns	

JTAG TIMING DIAGRAM



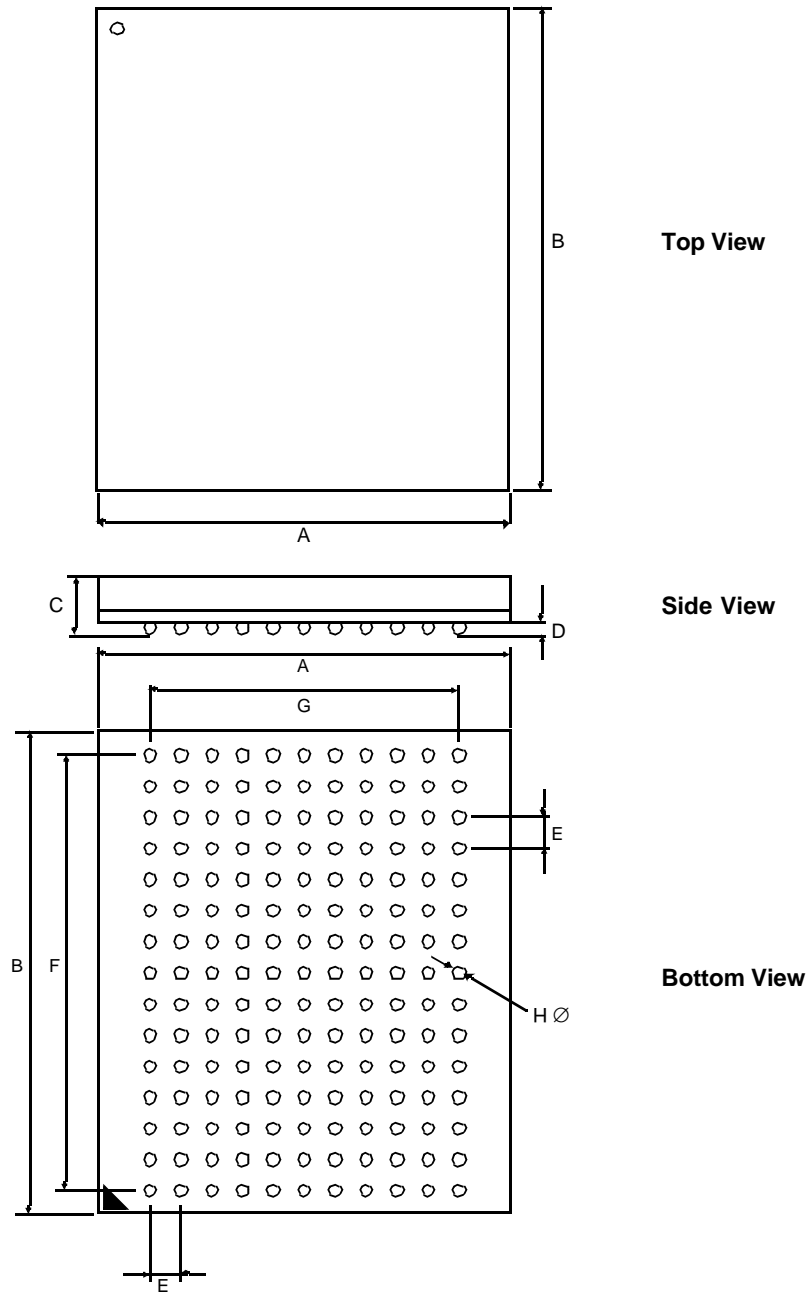
K7R323684M  
 K7R321884M  
 K7R320884M

*Preliminary*

1Mx36 & 2Mx18 & 4Mx8 QDR™ II b4 SRAM

**165 FBGA PACKAGE DIMENSIONS**

15mm x 17mm Body, 1.0mm Bump Pitch, 11x15 Ball Array



Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	15 ± 0.1	mm		E	1.0	mm	
B	17 ± 0.1	mm		F	14.0	mm	
C	1.3 ± 0.1	mm		G	10.0	mm	
D	0.35 ± 0.05	mm		H	0.5 ± 0.05	mm	