256Mb B-die Page NOR FLASH

256M Bit (16M x16, 32M x8), Page Mode

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	Initial draft	May. 07, 2009	Target	-
0.1	- Revised Hardware Sequence Flags Table.	Jun. 02, 2009	Target	-
	- Devide DQ5 and DQ6 in Indicator Bit Codes table. DQ6 indicates Customer Lock bit information.			
1.0	- Specification finalized	Jun. 04, 2010		-

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256M Bit (16M x16, 32Mb x8) Page Mode / Page NOR Flash Memory

1.0 FEATURES

- Single Voltage, 2.7V to 3.6V for Read and Write operations
  Voltage range of 2.7V to 3.1V valid for MCP product
- Organization
  16M x16 bit (Word mode)
  32M x 8 bit (Byte mode)
- Fast Read Access Time : 80ns
- Page Mode Operation
  8 Words Page access allows fast asychronous read
  Page Read Access Time : 30ns
- Read While Program/Erase Operation
- Multiple Bank Architecture (4 Banks)
  Bank 0: 32Mbit (64Kw x 32)
  Bank 1: 96Mbit (64Kw x 96)
  Bank 2: 96Mbit (64Kw x 96)
  Bank 3: 32Mbit (64Kw x 32)
- OTP Block : Extra 256 word
  - 128word for factory and 128word for customer OTP
- Power Consumption (typical value)
  - Active Read Current : 30mA (@5MHz)
  - Program/Erase Current : 25mA
  - Read While Program or Read While Erase Current : 65mA
  - Standby Mode/Auto Sleep Mode : 20uA
- Support Single & 32word Buffer Program
- $\overline{WP}$/ACC input pin
  - Allows special protection of first or last block of flash array at V_{IL}, regardless of block protect status
  - Removes special protection at V_{IH}, the first or last block of flash array return to normal block protect status
  - Reduce program time at V_{HH} : 6us/word at Write Buffer
- Erase Suspend/Resume
- Program Suspend/Resume
- Unlock Bypass Mode
- Hardware $\overline{RESET}$ Pin
- Command Register Operation
- Supports Common Flash Memory Interface
- Industrial Temperature : -40°C to 85°C
- Extended Temperature : -25°C to 85°C
- Endurance : 100Kcycle
- Vio options at 1.8V and 3V I/O
- Package options
  - 56 Pin TSOP (20x14mm)
  - 64 Ball FBGA (11x13, 1.0mm Ball Pitch)

2.0 GENERAL DESCRIPTION

The K8P5616UZB featuring single 3.0V power supply, is an 256Mbit NOR-type Flash Memory organized as 32M x 8 or 16M x16. The memory architecture of the device is designed to divide its memory arrays into 256 blocks with independent hardware protection. This block architecture provides highly flexible erase and program capability. The K8P5616UZB NOR Flash consists of four banks. This device is capable of reading data from one bank while programming or erasing in the other banks.

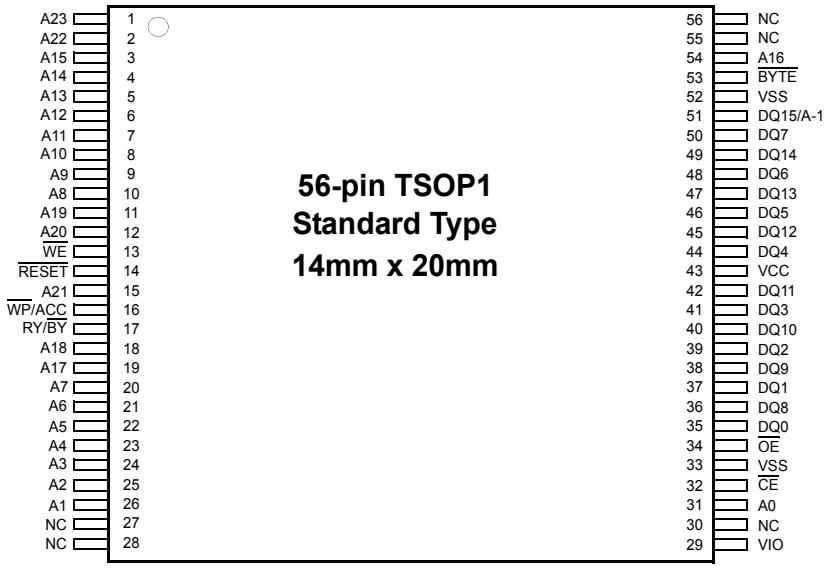
The K8P5616UZB offers page access time of 30ns with random access time of 80ns. The device's fast access times allow high speed microprocessors to operate without wait states. The device performs a program operation in unit of 16 bits (Word) and erases in units of a block. Single or multiple blocks can be erased. The block erase operation is completed within typically 0.7 sec. The device requires 25mA as program/erase current in the commercial and extended temperature ranges.

The K8P5616UZB NOR Flash Memory is created by using Samsung's advanced CMOS process technology. This device is available in 64FBGA and 56 Pin TSOP. The device is compatible with EPROM applications to require high-density and cost-effective nonvolatile read/write storage solutions.

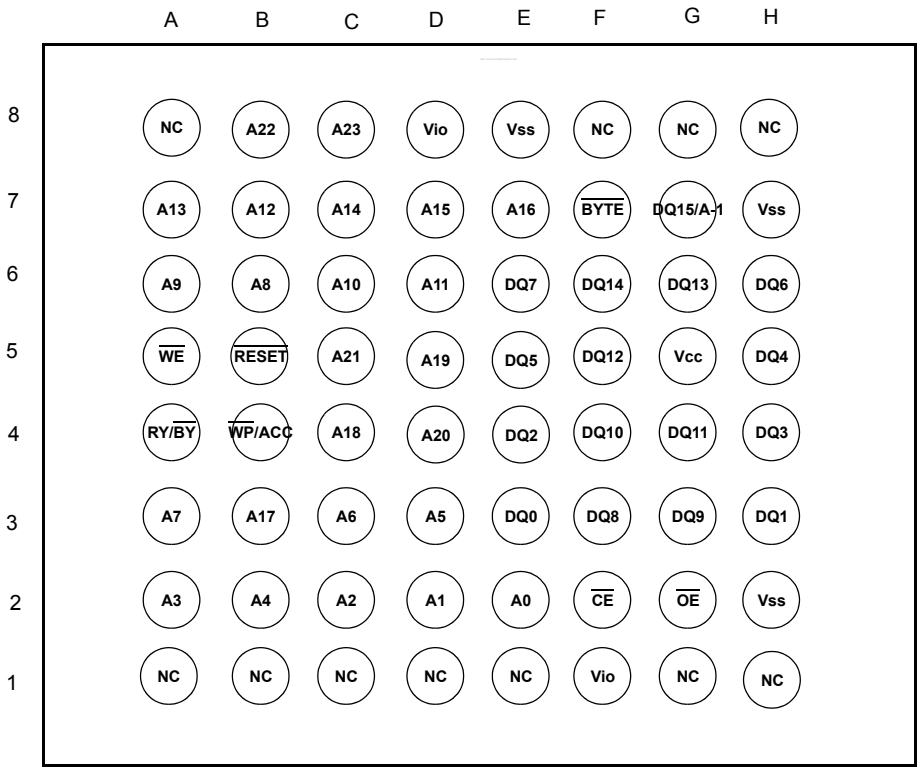
3.0 PIN DESCRIPTION

Pin Name	Pin Function
A0 - A23	Address Inputs
DQ0 - DQ14	Data Inputs / Outputs
DQ15/A-1	DQ15 - Data Inputs / Outputs in word mode A-1 - Address input in byte mode
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{RESET}$	Hardware Reset Pin
$\overline{BYTE}$	Word/Byte selection
RY/$\overline{BY}$	Ready/Busy Output
$\overline{WE}$	Write Enable
$\overline{WP}$/ACC	Hardware Write Protection/Program Acceleration
Vcc	Power Supply
Vss	Ground
NC	No Connection

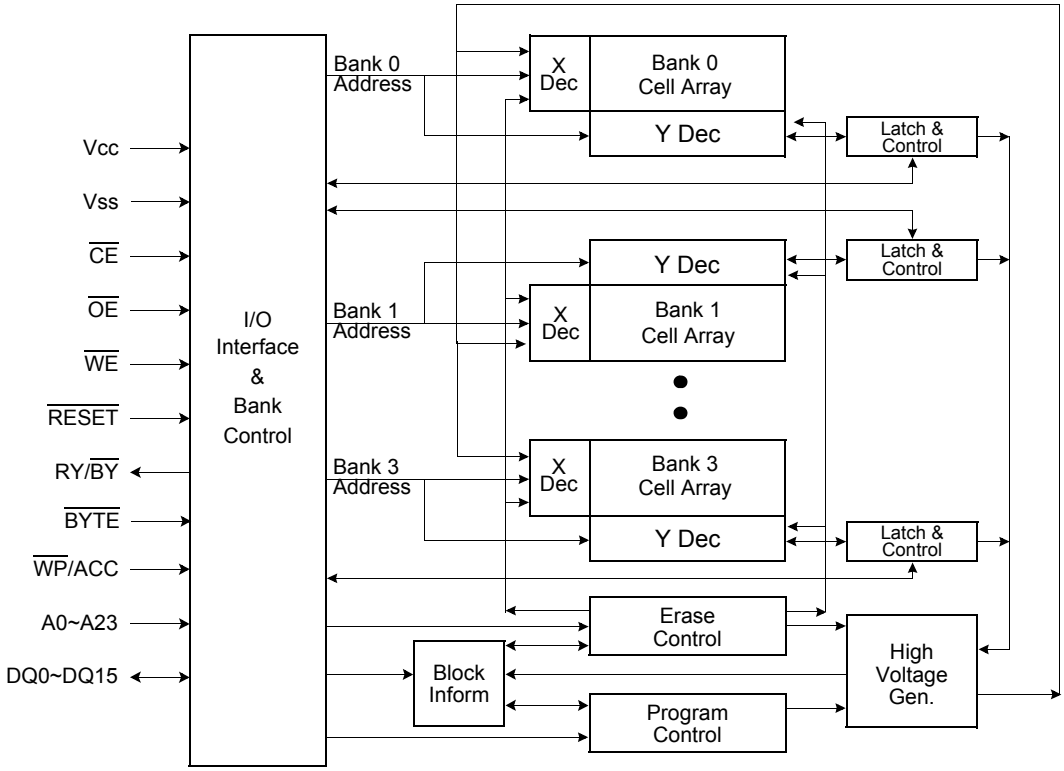
4.0 56TSOP PIN CONFIGURATION



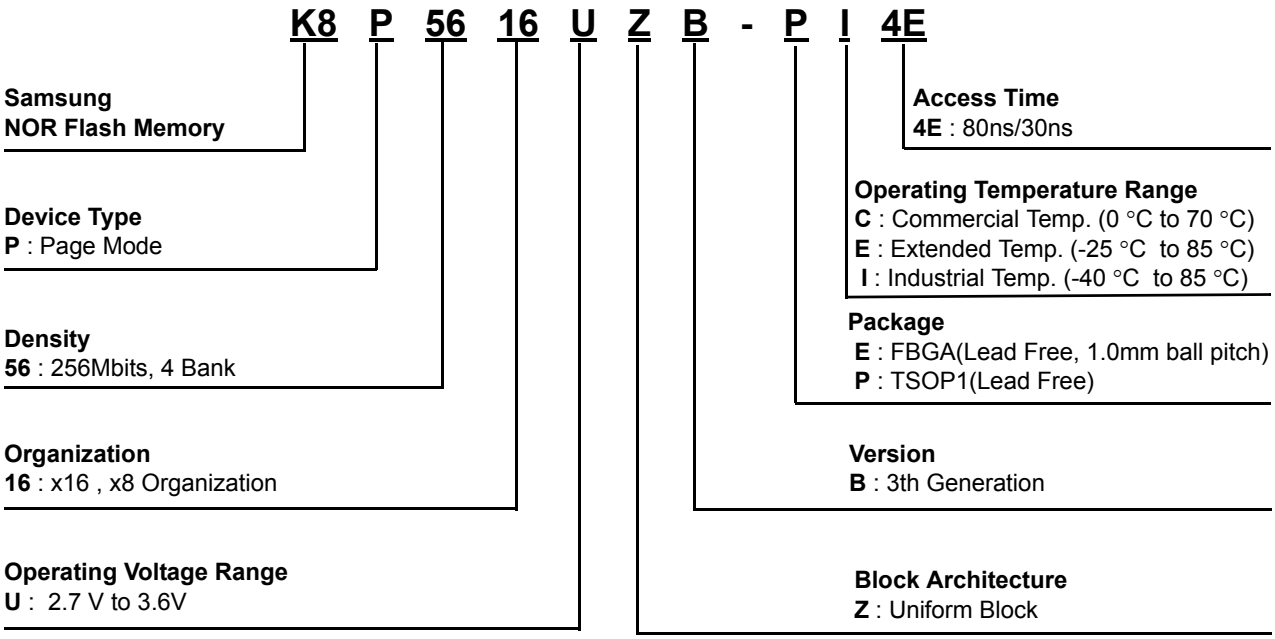
5.0 64 Ball FBGA TOP VIEW (BALL DOWN)



6.0 FUNCTIONAL BLOCK DIAGRAM



7.0 ORDERING INFORMATION



[Table 1] PRODUCT LINE-UP

	4E
Vcc	2.7V~3.6V
VIO	1.7V~Vcc
Max. Address Access Time (ns)	80ns
Max. $\overline{CE}$ Access Time (ns)	80ns
Max. $\overline{OE}$ Access Time (ns)	30ns
Max. Page Access Time (ns)	30ns

[Table 2] K8P5616UZB DEVICE BLOCK DIVISIONS

Bank 0, Bank 3		Bank 1, Bank 2	
Mbit	**Block Sizes**	**Mbit**	**Block Sizes**
32 Mbit	64 Kw x 32	96 Mbit	64 Kw x 96

[Table 3] OTP BLOCK

	Block Address A23~A8	Area	Block Size	Address Range
OTP	0000h	Factory-Locked Area	128 words	000000h-00007Fh
		Customer-Locked Area	128 words	000080h-0000FFh

After entering OTP block, any issued addresses should be in the range of OTP block address

8.0 PRODUCT INTRODUCTION

The K8P5616UZB is 256Mbit NOR-type Flash memory. The device features single voltage power supply operating within the range of 2.7V to 3.6V. The device is programmed by using the Channel Hot Electron (CHE) injection mechanism which is used to program EPROMs. The device is erased electrically by using Fowler-Nordheim tunneling mechanism. To provide highly flexible erase and program capability, the device adapts a block memory architecture that divides its memory array into 256 blocks (64 Kw x 256). Programming is done in units of 16 bits (Word) or 8 bits (Byte). All bits of data in one or multiple blocks can be erased simultaneously when the device executes the erase operation. The device offers page access time of 30ns with random access time of 80ns supporting high speed microprocessors to operate without any wait states.
The command set of K8P5616UZB is fully compatible with standard Flash devices. The device is controlled by chip enable ($\overline{CE}$), output enable ($\overline{OE}$) and write enable ($\overline{WE}$). Device operations are executed by selective command codes. The command codes to be combined with addresses and data are sequentially written to the command registers using microprocessor write timing. The command codes serve as inputs to an internal state machine which controls the program/erase circuitry. Register contents also internally latch addresses and data necessary to execute the program and erase operations. The K8P5616UZB is implemented with Internal Program/Erase Algorithms to execute the program/erase operations. The Internal Program/Erase Algorithms are invoked by program/erase command sequences. The Internal Program Algorithm automatically programs and verifies data at specified addresses. The Internal Erase Algorithm automatically pre-programs the memory cell which is not programmed and then executes the erase operation. The K8P5616UZB has means to indicate the status of completion of program/erase operations. The status can be indicated via the RY/$\overline{BY}$ pin, $\overline{Data}$ polling of DQ7, or the Toggle bit (DQ6). Once the operations have been completed, the device automatically resets itself to the read mode.

[Table 4] Operations Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{WP}$/ACC	A0(A-1) ~ A23	DQ0 ~ DQ7	DQ8 ~ DQ15		$\overline{RESET}$
							$\overline{BYTE}$ = V_{IH}	$\overline{BYTE}$ = V_{IL}	
Read	L	L	H	X	A_{IN}	DOUT	DOUT	DQ8 ~ 14 = High-z DQ15 = A-1	H
Stand-by	Vcc±0.3V	X	X	H	X	High-Z	High-Z	High-Z	Vcc±0.3V
Output Disable	L	H	H	X	X	High-Z	High-Z	High-Z	H
Reset	X	X	X	X	X	High-Z	High-Z	High-Z	L
Write	L	H	L	X[1)]	A_{IN}	DIN	DIN	DQ8 ~ 14 = High-z DQ15 = A-1	H

L = V_{IL} (Low), H = V_{IH} (High), A_{IN} = Address in, D_{IN} = Data in, D_{OUT} = Data out, X = Don't care.

NOTE :
1) $\overline{WP}$/ACC must be V_{IH} when writing on the outermost block. (BA0 or BA255)
2) Address for word mode is AMax:0.
Address for byte mode is AMax:A-1.

9.0 COMMAND DEFINITIONS

The K8P5616UZB operates by selecting and executing its operational modes. Each operational mode has its own command set. In order to select a certain mode, a proper command with specific address and data sequences must be written into the command register. Writing incorrect information which include address and data or writing an improper command will reset the device to the read mode. The defined valid register command sequences are stated in Table 5.

[Table 5] Command Sequences (x16)

Command Sequence		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Read	Addr	1	RA					
	Data		RD					
Reset	Addr	1	XXXH					
	Data		F0H					
Autoselect Manufacturer ID 1), 2)	Addr	4	555H	2AAH	(DA)555H	(DA)X00H		
	Data		AAH	55H	90H	ECH		
Autoselect Device ID 1), 2), 3)	Addr	6	555H	2AAH	(DA)555H	(DA)X01H	(DA)X0EH	(DA)X0FH
	Data		AAH	55H	90H	227EH	2264H	2260H
Autoselect Block Protect Verify 1), 2)	Addr	4	555H	2AAH	(DA)555H	BA / X02H		
	Data		AAH	55H	90H	(SeeTable6)		
Autoselect Indicator Bit 1), 2)	Addr	4	555H	2AAH	(DA)555H	(DA)X03H		
	Data		AAH	55H	90H	(See Table 6)		
Autoselect Master Locking Bit 1), 2)	Addr	4	555H	2AAH	(DA)555H	(DA)X07H		
	Data		AAH	55H	90H	(See Table 6)		
Program	Addr	4	555H	2AAH	555H	PA		
	Data		AAH	55H	A0H	PD		
Write to Buffer 4)	Addr	6	555H	2AAH	BA	BA	WBL	WBL
	Data		AAH	55H	25H	WC	PD	PD
Program Buffer to Flash	Addr	1	BA					
	Data		29H					
Write to Buffer Abort Reset4)	Addr	3	555H	2AAH	555H			
	Data		AAH	55H	F0H			
Unlock Bypass	Addr	3	555H	2AAH	555H			
	Data		AAH	55H	20H			
Unlock Bypass Program	Addr	2	XXXH	PA				
	Data		A0H	PD				
Unlock Bypass Block Erase	Addr	2	XXXH	BA				
	Data		80H	30H				
Unlock Bypass Chip Erase	Addr	2	XXXH	XXXH				
	Data		80H	10H				
Unlock Bypass Reset	Addr	2	XXXH	XXXH				
	Data		90H	00H				
Chip Erase	Addr	6	555H	2AAH	555H	555H	2AAH	555H
	Data		AAH	55H	80H	AAH	55H	10H
Block Erase	Addr	6	555H	2AAH	555H	555H	2AAH	BA
	Data		AAH	55H	80H	AAH	55H	30H
Block Erase Suspend 5), 6)	Addr	1	(DA)XXXH					
	Data		B0H					
Block Erase Resume	Addr	1	(DA)XXXH					
	Data		30H					

Command Definitions		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Program Suspend [7),8)]	Addr	1	(DA)XXXH					
	Data		B0H					
Program Resume	Addr	1	(DA)XXXH					
	Data		30H					
CFI Query [9)]	Addr	1	(DA)X55H					
	Data		98H					
Enter OTP Block Region	Addr	3	555H	2AAH	555H			
	Data		AAH	55H	88H			
OTP Block Program	Addr	4	555H	2AAH	555H	PA		
	Data		AAH	55H	A0H	PD		
OTP Block Read	Addr	1	RA					
	Data		RD					
Exit OTP Block Region	Addr	4	555H	2AAH	555H	XXXH		
	Data		AAH	55H	90H	00H		

NOTE :
- RA : Read Address, PA : Program Address, RD : Read Data, PD : Program Data, WBL : Write Buffer Location
- BA : Block Address (A16 - A23), ABP : Address of the block to be protected or unprotected, X = Don't care ., DA : Bank Address
- DQ8 - DQ15 are don't care in command sequence, except for RD and PD
- A14 - A23 are also don't care, except for the case of special notice.

1) To terminate the Autoselect Mode, it is necessary to write Reset command to the register.
2) The 4th cycle data of Autoselect mode is output data.
3) Device ID must be read across cycles 4, 5 and 6.
   Device ID data : X0EH = "2264H", X0FH = "2260H" for 256Mb Uniform Block Device
4) Command sequence resets device for next command after write-to-buffer operation.
5) The Read / Program operations at non-erasing blocks and the autoselect mode are allowed in the Erase Suspend mode.
6) The Erase Suspend command is applicable only to the Block Erase operation.
7) The Read Operation is allowed in the Program Suspend mode.
8) The Program Suspend command is applicable to Program and Erase Suspend - Program operation.
9) Command is valid when the device is in read mode or Autoselect mode.

[Table 5-1]Command Sequences (x8)

Command Sequence		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Read	Addr	1	RA					
	Data		RD					
Reset	Addr	1	XXXH					
	Data		F0H					
Autoselect Manufacturer ID[1), 2)]	Addr	4	AAAH	555H	(DA)AAAH	(DA)X00H		
	Data		AAH	55H	90H	ECH		
Autoselect Device ID [1), 2), 3)]	Addr	6	AAAH	555H	(DA)AAAH	(DA)X02H	(DA)X1CH	(DA)X1EH
	Data		AAH	55H	90H	XX7EH	XX64H	XX60H
Autoselect Block Protect Verify [1), 2)]	Addr	4	AAAH	555H	(DA)AAAH	BA / X04H		
	Data		AAH	55H	90H	(See Table 6)		
Autoselect Indicator Bit [1), 2)]	Addr	4	AAAH	555H	(DA)AAAH	(DA)X06H		
	Data		AAH	55H	90H	(See Table 6)		
Program	Addr	4	AAAH	555H	AAAH	PA		
	Data		AAH	55H	A0H	PD		
Write to Buffer [4)]	Addr	6	AAAH	555H	BA	BA	WBL	WBL
	Data		AAH	55H	25H	WC	PD	PD
Program Buffer to Flash	Addr	1	BA					
	Data		29H					
Write to Buffer Abort Reset[4)]	Addr	3	AAAH	555H	555H			
	Data		AAH	55H	F0H			
Unlock Bypass	Addr	3	AAAH	555H	AAAH			
	Data		AAH	55H	20H			
Unlock Bypass Program	Addr	2	XXXH	PA				
	Data		A0H	PD				
Unlock Bypass Block Erase	Addr	2	XXXH	BA				
	Data		80H	30H				
Unlock Bypass Chip Erase	Addr	2	XXXH	XXXH				
	Data		80H	10H				
Unlock Bypass Reset	Addr	2	XXXH	XXXH				
	Data		90H	00H				
Chip Erase	Addr	6	AAAH	555H	AAAH	AAAH	555H	AAAH
	Data		AAH	55H	80H	AAH	55H	10H
Block Erase	Addr	6	AAAH	555H	AAAH	AAAH	555H	BA
	Data		AAH	55H	80H	AAH	55H	30H
Block Erase Suspend [5), 6)]	Addr	1	(DA)XXXH					
	Data		B0H					
Block Erase Resume	Addr	1	(DA)XXXH					
	Data		30H					

Command Definitions		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Program Suspend [7),8)]	Addr	1	(DA)XXXH					
	Data		B0H					
Program Resume	Addr	1	(DA)XXXH					
	Data		30H					
CFI Query [9)]	Addr	1	(DA)AAH					
	Data		98H					
Enter OTP Block Region	Addr	3	AAAH	555H	AAAH			
	Data		AAH	55H	88H			
OTP Block Program	Addr	4	AAAH	555H	AAAH	PA		
	Data		AAH	55H	A0H	PD		
OTP Block Read	Addr	1	RA					
	Data		RD					
Exit OTP Block Region	Addr	4	AAAH	555H	AAAH	XXXH		
	Data		AAH	55H	90H	00H		

NOTE :
- RA : Read Address, PA : Program Address, RD : Read Data, PD : Program Data, WBL : Write Buffer Location
- BA : Block Address (A16 - A23), ABP : Address of the block to be protected or unprotected, X = Don't care ., DA : Bank Address
- DQ8 - DQ15 are don't care in command sequence, except for RD and PD
- A14 - A23 are also don't care, except for the case of special notice.

1) To terminate the Autoselect Mode, it is necessary to write Reset command to the register.
2) The 4th cycle data of Autoselect mode is output data.
3) Device ID must be read across cycles 4, 5 and 6.
   Device ID data : X0EH = "2264H", X0FH = "2260H" for 256Mb Top and Boot Block Device
4) Command sequence resets device for next command after write-to-buffer operation.
5) The Read / Program operations at non-erasing blocks and the autoselect mode are allowed in the Erase Suspend mode.
6) The Erase Suspend command is applicable only to the Block Erase operation.
7) The Read Operation is allowed in the Program Suspend mode.
8) The Program Suspend command is applicable to Program and Erase Suspend - Program operation.
9) Command is valid when the device is in read mode or Autoselect mode.

10.0 DEVICE OPERATION

10.1 Read Mode

The K8P5616UZB is controlled by Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$) and Write Enable ($\overline{WE}$). When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the specified address location,will be the output of the device. The outputs are in high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high.
The K8P5616UZB is available for 8-Word Page mode. Page mode provides fast access time for high performance system.
After address access time(tAA), eight data words are loaded into an internal page buffer. A0 (A-1 in byte mode)~A2 bits determine which page word is output during a read operation. A3~A23 bits must be stable throughout the page read access. Figure 13 shows the asynchronous page read more timing.

10.2 Standby Mode

The K8P5616UZB features Stand-by Mode to reduce power consumption. This mode puts the device on hold when the device is deselected by making $\overline{CE}$ high ($\overline{CE}$ = V_{IH}). Refer to the DC characteristics for more details on stand-by modes.

10.3 Output Disable

The device outputs are disabled when $\overline{OE}$ is High ($\overline{OE}$ = V_{IH}). The output pins are in high impedance state.

10.4 Automatic Sleep Mode

The K8P5616UZB features Automatic Sleep Mode to minimize the device power consumption. When addresses remain steady for t_{AA}+30ns, the device automatically activates the Automatic Sleep Mode. In the sleep mode, output data is latched and always available to the system. When addresses are changed, the device provides new data without wait time.

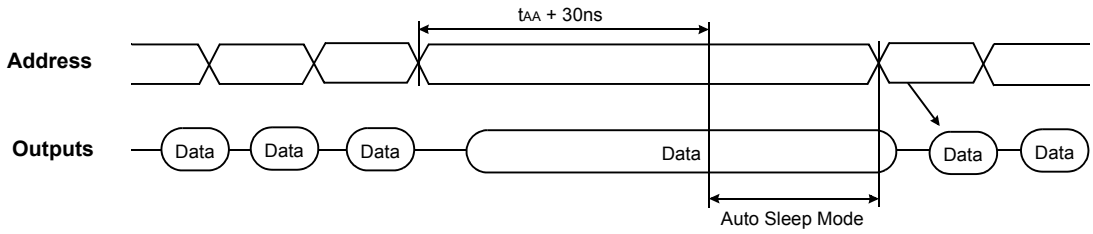


Figure 1: Auto Sleep Mode Operation

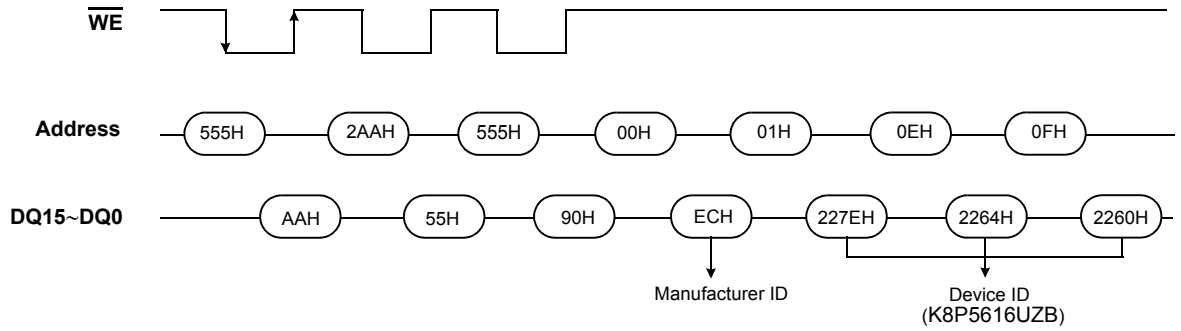
10.5 Autoselect Mode

The K8P5616UZB offers the Autoselect Mode to identify manufacturer, device type and block protection verification by reading a binary code. The Autoselect Mode allows programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The manufacturer, device code ,block protection verification and indicator bit can be read via the command register. The Command Sequence is shown in Table 6 and Figure 2. In addition, below Table 7 shows indicator bit in detail. The autoselect operation of block protection verification is initiated by first writing two unlock cycle. To terminate the autoselect operation, write Reset command (F0H) into the command register.

NOTE : To access the Autoselect codes, the host system must issue the Autoselect command. The Autoselect command sequence can be written to an address within a device that is either in the read or erase-suspend-read mode. The Autoselect command cannot be written while the device is actively programming or erasing. Autoselect does not support page modes. The system must write the reset command to return to the read mode (or erase-suspend read mode if the device was previously in Erase Suspend).

[Table 6] Indicator Bit Codes.

Description	DQ15 to DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Indicator Bit	L	1=Factory-Locked 0=Not Locked	1 = Customer Lock bit , Locked 0 = Not Locked	L	0 = WP Protects Block 255 1 = WP Protects Block 0	H	L	L	L



NOTE : Please refer to Table 6 for device code.

Figure 2: Autoselect Operation (by Command Sequence Method)

10.6 Write (Program/Erase) Mode

The K8P5616UZB executes its program/erase operations by writing commands into the command register. In order to write the commands to the register, $\overline{CE}$ and $\overline{WE}$ must be low and $\overline{OE}$ must be high. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ (whichever occurs last) and the data are latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever occurs first). The device uses standard microprocessor write timing.

10.6.1 Program

The K8P5616UZB can be programmed in units of a word. Programming is writing 0's into the memory array by executing the Internal Program Routine. In order to perform the Internal Program Routine, a four-cycle command sequence is necessary. The first two cycles are unlock cycles. The third cycle is assigned for the program setup command. In the last cycle, the address of the memory location and the data to be programmed at that location are written. The device automatically generates adequate program pulses and verifies the programmed cell margin by the Internal Program Routine. During the execution of the Routine, the system is not required to provide further controls or timings.
During the Internal Program Routine, commands written to the device will be ignored. Note that a hardware reset during a program operation will cause data corruption at the corresponding location.

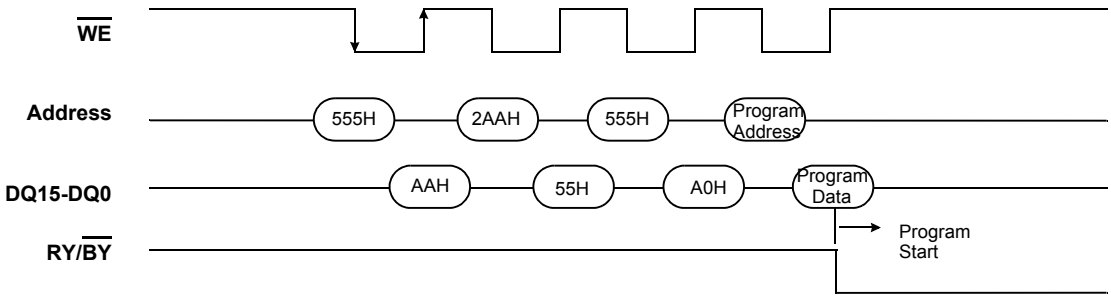


Figure 3: Program Command Sequence

In accross block boundaries and any sequence programming is allowed. A bit cannot be programmed from ’0’ back to ’1’. If attempting to do, it may cause that device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still ’0’. Only erase operations can convert a ’0’ to a ’1’.

10.6.2 Writer Buffer Programming

Write Buffer Programming allows the system write to a maximum of 32 words in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initi-ated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the block address in which programming will occur. The fourth cycle writes the block address and the number of word locations, minus one, to be programmed. For example, if the system will program 19 unique address locations, then 12h should be written to the device. This tells the device how many write buffer addresses will be loaded with data. The number of locations to program cannot exceed the size of the write buffer or the operation will abort. The fifth cycle writes the first address location and data to be programmed. **The write-buffer-page is selected by address bits A23(max.) ~ A5 entered at fifth cycle**. **All subsequent address/ data pairs must fall within the selected write-buffer-page, so that all subsequent addresses must have the same address bit A23(max.) ~ A5 as those entered at fifth cycle. Write buffer locations may be loaded in any order.**
Once the specified number of write buffer locations have been loaded, the system must then write the "Program Buffer to Flash" com mand at the block address. Any other command address/data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 can be monitored to determine the device status during Write Buffer Programming. The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.
Note also that an address loaction cannot be loaded more than once into the write-buffer-page.

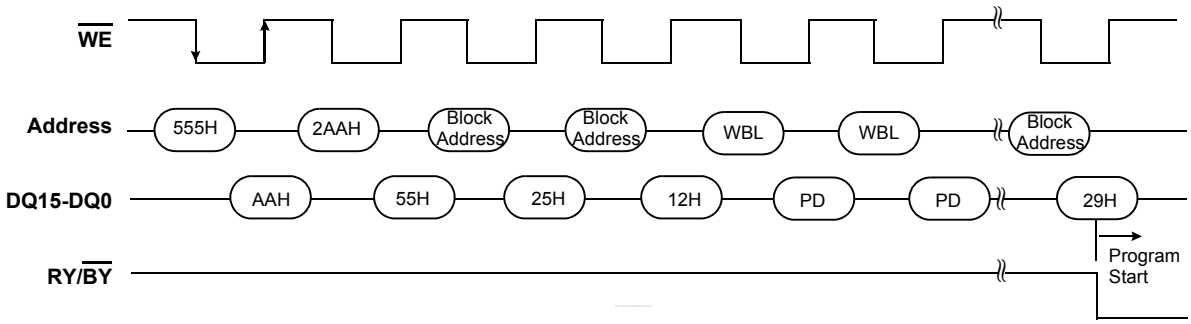


Figure 4: Write Buffer Program Command Sequence

The Write Buffer Programming Sequence can be aborted in the following ways:
- Loading a value that is greater than the buffer size(32-word) during then number of word locations to Program step. (In case, WC > 1FH @Table6)
- The number of Program address/data pairs entered is different to the number of word locations initially defined with WC (@Table 5)
- Writing a Program address to have a different write-buffer-page with selected write-buffer-page (Address bits A23(max) ~ A5 are different)
- Writing non-exact "Program Buffer to Flash" command

The abort condition is indicated by DQ1 = 1, DQ7 = $\overline{\text{DATA}}$ (for the last address location loaded), DQ6 = toggle, and DQ5=0. A "Write-to-Buffer-Abort Reset" command sequence must be written to reset the device for the next operation. Note that the third cycle of Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

And from the third cycle to the last cycle of Write to Buffer command is also required when using Write-Buffer-Programming features in Unlock Bypass mode.

10.6.3 Accelerated Program Operation

Accelerated program operation reduces the program time through the ACC function. This is one of two functions provided by the $\overline{WP}$/ACC pin. When the $\overline{WP}$/ACC pin is asserted as V_{HH}, the device automatically enters the Unlock Bypass mode, and reduces the program operation time. Removing V_{HH} from the $\overline{WP}$/ACC pin returns the device to normal operation.
Blocks must be unprotected before raising $\overline{WP}$/ACC to V_{HH}.
Recommend that the $\overline{WP}$/ACC pin must not be asserted at V_{HH} except on accelerated program operation, or the device may be damaged. In addition, the $\overline{WP}$/ACC pin must not be in the state of floating or unconnected, otherwise the device may be led to malfunction.

Single word accelerated program operation

The system would use two-cycle program sequence (One-cycle (XXX - A0H) is for single word program command, and Next one-cycle (PA - PD) is for program address and data).

Accelerated Write Buffer Programming

In accelerated Write Buffer Program mode, the system must enter "Write to Buffer" and "Program Buffer to Flash" command sequence to be same as them of normal Write Buffer Programming and only can reduce the program time. Note that the third cycle of "Write to Buffer Abort Reset" command sequence is required in an Accelerated mode.

Note that Read While Accelerated Write Buffer Program and Program suspend mode are not guaranteed.

When the $\overline{WP}$/ACC pin is asserted as V_{HH}, the device automatically enters the Unlock Bypass mode, and reduces the program operation time. Removing V_{HH} from the $\overline{WP}$/ACC pin returns the device to normal operation.

- Program/Erase cycling must be limited below 100cycles for optimum performance.
- Ambient temperature requirements : T_A = 30°C±10°C
- The device automatically generates adequate program pulses and ignores other command after program command

10.6.4 Unlock Bypass

The K8P5616UZB provides the unlock bypass mode to save its operation time. This mode is possible for program, CFI, block erase and chip erase operation. There are two methods to enter the unlock bypass mode. The mode is invoked by the unlock bypass command sequence. Unlike the standard program/erase command sequence that contains four to six bus cycles, the unlock bypass program/erase command sequence comprises only two bus cycles. The unlock bypass mode is engaged by issuing the unlock bypass command sequence which is comprised of three bus cycles. Writing first two unlock cycles is followed by a third cycle containing the unlock bypass command (20H). Once the device is in the unlock bypass mode, the unlock bypass program/erase command sequence is necessary. The unlock bypass program command sequence is comprised of only two bus cycles; writing the unlock bypass program command (A0H) is followed by the program address and data. This command sequence is the only valid one for programming the device in the unlock bypass mode. The unlock bypass CFI command sequence is comprised of only one bus cycle; writing the unlock bypass program command (98H). This command sequence is the only valid one for programming the device in the unlock bypass mode. Also, The unlock bypass erase command sequence is comprised of two bus cycles; writing the unlock bypass block erase command(80H-30H) or writing the unlock bypass chip erase command(80H-10H). This command sequences are the only valid ones for erasing the device in the unlock bypass mode. The unlock bypass reset command sequence is the only valid command sequence to exit the unlock bypass mode. The unlock bypass reset command sequence consists of two bus cycles. The first cycle must contain the data (90H). The second cycle contains only the data (00H). Then, the device returns to the read mode.

10.6.5 Chip Erase

To erase a chip is to write 1′s into the entire memory array by executing the Internal Erase Routine. The Chip Erase requires six bus cycles to write the command sequence. The erase set-up command is written after first two "unlock" cycles. Then, there are two more write cycles prior to writing the chip erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory for an all zero data pattern prior to erasing. The automatic erase begins on the rising edge of the last $\overline{WE}$ or $\overline{CE}$ pulse in the command sequence and terminates when DQ7 is "1". After that the device returns to the read mode.

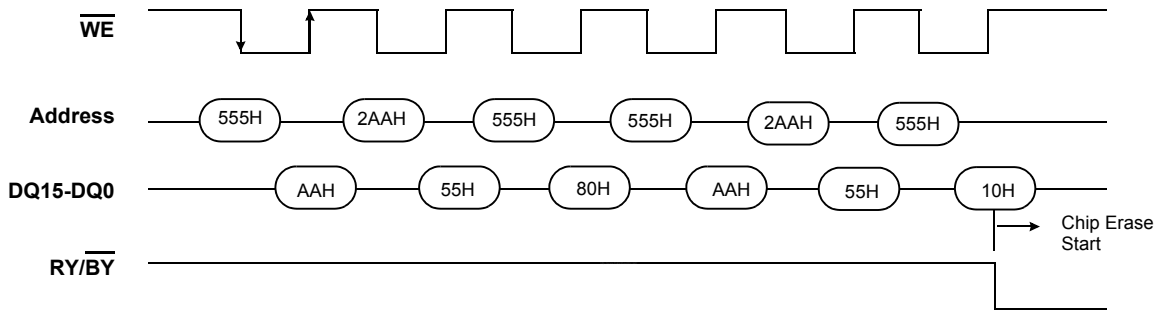


Figure 5: Chip Erase Command Sequence

10.6.6 Block Erase

To erase a block is to write 1′s into the desired memory block by executing the Internal Erase Routine. The Block Erase requires six bus cycles to write the command sequence shown in Table 5. After the first two "unlock" cycles, the erase setup command (80H) is written at the third cycle. Then there are two more "unlock" cycles followed by the Block Erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory prior to erasing it. The block address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, while the Block Erase command is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$. Multiple blocks can be erased sequentially by writing the six bus-cycle. Upon completion of the last cycle for the Block Erase, additional block address and the Block Erase command (30H) can be written to perform the Multi-Block Erase. An 50us (typical) "time window" is required between the Block Erase command writes. The Block Erase command must be written within the 50us "time window", otherwise the Block Erase command will be ignored. The 50us "time window" is reset when the falling edge of the $\overline{WE}$ occurs within the 50us of "time window" to latch the Block Erase command. During the 50us of "time window", any command other than the Block Erase or the Erase Suspend command written to the device will reset the device to read mode. After the 50us of "time window", the Block Erase command will initiate the Internal Erase Routine to erase the selected blocks. Any Block Erase address and command following the exceeded "time window" may or may not be accepted. No other commands will be recognized except the Erase Suspend command.

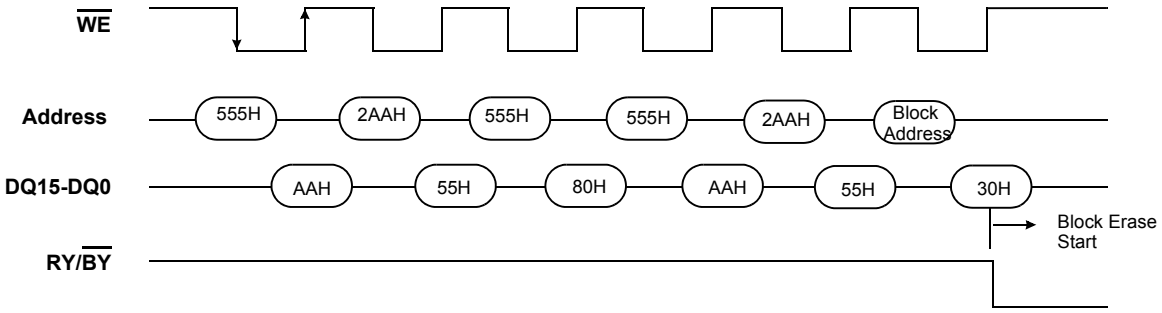


Figure 6: Block Erase Command Sequence

10.7 Erase Suspend / Resume

The Erase Suspend command interrupts the Block Erase to read or program data in a block that is not being erased. The Erase Suspend command is only valid during the Block Erase operation including the time window of 50us. The Erase Suspend command is not valid while the Chip Erase or the Internal Program Routine sequence is running.
When the Erase Suspend command is written during a Block Erase operation, the device requires a maximum of 20us to suspend the erase operation. But, when the Erase Suspend command is written during the block erase time window (50us) , the device immediately terminates the block erase time window and suspends the erase operation.
After the erase operation has been suspended, the device is availble for reading or programming data in a block that is not being erased. The system may also write the autoselect command sequence when the device is in the Erase Suspend mode.
When the Erase Resume command is executed, the Block Erase operation will resume. When the Erase Suspend or Erase Resume command is executed, the addresses are in don't care state. **While erase can be suspended and resumed multiple times, a minimum 30us is required from resume to the next suspend.**
In the erase suspend mode, protect/unprotect command is prohibited.

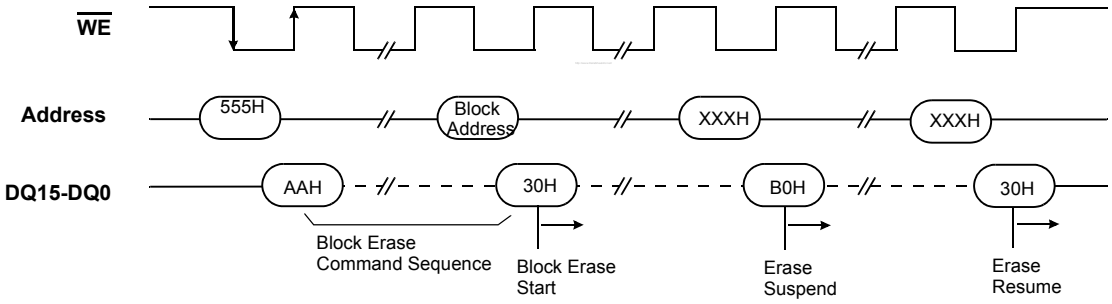


Figure 7: Erase Suspend/Resume Command Sequence

10.8 Program Suspend / Resume

The Program Suspend command interrupts the Program operation. Also the Program Suspend command interrupts the Program operation during Erase Suspend Mode. The Read operation is available only during Program Suspend. When the Program Suspend command is written during a Program operation, the device requires a maximum of 10us to suspend the Program operation. The system may also write the autoselect command sequence when the device is in the Program Suspend mode. When the Program Resume command is executed, the Program operation will resume. When the Program Suspend or Program Resume command is executed, the addresses are in don't care state. **While program can be suspended and resumed multiple times, a minimum 30us is required from resume to the next suspend.**
In the program suspend mode, protect/unprotect command is prohibited.

10.9 Read While Write

The K8P5616UZB provides multi-bank memory architecture that divides the memory array into four banks. The device is capable of reading data from one bank and writing data to the other bank simultaneously. This is so called the Read While Write operation with multi-bank architecture; this feature provides the capability of executing the read operation during Program/Erase or Erase-Suspend-Program operation. The Read While Write operation is prohibited during the chip erase operation. It is also allowed during erase operation when either single block or multiple blocks from same bank are loaded to be erased. It means that the Read While Write operation is prohibited when blocks from one Bank and another blocks from the other Bank are loaded all together for the multi-block erase operation.

10.10 Write Protect ($\overline{WP}$)

The $\overline{WP}$/ACC pin has two useful functions. The one is that certain block is protected by the hardware method not to use V_{ID}. The other is that program operation is accelerated to reduce the program time (Refer to Accelerated program Operation Paragraph).
When the $\overline{WP}$/ACC pin is asserted at VIL, the device can not perform program and erase operation in the outermost 64 Kword block (BA255 or BA0) on end of the flash array independently of whether that block was protected or unprotected. The write protected blocks can only be read. This is useful method to preserve an important program data.
When the $\overline{WP}$/ACC pin is asserted at V_{IH}, the device reverts the outermost 64Kword block on an end to default protection state. Note that the $\overline{WP}$/ACC pin must not be at V_{HH}, for operations other than accelerated programming, or device damage may result.

10.11 Software Reset

The reset command provides that the bank is reseted to read mode or erase-suspend-read mode. The addresses are in don't Care state. The reset command is vaild between the sequence cycles in an erase command sequence before erasing begins, or in a program command sequence before programming begins. This resets the bank in which was operating to read mode. if the device is be erasing or programming, the reset command is invalid until the operation is completed. Also, the reset command is valid between the sequence cycles in an autoselect command sequence. In the autoselect mode, the reset command returns the bank to read mode. If a bank entered the autoselect mode in the Erase Suspend mode, the reset command returns the bank to erase-suspend-read mode. If DQ5 is high on erase or program operation, the reset command return the bank to read mode or erase-suspend-read mode if the bank was in the Erase Suspend state.

10.12 Hardware Reset

The K8P5616UZB offers a reset feature by driving the $\overline{RESET}$ pin to V_{IL}. When the $\overline{RESET}$ pin is held low(V_{IL}) for at least a period of t_{RP}, the device immediatley terminates any operation in progress, tristates all outputs, and ignores all read/write commands for duration of the $\overline{RESET}$ pulse. The device also resets the internal state machine to asynchronous read mode. If a hardware reset occurs during a program operation, the data at that particular location will be lost. Once the $\overline{RESET}$ pin is taken high, the device requires 200ns of wake-up time until outputs are valid for read access. Also, note that all the data output pins are tri-stated for the duration of the $\overline{RESET}$ pulse. The $\overline{RESET}$ pin may be tied to the system reset pin. If a system reset occurs during the Internal Program and Erase Routine, the device will be automatically reset to the read mode ; this will enable the systems microprocessor to read the boot-up firmware from the Flash memory.

10.13 Power-up Protection

To avoid initiation of a write cycle during Vcc Power-up, $\overline{\text{RESET}}$ low must be asserted during power-up. After $\overline{\text{RESET}}$ goes high, the device is reset to the read mode.

10.14 Low Vcc Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than 2.3V. If Vcc < V_{LKO} (Lock-Out Voltage), the command register and all internal program/erase circuits are disabled. Under this condition the device will reset itself to the read mode. Subsequent writes will be ignored until the Vcc level is greater than V_{LKO}. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above 2.3V.

10.15 Write Pulse Glitch Protection

Noise pulses of less than 5ns(typical) on $\overline{\text{CE}}$, $\overline{\text{OE}}$, or $\overline{\text{WE}}$ will not initiate a write cycle.

10.16 Logical Inhibit

Writing is inhibited under any one of the following conditions : $\overline{\text{OE}}$ = V_{IL}, $\overline{\text{CE}}$ = V_{IH} or $\overline{\text{WE}}$ = V_{IH}. To initiate a write, $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be "0", while $\overline{\text{OE}}$ is "1".

11.0 Commom Flash Memory Interface

Common Flash Momory Interface is contrived to increase the compatibility of host system software. It provides the specific information of the device, such as memory size, word configuration, and electrical features. Once this information has been obtained, the system software will know which command sets to use to enable flash writes, block erases, and control the flash component.
When the system writes the CFI command(98H) to address 55H in word mode, the device enters the CFI mode. And then if the system writes the address shown in Table 11, the system can read the CFI data. Query data are always presented on the lowest-order data outputs(DQ0-7) only. In word(x16) mode, the upper data outputs(DQ8-15) is 00h. To terminate this operation, the system must write the reset command.

12.0 OTP Block Region

The OTP Block feature provides a 256-word Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The OTP Block is customer lockable and shipped with itself unlocked, allowing customers to untilize the that block in any manner they choose. Indicator bits DQ6 and DQ7 are used to indicate the factory-locked and customer locked status of the part. The DQ7 is "1" for factory locked.
The system accesses the OTP Block through a command sequence (see "Enter OTP Block / Exit OTP Block Command sequence" at Table 5 on page 11). After the system has written the "Enter OTP Block" Command sequence, it may read the OTP Block by using the addresses (000000h~0000FFh) normally and may check the Protection Verify Bit (DQ7,DQ6) by using the "Autoselect Indicator Bit" Command sequence with OTP Block address. This mode of operation continues until the system issues the "Exit OTP Block" Command suquence, a hardware reset or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to main blocks. Note that the Accelerated function and unlock bypass modes are not available when the OTP Block is enabled.

• After Enter OTP Block command sequence is written, read while write operation are disabled until exiting this mode and any issued addresses should be in the range of OTP block address.

12.1 OTP Block Protection

In a Customer lockable device, The OTP Block is one-time programmable and can be locked only once. Locking operation to the OTP Block is started by writing the "Enter OTP Block Lock Register Region" Command sequence, and then the "OTP Block Lock Register Bit Program" Command sqeunce (Table 5) with data that have zero(setting to 0) in DQ0. Note that the other DQs except DQ0 will be ignored. The Locking operation has to be above 100us. After that timing, "Exit OTP Block Lock Register Region" command sequence or Hardware reset must be issued in order to exit OTP block mode and revert the device to read mode in main array.

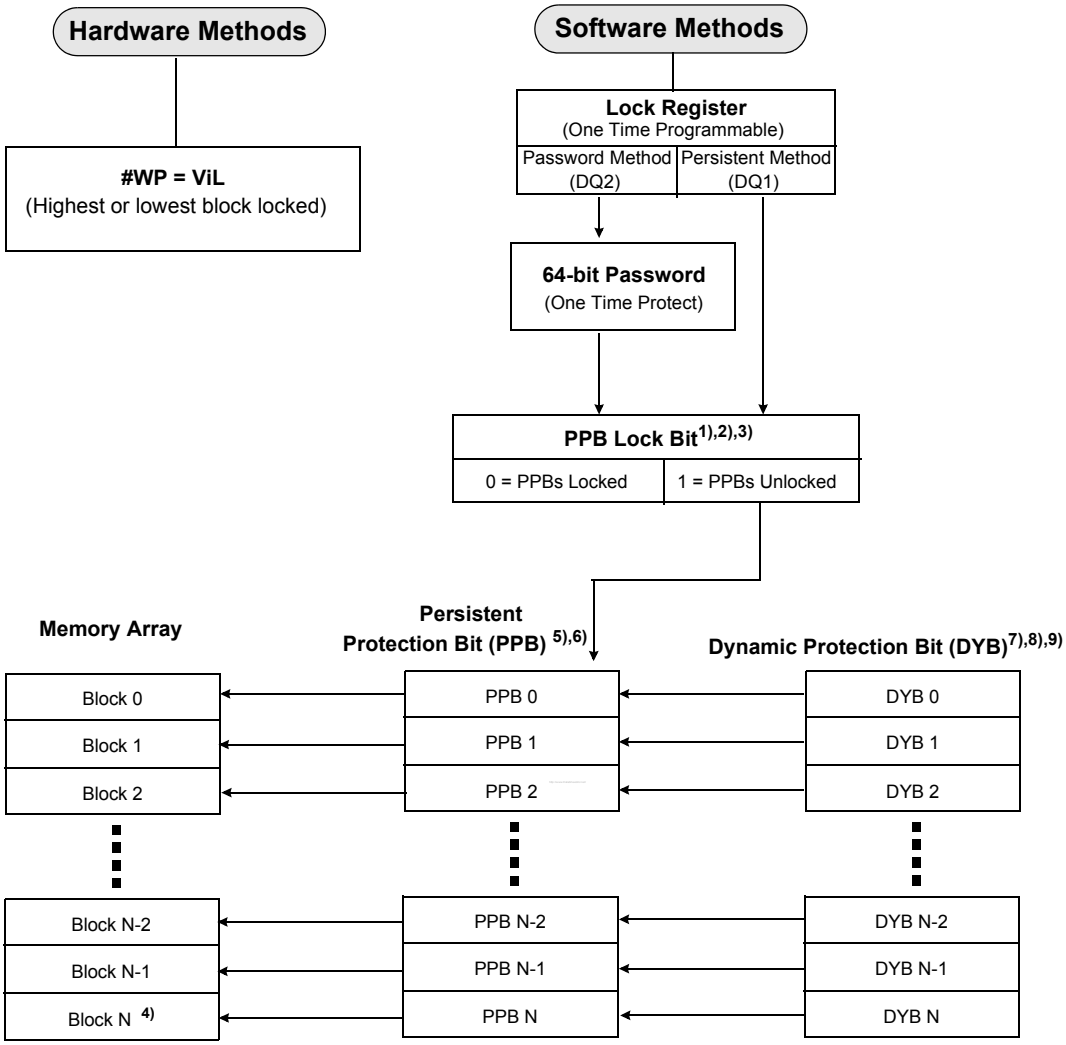
• The OTP Block Lock operation must be used with caution since, once locked, there is no procedure available for unlocking and none of the bits in the OTP Block space can be modified in any way.

• Suspend and resume operation are not supported during OTP protect, nor is OTP protect supported during any suspend operation.

• After Enter OTP Block Lock Register Region command sequence is written, read while write operation are disabled until exiting this mode.

13.0 Enhanced Block Protection / Unprotection

The Enhanced Block Protection / Unprotection feature disables or enables programming or erase operations in any or all blocks and can be implemented through software and/or hardware methods, which are independent of each other.



NOTE :
1) Bit is volatile, and defaults to 1 on reset.
2) Programming to 0 locks all PPBs to their current state.
3) Once programmed to 0, requires hardware reset to unlock.
4) N = Highest Address Block.
5) 0 = Sector Protected,1 = Sector Unprotected.
6) PPBs programmed individually, but cleared collectively.
7) 0 = Sector Protected,1 = Sector Unprotected.
8) Protect effective only if PPB Lock Bit is unlocked and corresponding PPB is 1 (unprotected).
9) Volatile Bits: defaults to user choice upon power-up (see ordering options).

Figure 8: Enhanced Block Protection / Unprotection

13.1 Block Protection

Lock Register

As shipped from the factory, all devices default to the persistent mode when power is applied, and all blocks are unprotected. (DYB is default to clear status : unprotected) For DYB set (protected status) in default, contact your local sales office for details. The device programmer or host system must then choose which block protection method to use. Programming (setting to 0) any one of the following two one-time programmable, non-volatile bits locks the part permanently in that mode:

- Lock Register Persistent Protection Mode Lock Bit (DQ1)
- Lock Register Password Protection Mode Lock Bit (DQ2)

[Table 7] Lock Register.

Device	DQ15 to DQ4	DQ3	DQ2	DQ1	DQ0
K8P5616UZB	Don't Care	PPB One-Time Programmable Bit 0 = All PPB erase command disabled 1 = All PPB Erase command enabled	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	OTP Block Protection Bit

NOTE :
1) If the password mode is chosen, the password must be programmed before setting the corresponding lock register bit.
2) After the Lock Register Bits Command Set Entry command sequence is written, reads and writes for Bank0 are disabled, while reads from other banks are allowed until exiting this mode.
3) If both lock bits are selected to be programmed (to zeros) at the same time, the operation aborts.
4) Once the Password Mode Lock Bit is programmed, the Persistent Mode Lock Bit is permanently disabled, and no changes to the protection scheme are allowed. Similarly, if the Persistent Mode Lock Bit is programmed, the Password Mode is permanently disabled.

After selecting a block protection method, each block can operate in any of the following three states:
1. Constantly locked. The selected blocks are protected and cannot be reprogrammed unless PPB lock bit is cleared via a password, hardware reset, or power cycle.
2. Dynamically locked. The selected blocks are protected and can be altered via software commands.
3. Unlocked. The blocks are unprotected and can be erased and/or programmed.

13.2 Persistent Protection Bits

The Persistent Protection Bits are unique and nonvolatile for each block and have the same endurances as the Flash memory. Preprogramming and verification prior to erasure are handled by the device, and therefore do not require system monitoring.

NOTE :
1) Each PPB is individually programmed and all are erased in parallel.
2) Entry command disables reads and writes for the bank selected.
3) Reads within that block 0 return the PPB status for that bank.
4) Read and Write from other banks than bank 0 are allowed.
5) All Reads must be performed using the Asynchronous mode.
6) The specific block addresses (A23~A16) are written at the same time as the program command.
7) If the PPB Lock Bit is set, the PPB Program or erase command does not execute and timesout without programming or erasing the PPB.
8) There are no means for individually erasing a specific PPB and no specific block address is required for this operation.
9) Exit command must be issued after the execution which resets the device to read mode and re-enables reads and writes for bank 0.
10) The programming state of the PPB for a given block can be verified by writing a PPB Status Read Command to the device as described by the flow chart Below.

13.3 Dynamic Protection Bits

Dynamic Protection Bits are volatile and unique for each block and can be individually modified. DYBs only control the protection scheme for unprotected blocks that have their PPBs cleared (erased to 1). By issuing the DYB Set or Clear command sequences, the DYBs are set (programmed to 0) or cleared (erased to 1), thus placing each block in the protected or unprotected state respectively. This feature allows software to easily protect blocks against inadvertent changes yet does not prevent the easy removal of protection when changes are needed.

NOTE :
1) The DYBs can be set (programmed to 0) or cleared (erased to 1) as often as needed. When the parts are first shipped, the PPBs are cleared (erased to 1) and upon power up or reset, the DYBs is cleared. For DYB set (protected status) in default, contact your local sales office for details.
2) If the option to clear the DYBs after power up is chosen, (erased to 1), then the blocks maybe modified depending upon the PPB state of that block.
3) The blocks would be in the protected state If the option to set the DYBs after power up is chosen (programmed to 0).
4) It is possible to have blocks that are persistently locked with blocks that are left in the dynamic state.
5) The DYB Set or Clear commands for the dynamic blocks signify protected or unprotected state of the blocks respectively. However, if there is a need to change the status of the persistently locked blocks, a few more steps are required. First, the PPB Lock Bit must be cleared by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again locks the PPBs, and the device operates normally again.
6) To achieve the best protection, it is recommended to execute the PPB Lock Bit Set command early in the boot code and protect the boot code by holding WP# = VIL. Note that the PPB and DYB bits have the same function when $\overline{WP}$/ACC = VHH as they do when $\overline{WP}$/ACC = VIH.

13.4 Persistent Protection Bit Lock Bit

The Persistent Protection Bit Lock Bit is a global volatile bit for all blocks. When set (programmed to 0), this bit locks all PPB and when cleared (programmed to 1), unlocks each block. There is only one PPB Lock Bit per device.

NOTE :
1) No software command sequence unlocks this bit unless the device is in the password protection mode; only a hardware reset or a power-up clears this bit.
2) The PPB Lock Bit must be set (programmed to 0) only after all PPBs are configured to the desired settings.

13.5 Password Protection Method

The Password Protection Method allows an even higher level of security than the Persistent block Protection Mode by requiring a 64-bit password for unlocking the device PPB Lock Bit. In addition to this password requirement, after power up and reset, the PPB Lock Bit is set 0 to maintain the password mode of operation. Successful execution of the Password Unlock command by entering the entire password clears the PPB Lock Bit, allowing for block PPBs modifications.

NOTE :
1) There is no special addressing order required for programming the password. Once the Password is written and verified, the Password Mode Locking Bit must be set to prevent access.
2) The Password Program Command is only capable of programming 0s. Programming a 1 after a cell is programmed as a 0 results in a time-out with the cell as a 0.
3) The password is all 1s when shipped from the factory.
4) All 64-bit password combinations are valid as a password.
5) There is no means to verify what the password is after it is set.
6) The Password Mode Lock Bit, once set, prevents reading the 64-bit password on the data bus and further password programming.
7) The Password Mode Lock Bit is not erasable.
8) The lower two address bits (A1~ A0(A-1 in byte mode)) are valid during the Password Read, Password Program, and Password Unlock.
9) The exact password must be entered in order for the unlocking function to occur.
10) The Password Unlock command cannot be issued any faster than 1us at a time to prevent a hacker from running through all the 64-bit combinations in an attempt to correctly match a password.
11) Approximately 1us is required for unlocking the device after the valid 64-bit password is given to the device.
12) Password verification is only allowed during the password programming operation.
13) All further commands to the password region are disabled and all operations are ignored.
14) If the password is lost after setting the Password Mode Lock Bit, there is no way to clear the PPB Lock Bit.
15) Entry command sequence must be issued prior to any of any operation and it disables reads and writes for bank 0. Reads and writes for other banks excluding bank 0 are allowed.
16) If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode.
17) A program or erase command to a protected block enables status polling and returns to read mode without having modified the contents of the protected block.
18) The programming of the DYB, PPB, and PPB Lock for a given block can be verified by writing individual status read commands DYB Status, PPB Status, and PPB Lock Status to the device.

13.6 Master locking bit set

This Master locking bit can ensure that protected blocks be permanently unalterable.
Master locking bit is non-volatile bit. Master locking bit controls protection status of entire blocks that is protected by PPB.
To make permanent protection block, PPB should be protected first.
The usage of the master locking bit command sequence is absolutely required to ensure full protection of data from future alterations. If master locking bit is set ("0"), entire blocks that were protected by PPB are permanently protected. They are not changed and altered by any future lock/unlock commands. Anyone who uses this fuction needs much attention. Because there is no way to return to unlock status. Default status of master locking bit is unlock status("1").
If Master locking bit sets on unprotected block, the block still are remaining in status of unprotected block.
Additionally the unprotected block can be protected by PPB program command. And then the block is protected permanently.

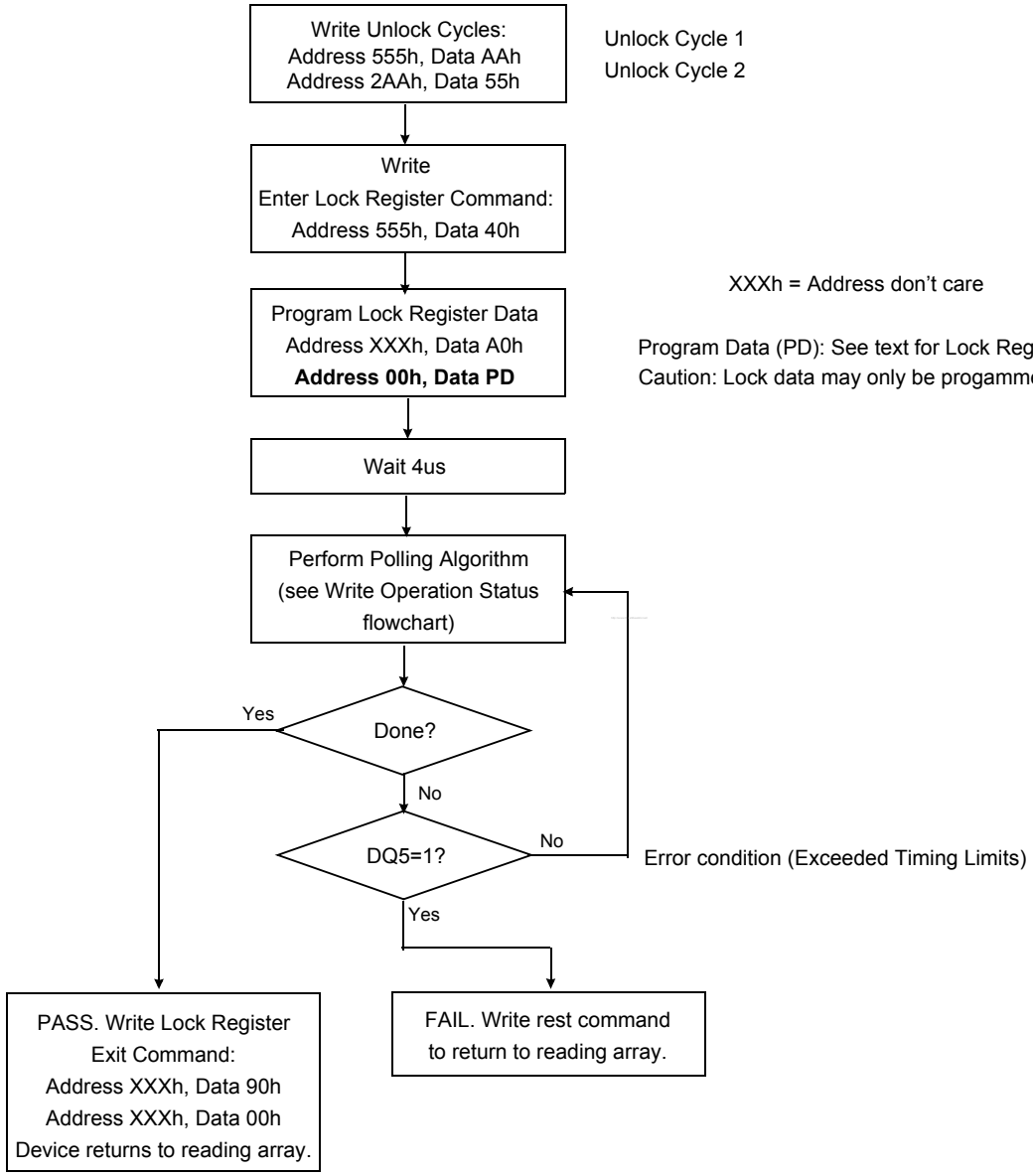


Figure 9: Lock Register Program Algorithm

[Table 8] Block Protection examples

Unique Device PPB Lock Bit 0 = locked, 1 = unlocked		Block PPB 0 = protected	Block DYB 0 = protected	Block Protection Status
Any Block	0	0	X	Protected through PPB
Any Block	0	0	X	Protected through PPB
Any Block	0	1	1	Unprotected
Any Block	0	1	0	Protected through DYB
Any Block	1	0	X	Protected through PPB
Any Block	1	0	X	Protected through PPB
Any Block	1	1	0	Protected through DYB
Any Block	1	1	1	Unprotected

[Table 9] Block protection commands (x16)

Command Definitions		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle	7th Cycle
Enter Lock Register Region [25]	Addr	3	555H	2AAH	555H				
	Data		AAH	55H	40H				
Lock Register Bit Read	Addr	1	00H						
	Data		RD						
Lock Register Bit Program [26]	Addr	2	XXXH	XXXH					
	Data		A0H	DATA					
Exit Lock Register Region [27]	Addr	2	XXXH	XXXH					
	Data		90H	00H					
Password Protection Command Set Entry [25]	Addr	3	555H	2AAH	555H				
	Data		AAH	55H	60H				
Password Program	Addr	2	XXXH	PWA0/PWA1/ PWA2/PWA3					
	Data		A0H	PWD0/PWD1 /PWD2/PWD3					
Password Read	Addr	4	00H	01H	02H	03H			
	Data		PWD0	PWD1	PWD2	PWD3			
Password Unlock	Addr	7	00H	00H	00H	01H	02H	03H	00H
	Data		25H	03H	PWD0	PWD1	PWD2	PWD3	29H
Password Protection Command Set Exit [27]	Addr	2	XXXH	XXXH					
	Data		90H	00H					
PPB Block Protection Command Set Entry [25]	Addr	3	555H	2AAH	(DA)555H				
	Data		AAH	55H	C0H				
PPB Program	Addr	2	XXXH	BA					
	Data		A0H	00H					
All PPB Erase [22]	Addr	2	XXXH	00H					
	Data		80H	30H					
PPB Status Read	Addr	1	BA						
	Data		RD(0)						
PPB Block Protection Command Set Exit [27]	Addr	2	XXXH	XXXH					
	Data		90H	00H					
PPB Lock Bit Command Set Entry [25]	Addr	3	555H	2AAH	555H				
	Data		AAH	55H	50H				
PPB Lock Bit Set	Addr	2	XXXH	XXXH					
	Data		A0H	00H					
PPB Lock Bit Status Read	Addr	1	XXXH						
	Data		RD(0)						
PPB Lock Bit Command Set Exit [27]	Addr	2	XXXH	XXXH					
	Data		90H	00H					
DYB Command Set Entry [25]	Addr	3	555H	2AAH	(DA)555H				
	Data		AAH	55H	E0H				
DYB Set	Addr	2	XXXH	BA					
	Data		A0H	00H					
DYB Clear	Addr	2	XXXH	BA					
	Data		A0H	01H					
DYB Status Read	Addr	1	BA						
	Data		RD(0)						
DYB Command Set Exit [28]	Addr	2	XXXH	XXXH					
	Data		90H	00H					
Master Locking Bit Set	Addr	3	555H	2AAH	555H				
	Data		AAH	55H	F1H				

NOTE :

- RA : Read Address, PA : Program Address, RD : Read Data, PD : Program Data, WBL : Write Buffer Location
- BA : Block Address (A16 - A23), ABP : Address of the block to be protected or unprotected, X = Don't care .
- DQ8 - DQ15 are don't care in command sequence, except for RD and PD
- A14 - A23 are also don't care, except for the case of special notice.
- WC = Word Count. Number of write buffer locations to load minus 1.
- PWA3 ~ PWA0 = Password Address. PWD3 ~ PWD0 = Password Data.
  PD3 ~ PD0 present four 16 bit combinations that represent the 64-bit Password
- RD(0) = DQ0 protection indicator bit. If protected, DQ0 = 0, if unprotected, DQ0 = 1.

1) See bus operations description
2) All values are in hexadecimal.
3) Except for the following, all bus cycles are write cycle: read cycle, fourth through sixth cycles of the Autoselect commands, and password verify commands, and any cycle reading at RD(0) and RD(1).
4) Data bits DQ15 ~ DQ8 are don't care in command sequences, except for RD, PD, WD, PWD, and PWD3 ~ PWD0.
5) Unless otherwise noted, these address bits are don't cares: (A23 ~ A14)
6) Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.
7) No unlock or command cycles required when reading array data.
8) The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when the deviceis in the autoselect mode, or if DQ5 goes high (while the device is providing status information) or performing block lock/unlock.
9) The fourth cycle of the autoselect command sequence is a read cycle. See Autoselect.
10) The data is 0000h for an unlocked block and 0001h for a locked block.
11) Device ID data : X0EH = "2264H", X0FH = "2260H" for 256Mb Uniform Block Device
12) See Autoselect.
13) The Unlock Bypass command sequence is required prior to this command sequence.
14) The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.The system may read and program in non-erasing blocks, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a block erase operation.
15) The Erase Resume command is valid only during the Erase Suspend mode.
16) Command is valid when device is ready to read array data or when device is in autoselect mode.The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 37.
17) The entire four bus-cycle sequence must be entered for which portion of the password.
18) The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.The system may read and program in non-erasing blocks, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a block erase operation.
19) The Erase Resume command is valid only during the Erase Suspend mode.
20) Command is valid when device is ready to read array data or when device is in autoselect mode.The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 37.
21) The entire four bus-cycle sequence must be entered for which portion of the password.
22) The ALL PPB ERASE command pre-programs all PPBs before erasure to prevent over-erasure of PPBs.
23) $\overline{WP}$/ACC must be at VHH during the entire operation of this command.
24) Command sequence resets device for next command after write-to-buffer operation.
25) Entry commands are needed to enter a specific mode to enable instructions only available within that mode.
26) If both the Persistent Protection Mode Locking Bit and the password Protection Mode Locking Bit are set a the same time, the command operation aborts and returns the device to the default Persistent block Protection Mode.
27) The Exit command must be issued to reset the Block 0 of device into read mode. Otherwise the device hangs.
28) The Exit command must be issued to reset device into read mode. Otherwise the device hangs.

[Table 10] Block protection commands (x8)

Command Definitions		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle	7th Cycle
Enter Lock Register Region [25]	Addr	3	AAAH	555H	AAAH				
	Data		AAH	55H	40H				
Lock Register Bit Read	Addr	1	00H						
	Data		RD						
Lock Register Bit Program [26]	Addr	2	XXXH	XXXH					
	Data		A0H	DATA					
Exit Lock Register Region [27]	Addr	2	XXXH	XXXH					
	Data		90H	00H					
Password Protection Command Set Entry [25]	Addr	3	AAAH	555H	AAAH				
	Data		AAH	55H	60H				
Password Program	Addr	2	XXXH	PWAx					
	Data		A0H	PWDx					
Password Read	Addr	8	00H	01H	02H	03H	04H	05H	06H
	Data		PWD0	PWD1	PWD2	PWD3	PWD4	PWD5	PWD6
	Addr		07H						
	Data		PWD7						
Password Unlock	Addr	11	00H	00H	00H	01H	02H	03H	04H
	Data		25H	03H	PWD0	PWD1	PWD2	PWD3	PWD4
	Addr		05H	06H	07H	00H			
	Data		PWD5	PWD6	PWD7	29			
Password Protection Command Set Exit [27]	Addr	2	XXXH	XXXH					
	Data		90H	00H					
PPB Block Protection Command Set Entry [25]	Addr	3	AAAH	555H	AAAH				
	Data		AAH	55H	C0H				
PPB Program	Addr	2	XXXH	BA					
	Data		A0H	00H					
All PPB Erase [22]	Addr	2	XXXH	00H					
	Data		80H	30H					
PPB Status Read	Addr	1	BA						
	Data		RD(0)						
PPB Block Protection Command Set Exit [27]	Addr	2	XXXH	XXXH					
	Data		90H	00H					
PPB Lock Bit Command Set Entry [25]	Addr	3	AAAH	555H	(DA)AAAH				
	Data		AAH	55H	50H				
PPB Lock Bit Set	Addr	2	XXXH	XXXH					
	Data		A0H	00H					
PPB Lock Bit Status Read	Addr	1	XXXH						
	Data		RD(0)						
PPB Lock Bit Command Set Exit [27]	Addr	2	XXXH	XXXH					
	Data		90H	00H					
DYB Command Set Entry [25]	Addr	3	AAAH	555H	(DA)AAAH				
	Data		AAH	55H	E0H				
DYB Set	Addr	2	XXXH	BA					
	Data		A0H	00H					
DYB Clear	Addr	2	XXXH	BA					
	Data		A0H	01H					
DYB Status Read	Addr	1	BA						
	Data		RD(0)						
DYB Command Set Exit [28]	Addr	2	XXXH	XXXH					
	Data		90H	00H					
Master Locking Bit Set	Addr	3	AAAH	555H	AAAH				
	Data		AAH	55H	F1H				

NOTE :

- RA : Read Address, PA : Program Address, RD : Read Data, PD : Program Data, WBL : Write Buffer Location
- BA : Block Address (A16 - A23), ABP : Address of the block to be protected or unprotected, X = Don't care .
- DQ8 - DQ15 are don't care in command sequence, except for RD and PD
- A14 - A23 are also don't care, except for the case of special notice.
- WC = Word Count. Number of write buffer locations to load minus 1.
- PWA3 ~ PWA0 = Password Address. PWD7 ~ PWD0 = Password Word0, Word1, Word2, Word3
  PD3 ~ PD0 present four 16 bit combinations that represent the 64-bit Password
- RD(0) = DQ0 protection indicator bit. If protected, DQ0 = 0, if unprotected, DQ0 = 1.

1) See bus operations description

2) All values are in hexadecimal.

3) Except for the following, all bus cycles are write cycle: read cycle, fourth through sixth cycles of the Autoselect commands, and password verify commands, and any cycle reading at RD(0) and RD(1).

4) Data bits DQ15 ~ DQ8 are don't care in command sequences, except for RD, PD, WD, PWD, and PWD3 ~ PWD0.

5) Unless otherwise noted, these address bits are don't cares: (A23 ~ A14)

6) Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.

7) No unlock or command cycles required when reading array data.

8) The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the autoselect mode, or if DQ5 goes high (while the device is providing status information) or performing block lock/unlock.

9) The fourth cycle of the autoselect command sequence is a read cycle. See Autoselect.

10) The data is 0000h for an unlocked block and 0001h for a locked block.

11) Device ID data : X0EH = "2264H", X0FH = "2260H" for 256Mb Uniform Block Device

12) See Autoselect.

13) The Unlock Bypass command sequence is required prior to this command sequence.

14) The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.The system may read and program in non-erasing blocks, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a block erase operation.

15) The Erase Resume command is valid only during the Erase Suspend mode.

16) Command is valid when device is ready to read array data or when device is in autoselect mode.The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 37.

17) The entire four bus-cycle sequence must be entered for which portion of the password.

18) The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.The system may read and program in non-erasing blocks, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a block erase operation.

19) The Erase Resume command is valid only during the Erase Suspend mode.

20) Command is valid when device is ready to read array data or when device is in autoselect mode.The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 37.

21) The entire four bus-cycle sequence must be entered for which portion of the password.

22) The ALL PPB ERASE command pre-programs all PPBs before erasure to prevent over-erasure of PPBs.

23) $\overline{WP}$/ACC must be at VHH during the entire operation of this command.

24) Command sequence resets device for next command after write-to-buffer operation.

25) Entry commands are needed to enter a specific mode to enable instructions only available within that mode.

26) If both the Persistent Protection Mode Locking Bit and the password Protection Mode Locking Bit are set a the same time, the command operation aborts and returns the device to the default Persistent block Protection Mode.

27) The Exit command must be issued to reset the Block 0 of device into read mode. Otherwise the device hangs.

28) The Exit command must be issued to reset device into read mode. Otherwise the device hangs.

[Table 11] Common Flash Memory Interface Code

Description	Addresses (Word Mode)	Addresses (Byte Mode)	Data
Query Unique ASCII string "QRY"	10H 11H 12H	20H 22H 24H	0051H 0052H 0059H
Primary OEM Command Set	13H 14H	26H 28H	0002H 0000H
Address for Primary Extended Table	15H 16H	2AH 2CH	0040H 0000H
Alternate OEM Command Set (00h = none exists)	17H 18H	2EH 30H	0000H 0000H
Address for Alternate OEM Extended Table (00h = none exists)	19H 1AH	32H 34H	0000H 0000H
Vcc Min. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1BH	36H	0027H
Vcc Max. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1CH	38H	0036H
Vpp Min. voltage(00H = no Vpp pin present)	1DH	3AH	0000H
Vpp Max. voltage(00H = no Vpp pin present)	1EH	3CH	0000H
Typical timeout per single word write 2^N us	1FH	3EH	0006H
Typical timeout for Min. size buffer write 2^N us(00H = not supported)	20H	40H	0006H
Typical timeout per individual block erase 2^N ms	21H	42H	0009H
Typical timeout for full chip erase 2^N ms(00H = not supported)	22H	44H	0013H
Max. timeout for word write 2^N times typical	23H	46H	0003H
Max. timeout for buffer write 2^N times typical	24H	48H	0005H
Max. timeout per individual block erase 2^N times typical	25H	4AH	0003H
Max. timeout for full chip erase 2^N times typical(00H = not supported)	26H	4CH	0002H
Device Size = 2^N byte	27H	4EH	0019H
Flash Device Interface description	28H 29H	50H 52H	0002H 0000H
Max. number of byte in multi-byte write = 2^N	2AH 2BH	54H 56H	0006H 0000H
Number of Erase Block Regions within device	2CH	58H	0001H
Erase Block Region 1 Information	2DH 2EH 2FH 30H	5AH 5CH 5EH 60H	00FFH 0000H 0000H 0002H
Erase Block Region 2 Information	31H 32H 33H 34H	62H 64H 66H 68H	0000H 0000H 0000H 0000H
Erase Block Region 3 Information	35H 36H 37H 38H	6AH 6CH 6EH 70H	0000H 0000H 0000H 0000H
Erase Block Region 4 Information	39H 3AH 3BH 3CH	72H 74H 76H 78H	0000H 0000H 0000H 0000H

Description	Addresses (Word Mode)	Addresses (Byte Mode)	Data
Query-unique ASCII string "PRI"	40H 41H 42H	80H 82H 84H	0050H 0052H 0049H
Major version number, ASCII	43H	86H	0031H
Minor version number, ASCII	44H	88H	0033H
Address Sensitive Unlock(Bits 1-0) 0 = Required, 1= Not Required Silcon Revision Number(Bits 7-2)	45H	8AH	0014H
Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write	46H	8CH	0002H
Block Protect 00 = Not Supported, 01 = Supported	47H	8EH	0001H
Block Temporary Unprotect 00 = Not Supported, 01 = Supported	48H	90H	0000H
Block Protect/Unprotect scheme, 08 = Enhanced Block Protection	49H	92H	0008H
Simultaneous Operation 00 = Not Supported, XX = Number of Blocks except Bank 0	4AH	94H	00DFH
Burst Mode Type 00 = Not Supported, 01 = Supported	4BH	96H	0000H
Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page	4CH	98H	0002H
ACC(Acceleration) Supply Minimum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	4DH	9AH	0085H
ACC(Acceleration) Supply Maximum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	4EH	9CH	0095H
$\overline{WP}$ protect 04 = Uniform Blocks Bottom $\overline{WP}$ protect. 05 = Uniform Blocks Top $\overline{WP}$ protect.	4FH	9EH	00XXH
Program Suspend 00 = Not Supported. 01 = Supported.	50H	A0H	0001H

14.0 DEVICE STATUS FLAGS

The K8P5616UZB has means to indicate its status of operation in the bank where a program or erase operation is in processes. The status is indicated by raising the bank status flag via corresponding DQ pins or the RY/ $\overline{BY}$ pin. The corresponding DQ pins are DQ7, DQ6, DQ5, DQ3, DQ2 and DQ1. The statues are as follows :

[Table 12] Hardware Sequence Flags

	Status		DQ7	DQ6	DQ5	DQ3	DQ2	DQ1
In Progress	Programming		$\overline{DQ7}$	Toggle	0	0	1	0
	Block Erase or Chip Erase		0	Toggle	0	1	Toggle	1
	Erase Suspend Read	Erase Suspended Block	1	1	0	0	Toggle 1)	1
	Erase Suspend Read	Non-Erase Suspended Block	Data	Data	Data	Data	Data	Data
	Erase Suspend Program	Non-Erase Suspended Block	$\overline{DQ7}$	Toggle	0	0	1	0
	Program Suspend Read	Program Suspended Block	DQ7	1	0	0	Toggle1)	1
	Program Suspend Read	Non-Program Suspended Block	Data	Data	Data	Data	Data	Data
Exceeded Time Limits	Programming		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
	Block Erase or Chip Erase		0	Toggle	1	1	(Note 2)	1
	Erase Suspend Program		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
Write to Buffer (Note 3)	BUSY State		$\overline{DQ7}$	Toggle	0	0	No Toggle	0
	Exceeded Timing Limits		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
	ABORT State		$\overline{DQ7}$	Toggle	0	0	No Toggle	1

NOTE :

1) DQ2 will toggle when the device performs successive read operations from the erase/program suspended block.

2) If DQ5 is High (exceeded timing limits), successive reads from a problem block will cause DQ2 to toggle.

3) Note that $\overline{DQ7}$ during Write-to-Buffer-Programming indicates the data-bar for DQ7 for the last loaded write-buffer address location.

DQ7 : $\overline{\text{Data}}$ Polling

When an attempt to read the device is made while executing the Internal Program, the complement of the data is written to DQ7 as an indication of the Routine in progress. When the Routine is completed an attempt to access to the device will produce the true data written to DQ7. When a user attempts to read the block being erased, DQ7 will be low. If the device is placed in the Erase/Program Suspend Mode, the status can be detected via the DQ7 pin. If the system tries to read an address which belongs to a block that is being erase suspended, DQ7 will be high. And, if the system tries to read an address which belongs to a block that is being program suspended, the output will be the true data of DQ7 itself. If a non-erase-suspended or non-program-suspended block address is read, the device will produce the true data to DQ7. If an attempt is made to program a protected block, DQ7 outputs complements the data for approximately 1μs and the device then returns to the Read Mode without changing data in the block. If an attempt is made to erase a protected block, DQ7 outputs complement data in approximately 100us and the device then returns to the Read Mode without erasing the data in the block.

DQ6 : Toggle Bit

Toggle bit is another option to detect whether an Internal Routine is in progress or completed. Once the device is at a busy state, DQ6 will toggle. Toggling DQ6 will stop after the device completes its Internal Routine. If the device is in the Erase/Program Suspend Mode, an attempt to read an address that belongs to a block that is being erased or programmed will produce a high output of DQ6. If an address belongs to a block that is not being erased or programmed, toggling is halted and valid data is produced at DQ6. If an attempt is made to program a protected block, DQ6 toggles for approximately 1us and the device then returns to the Read Mode without changing the data in the block. If an attempt is made to erase a protected block, DQ6 toggles for approximately 100μs and the device then returns to the Read Mode without erasing the data in the block.

DQ5 : Exceed Timing Limits

If the Internal Program/Erase Routine extends beyond the timing limits, DQ5 will go High, indicating program/erase failure.

DQ3 : Block Erase Timer

The status of the multi-block erase operation can be detected via the DQ3 pin. DQ3 will go High if 50μs of the block erase time window expires. In this case, the Internal Erase Routine will initiate the erase operation.Therefore, the device will not accept further write commands until the erase operation is completed. DQ3 is Low if the block erase time window is not expired. Within the block erase time window, an additional block erase command (30H) can be accepted. To confirm that the block erase command has been accepted, the software may check the status of DQ3 following each block erase command.

DQ2 : Toggle Bit 2

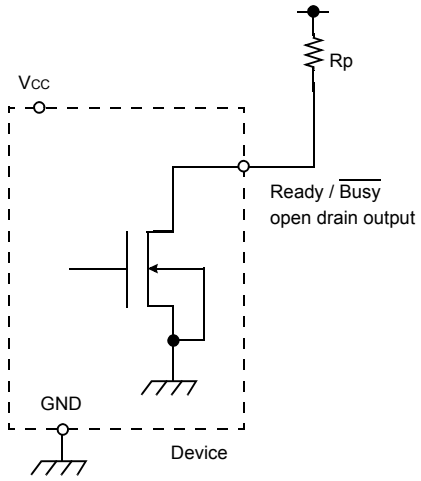
The device generates a toggling pulse in DQ2 only if an Internal Erase Routine or an Erase/Program Suspend is in progress. When the device executes the Internal Erase Routine, DQ2 toggles only if an erasing bank is read. Although the Internal Erase Routine is in the Exceeded Time Limits, DQ2 toggles only if an erasing block in the Exceeded Time Limits is read. When the device is in the Erase/Program Suspend mode, DQ2 toggles only if an address in the erasing or programming block is read. If a non-erasing or non-programmed block address is read during the Erase/Program Suspend mode, then DQ2 will produce valid data. DQ2 will go High if the user tries to program a non-erase suspend block while the device is in the Erase Suspend mode.

DQ1 : Buffer Program Abort Indicator

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data.

RY/$\overline{BY}$: Ready/$\overline{Busy}$

The pin is an open drain output, allowing two or more Ready/ $\overline{Busy}$ outputs to be OR-tied. An appropriate pull-up resistor by system is required for proper operation.
The K8P5616UZB has a Ready / $\overline{Busy}$ output that indicates either the completion of an operation or the status of Internal Algorithms. If the output is Low, the device is busy with either a program or an erase operation. If the output is High, the device is ready to accept any read/write or erase operation. When the RY/ $\overline{BY}$ pin is low, the device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If the K8P5616UZB is placed in an Erase Suspend mode, the RY/ $\overline{BY}$ output will be High. For programming, the RY/ $\overline{BY}$ is valid (RY/ $\overline{BY}$ = 0) after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For Chip Erase, RY/ $\overline{BY}$ is also valid after the rising edge of $\overline{WE}$ pulse in the six write pulse sequence. For Block Erase, RY/ $\overline{BY}$ is also valid after the rising edge of the sixth $\overline{WE}$ pulse.



$$Rp = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \Sigma I_L} = \frac{3.5\ V}{2.1mA + \Sigma I_L}$$

where ΣI_L is the sum of the input currents of all devices tied to the Ready / $\overline{Busy}$ pin.

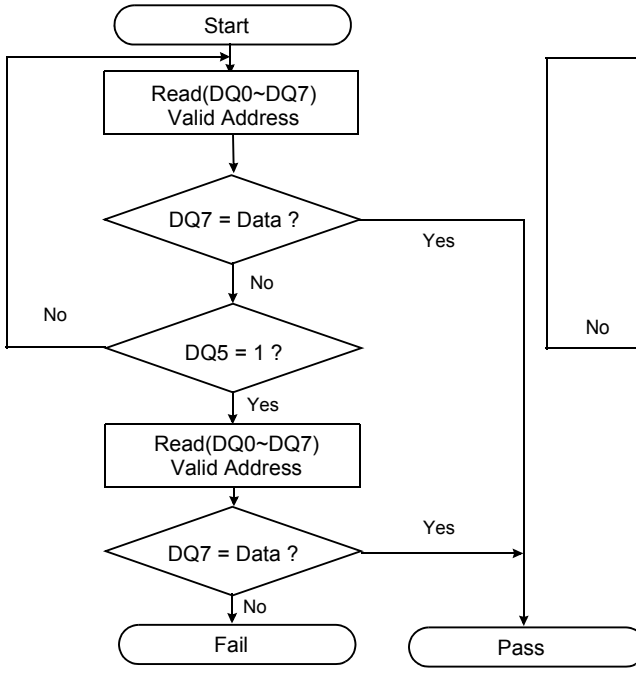


Figure 10: Data Polling Algorithms

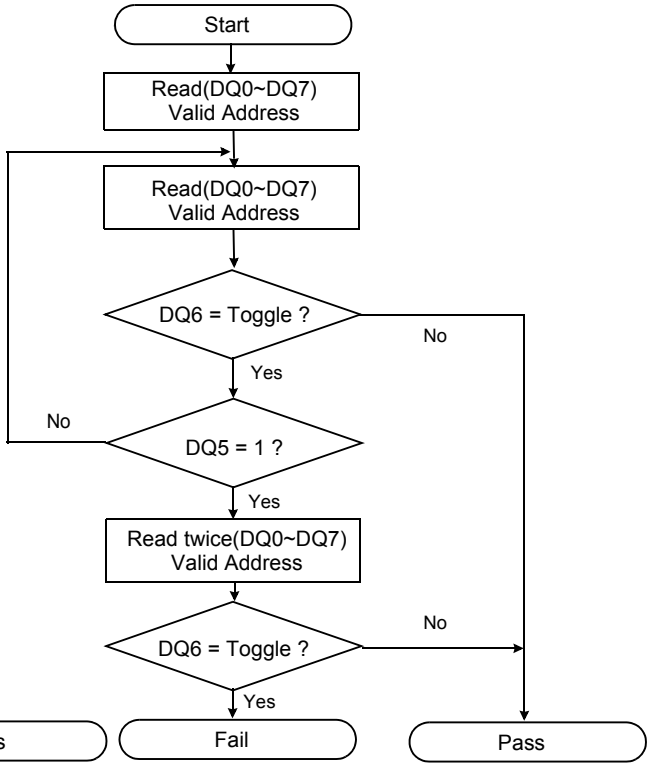


Figure 11: Toggle Bit Alogorithms

15.0 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	Vcc	Vcc	-0.5 to +4.0	V
	V_{IO}	V_{IO}	-0.5 to +4.0	
	$\overline{WP}$/ACC	V_{IN}	-0.5 to +9.5	
	All Other Pins		-0.5 to Vcc+0.5	
Temperature Under Bias	Commercial	T_{bias}	-10 to +125	°C
	Extended		-25 to +125	
Storage Temperature		T_{stg}	-65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA
Operating Temperature		T_A (Industrial Temp.)	-40 to +85	°C
		T_A (Extended Temp.)	-25 to + 85	°C

NOTE :

1) Minimum DC voltage is -0.5V on Input/ Output pins. During transitions, this level may fall to -2.0V for periods <20ns. Maximum DC voltage on input / output pins is Vcc+0.5V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.
2) Minimum DC voltage is -0.5V on $\overline{WP}$/ACC pins. During transitions, this level may fall to -2.0V for periods <20ns. Maximum DC voltage on $\overline{WP}$/ACC pins is 9.5V which, during transitions, may overshoot to 10.5V for periods <20ns.
3) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

16.0 RECOMMENDED OPERATING CONDITIONS (Voltage reference to GND)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	2.7	3.0	3.6	V
V_{IO} Supply Voltage	V_{IO}	1.65	-	Vcc	V
Supply Voltage	Vss	0	0	0	V

17.0 DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc, Vcc=Vccmax	– 1.0	-	+ 1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=Vss to Vcc,Vcc=Vccmax	– 1.0	-	+ 1.0	µA
Vcc Active Read Current [1]			TBD		TBD	TBD
V_{IO} Non-Active Output			TBD		TBD	TBD
Active Write Current [2]	I_{CC2}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}, $\overline{WE}$=V_{IL}	-	25	50	mA
Read While Program Current [5]	I_{CC3}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH} (@5Mhz)	-	35	50	mA
Read While Erase Current [5]	I_{CC4}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH} (@10Mhz)	-	35	50	mA
Program While Erase Suspend Current	I_{CC5}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	-	27	55	mA
Page Read Current	I_{CC6}	$\overline{OE}$=VIH, 8-word Page Read 40MHz	-	10	15	mA
ACC Accelerated Program Current	I_{ACC}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	-	15	30	mA
Standby Current	I_{SB1}	$\overline{CE}$, $\overline{RESET}$, $\overline{WP}$/ACC= Vcc± 0.3	-	20	40	µA
Standby Current During Reset	I_{SB2}	$\overline{RESET}$= Vss± 0.3	-	20	40	µA
Automatic Sleep Mode	I_{SB3}	V_{IH}=Vcc ± 0.3V, V_{IL}=Vss ±0.2V	-	20	40	µA
Input Low Level	V_{IL}	Vcc=2.7~3.6V	-0.5	-	0.8	V
Input High Level	V_{IH}	Vcc=2.7~3.6V	V_{CC}x0.7	-	Vcc+0.3	V
Voltage for Program Acceleration [4]	V_{HH}	Vcc = 2.7~3.6V	8.5	-	9.5	V
Voltage for Autoselect and Temporary Sector Unprotect	V_{ID}	Vcc = 2.7~3.6V	8.5	-	9.5	V
Output Low Level	V_{OL}	IOL =100uA,Vcc=VCCmin	-	-	0.1	V
Output High Level	V_{OH}	IOH = -100uA, Vcc=VCCmin	Vcc - 0.2	-	-	V
Low VCC Lock-out Voltage [5]	V_{LKO}		2.3	-	2.5	V

NOTE :
1) The Icc current listed includes both the DC operating current and the frequency dependent component(at 5 MHz).
2) Icc active during Internal Routine(program or erase) is in progress..
3) The high voltage (V_{HH}) must be used in the range of Vcc = 2.7V ~ 3.6V
4.)Not 100% tested.
5) Icc active during Read while Write is in progress.

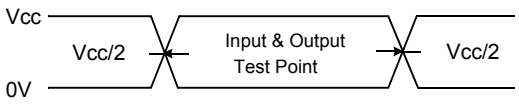
18.0 CAPACITANCE (TA = 25 °C, VCC = 3.0V, f = 1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	10	pF
Control Pin Capacitance	C_{IN2}	V_{IN}=0V	-	10	pF

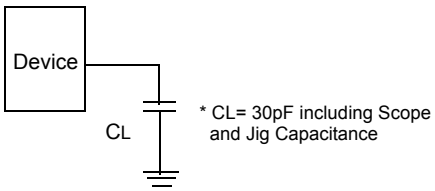
NOTE : Capacitance is periodically sampled and not 100% tested.

19.0 AC TEST CONDITION

Parameter	Value
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load	C_L = 30pF



Input Pulse and Test Point



Output Load

20.0 AC CHARACTERISTICS

20.1 Read Operations

Parameter	Symbol	Vcc = 2.7V~3.6V		Unit
		4E		
		Min	Max	
Read Cycle Time [1]	t_{RC}	80	-	ns
Page Read Cycle Time	t_{PRC}	30	-	ns
Address Access Time	t_{AA}	-	80	ns
Chip Enable Access Time	t_{CE}	-	80	ns
Output Enable Time	t_{OE}	-	30	ns
Page Address Access Time	t_{PA}	-	30	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time[1]	t_{DF}	-	16	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$ [1]	t_{OH}	5	-	ns

NOTE :
1) Not 100% tested.
The device supports only 4E at VIO = 1.7~1.95V.

SWITCHING WAVEFORMS

Conventional Read Operations

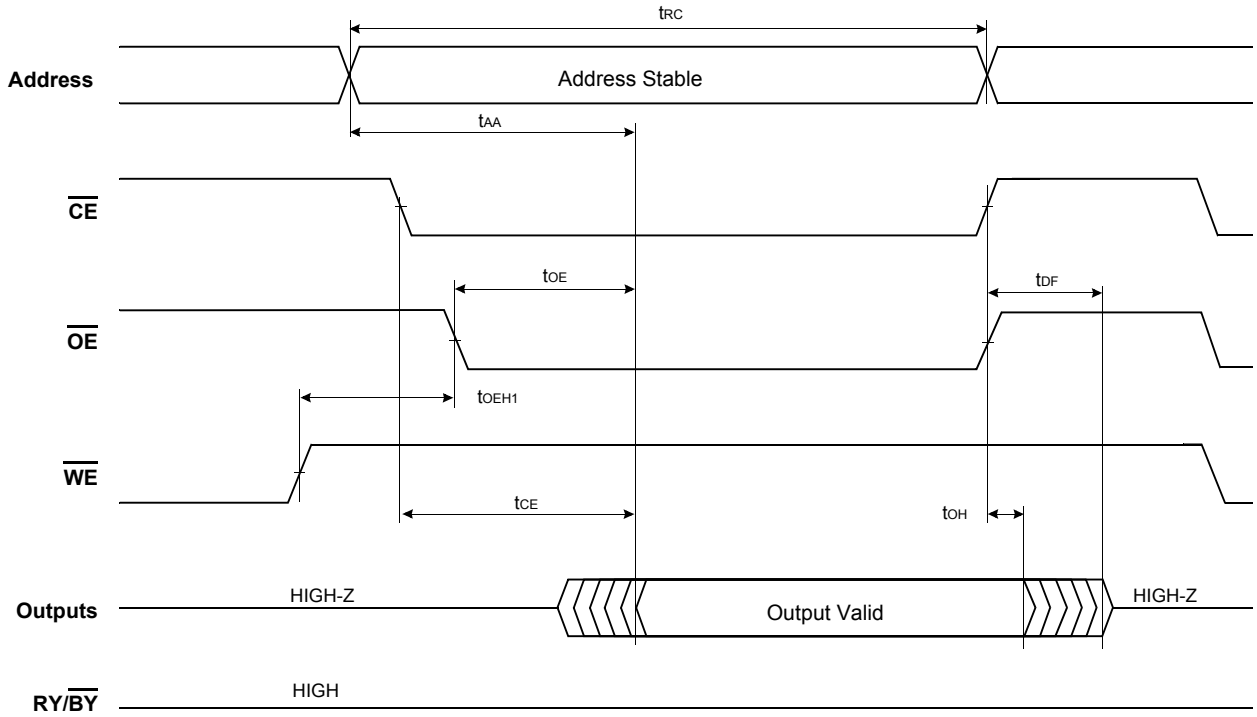


Figure 12: Conventional Read Operation Timings

Page Read Operations

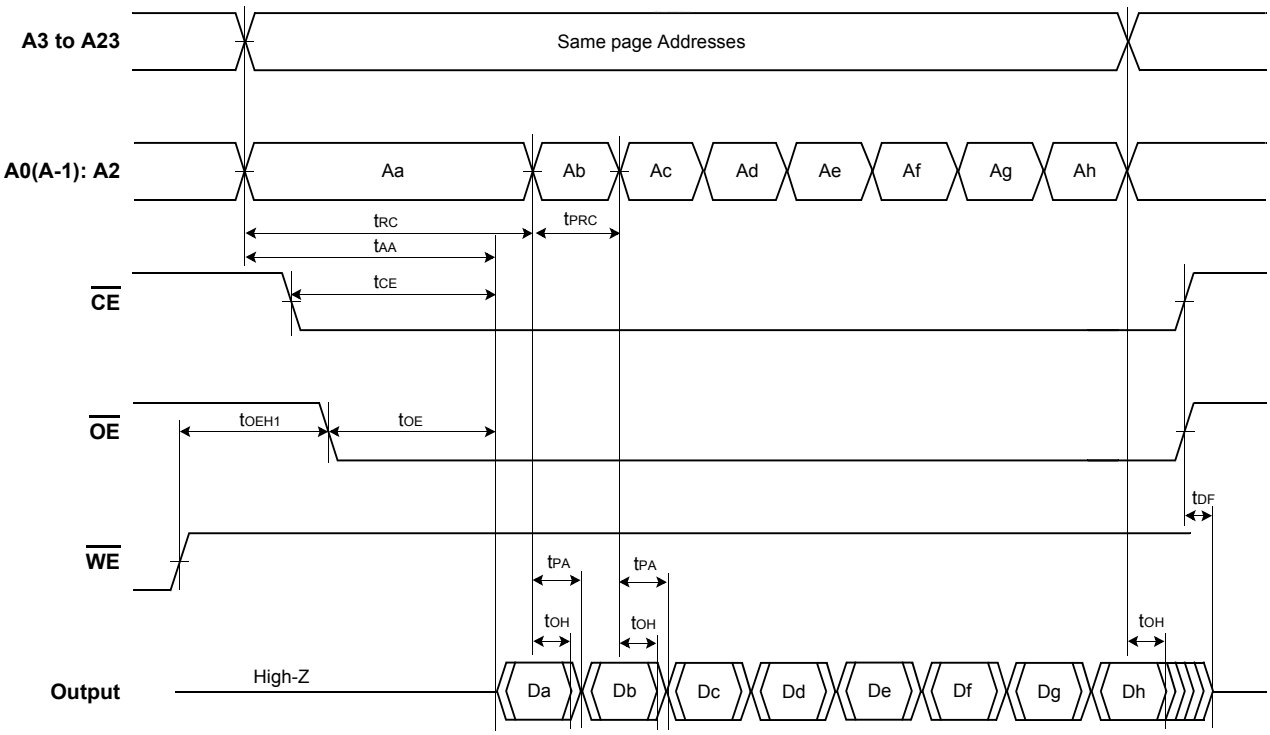


Figure 13: Page Read Operation Timings

SWITCHING WAVEFORMS
Hardware Reset/Read Operations

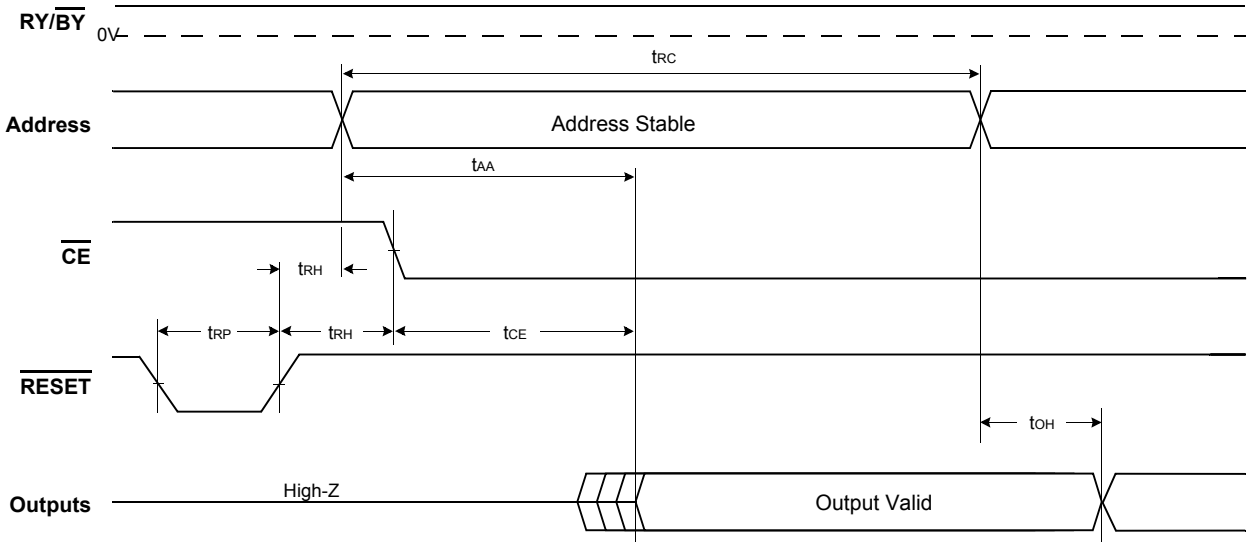


Figure 14: Hardware Reset/Read Operation Timings

Parameter	Symbol	4E		Unit
		Min	Max	
Read Cycle Time	t_{RC}	80	-	ns
Address Access Time	t_{AA}	-	80	ns
Chip Enable Access Time	t_{CE}	-	80	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$	t_{OH}	5	-	ns
RY/$\overline{BY}$ Recovery Time	t_{RB}	0	-	ns
$\overline{RESET}$ Low to Standby Mode	t_{RPD}	20	-	μs
$\overline{RESET}$ Pulse Width	t_{RP}	30	-	μs
$\overline{RESET}$ High Time Before Read	t_{RH}	200	-	ns

NOTE :
The device supports only 4E at VIO = 1.7~1.95V.

AC CHARACTERISTICS

20.2 Write(Erase/Program)Operations

Parameter		Symbol	VCC = 2.7V ~ 3.6V		Unit
			4E		
			Min	Max	
Write Cycle Time [1), 3)]		t_{WC}	80	-	ns
Address Setup Time		t_{AS}	0	-	ns
Address Setup Time to $\overline{OE}$ low during toggle bit polling		t_{ASO}	15		ns
Address Hold Time		t_{AH}	35	-	ns
		t_{AHT}	0	-	ns
Data Setup Time		t_{DS}	30	-	ns
Data Hold Time		t_{DH}	0	-	ns
Output Enable Setup Time [1)]		t_{OES}	0	-	ns
Output Enable Hold Time	Read [1)]	t_{OEH1}	0	-	ns
	Toggle and $\overline{Data}$ Polling [1)]	t_{OEH2}	10	-	ns
$\overline{CE}$ Setup Time		t_{CS}	0	-	ns
$\overline{CE}$ Hold Time		t_{CH}	0	-	ns
Write Pulse Width		t_{WP}	35	-	ns
Write Pulse Width High		t_{WPH}	25	-	ns
Programming Operation [2)]		t_{PGM}	40(typ.)		µs
Accelerated Programming Operation [2)]		t_{ACCPGM}	24(typ.)		µs
Block Erase Operation [2)]		t_{BERS}	0.7(typ)		sec
VCC Set Up Time		t_{VCS}	250	-	µs
VHH Set Up Time		t_{VHH}	250	-	ns
ACC Setup Time (During Accelerated Programming)		t_{VPS}	1	-	us
Write Recovery Time from RY/$\overline{BY}$		t_{RB}	0	-	ns
Program/Erase Valid to RY/$\overline{BY}$ Delay		t_{BUSY}	-	90	ns
Read Recovery Time Before Write		t_{GHWL}	0	-	ns
$\overline{CE}$ High during toggling bit polling		t_{CEPH}	20	-	ns
$\overline{OE}$ High during toggling bit polling		t_{OEPH}	10	-	ns
Block Erase Accept Time-out		t_{BEA}	-	50	us
Erase Suspend Latency		t_{ESL}	-	20	us
Program Suspend Latency		t_{PSL}	-	10	us
Toggle Time During Block Protection		t_{ASP}	100(typ)		us
Toggle Time During Programming Within a Protected Block		t_{PSP}	1(typ)		us

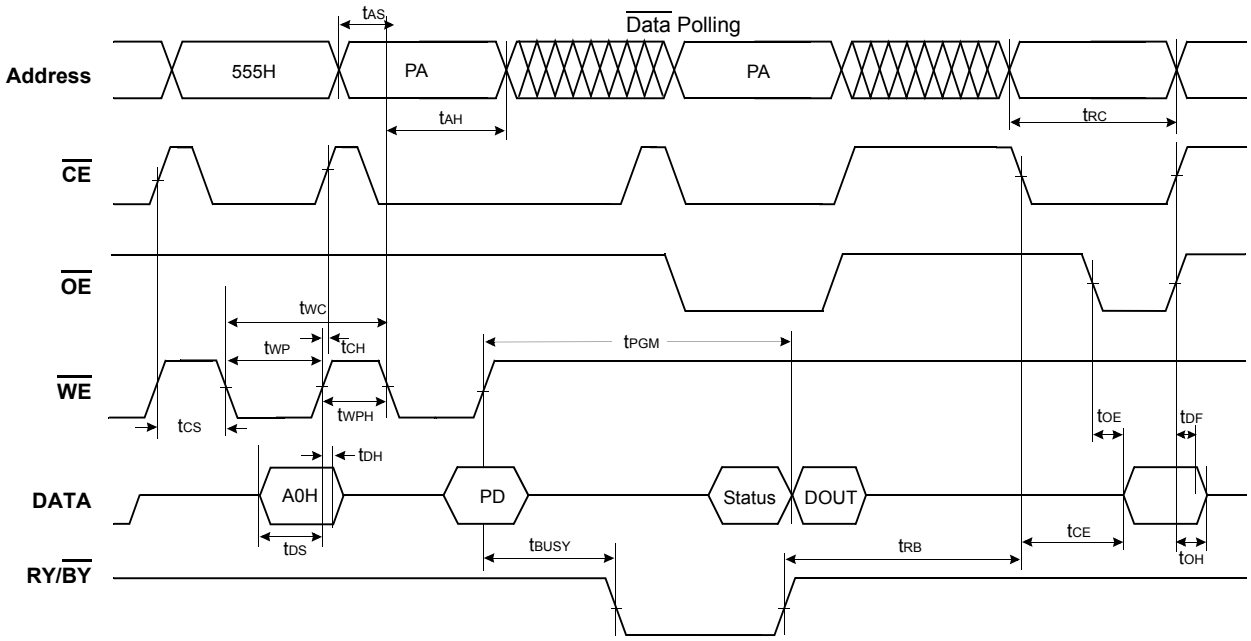
NOTE :
1) Not 100% tested.
2) The duration of the Program or Erase operation varies and is calculated in the internal algorithms.
3) tWC : 80ns(min) : 4E option

21.0 ERASE AND PROGRAM PERFORMANCE

Parameter		Condition	Limits			Unit	Comments
			Min	Typ	Max		
Block Erase Time	64 Kword	V_{CC}	-	1.4	7	sec	Includes 00H programming prior to erasure
		A_{CC}		TBD			
Chip Erase Time		V_{CC}	-	179.2		sec	Includes 00H programming prior to erasure
		A_{CC}		TBD			
Word Programming Time		V_{CC}	-	40	400	µs	Excludes system-level overhead
		A_{CC}		24	240		
Word Programming time with 32-words Buffer		V_{CC}	-	9.4	94	µs	Excludes system-level overhead
		A_{CC}		6	60		
Total 32-words Buffer Programming Time		V_{CC}	-	300	3000	µs	Excludes system-level overhead
		A_{CC}		192	1920		
Chip Programming Time with 32-word Buffer		V_{CC}	-	157.3	315	sec	Excludes system-level overhead

NOTE :
1) 25 °C, VCC = 3.0V 100,000 cycles, Typical (Checkerboard pattern), All values are subject to change.
2) System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each word.
In the preprogramming step of the Internal Erase Routine, all words are programmed to 00H before erasure.

SWITCHING WAVEFORMS
Program Operations



NOTE :
1) $\overline{DQ7}$ is the output of the complement of the data written to the device.
2) D_{OUT} is the output of the data written to the device.
3) PA : Program Address, PD : Program Data
4) The illustration shows the last two cycles of the program command sequence.

Figure 15: Program Operation Timings

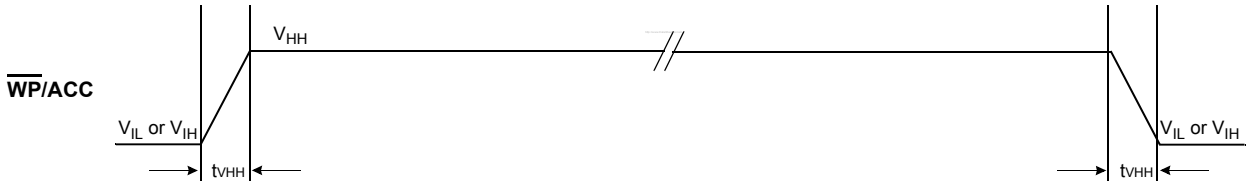


Figure 16: Accelerated Program Timings

While Write Operations

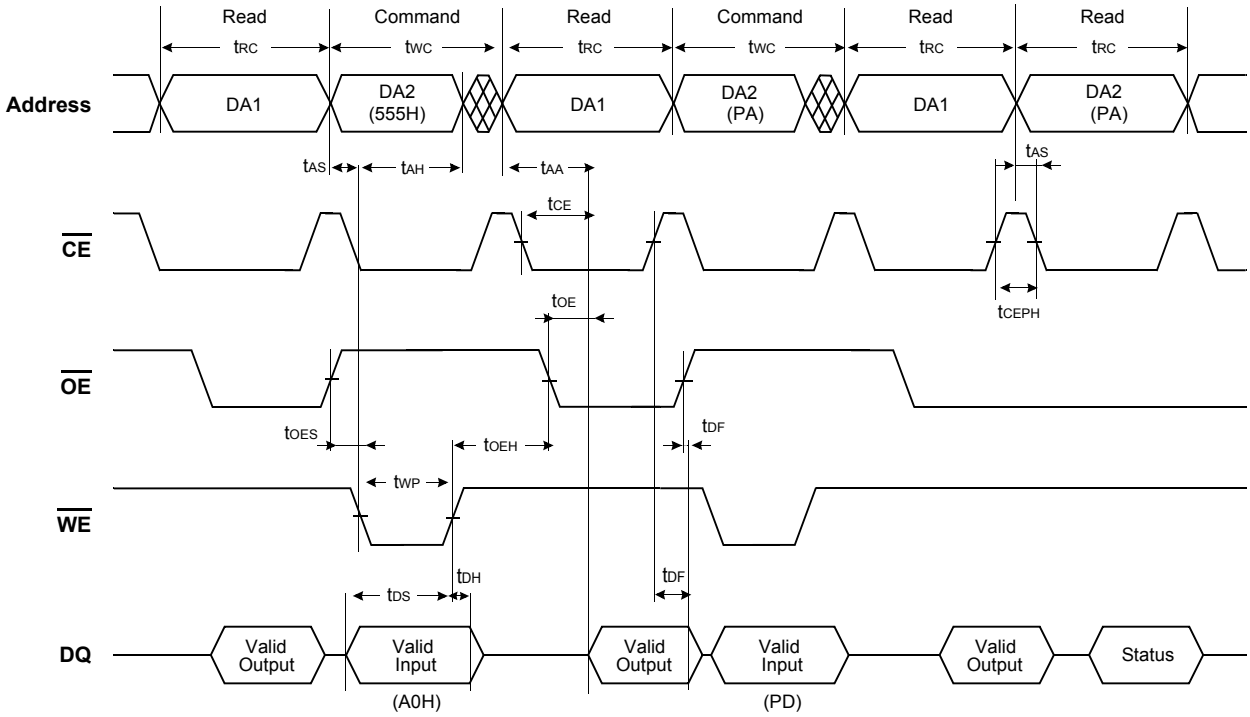


Figure 17: Read While Write Operation Timings

NOTE : This is an example in the program-case of the Read While Write function.
DA1 : Address of Bank1, DA2 : Address of Bank 2, PA = Program Address at one bank , RA = Read Address at the other bank,
PD = Program Data In , RD = Read Data Out

SWITCHING WAVEFORMS
Chip/Block Erase Operations

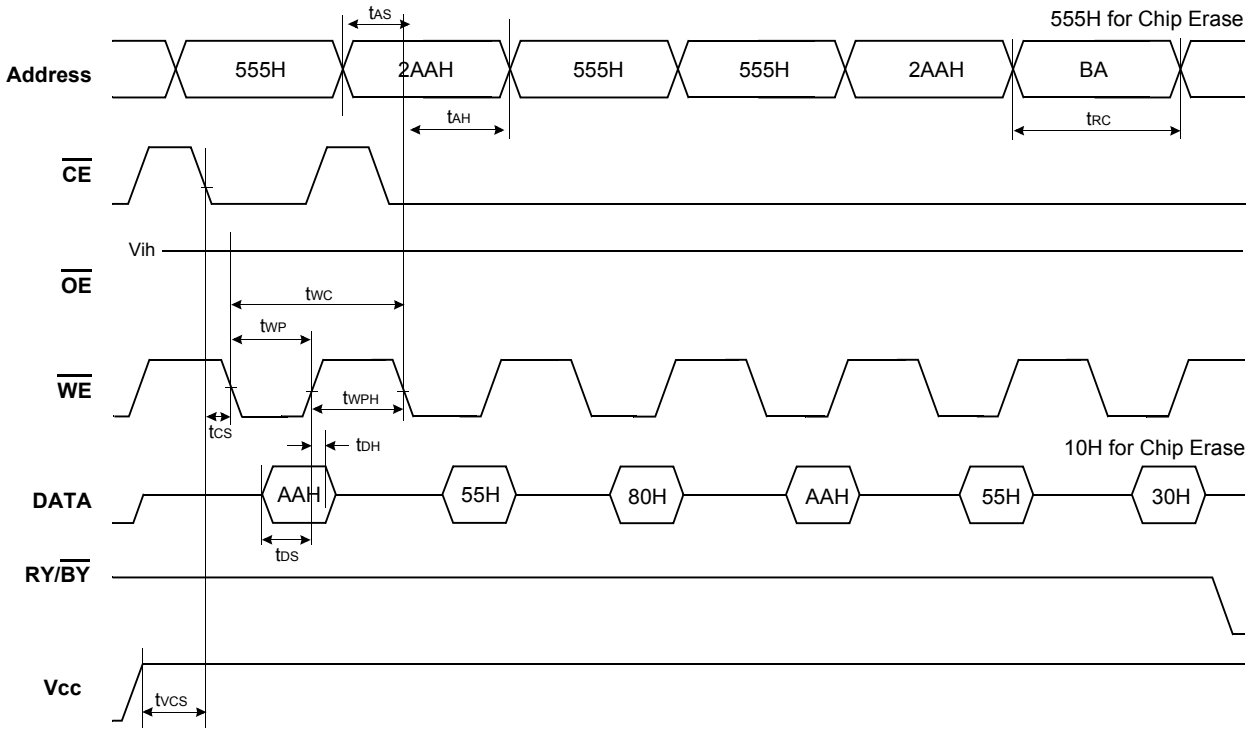
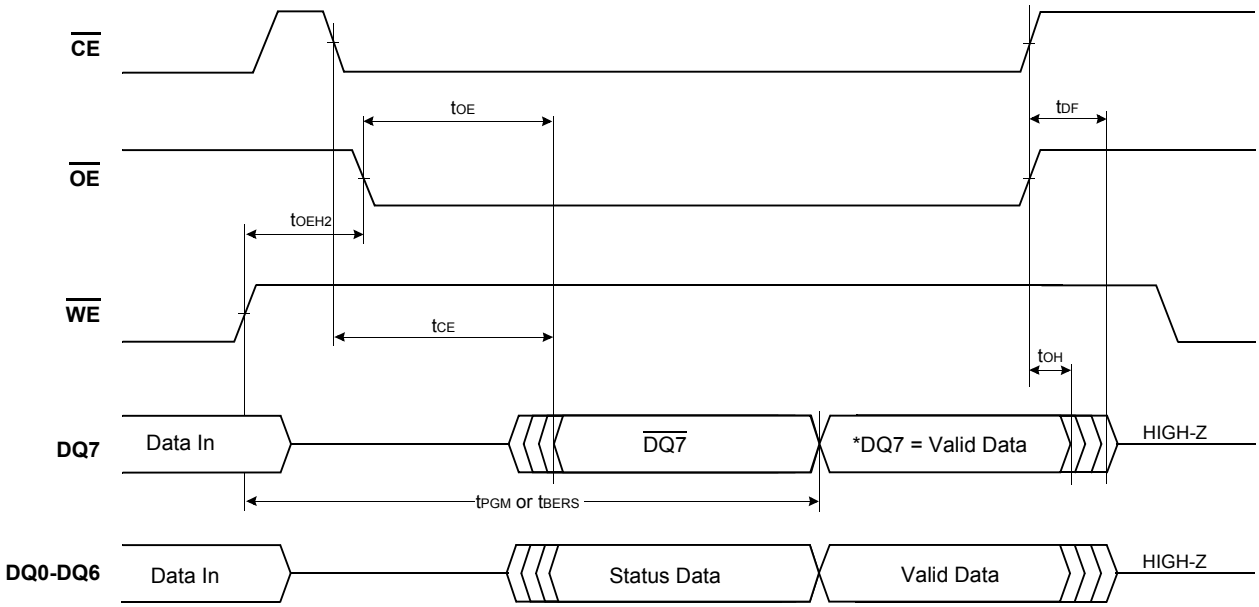


Figure 18: Chip/Block Erase Operation Timings

NOTE :
1) BA : Block Address

SWITCHING WAVEFORMS

Data Polling During Internal Routine Operation



NOTE :
DQ7=Vaild Data (The device has completed the internal operation).

Figure 19: Data Polling During Internal Routine Operation Timings

RY/BY Timing Diagram During Program/Erase Operation

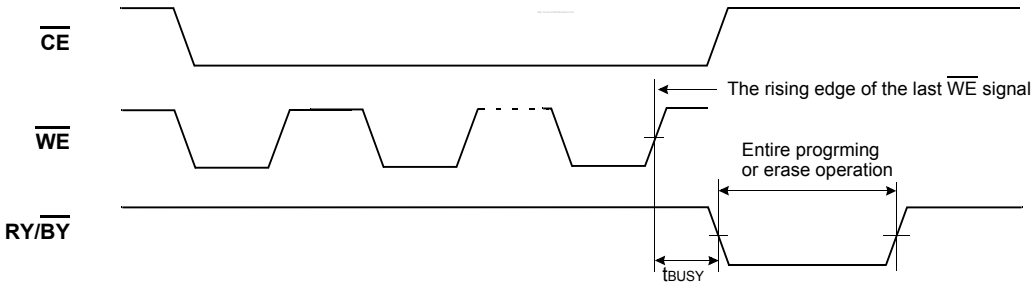
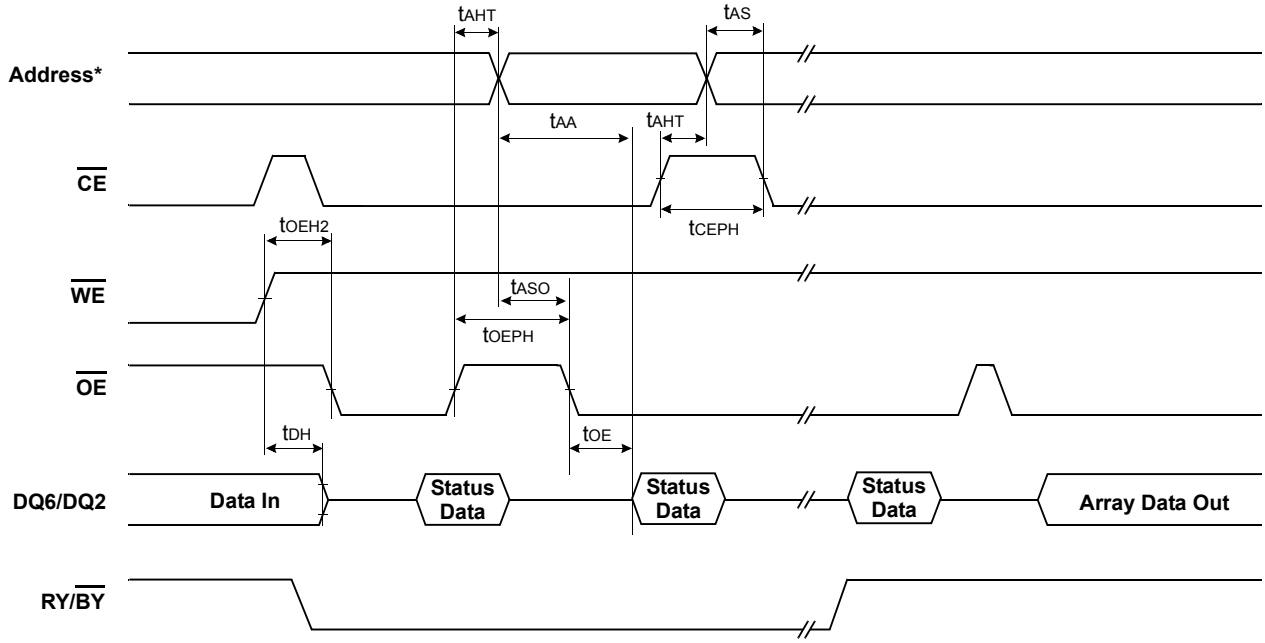


Figure 20: RY/BY Timing Diagram During Program/Erase Operation Timings

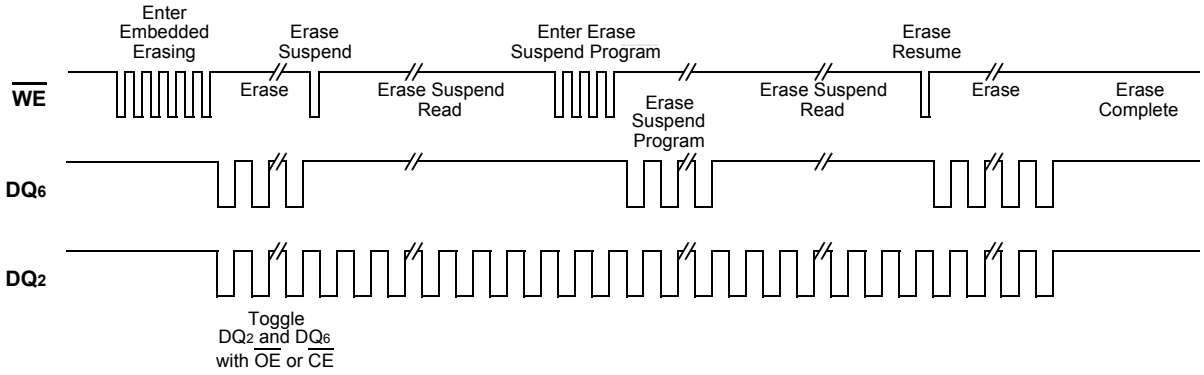
Parameter	Symbol	4E		Unit
		Min	Max	
Program/Erase Valid to RY/BY Delay	tBUSY	-	90	ns
Chip Enable Access Time	tCE	-	80	ns
Output Enable Time	tOE	-	30	ns
CE & OE Disable Time	tDF	-	16	ns
Output Hold Time from Address, CE or OE	tOH	5	-	ns
OE Hold Time	tOEH2	10	-	ns

NOTE :
The device supports only 4E at VIO = 1.7~1.95V.

SWITCHING WAVEFORMS
Toggle Bit During Internal Routine Operation



NOTE :
A = Valid Address ; Not required for DQ6. The switching waveform shows first two status cycle after command sequence, last status read cycle, and array data read cycle CE does not need to go high between status bit reads.
Address for the write operation must include a bank address (A21~A23) where the data is written.

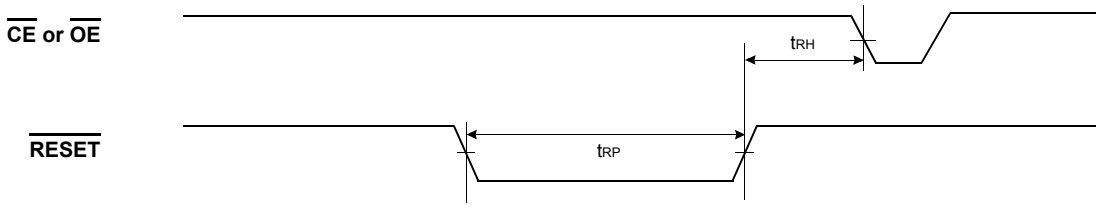


NOTE : DQ2 is read from the erase-suspended block.

Figure 21: Toggle Bit During Internal Routine Operation Timings

SWITCHING WAVEFORMS

RESET Timing Diagram



Power-up and RESET Timing Diagram

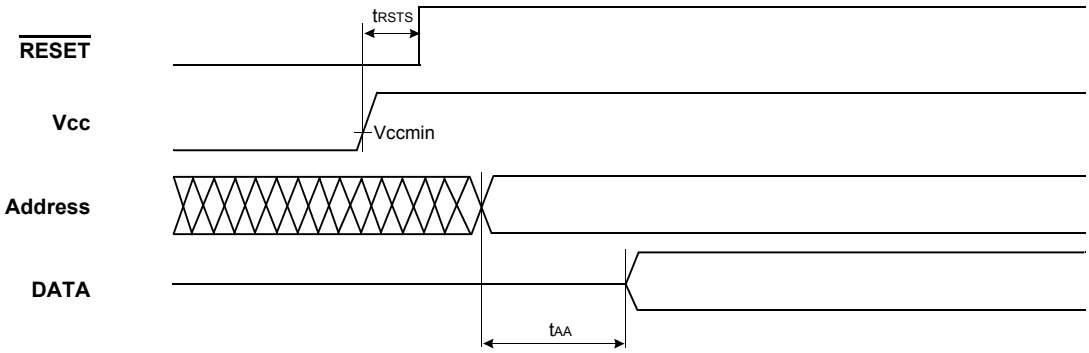
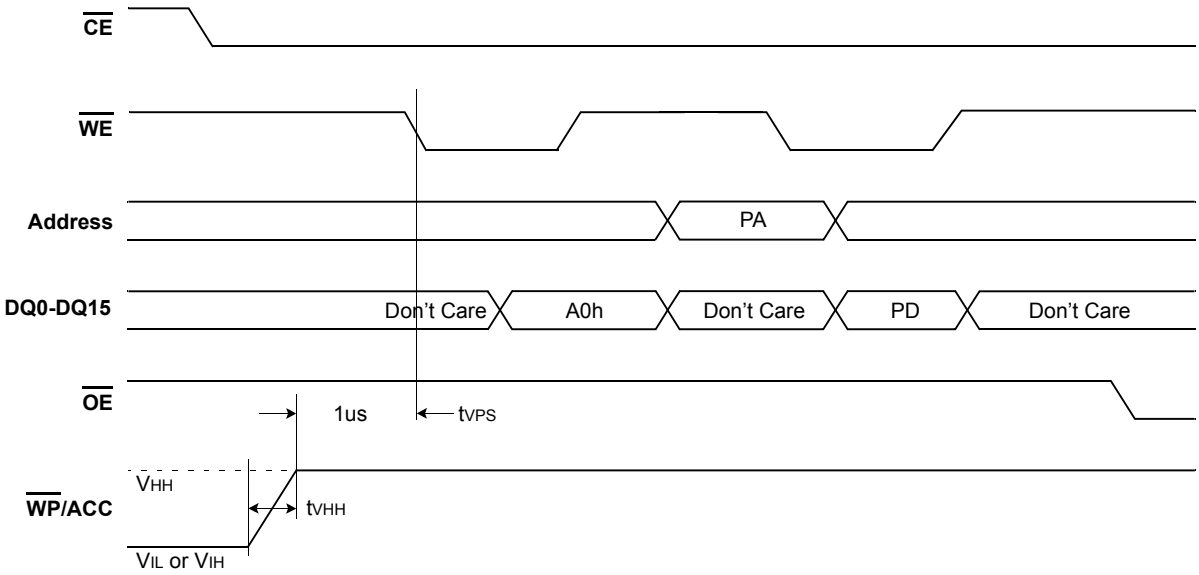


Figure 22: Power-up and RESET Timing Diagram

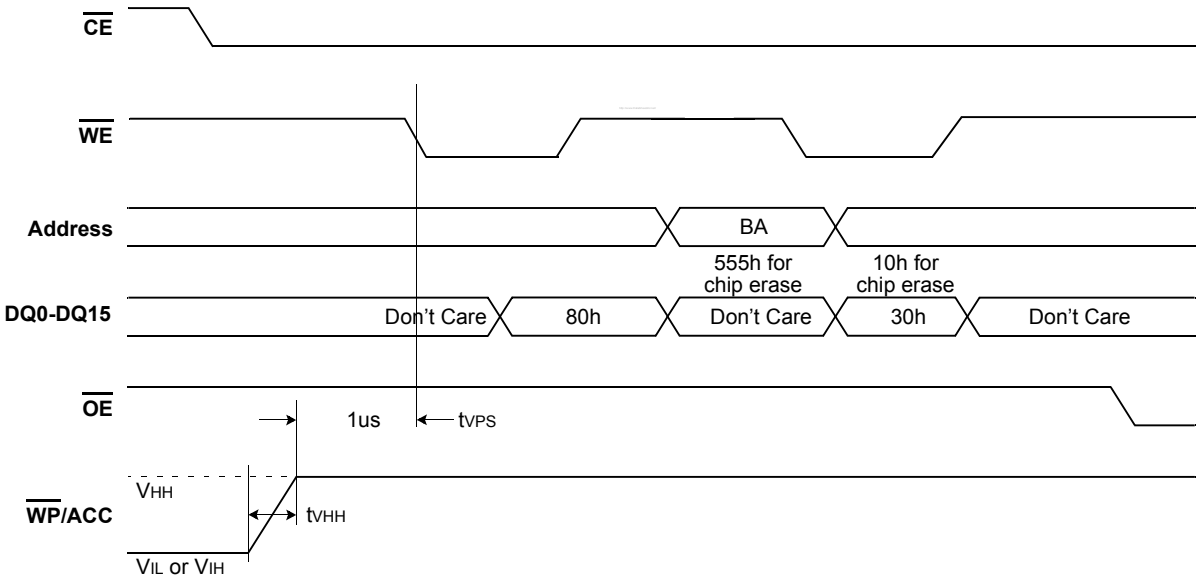
Parameter	Symbol	All Speed		Unit
		Min	Max	
RESET Pulse Width	tRP	30	-	μs
RESET High Time Before Read	tRH	200	-	ns
RESET Low Set-up Time	tRSTS	250	-	μs

SWITCHING WAVEFORMS

Unlock Bypass Program Operations(Accelerated Program)



Unlock Bypass Block Erase Operations(Accelerated Program)



NOTE :

1) VHH can be left high for subsequent programming pulses.
2) Use setup and hold times from conventional program operations.
3) Unlock Bypass Program/Erase commands can be used when the VHH is applied to $\overline{WP}$/ACC

Figure 23: Unlock Bypass Operation Timings

[Table 13] Address Table

Bank	Block	Block Size	(x16) Address Range
Bank3	BA255	64 kwords	FF0000h-FFFFFFh
	BA254	64 kwords	FE0000h-FEFFFFh
	BA253	64 kwords	FD0000h-FDFFFFh
	BA252	64 kwords	FC0000h-FCFFFFh
	BA251	64 kwords	FB0000h-FBFFFFh
	BA250	64 kwords	FA0000h-FAFFFFh
	BA249	64 kwords	F90000h-F9FFFFh
	BA248	64 kwords	F80000h-F8FFFFh
	BA247	64 kwords	F70000h-F7FFFFh
	BA246	64 kwords	F60000h-F6FFFFh
	BA245	64 kwords	F50000h-F5FFFFh
	BA244	64 kwords	F40000h-F4FFFFh
	BA243	64 kwords	F30000h-F3FFFFh
	BA242	64 kwords	F20000h-F2FFFFh
	BA241	64 kwords	F10000h-F1FFFFh
	BA240	64 kwords	F00000h-F0FFFFh
	BA239	64 kwords	EF0000h-EFFFFFh
	BA238	64 kwords	EE0000h-EEFFFFh
	BA237	64 kwords	ED0000h-EDFFFFh
	BA236	64 kwords	EC0000h-ECFFFFh
	BA235	64 kwords	EB0000h-EBFFFFh
	BA234	64 kwords	EA0000h-EAFFFFh
	BA233	64 kwords	E90000h-E9FFFFh
	BA232	64 kwords	E80000h-E8FFFFh
	BA231	64 kwords	E70000h-E7FFFFh
	BA230	64 kwords	E60000h-E6FFFFh
	BA229	64 kwords	E50000h-E5FFFFh
	BA228	64 kwords	E40000h-E4FFFFh
	BA227	64 kwords	E30000h-E3FFFFh
	BA226	64 kwords	E20000h-E2FFFFh
	BA225	64 kwords	E10000h-E1FFFFh
	BA224	64 kwords	E00000h-E0FFFFh
Bank2	BA223	64 kwords	DF0000h-DFFFFFh
	BA222	64 kwords	DE0000h-DEFFFFh
	BA221	64 kwords	DD0000h-DDFFFFh
	BA220	64 kwords	DC0000h-DCFFFFh
	BA219	64 kwords	DB0000h-DBFFFFh
	BA218	64 kwords	DA0000h-DAFFFFh
	BA217	64 kwords	D90000h-D9FFFFh
	BA216	64 kwords	D80000h-D8FFFFh
	BA215	64 kwords	D70000h-D7FFFFh
	BA214	64 kwords	D60000h-D6FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank2	BA213	64 kwords	D50000h-D5FFFFh
	BA212	64 kwords	D40000h-D4FFFFh
	BA211	64 kwords	D30000h-D3FFFFh
	BA210	64 kwords	D20000h-D2FFFFh
	BA209	64 kwords	D10000h-D1FFFFh
	BA208	64 kwords	D00000h-D0FFFFh
	BA207	64 kwords	CF0000h-CFFFFFh
	BA206	64 kwords	CE0000h-CEFFFFh
	BA205	64 kwords	CD0000h-CDFFFFh
	BA204	64 kwords	CC0000h-CCFFFFh
	BA203	64 kwords	CB0000h-CBFFFFh
	BA202	64 kwords	CA0000h-CAFFFFh
	BA201	64 kwords	C90000h-C9FFFFh
	BA200	64 kwords	C80000h-C8FFFFh
	BA199	64 kwords	C70000h-C7FFFFh
	BA198	64 kwords	C60000h-C6FFFFh
	BA197	64 kwords	C50000h-C5FFFFh
	BA196	64 kwords	C40000h-C4FFFFh
	BA195	64 kwords	C30000h-C3FFFFh
	BA194	64 kwords	C20000h-C2FFFFh
	BA193	64 kwords	C10000h-C1FFFFh
	BA192	64 kwords	C00000h-C0FFFFh
	BA191	64 kwords	BF0000h-BFFFFFh
	BA190	64 kwords	BE0000h-BEFFFFh
	BA189	64 kwords	BD0000h-BDFFFFh
	BA188	64 kwords	BC0000h-BCFFFFh
	BA187	64 kwords	BB0000h-BBFFFFh
	BA186	64 kwords	BA0000h-BAFFFFh
	BA185	64 kwords	B90000h-B9FFFFh
	BA184	64 kwords	B80000h-B8FFFFh
	BA183	64 kwords	B70000h-B7FFFFh
	BA182	64 kwords	B60000h-B6FFFFh
	BA181	64 kwords	B50000h-B5FFFFh
	BA180	64 kwords	B40000h-B4FFFFh
	BA179	64 kwords	B30000h-B3FFFFh
	BA178	64 kwords	B20000h-B2FFFFh
	BA177	64 kwords	B10000h-B1FFFFh
	BA176	64 kwords	B00000h-B0FFFFh
	BA175	64 kwords	AF0000h-AFFFFFh
	BA174	64 kwords	AE0000h-AEFFFFh
	BA173	64 kwords	AD0000h-ADFFFFh
	BA172	64 kwords	AC0000h-ACFFFFh
	BA171	64 kwords	AB0000h-ABFFFFh
	BA170	64 kwords	AA0000h-AAFFFFh
	BA169	64 kwords	A90000h-A9FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank2	BA168	64 kwords	A80000h-A8FFFFh
	BA167	64 kwords	A70000h-A7FFFFh
	BA166	64 kwords	A60000h-A6FFFFh
	BA165	64 kwords	A50000h-A5FFFFh
	BA164	64 kwords	A40000h-A4FFFFh
	BA163	64 kwords	A30000h-A3FFFFh
	BA162	64 kwords	A20000h-A2FFFFh
	BA161	64 kwords	A10000h-A1FFFFh
	BA160	64 kwords	A00000h-A0FFFFh
	BA159	64 kwords	9F0000h-9FFFFFh
	BA158	64 kwords	9E0000h-9EFFFFh
	BA157	64 kwords	9D0000h-9DFFFFh
	BA156	64 kwords	9C0000h-9CFFFFh
	BA155	64 kwords	9B0000h-9BFFFFh
	BA154	64 kwords	9A0000h-9AFFFFh
	BA153	64 kwords	990000h-99FFFFh
	BA152	64 kwords	980000h-98FFFFh
	BA151	64 kwords	970000h-97FFFFh
	BA150	64 kwords	960000h-96FFFFh
	BA149	64 kwords	950000h-95FFFFh
	BA148	64 kwords	940000h-94FFFFh
	BA147	64 kwords	930000h-93FFFFh
	BA146	64 kwords	920000h-92FFFFh
	BA145	64 kwords	910000h-91FFFFh
	BA144	64 kwords	900000h-90FFFFh
	BA143	64 kwords	8F0000h-8FFFFFh
	BA142	64 kwords	8E0000h-08EFFFFh
	BA141	64 kwords	8D0000h-8DFFFFh
	BA140	64 kwords	8C0000h-8CFFFFh
	BA139	64 kwords	8B0000h-8BFFFFh
	BA138	64 kwords	8A0000h-8AFFFFh
	BA137	64 kwords	890000h-89FFFFh
	BA136	64 kwords	880000h-88FFFFh
	BA135	64 kwords	870000h-87FFFFh
	BA134	64 kwords	860000h-86FFFFh
	BA133	64 kwords	850000h-85FFFFh
	BA132	64 kwords	840000h-84FFFFh
	BA131	64 kwords	830000h-83FFFFh
	BA130	64 kwords	820000h-82FFFFh
	BA129	64 kwords	810000h-81FFFFh
	BA128	64 kwords	800000h-80FFFFh
Bank1	BA127	64 kwords	7F0000h-7FFFFFh
	BA126	64 kwords	7E0000h-7EFFFFh
	BA125	64 kwords	7D0000h-7DFFFFh
	BA124	64 kwords	7C0000h-7CFFFFh

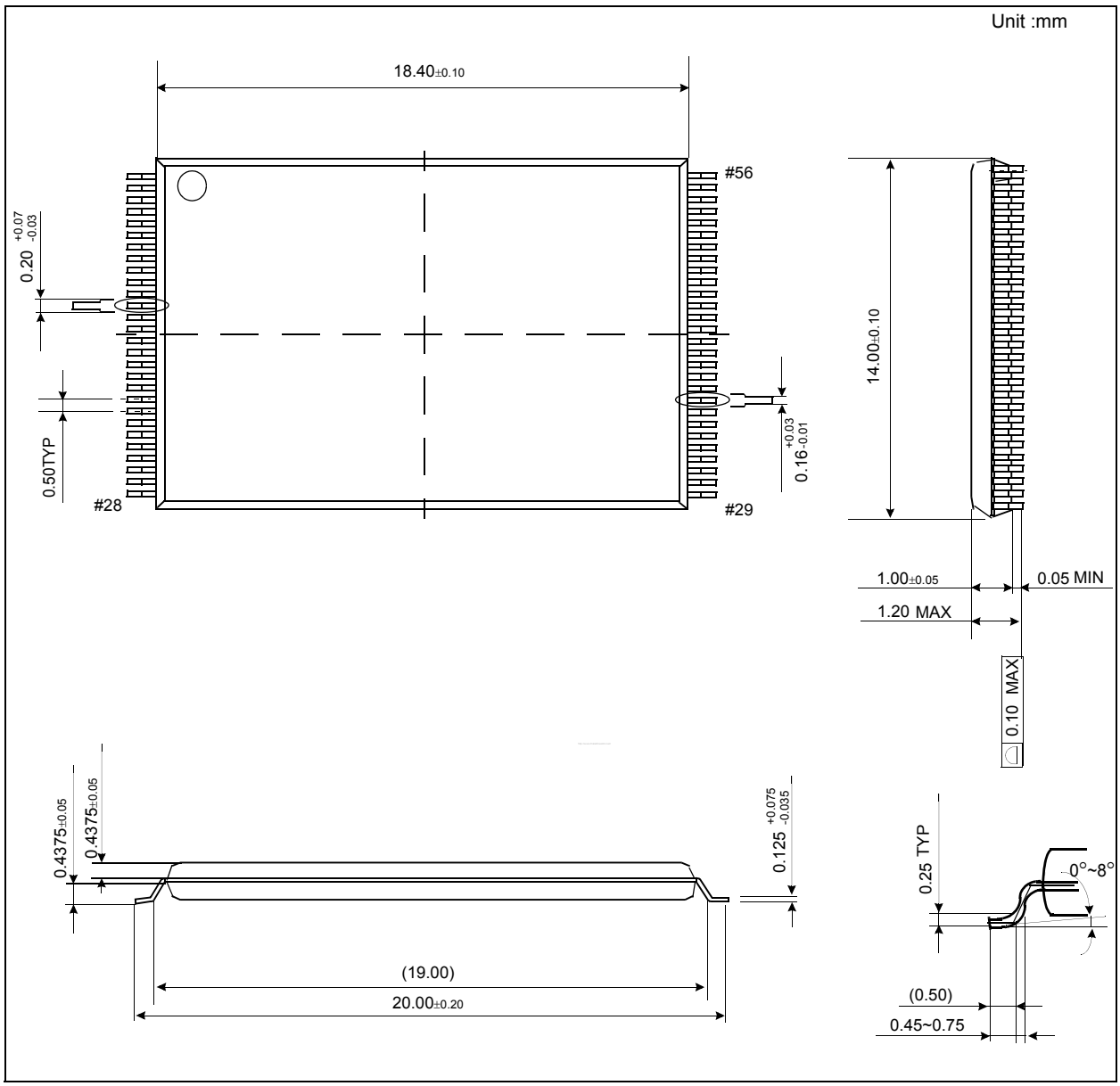
Bank	Block	Block Size	(x16) Address Range
Bank1	BA123	64 kwords	7B0000h-7BFFFFh
	BA122	64 kwords	7A0000h-7AFFFFh
	BA121	64 kwords	790000h-79FFFFh
	BA120	64 kwords	780000h-78FFFFh
	BA119	64 kwords	770000h-77FFFFh
	BA118	64 kwords	760000h-76FFFFh
	BA117	64 kwords	750000h-75FFFFh
	BA116	64 kwords	740000h-74FFFFh
	BA115	64 kwords	730000h-73FFFFh
	BA114	64 kwords	720000h-72FFFFh
	BA113	64 kwords	710000h-71FFFFh
	BA112	64 kwords	700000h-70FFFFh
	BA111	64 kwords	6F0000h-6FFFFFh
	BA110	64 kwords	6E0000h-6EFFFFh
	BA109	64 kwords	6D0000h-6DFFFFh
	BA108	64 kwords	6C0000h-6CFFFFh
	BA107	64 kwords	6B0000h-6BFFFFh
	BA106	64 kwords	6A0000h-6AFFFFh
	BA105	64 kwords	690000h-69FFFFh
	BA104	64 kwords	680000h-68FFFFh
	BA103	64 kwords	670000h-67FFFFh
	BA102	64 kwords	660000h-66FFFFh
	BA101	64 kwords	650000h-65FFFFh
	BA100	64 kwords	640000h-64FFFFh
	BA99	64 kwords	630000h-63FFFFh
	BA98	64 kwords	620000h-62FFFFh
	BA97	64 kwords	610000h-61FFFFh
	BA96	64 kwords	600000h-60FFFFh
	BA95	64 kwords	5F0000h-5FFFFFh
	BA94	64 kwords	5E0000h-5EFFFFh
	BA93	64 kwords	5D0000h-5DFFFFh
	BA92	64 kwords	5C0000h-5CFFFFh
	BA91	64 kwords	5B0000h-5BFFFFh
	BA90	64 kwords	5A0000h-5AFFFFh
	BA89	64 kwords	590000h-59FFFFh
	BA88	64 kwords	580000h-58FFFFh
	BA87	64 kwords	570000h-57FFFFh
	BA86	64 kwords	560000h-56FFFFh
	BA85	64 kwords	550000h-55FFFFh
	BA84	64 kwords	540000h-54FFFFh
	BA83	64 kwords	530000h-53FFFFh
	BA82	64 kwords	520000h-52FFFFh
	BA81	64 kwords	510000h-51FFFFh
	BA80	64 kwords	500000h-50FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank1	BA79	64 kwords	4F0000h-4FFFFFh
	BA78	64 kwords	4E0000h-4EFFFFh
	BA77	64 kwords	4D0000h-4DFFFFh
	BA76	64 kwords	4C0000h-4CFFFFh
	BA75	64 kwords	4B0000h-4BFFFFh
	BA74	64 kwords	4A0000h-4AFFFFh
	BA73	64 kwords	490000h-49FFFFh
	BA72	64 kwords	480000h-48FFFFh
	BA71	64 kwords	470000h-47FFFFh
	BA70	64 kwords	460000h-46FFFFh
	BA69	64 kwords	450000h-45FFFFh
	BA68	64 kwords	440000h-44FFFFh
	BA67	64 kwords	430000h-43FFFFh
	BA66	64 kwords	420000h-42FFFFh
	BA65	64 kwords	410000h-41FFFFh
	BA64	64 kwords	400000h-40FFFFh
	BA63	64 kwords	3F0000h-3FFFFFh
	BA62	64 kwords	3E0000h-3EFFFFh
	BA61	64 kwords	3D0000h-3DFFFFh
	BA60	64 kwords	3C0000h-3CFFFFh
	BA59	64 kwords	3B0000h-3BFFFFh
	BA58	64 kwords	3A0000h-3AFFFFh
	BA57	64 kwords	390000h-39FFFFh
	BA56	64 kwords	380000h-38FFFFh
	BA55	64 kwords	370000h-37FFFFh
	BA54	64 kwords	360000h-36FFFFh
	BA53	64 kwords	350000h-35FFFFh
	BA52	64 kwords	340000h-34FFFFh
	BA51	64 kwords	330000h-33FFFFh
	BA50	64 kwords	320000h-32FFFFh
	BA49	64 kwords	310000h-31FFFFh
	BA48	64 kwords	300000h-30FFFFh
	BA47	64 kwords	2F0000h-2FFFFFh
	BA46	64 kwords	2E0000h-2EFFFFh
	BA45	64 kwords	2D0000h-2DFFFFh
	BA44	64 kwords	2C0000h-2CFFFFh
	BA43	64 kwords	2B0000h-2BFFFFh
	BA42	64 kwords	2A0000h-2AFFFFh
	BA41	64 kwords	290000h-29FFFFh
	BA40	64 kwords	280000h-28FFFFh
	BA39	64 kwords	270000h-27FFFFh
	BA38	64 kwords	260000h-26FFFFh
	BA37	64 kwords	250000h-25FFFFh
	BA36	64 kwords	240000h-24FFFFh
	BA35	64 kwords	230000h-23FFFFh

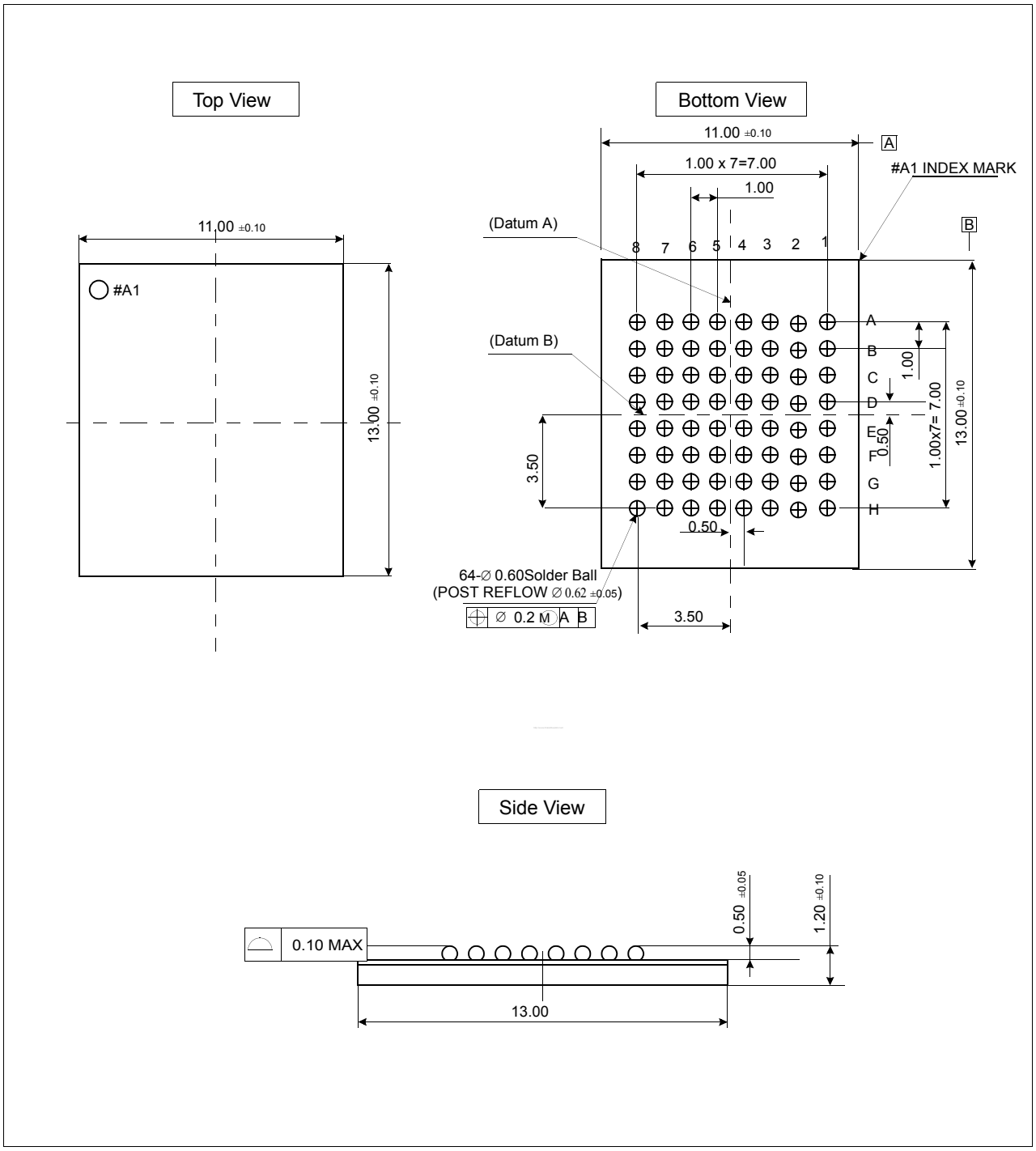
Bank	Block	Block Size	(x16) Address Range
Bank1	BA34	64 kwords	220000h-22FFFFh
	BA33	64 kwords	210000h-21FFFFh
	BA32	64 kwords	200000h-20FFFFh
Bank0	BA31	64 kwords	1F0000h-1FFFFFh
	BA30	64 kwords	1E0000h-1EFFFFh
	BA29	64 kwords	1D0000h-1DFFFFh
	BA28	64 kwords	1C0000h-1CFFFFh
	BA27	64 kwords	1B0000h-1BFFFFh
	BA26	64 kwords	1A0000h-1AFFFFh
	BA25	64 kwords	190000h-19FFFFh
	BA24	64 kwords	180000h-18FFFFh
	BA23	64 kwords	170000h-17FFFFh
	BA22	64 kwords	160000h-16FFFFh
	BA21	64 kwords	150000h-15FFFFh
	BA20	64 kwords	140000h-14FFFFh
	BA19	64 kwords	130000h-13FFFFh
	BA18	64 kwords	120000h-12FFFFh
	BA17	64 kwords	110000h-11FFFFh
	BA16	64 kwords	100000h-10FFFFh
	BA15	64 kwords	0F0000h-0FFFFFh
	BA14	64 kwords	0E0000h-0EFFFFh
	BA13	64 kwords	0D0000h-0DFFFFh
	BA12	64 kwords	0C0000h-0CFFFFh
	BA11	64 kwords	0B0000h-0BFFFFh
	BA10	64 kwords	0A0000h-0AFFFFh
	BA9	64 kwords	090000h-09FFFFh
	BA8	64 kwords	080000h-08FFFFh
	BA7	64 kwords	070000h-07FFFFh
	BA6	64 kwords	060000h-06FFFFh
	BA5	64 kwords	050000h-05FFFFh
	BA4	64 kwords	040000h-04FFFFh
	BA3	64 kwords	030000h-03FFFFh
	BA2	64 kwords	020000h-02FFFFh
	BA1	64 kwords	010000h-01FFFFh
	BA0	64 kwords	000000h-00FFFFh

22.0 PACKAGE DIMENSIONS

22.1 54TSOP



22.2 64FBGA


Top View
Bottom View
Side View
11.00 ±0.10
#A1
13.00 ±0.10
#A1 INDEX MARK
(Datum A)
(Datum B)
1.00 x 7=7.00
1.00
8 7 6 5 4 3 2 1
A B C D E F G H
3.50
0.50
1.00x7= 7.00
64-Ø 0.60Solder Ball
(POST REFLOW Ø 0.62 ±0.05)
Ø 0.2 M A B
0.10 MAX
0.50 ±0.05
1.20 ±0.10
13.00