

Document Title**16M x 8 Bit NAND Flash Memory**Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial issue.	Apr. 15th 2002	Advance
1.0	TBGA PKG Dimension Change 48-Ball, 6.0mm x 8.5mm --> 63-Ball, 9.0mm x 11.0mm	Sep. 5th 2002	Advance
2.0	1.A3 Pin assignment of TBGA Package is changed.(Page 4) (before) NC --> (after) Vss 2. Add the Rp vs tr ,tf & Rp vs ibusy graph for 1.8V device (Page 32) 3. Add the data protection Vcc guidance for 1.8V device - below about 1.1V. (Page 33)	Dec.10th 2002	Preliminary
2.1	The min. Vcc value 1.8V devices is changed. K9F28XXQ0C : Vcc 1.65V~1.95V --> 1.70V~1.95V	Mar. 6th 2003	
2.2	Pb-free Package is added. K9F2808U0C-FCB0,FIB0 K9F2808Q0C-HCB0,HIB0 K9F2816U0C-HCB0,HIB0 K9F2816U0C-PCB0,PIB0 K9F2816Q0C-HCB0,HIB0 K9F2808U0C-HCB0,HIB0 K9F2808U0C-PCB0,PIB0	Mar. 13rd 2003	
2.3	Some AC parameters are changed(K9F28XXQ0C). tWC tWH tWP tRC tREH tRP tREA tCEA Before 45 15 25 50 15 25 30 45 After 60 20 40 60 20 40 40 55		
2.4	1. New definition of the number of invalid blocks is added. (Minimum 502 valid blocks are guaranteed for each contiguous 64Mb memory space) 2. Note is added. (VIL can undershoot to -0.4V and VIH can overshoot to VCC +0.4V for durations of 20 ns or less.)	Mar. 26th 2003	
2.5	1. K9F2808U(Q)0C-DC(I)B0,K9F2816U(Q)0C-DC(I)B0 is deleted. 2. tWC is changed. 45ns(Before) ---> 50ns(After) 3. Minimum valid block number is changed. 1004(Before) --> 1009(After)	May. 24th 2003	
2.6	1. Minimum valid block number is changed. 1009(Before) --> 1004(After)	Oct. 10th 2003	

Note : For more detailed features and specifications including FAQ, please refer to Samsung's Flash web site.  
<http://www.samsung.com/Products/Semiconductor/Flash/TechnicalInfo/datasheets.htm>

The attached datasheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions about device. If you have any questions, please contact the SAMSUNG branch office near you.



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2.7	1. Add the Protrusion/Burr value in WSOP1 PKG Diagram 2. PKG(TSOP1, WSOP1) Dimension Change	May 21th 2004
2.8	1. NAND Flash Technical Notes is changed. -Invalid block -> initial invalid block ( page 13) -Error in write or read operation ( page 14 ) -Program Flow Chart ( page 14 )	Oct. 25th. 2004
2.9	1. The flow chart to creat the initial invalid block table is changed.	May 6th 2005

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## 16M x 8 Bit NAND Flash Memory

### PRODUCT LIST

Part Number	Vcc Range	Organization	PKG Type
K9F2808U0C-Y,P	2.7 ~ 3.6V	X8	TSOP1
K9F2808U0C-V,F			WSOP1

### FEATURES

- Voltage Supply : 2.7 ~ 3.6 V
  - Organization
    - Memory Cell Array
    - (16M + 512K)bit x 8bit
    - Data Register
    - (512 + 16)bit x 8bit
  - Automatic Program and Erase
    - Page Program
    - (512 + 16)Byte
    - Block Erase :
    - (16K + 512)Byte
  - Page Read Operation
    - Page Size
    - (512 + 16)Byte
    - Random Access : 10μs(Max.)
    - Serial Page Access : 50ns(Min.)
  - Fast Write Cycle Time
    - Program time : 200μs(Typ.)
    - Block Erase Time : 2ms(Typ.)
  - Command/Address/Data Multiplexed I/O Port
  - Hardware Data Protection
    - Program/Erase Lockout During Power Transitions
  - Reliable CMOS Floating-Gate Technology
    - Endurance : 100K Program/Erase Cycles
    - Data Retention : 10 Years
  - Command Register Operation
  - Unique ID for Copyright Protection
  - Package
    - K9F2808U0C-YCB0/YIB0
    - 48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
    - K9F2808U0C-PCB0/PIB0
    - 48 - Pin TSOP I (12 x 20 / 0.5 mm pitch) - Pb-free Package
    - K9F2808U0C-VCB0/VIB0
    - 48 - Pin WSOP I (12X17X0.7mm)
    - K9F2808U0C-FCB0/FIB0
    - 48 - Pin WSOP I (12X17X0.7mm) - Pb-free Package
- \* K9F2808U0C-V/F(WSOP1 ) is the same device as K9F2808U0C-Y/P(TSOP1) except package type.

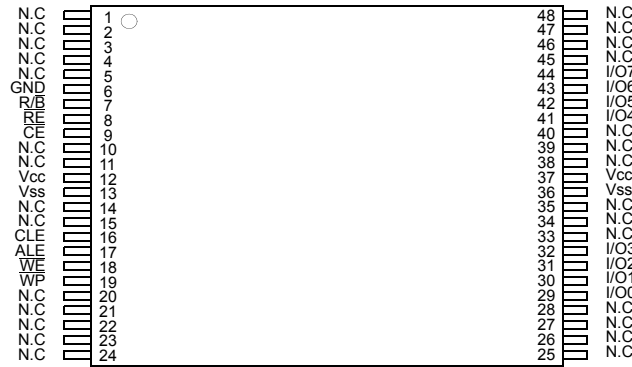
### GENERAL DESCRIPTION

Offered in 16Mx8bit , the K9F2808U0C is 128M bit with spare 4M bit capacity. The device is offered in 3.3V Vcc. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 200μs on the 528-byte page and an erase operation can be performed in typical 2ms on a 16K-byte block. Data in the page can be read out at 50ns cycle time per word. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9F2808U0C's extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm.

The K9F2808U0C is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

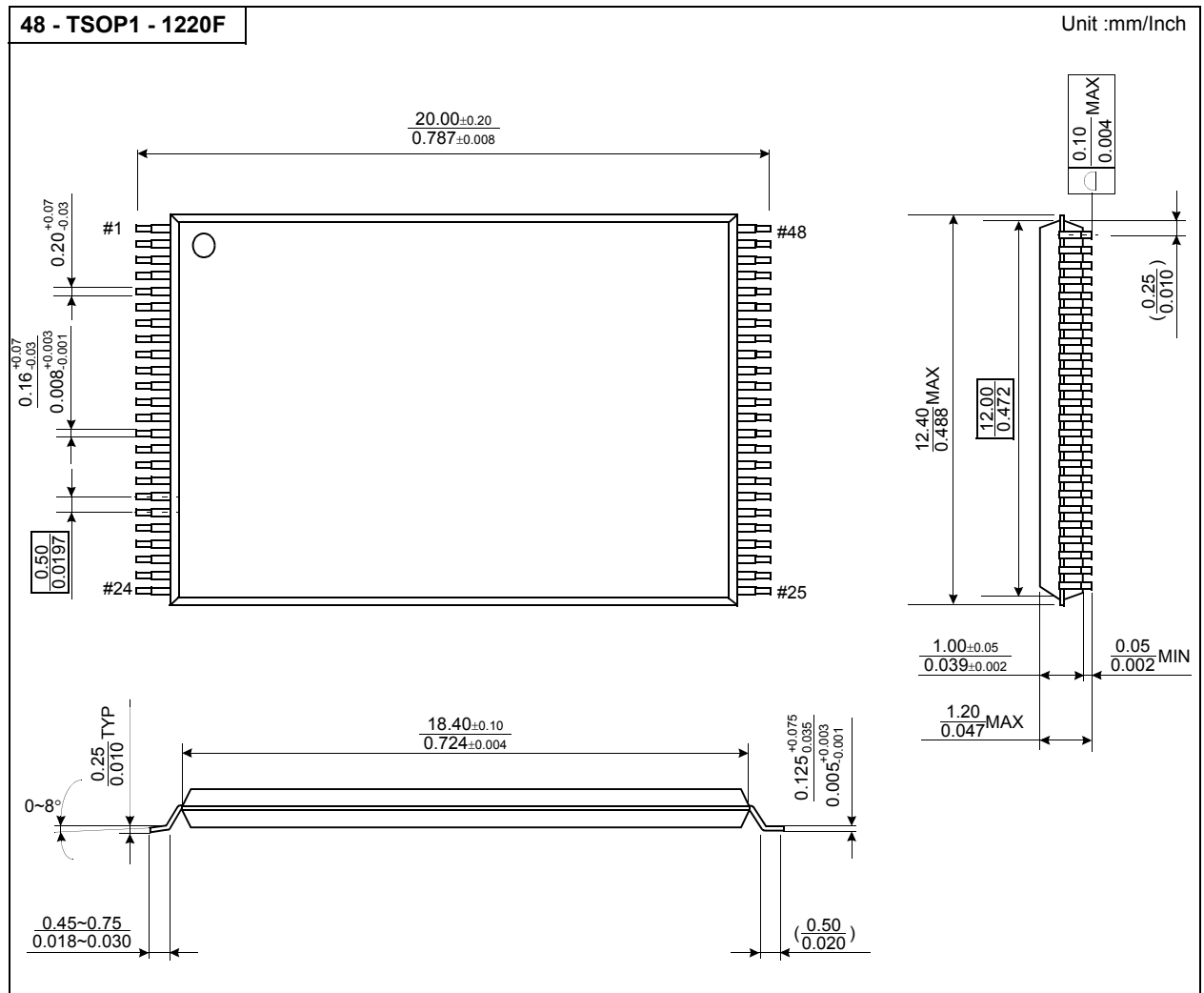
PIN CONFIGURATION (TSOP1)

K9F2808U0C-YCB0,PCB0/Y1B0,PIB0



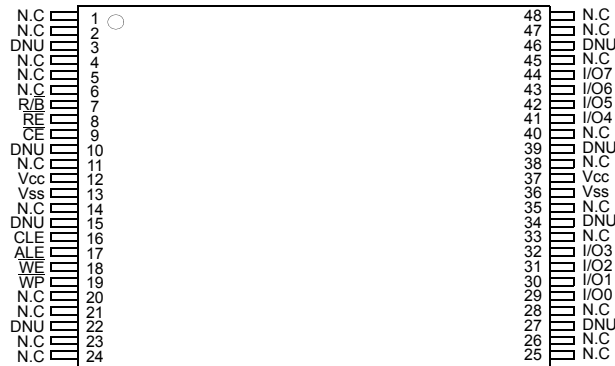
PACKAGE DIMENSIONS

48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)



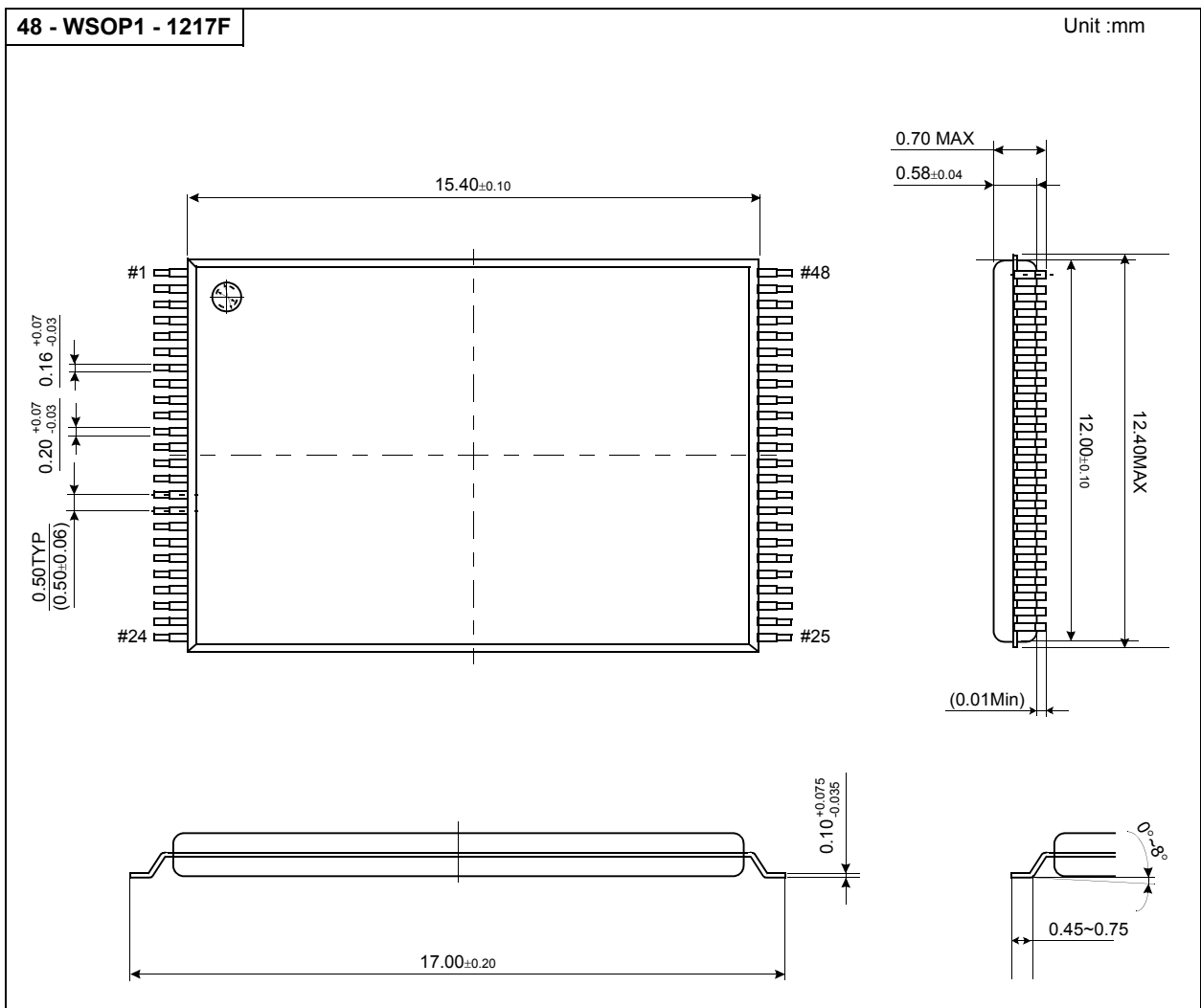
PIN CONFIGURATION (WSOP1)

K9F2808U0C-VCB0,FCB0/VIB0,FIB0



PACKAGE DIMENSIONS

48-PIN LEAD PLASTIC VERY VERY THIN SMALL OUT-LINE PACKAGE TYPE (I)



## PIN DESCRIPTION

Pin Name	Pin Function
I/O <sub>0</sub> ~ I/O <sub>7</sub>	<b>DATA INPUTS/OUTPUTS</b> The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	<b>COMMAND LATCH ENABLE</b> The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE signal.
ALE	<b>ADDRESS LATCH ENABLE</b> The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE with ALE high.
$\overline{\text{CE}}$	<b>CHIP ENABLE</b> The CE input is the device selection control. When the device is in the Busy state, CE high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE control during read operation, refer to 'Page read' section of Device operation .
$\overline{\text{RE}}$	<b>READ ENABLE</b> The RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE which also increments the internal column address counter by one.
$\overline{\text{WE}}$	<b>WRITE ENABLE</b> The WE input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE pulse.
$\overline{\text{WP}}$	<b>WRITE PROTECT</b> The WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP pin is active low.
R/B	<b>READY/BUSY OUTPUT</b> The R/B output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
Vccq	<b>OUTPUT BUFFER POWER</b> Vccq is the power supply for Output Buffer. Vccq is internally connected to Vcc, thus should be biased to Vcc.
Vcc	<b>POWER</b> Vcc is the power supply for device.
Vss	<b>GROUND</b>
N.C	<b>NO CONNECTION</b> Lead is not internally connected.
GND	<b>GND INPUT FOR ENABLING SPARE AREA</b> To do sequential read mode including spare area , connect this input pin to Vss or set to static low state or to do sequential read mode excluding spare area , connect this input pin to Vcc or set to static high state.
DNU	<b>DO NOT USE</b> Leave it disconnected.

**NOTE :**

Connect all Vcc and Vss pins of each device to common power supply outputs.  
Do not leave Vcc or Vss disconnected.

Figure 1-1. K9F2808U0C FUNCTIONAL BLOCK DIAGRAM

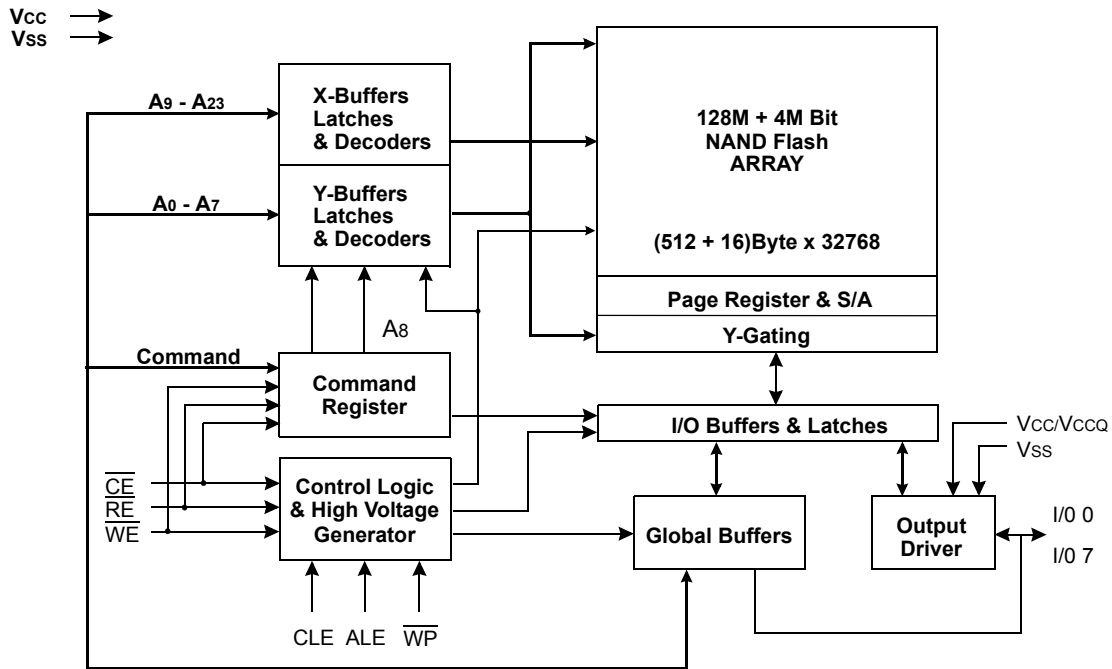
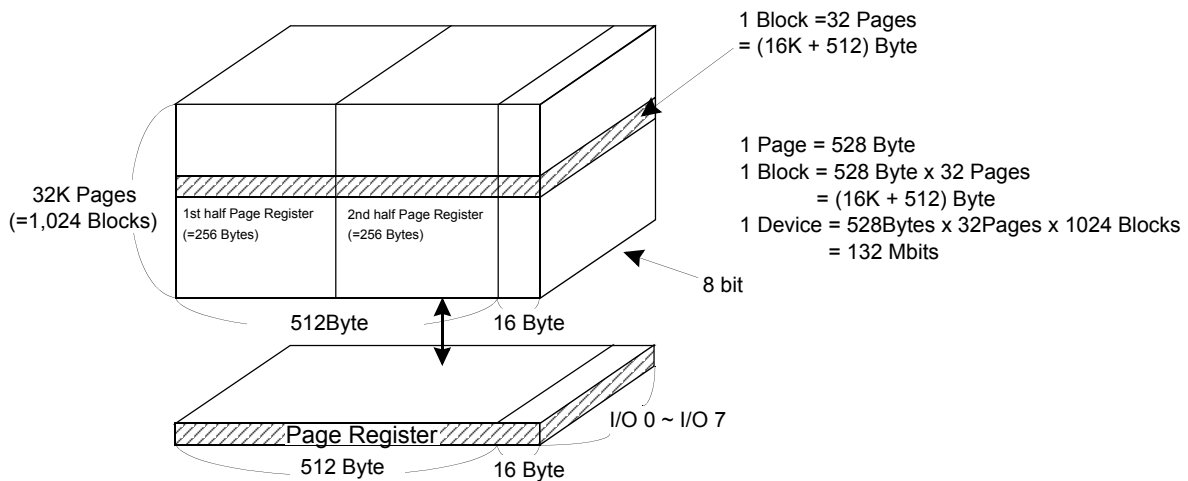


Figure 2-1. K9F2808U0C ARRAY ORGANIZATION



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16	Row Address (Page Address)
3rd Cycle	A17	A18	A19	A20	A21	A22	A23	L*	

NOTE : Column Address : Starting Address of the Register.

00h Command(Read) : Defines the starting address of the 1st half of the register.

01h Command(Read) : Defines the starting address of the 2nd half of the register.

\* A8 is set to "Low" or "High" by the 00h or 01h Command.

\* The device ignores any additional input of address cycles than required.

\* L must be set to "Low".

## PRODUCT INTRODUCTION

The K9F2808U0C is a 132Mbit(138,412,032 bit) memory organized as 32,768 rows(pages) by 528 columns. Spare eight columns are located from column address of 512~527. A 528-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of two NAND structured strings. A NAND structure consists of 16 cells. Total 135168 NAND cells reside in a block. The array organization is shown in Figure 2-1,2-2. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 1024 separately erasable 16K-Byte blocks. It indicates that the bit by bit erase operation is prohibited on the K9F2808U0C.

The K9F2808U0C has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts while providing high performance and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing  $\overline{WE}$  to low while  $\overline{CE}$  is low. Data is latched on the rising edge of  $\overline{WE}$ . Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset command, Read command, Status Read command, etc require just one cycle bus. Some other commands like Page Program and Block Erase, require two cycles: one cycle for setup and the other cycle for execution. The 16K-byte physical space requires 24 addresses, thereby requiring three cycles for word-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following the required command input. In Block Erase operation, however, only the two row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9F2808U0C.

The device includes one block sized OTP(One Time Programmable), which can be used to increase system security or to provide identification capabilities. Detailed information can be obtained by contact with Samsung.

**Table 1. COMMAND SETS**

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read 1	00h/01h <sup>(1)</sup>	-	
Read 2	50h	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Block Erase	60h	D0h	
Read Status	70h	-	O

**NOTE:** 1. The 00h command defines starting address of the 1st half of registers.

The 01h command defines starting address of the 2nd half of registers.

After data access on 2nd half of register by the 01h command, start pointer is automatically moved to 1st half register(00h) on the next cycle.

**Caution :** Any undefined command inputs are prohibited except for above command set of Table 1.



## ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V <sub>SS</sub>		V <sub>IN/OUT</sub>	-0.6 to + 4.6	V
		V <sub>CC</sub>	-0.6 to + 4.6	
		V <sub>CCQ</sub>	-0.6 to + 4.6	
Temperature Under Bias	K9F2808U0C-XCB0	T <sub>BIAS</sub>	-10 to +125	°C
	K9F2808U0C-XIB0		-40 to +125	
Storage Temperature	K9F2808U0C-XCB0	T <sub>STG</sub>	-65 to +150	°C
	K9F2808U0C-XIB0			
Short Circuit Current		I <sub>OS</sub>	5	mA

## NOTE :

- Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is V<sub>CC</sub>+0.3V which, during transitions, may overshoot to V<sub>CC</sub>+2.0V for periods <20ns.
- Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, K9F2808U0C-XCB0 :T<sub>A</sub>=0 to 70°C, K9F2808U0C-XIB0:T<sub>A</sub>=-40 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V <sub>CC</sub>	2.7	3.3	3.6	V
Supply Voltage	V <sub>CCQ</sub>	2.7	3.3	3.6	V
Supply Voltage	V <sub>SS</sub>	0	0	0	V

## DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit	
Operating Current	Sequential Read	I <sub>CC1</sub>	t <sub>RC</sub> =50ns, $\overline{CE}=V_{IL}$ I <sub>OUT</sub> =0mA	-	10	20	mA	
	Program	I <sub>CC2</sub>	-	-	10	20		
	Erase	I <sub>CC3</sub>	-	-	10	20		
Stand-by Current(TTL)		I <sub>SB1</sub>	$\overline{CE}=V_{IH}$ , $\overline{WP}=0V/V_{CC}$	-	-	1	μA	
Stand-by Current(CMOS)		I <sub>SB2</sub>	$\overline{CE}=V_{CC}-0.2$ , $\overline{WP}=0V/V_{CC}$	-	10	50		
Input Leakage Current		I <sub>LI</sub>	V <sub>IN</sub> =0 to V <sub>CC</sub> (max)	-	-	±10		
Output Leakage Current		I <sub>LO</sub>	V <sub>OUT</sub> =0 to V <sub>CC</sub> (max)	-	-	±10	V	
Input High Voltage		V <sub>IH</sub> *	I/O pins	2.0	-	V <sub>CCQ</sub> +0.3		
			Except I/O pins	2.0	-	V <sub>CC</sub> +0.3		
Input Low Voltage, All inputs		V <sub>IL</sub> *	-	-0.3	-	0.8		
Output High Voltage Level		V <sub>OH</sub>	I <sub>OH</sub> =-400μA	2.4	-	-		
Output Low Voltage Level		V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4		
Output Low Current(R/ $\overline{B}$ )		I <sub>OL</sub> (R/ $\overline{B}$ )	V <sub>OL</sub> =0.4V	8	10	-		mA

NOTE : V<sub>IL</sub> can undershoot to -0.4V and V<sub>IH</sub> can overshoot to V<sub>CC</sub> +0.4V for durations of 20 ns or less.

**VALID BLOCK**

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	NvB	1004	-	1024	Blocks

**NOTE :**

- The device may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for a appropriate management of invalid blocks.
- The 1st block, which is placed on 00h block address, is guaranteed to be a valid block, does not require Error Correction up to 1K program/erase cycles.
- Minimum 502 valid blocks are guaranteed for each contiguous 64Mb memory space.

**AC TEST CONDITION**

(K9F2808U0C-XCB0 :TA=0 to 70°C, K9F2808U0C-XIB0:TA=-40 to 85°C  
K9F2808U0C : Vcc=2.7V~3.6V unless otherwise noted)

Parameter	K9F2808U0C
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load (Vcc:3.0V +/-10%)	1 TTL GATE and CL=50pF
Output Load (Vcc:3.3V +/-10%)	1 TTL GATE and CL=100pF

**CAPACITANCE**(TA=25°C, VCC=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>IL</sub> =0V	-	10	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	10	pF

**NOTE :** Capacitance is periodically sampled and not 100% tested.

**MODE SELECTION**

CLE	ALE	$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{RE}}$	GND	$\overline{\text{WP}}$	Mode	
H	L	L		H	X	X	Read Mode	Command Input
L	H	L		H	X	X		Address Input(3clock)
H	L	L		H	X	H	Write Mode	Command Input
L	H	L		H	X	H		Address Input(3clock)
L	L	L		H	L	H	Data Input	
L	L	L		H	L	X	Data Output	
L	L	L	H		L	X	During Read(Busy)	
X	X	X	X	H	L	X	During Read(Busy)	
X	X	X	X	X	L	H	During Program(Busy)	
X	X	X	X	X	X	H	During Erase(Busy)	
X	X <sup>(1)</sup>	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V	0V/V <sub>CC</sub> <sup>(2)</sup>	Stand-by	

**NOTE :** 1. X can be V<sub>IL</sub> or V<sub>IH</sub>.

2.  $\overline{\text{WP}}$  should be biased to CMOS high or CMOS low for standby.

**Program/Erase Characteristics**

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t <sub>PROG</sub>	-	200	500	μs
Number of Partial Program Cycles in the Same Page	Main Array	-	-	2	cycles
	Spare Array	-	-	3	cycles
Block Erase Time	t <sub>BERS</sub>	-	2	3	ms

**NOTE :** Typical program time is defined as the time within which more than 50% of the whole pages are programmed at Vcc of 3.3V and temperature of 25°C.

## AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	K9F2808U0C		Unit
CLE Set-up Time	tCLS	0	-	ns
CLE Hold Time	tCLH	10	-	ns
$\overline{\text{CE}}$ Setup Time	tCS	0	-	ns
$\overline{\text{CE}}$ Hold Time	tCH	10	-	ns
$\overline{\text{WE}}$ Pulse Width	tWP	25	-	ns
ALE Setup Time	tALS	0	-	ns
ALE Hold Time	tALH	10	-	ns
Data Setup Time	tDS	20	-	ns
Data Hold Time	tDH	10	-	ns
Write Cycle Time	tWC	50	-	ns
$\overline{\text{WE}}$ High Hold Time	tWH	15	-	ns

NOTE : 1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

## AC Characteristics for Operation

Parameter	Symbol	K9F2808U0C		Unit	
Data Transfer from Cell to Register	tr	-	10	$\mu\text{s}$	
ALE to $\overline{\text{RE}}$ Delay	tAR	10	-	ns	
CLE to $\overline{\text{RE}}$ Delay	tCLR	10	-	ns	
Ready to $\overline{\text{RE}}$ Low	trr	20	-	ns	
$\overline{\text{RE}}$ Pulse Width	trp	25	-	ns	
$\overline{\text{WE}}$ High to Busy	tWB	-	100	ns	
Read Cycle Time	trc	50	-	ns	
$\overline{\text{CE}}$ Access Time	tCEA	-	45	ns	
$\overline{\text{RE}}$ Access Time	tREA	-	30	ns	
$\overline{\text{RE}}$ High to Output Hi-Z	trHZ	-	30	ns	
$\overline{\text{CE}}$ High to Output Hi-Z	tCHZ	-	20	ns	
$\overline{\text{RE}}$ or $\overline{\text{CE}}$ High to Output hold	toH	15	-	ns	
$\overline{\text{RE}}$ High Hold Time	treH	15	-	ns	
Output Hi-Z to $\overline{\text{RE}}$ Low	tIR	0	-	ns	
$\overline{\text{WE}}$ High to $\overline{\text{RE}}$ Low	tWHR	60	-	ns	
Device Resetting Time(Read/Program/Erase)	trST	-	5/10/500 <sup>(1)</sup>	$\mu\text{s}$	
K9F2808U0C- Y,P,V,F only	Last RE High to Busy (at sequential read)	trB	-	100	ns
	$\overline{\text{CE}}$ High to Ready(in case of interception by $\overline{\text{CE}}$ at read)	tCRY	-	50 +tr(R/ $\overline{\text{B}}$ ) <sup>(3)</sup>	ns
	$\overline{\text{CE}}$ High Hold Time(at the last serial read) <sup>(2)</sup>	tCEH	100	-	ns

NOTE : 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5 $\mu\text{s}$ .

2. To break the sequential read cycle,  $\overline{\text{CE}}$  must be held high for longer time than tCEH.

3. The time to Ready depends on the value of the pull-up resistor tied R/ $\overline{\text{B}}$  pin.

**NAND Flash Technical Notes**

**Initial Invalid Block(s)**

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is so called as the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction up to 1K program/erase cycles.

**Identifying Initial Invalid Block(s)**

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 6th byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 517. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the initial invalid block information is prohibited.

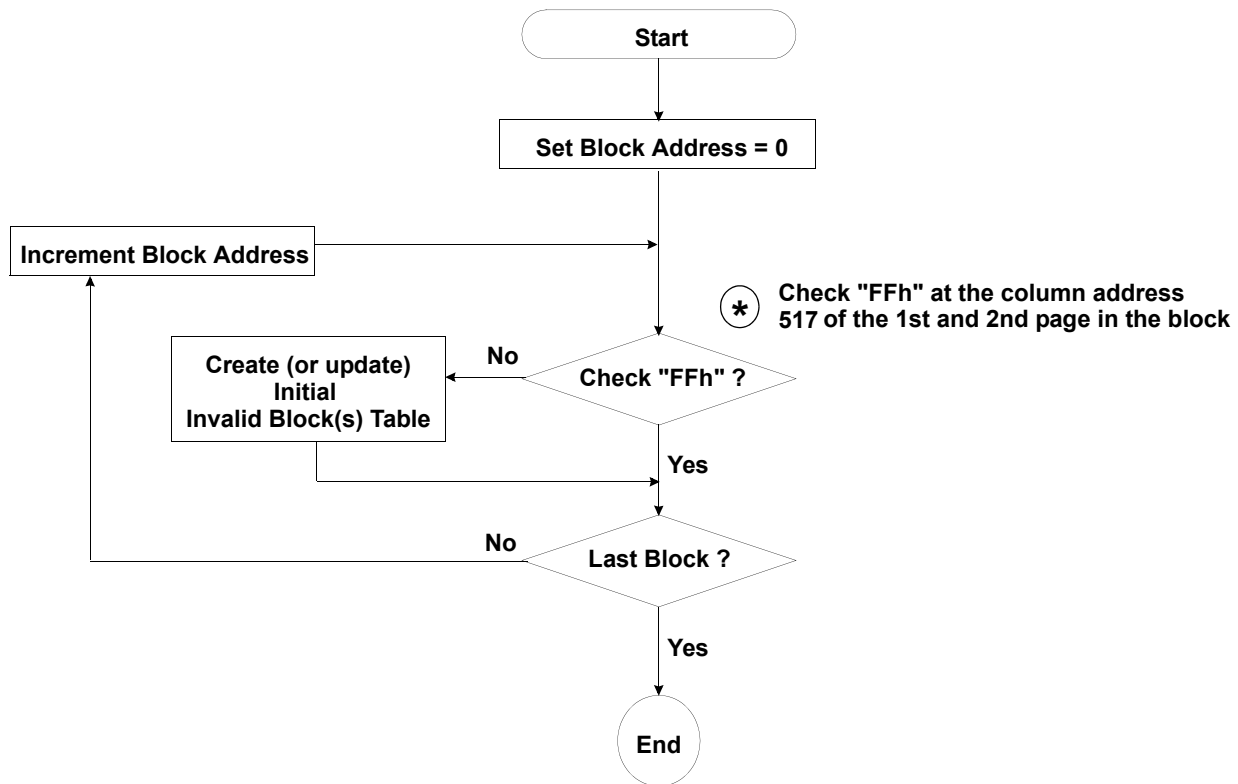


Figure 3. Flow chart to create initial invalid block table.

**NAND Flash Technical Notes** (Continued)

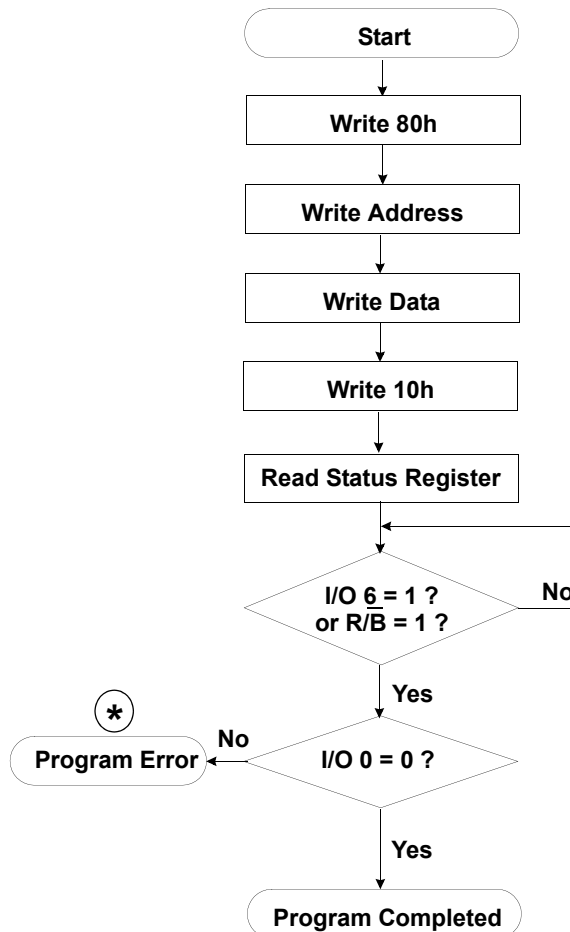
**Error in write or read operation**

Within its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Single Bit Failure	Verify ECC -> ECC Correction

**ECC** : Error Correcting Code --> Hamming Code etc.  
 Example) 1bit correction & 2bit detection

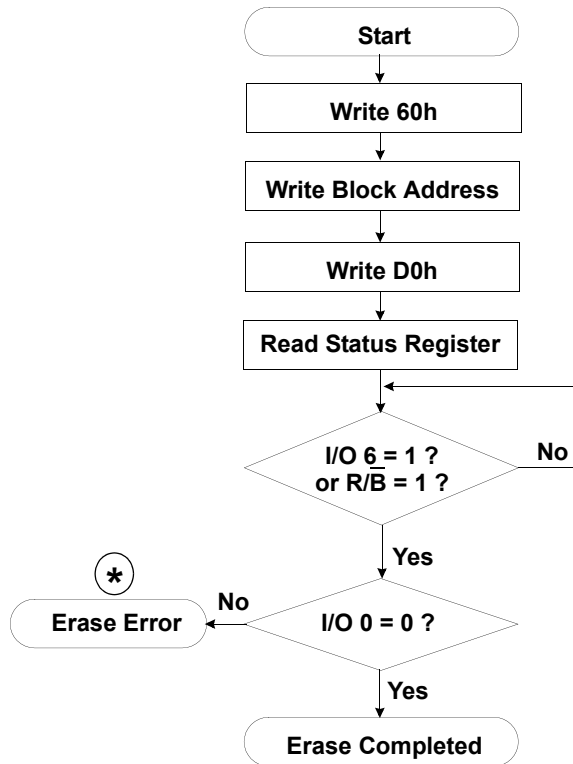
**Program Flow Chart**



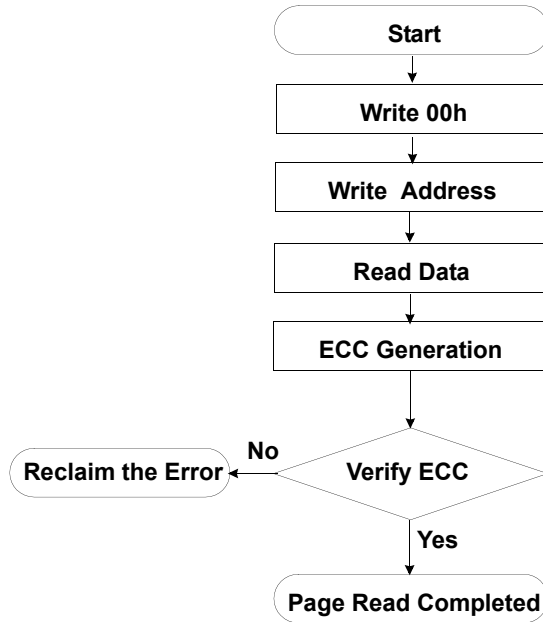
\* : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

**NAND Flash Technical Notes** (Continued)

**Erase Flow Chart**

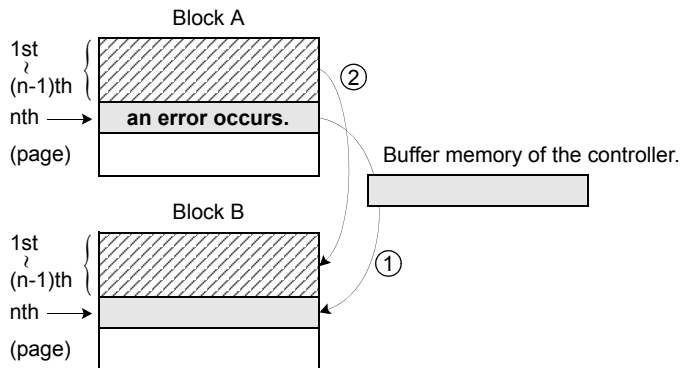


**Read Flow Chart**



\* : If erase operation results in an error, map out the failing block and replace it with another block.

**Block Replacement**



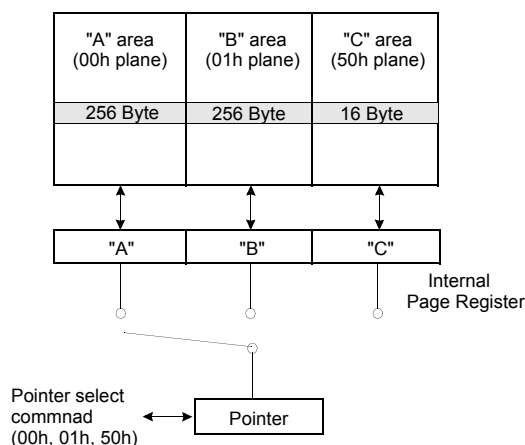
- \* Step1  
When an error happens in the nth page of the Block 'A' during erase or program operation.
- \* Step2  
Copy the nth page data of the Block 'A' in the buffer memory to the nth page of another free block. (Block 'B')
- \* Step3  
Then, copy the data in the 1st ~ (n-1)th page to the same location of the Block 'B'.
- \* Step4  
Do not further erase Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

### Pointer Operation of K9F2808U0C

Samsung NAND Flash has three address pointer commands as a substitute for the two most significant column addresses. '00h' command sets the pointer to 'A' area(0~255byte), '01h' command sets the pointer to 'B' area(256~511byte), and '50h' command sets the pointer to 'C' area(512~527byte). With these commands, the starting column address can be set to any of a whole page(0~527byte). '00h' or '50h' is sustained until another address pointer command is inputted. '01h' command, however, is effective only for one operation. After any operation of Read, Program, Erase, Reset, Power\_Up is executed once with '01h' command, the address pointer returns to 'A' area by itself. To program data starting from 'A' or 'C' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary. To program data starting from 'B' area, '01h' command must be inputted right before '80h' command is written.

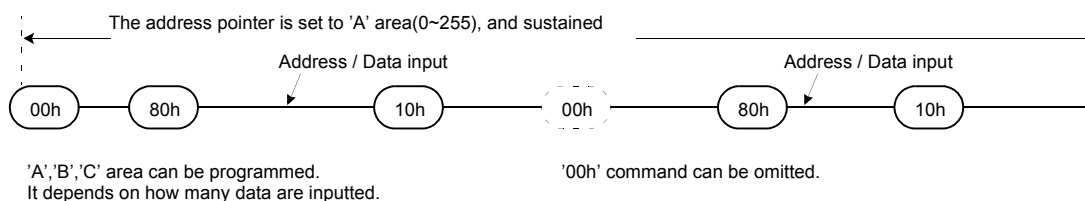
**Table 2. Destination of the pointer**

Command	Pointer position	Area
00h	0 ~ 255 byte	1st half array(A)
01h	256 ~ 511 byte	2nd half array(B)
50h	512 ~ 527 byte	spare array(C)

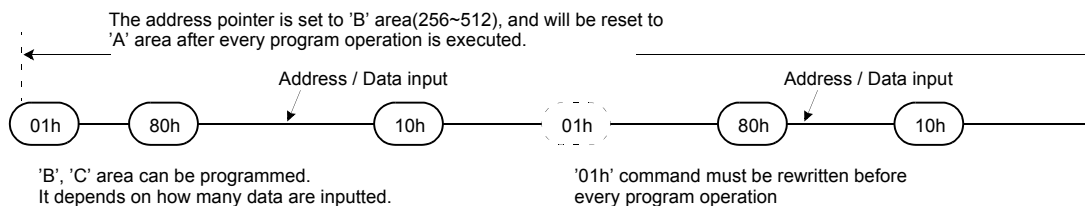


**Figure 4. Block Diagram of Pointer Operation**

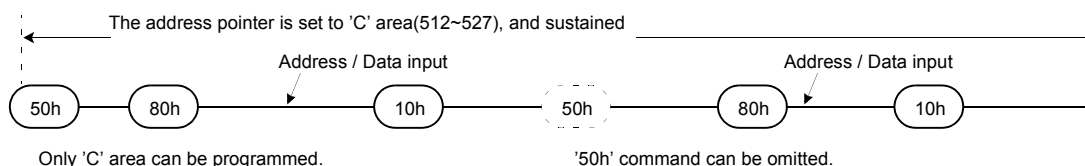
#### (1) Command input sequence for programming 'A' area



#### (2) Command input sequence for programming 'B' area



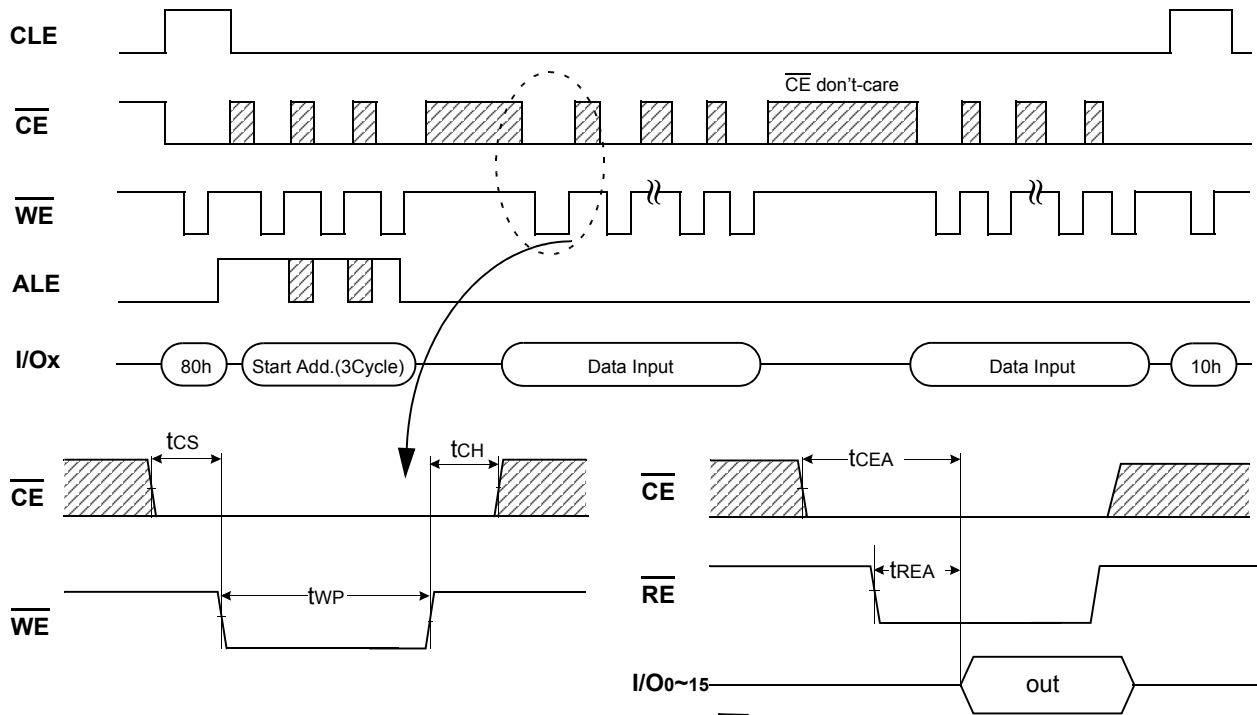
#### (3) Command input sequence for programming 'C' area



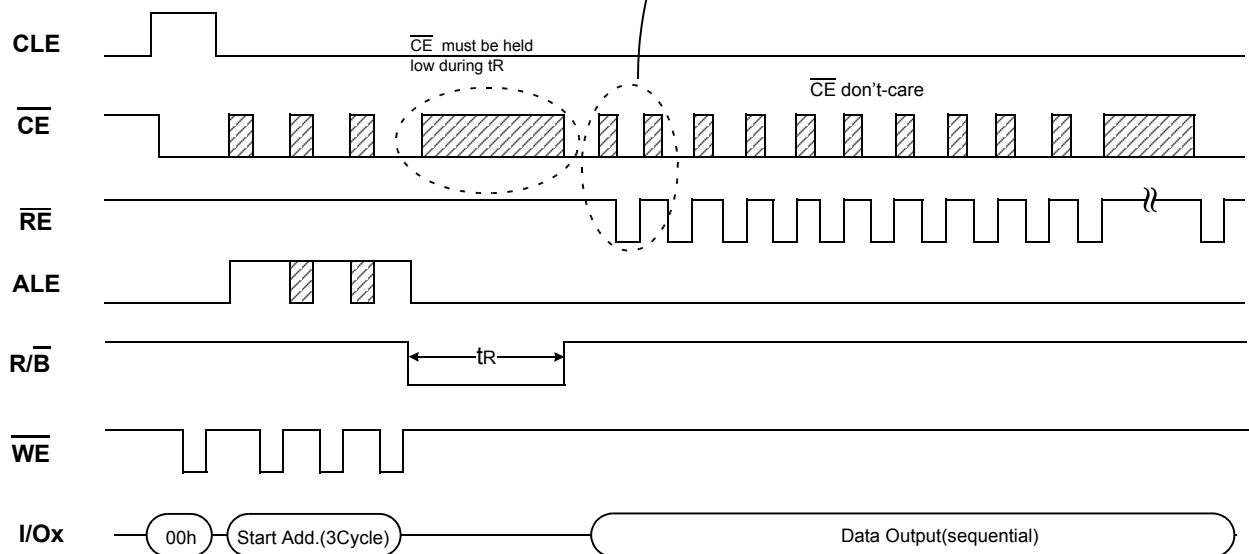
**System Interface Using  $\overline{CE}$  don't-care.**

For an easier system interface,  $\overline{CE}$  may be inactive during the data-loading or sequential data-reading as shown below. The internal 528byte page registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating  $\overline{CE}$  during the data-loading and reading would provide significant savings in power consumption.

**Figure 6. Program Operation with  $\overline{CE}$  don't-care.**



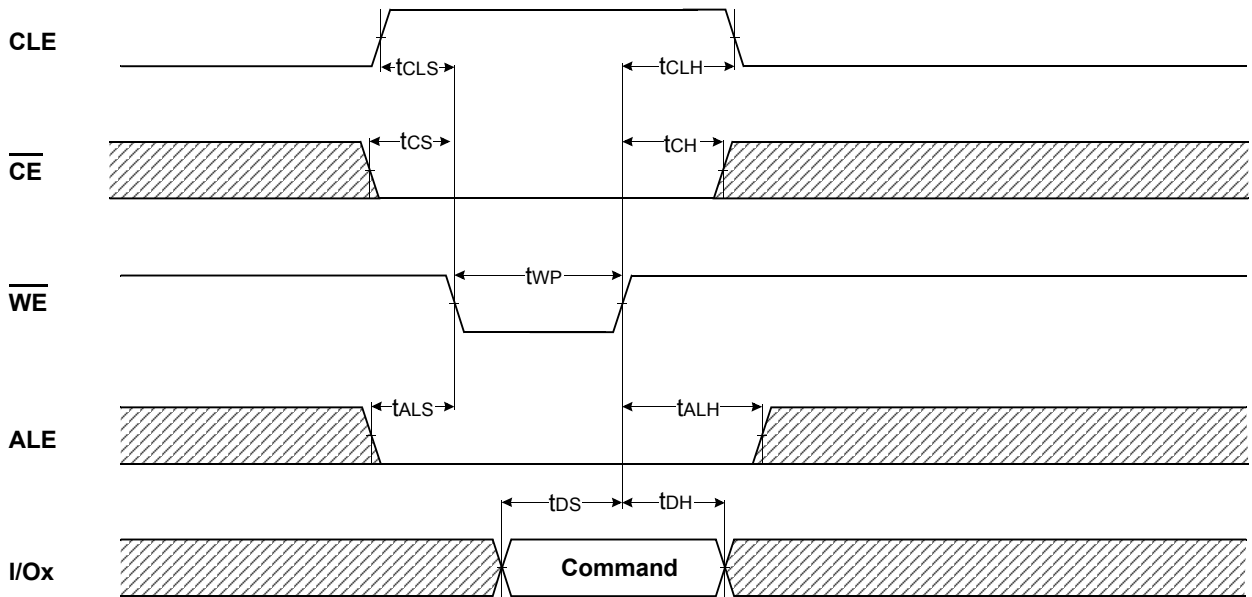
**Figure 7. Read Operation with  $\overline{CE}$  don't-care.**



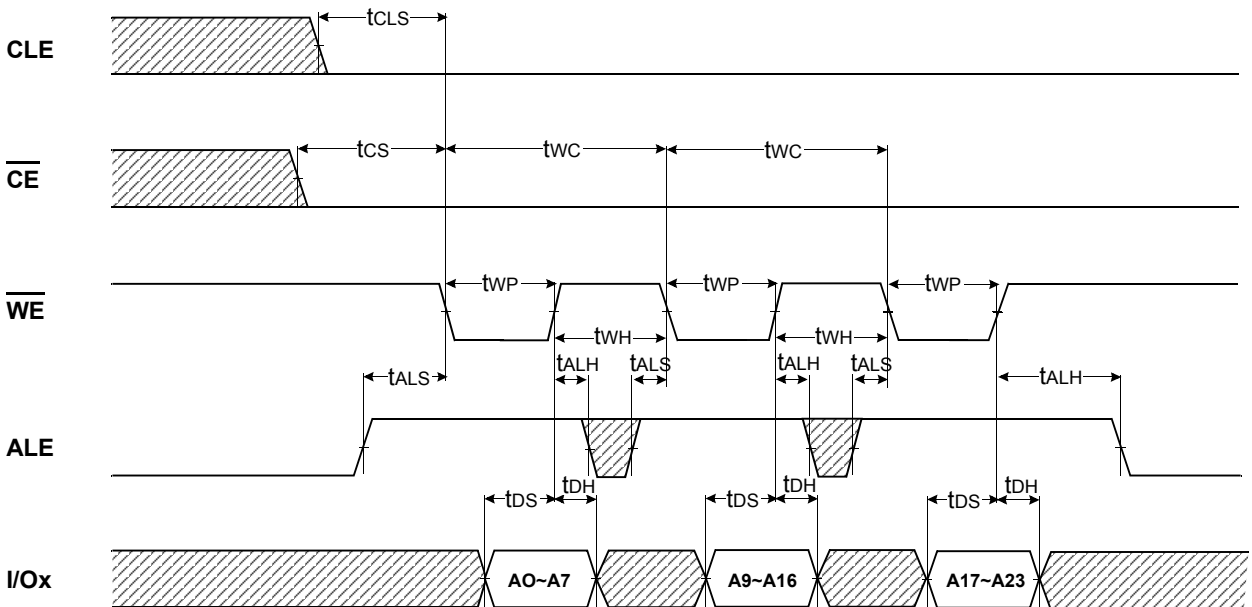


Device	I/O	DATA
	I/Ox	Data In/Out
K9F2808U0C	I/O 0 ~ I/O 7	~528byte

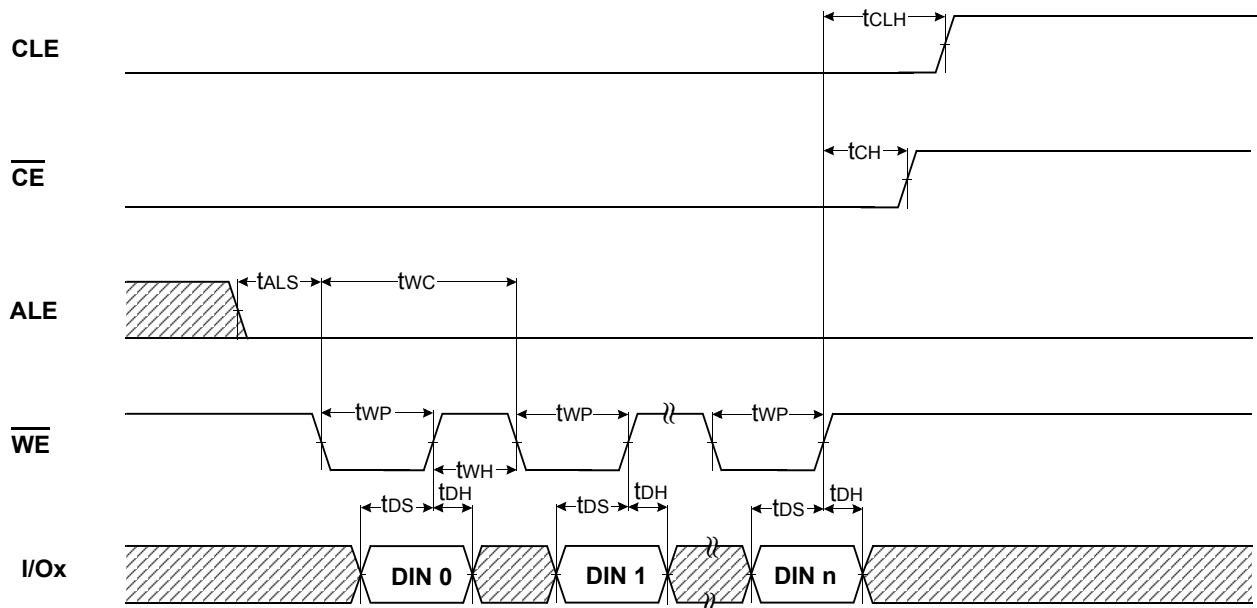
**Command Latch Cycle**



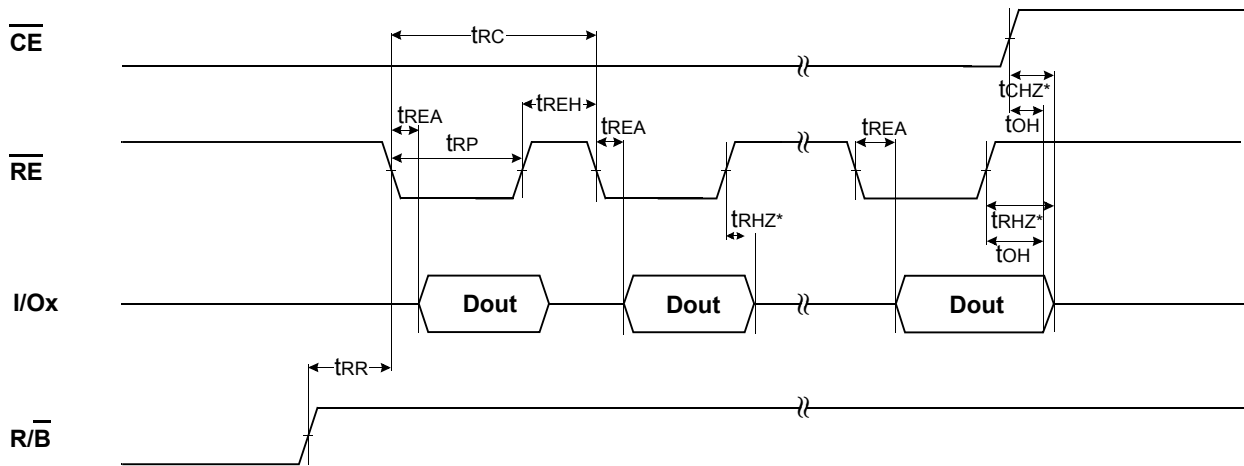
**Address Latch Cycle**



Input Data Latch Cycle

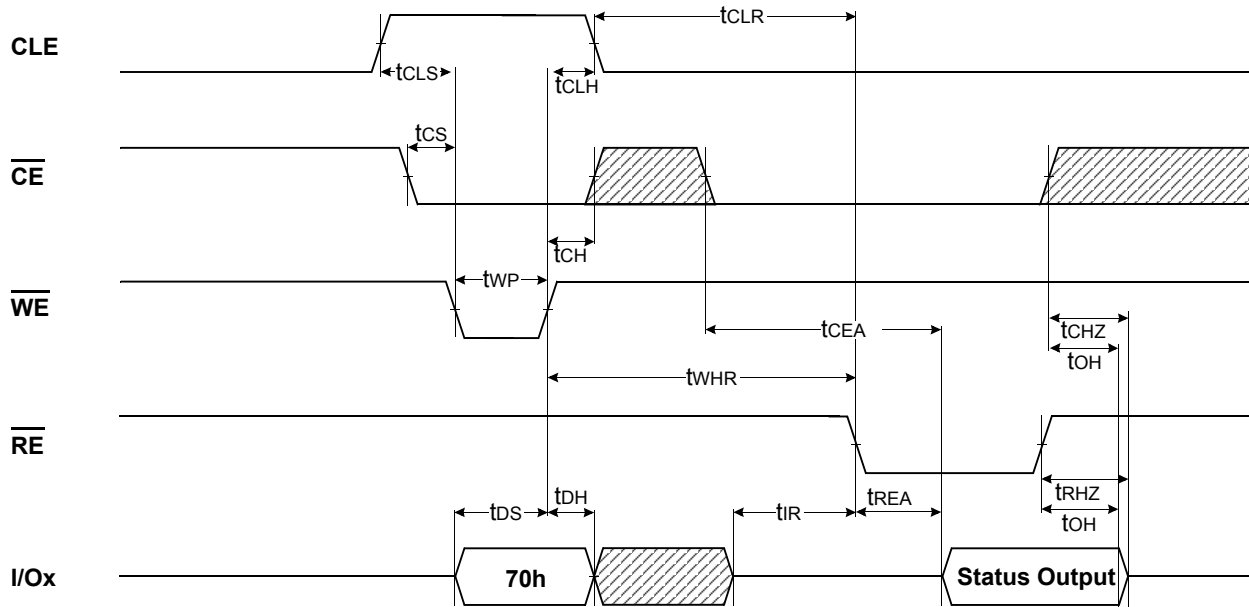


Serial access Cycle after Read (CLE=L, WE=H, ALE=L)

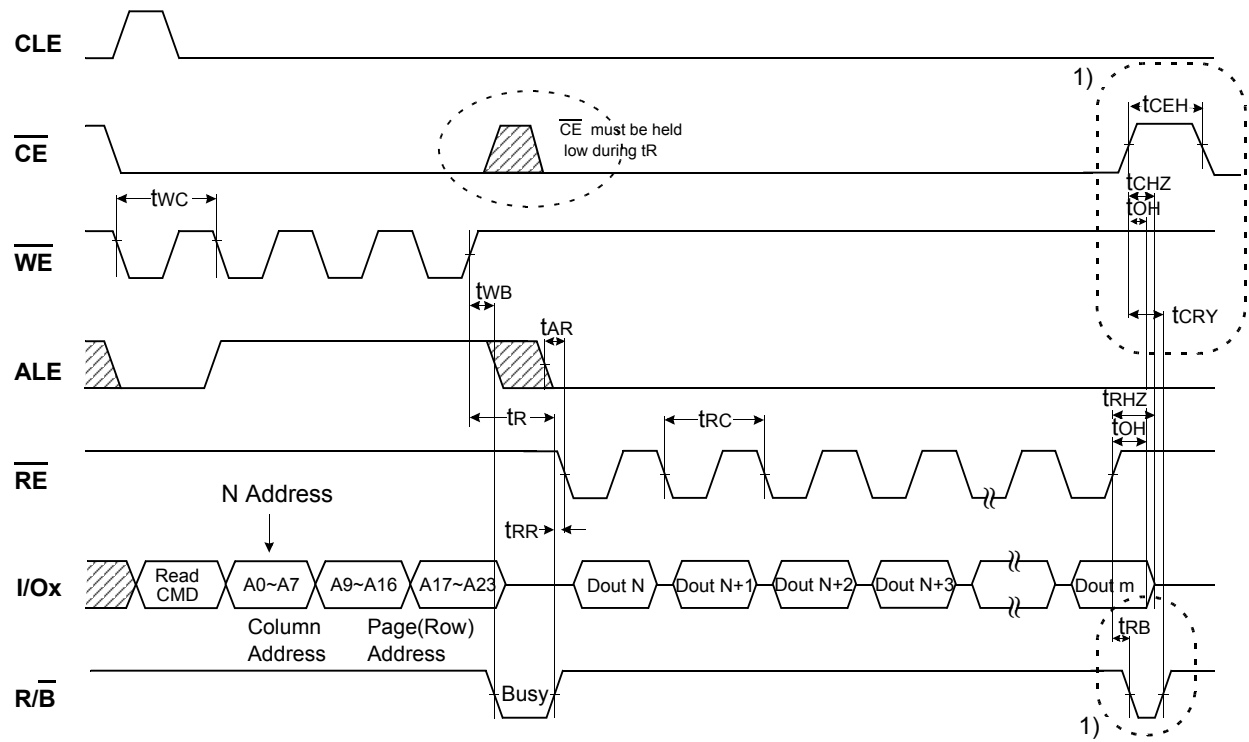


NOTES : Transition is measured  $\pm 200\text{mV}$  from steady state voltage with load.  
This parameter is sampled and not 100% tested.

Status Read Cycle

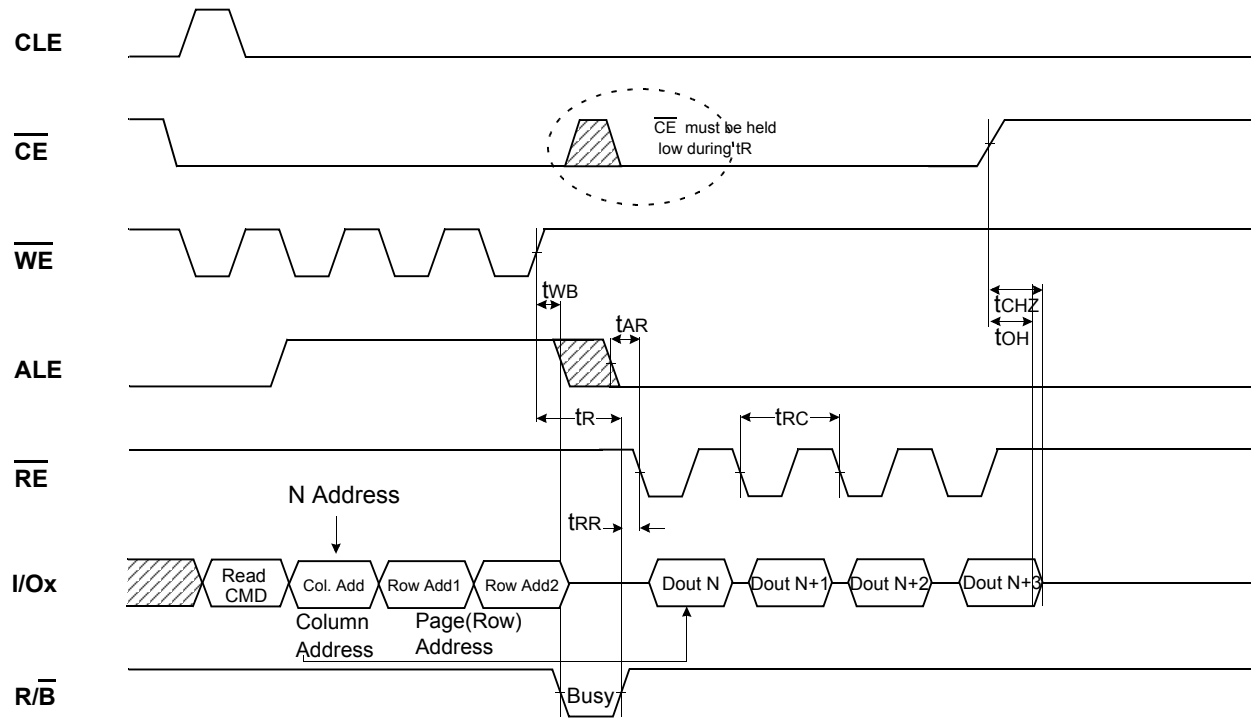


READ1 OPERATION(READ ONE PAGE)

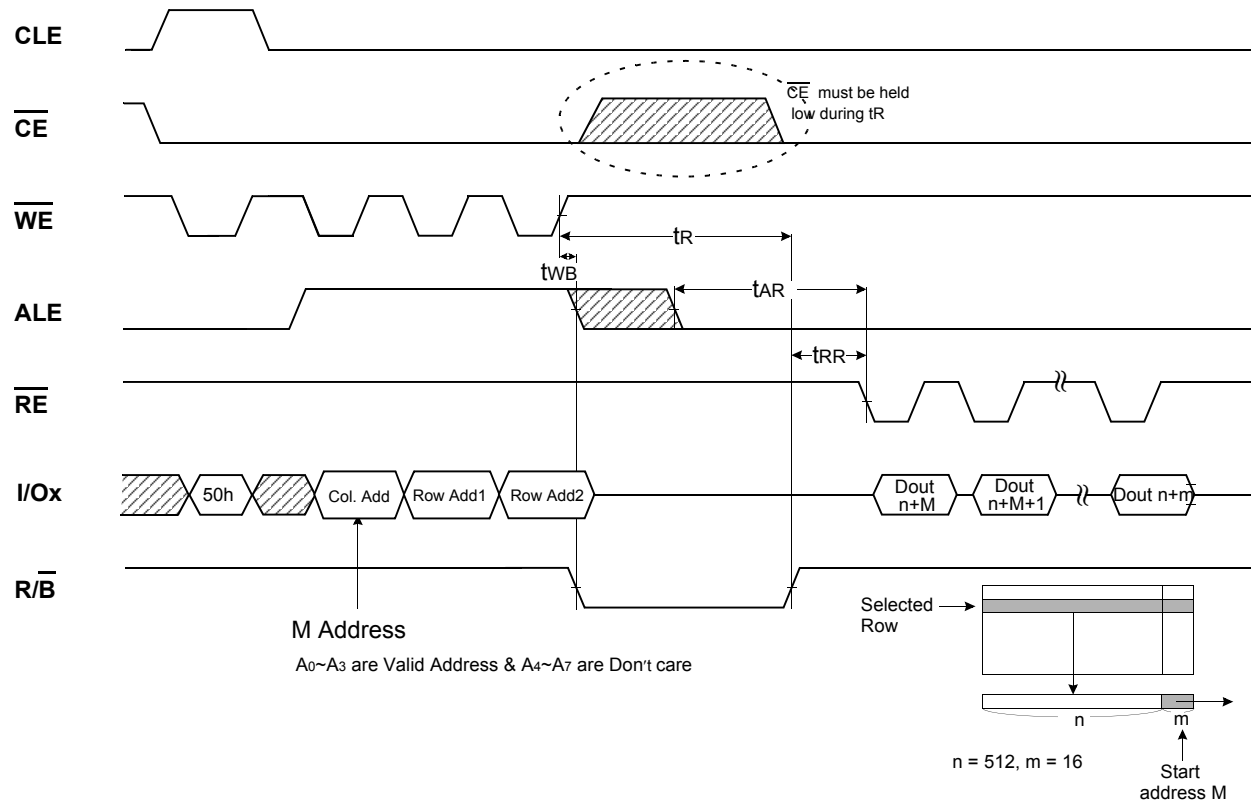


m = 528 , Read CMD = 00h or 01h

**READ1 OPERATION (INTERCEPTED BY  $\overline{CE}$ )**

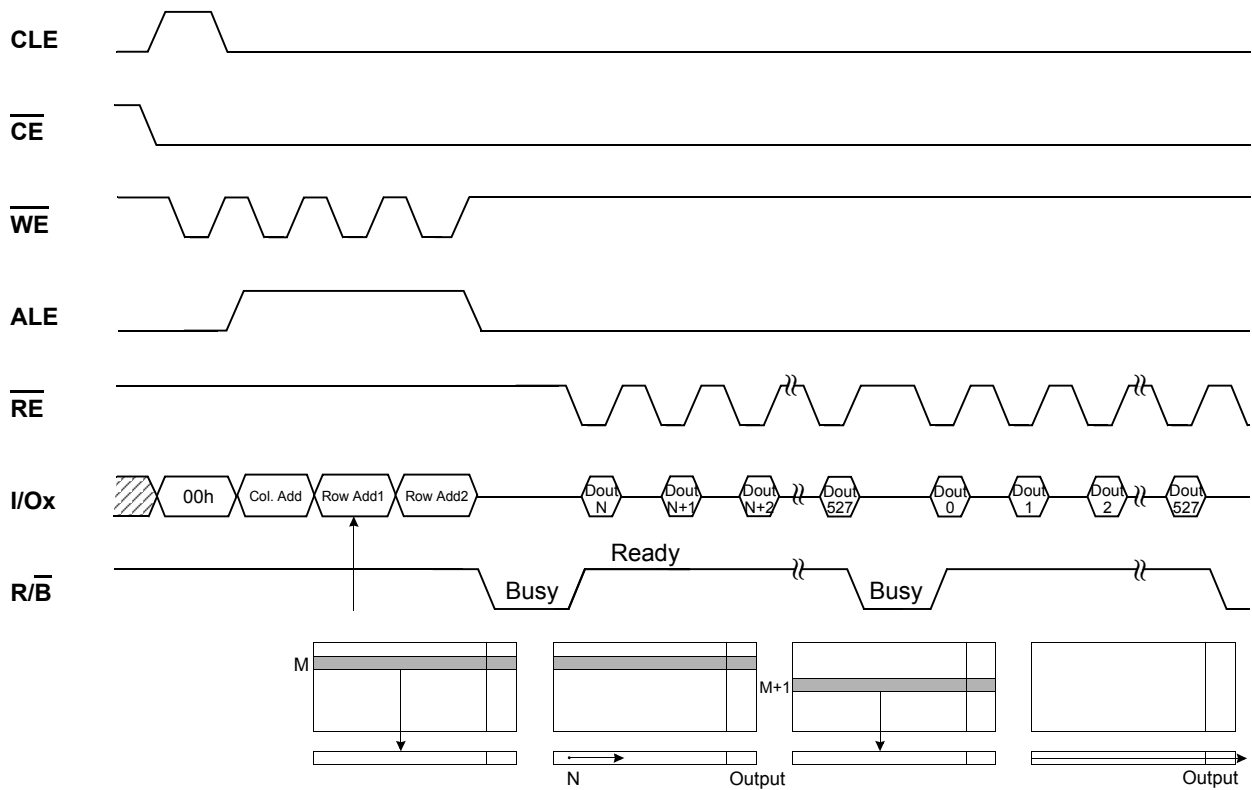


**READ2 OPERATION (READ ONE PAGE)**

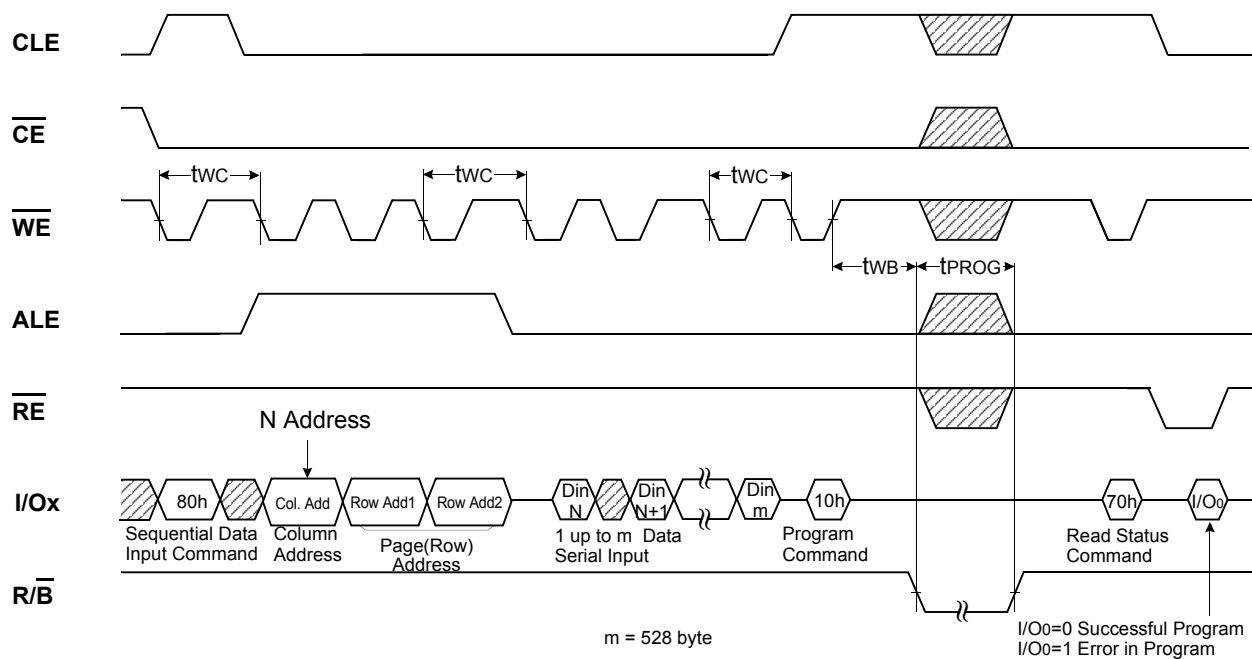


**SEQUENTIAL ROW READ OPERATION**

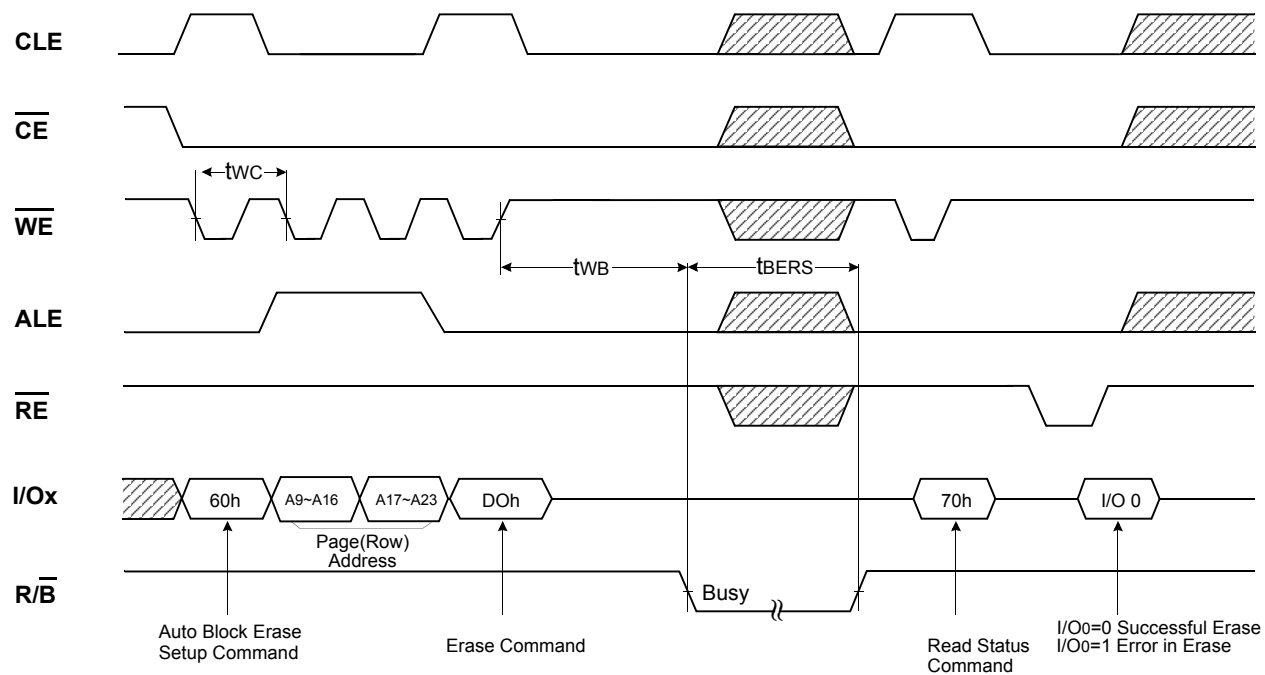
(only for K9F2808U0C-Y,P and K9F2808U0C-V,F valid within a block)



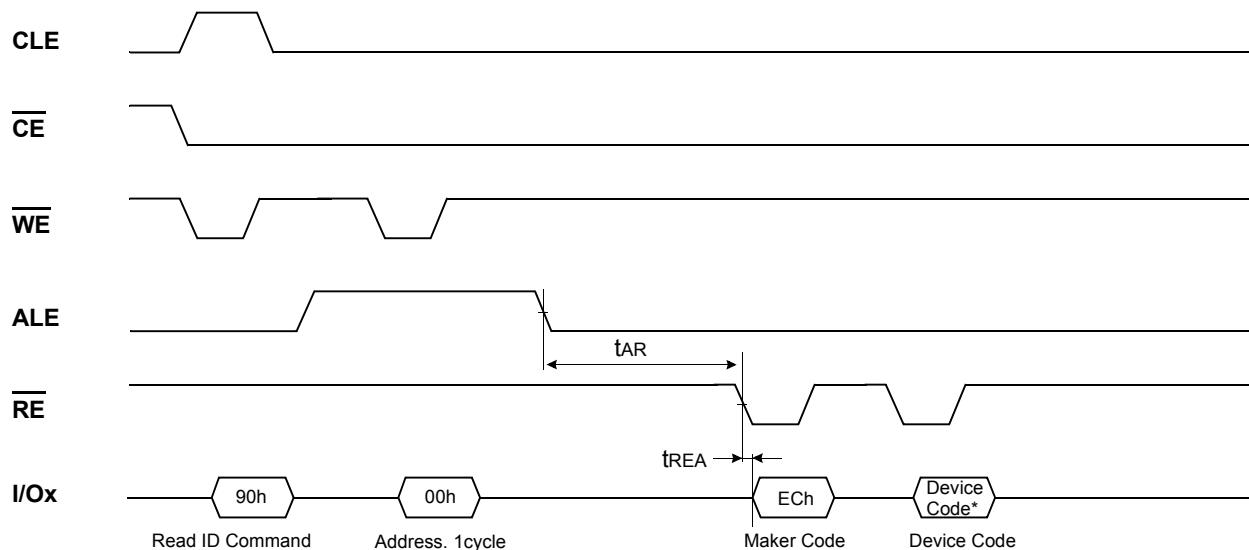
**PAGE PROGRAM OPERATION**



BLOCK ERASE OPERATION (ERASE ONE BLOCK)



MANUFACTURE & DEVICE ID READ OPERATION



Device	Device Code*
K9F2808U0C	73h

**DEVICE OPERATION**

**PAGE READ**

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Two types of operations are available : random read, serial page read.

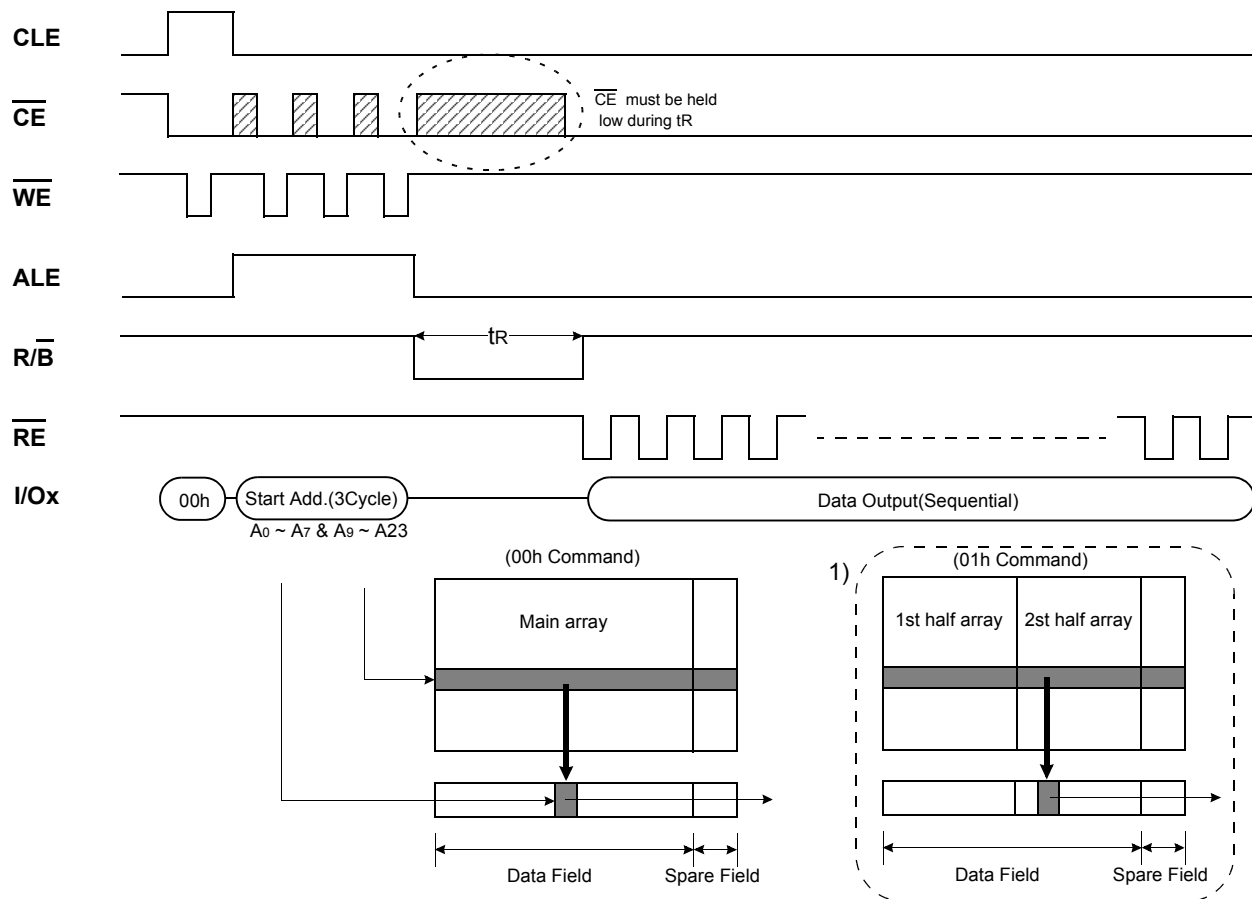
The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 10 $\mu$ s( $t_R$ ). The system controller can detect the completion of this data transfer( $t_R$ ) by analyzing the output of R/B pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing RE. High to low transitions of the RE clock output the data starting from the selected column address up to the last column address[column 511/ 527 depending on the state of GND input pin].

The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of 512 ~527 bytes may be selectively accessed by writing the Read2 command with GND input pin low. Addresses A0-A3 set the starting address of the spare area while addresses A4~A7 are ignored. The Read1 command is needed to move the pointer back to the main area. Figures 8, 9 show typical sequence and timings for each read operation.

**Sequential Row Read is available :**

After the data of last column address is clocked out, the next page is automatically selected for sequential row read. Waiting 10 $\mu$ s again allows reading the selected page. The sequential row read operation is terminated by bringing CE high. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Sequential Read 1 and 2 operation is allowed only within a block and after the last page of a block is readout, the sequential read operation must be terminated by bringing CE high. When the page address moves onto the next block, read command and address must be given. Figures 8-1, 9-1 show typical sequence and timings for sequential row read operation.

**Figure 8. Read1 Operation**



NOTE: 1) After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array (00h) at next cycle.



Figure 9. Read2 Operation

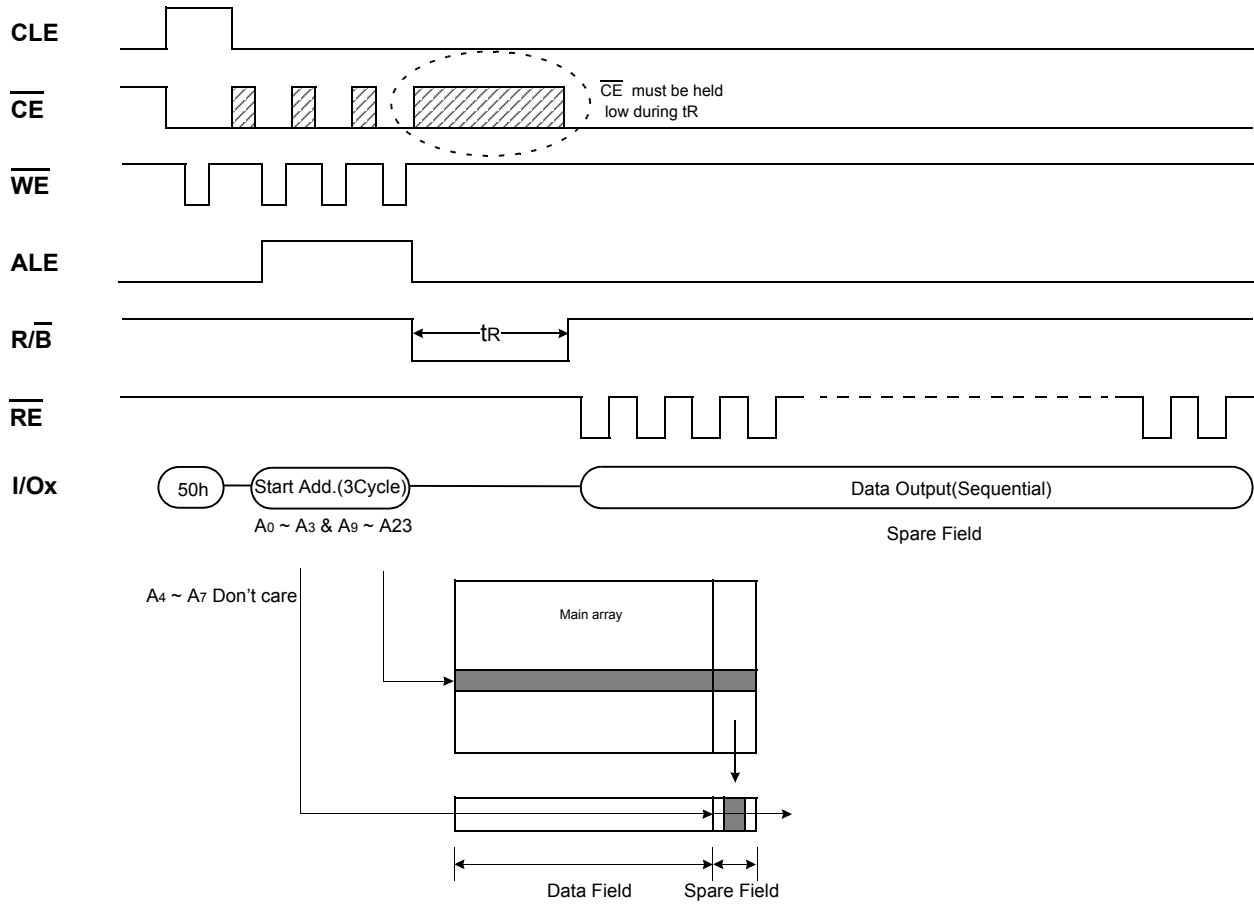


Figure 8-1. Sequential Row Read1 Operation

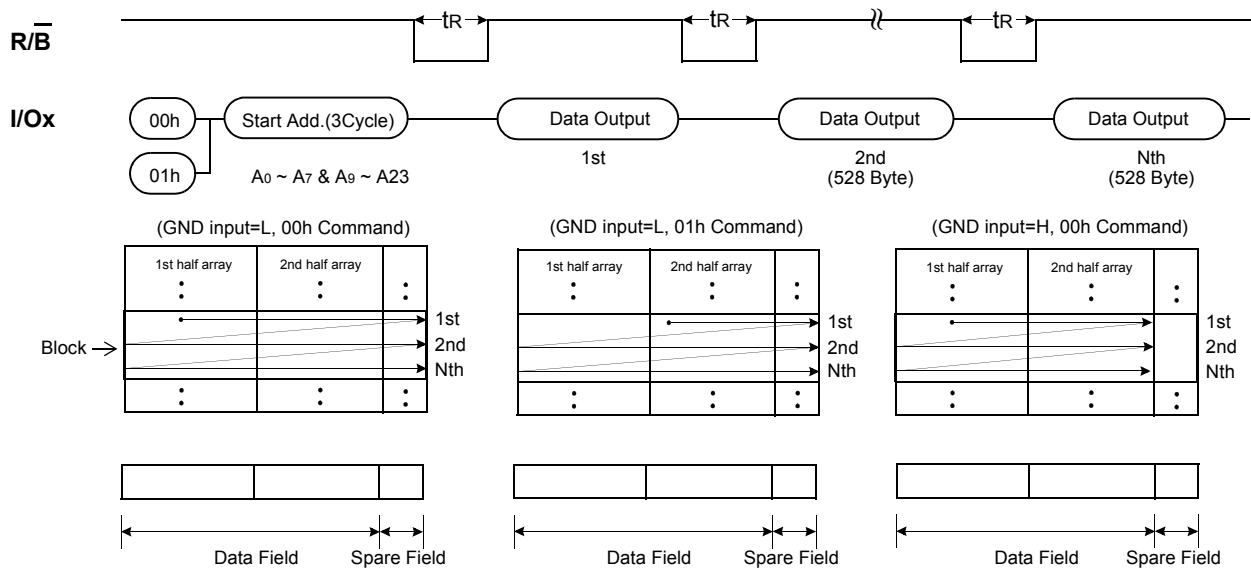
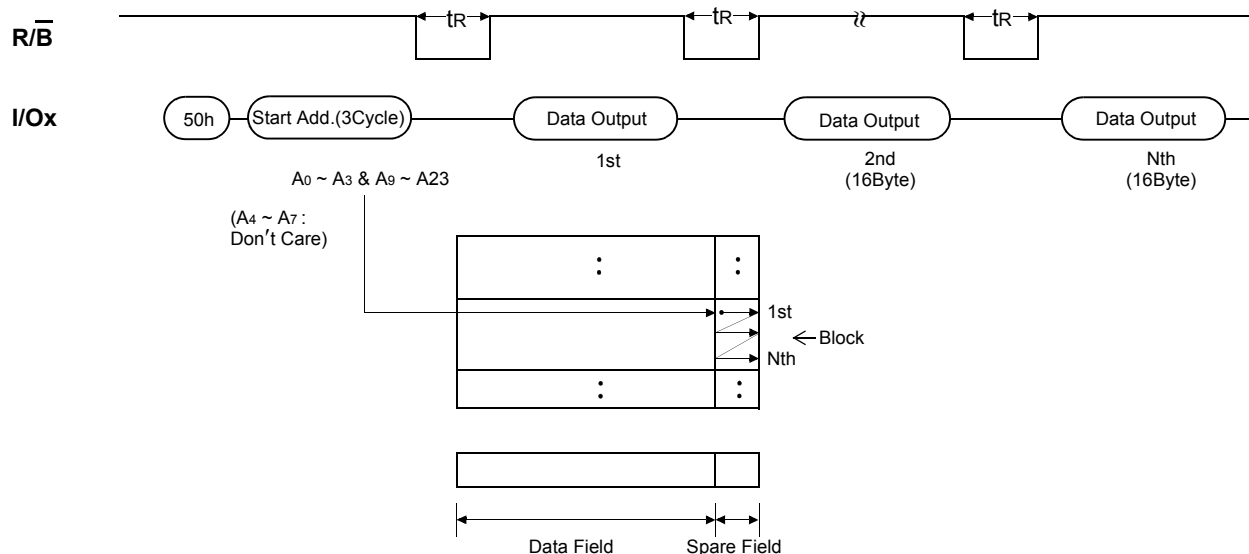


Figure 9-1. Sequential Row Read2 Operation (GND Input=Fixed Low)

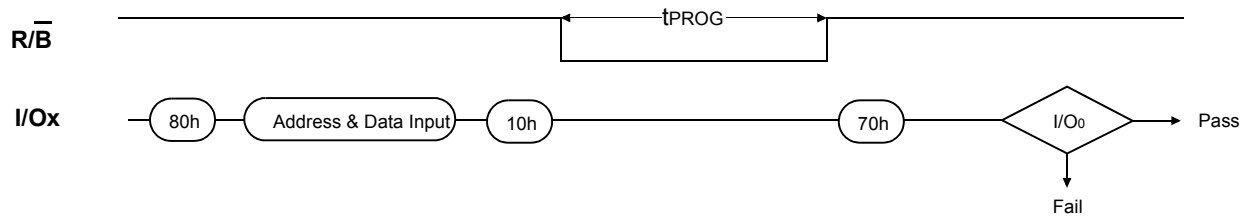


**PAGE PROGRAM**

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte/word or consecutive bytes/words up to 528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation should not exceed 2 for main array and 3 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. About the pointer operation, please refer to the attached technical notes.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the three cycle address input and then serial data loading. The words other than those to be programmed do not need to be loaded. The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with  $\overline{RE}$  and  $\overline{CE}$  low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the  $\overline{R/B}$  output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 10). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

**Figure 10. Program Operation**

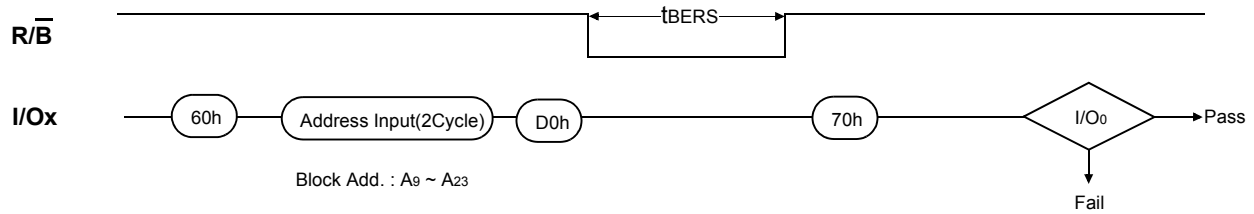


**BLOCK ERASE**

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address A<sub>14</sub> to A<sub>23</sub> is valid while A<sub>9</sub> to A<sub>13</sub> is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of  $\overline{WE}$  after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 11 details the sequence.

**Figure 11. Block Erase Operation**



**READ STATUS**

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of  $\overline{CE}$  or  $\overline{RE}$ , whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired.  $\overline{RE}$  or  $\overline{CE}$  does not need to be toggled for updated status. Refer to table 4 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

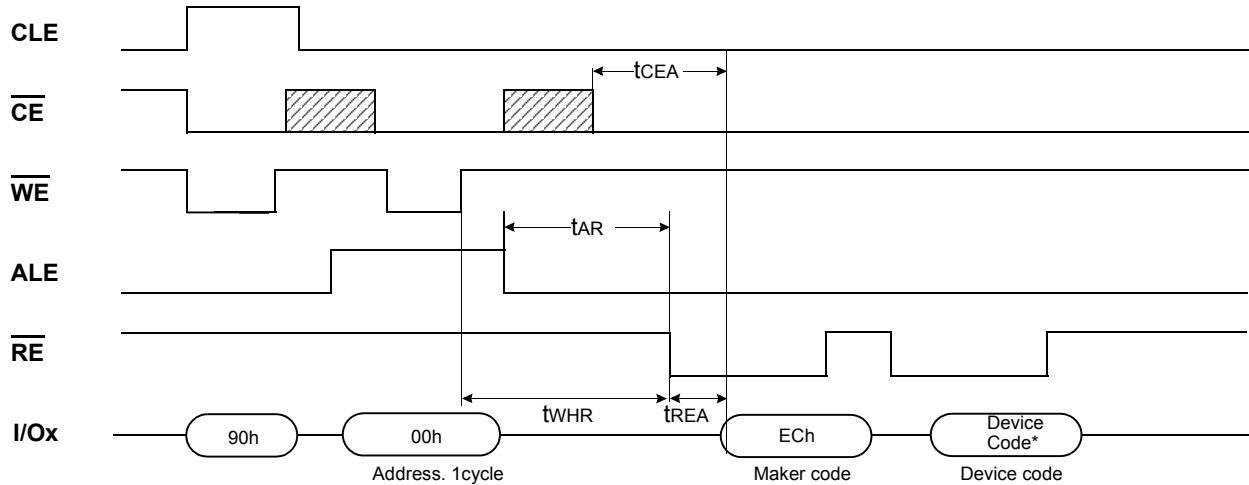
**Table4. Read Status Register Definition**

I/O #	Status	Definition
I/O 0	Program / Erase	"0" : Successful Program / Erase "1" : Error in Program / Erase
I/O 1	Reserved for Future Use	"0"
I/O 2		"0"
I/O 3		"0"
I/O 4		"0"
I/O 5		"0"
I/O 6	Device Operation	"0" : Busy      "1" : Ready
I/O 7	Write Protect	"0" : Protected      "1" : Not Protected

**READ ID**

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECh), and the device code respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 12 shows the operation sequence.

**Figure 12. Read ID Operation**

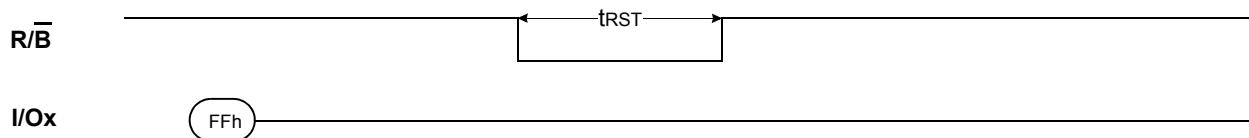


Device	Device Code*
K9F2808U0C	73h

**RESET**

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 5 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/B pin transitions to low for tRST after the Reset command is written. Refer to Figure 13 below.

**Figure 13. RESET Operation**

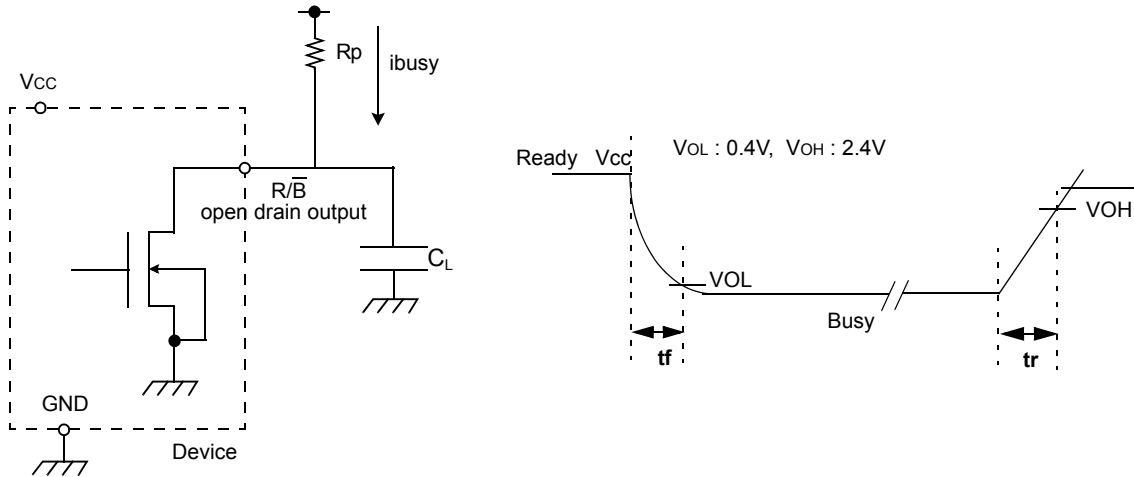


**Table5. Device Status**

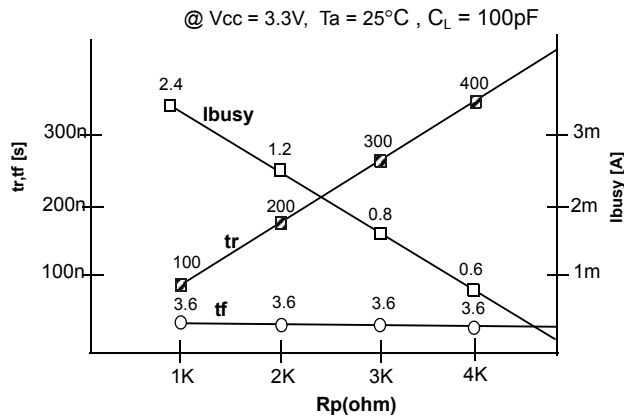
	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

**READY/ $\overline{\text{BUSY}}$**

The device has a  $\overline{\text{R/B}}$  output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The  $\overline{\text{R/B}}$  pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more  $\overline{\text{R/B}}$  outputs to be Or-tied. Because pull-up resistor value is related to  $t_r(\overline{\text{R/B}})$  and current drain during busy( $i_{\text{busy}}$ ), an appropriate value can be obtained with the following reference chart(Fig 14). Its value can be determined by the following guidance.



**Figure 14. Rp vs tr ,tf & Rp vs  $i_{\text{busy}}$**



**Rp value guidance**

$$R_{p(\text{min}, 3.3\text{V part})} = \frac{V_{cc(\text{Max.})} - V_{OL(\text{Max.})}}{I_{OL} + \sum I_L} = \frac{3.2\text{V}}{8\text{mA} + \sum I_L}$$

where  $I_L$  is the sum of the input currents of all devices tied to the  $\overline{\text{R/B}}$  pin.

$R_{p(\text{max})}$  is determined by maximum permissible limit of  $t_r$

**Data Protection & Power up sequence**

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V.  $\overline{WP}$  pin provides hardware protection and is recommended to be kept at V<sub>IL</sub> during power-up and power-down and recovery time of minimum 10 $\mu$ s is required before internal circuit gets ready for any command sequences as shown in Figure 15. The two step command sequence for program/erase provides additional software protection.

**Figure 15. AC Waveforms for Power Transition**

