

SPINDLE & VOICE COIL MOTOR ONE CHIP DRIVER

The KA3120 is an ASIC combination chip, which was designed for the HDD, includes the following functions: spindle motor drive, voice coil motor drive, retract and power management.

To drive and control the spindle, the digital ASIC provides the appropriate control signals (Start up, commutation, speed control) to the KA3120. The spindle motor condition is monitored by the FG output and the motor speed control is accomplished via the PWMSP input. The ASIC controls the voice coil motor current via PWMH and PWML inputs and the power management circuit always monitors the power supply voltages.



FEATURES

SPINDLE MOTOR DRIVE PART

- Soft switching
- Spindle brake after retract
- Adjustable brake delay time
- 2.0A max. current power driver
- Low output saturation voltage: 1V typical @1.6A
- PWM decoder & filter for soft switching
- The digital circuit (ASIC) based start-up, commutation and motor speed control

VOICE COIL MOTOR DRIVE PART

- Trimmed low offset current
- 1.2A max. current power driver
- Gain selection and adjustable gain
- Automatic power down retract function
- Class AB linear amplifier with no dead zone
- Low output saturation voltage: 0.8V typical @1.0A
- Internal full bridge with VPNP (Vertical PNP) & NPN
- VCM offset monitoring

ORDERING INFORMATION

Device	Package	Operating Temperature
KA3120	48-QFPH-1414	0 ~ 70°C

POWER MONITORING

- Power on reset with delay
- Hysteresis on both power comparators
- Over temperature & over current shut down
- 5V and 12V power monitor threshold accuracy $\pm 2\%$

PACKAGE

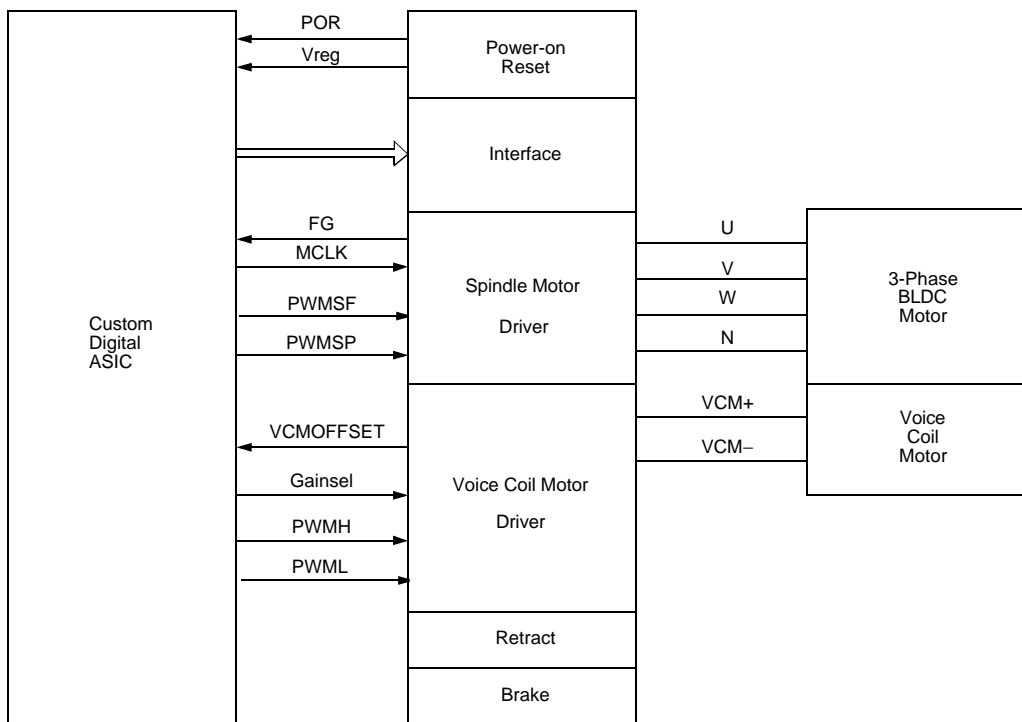
- 48QFPH (48 pin quad flat package heat-sink)

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APPLICATION

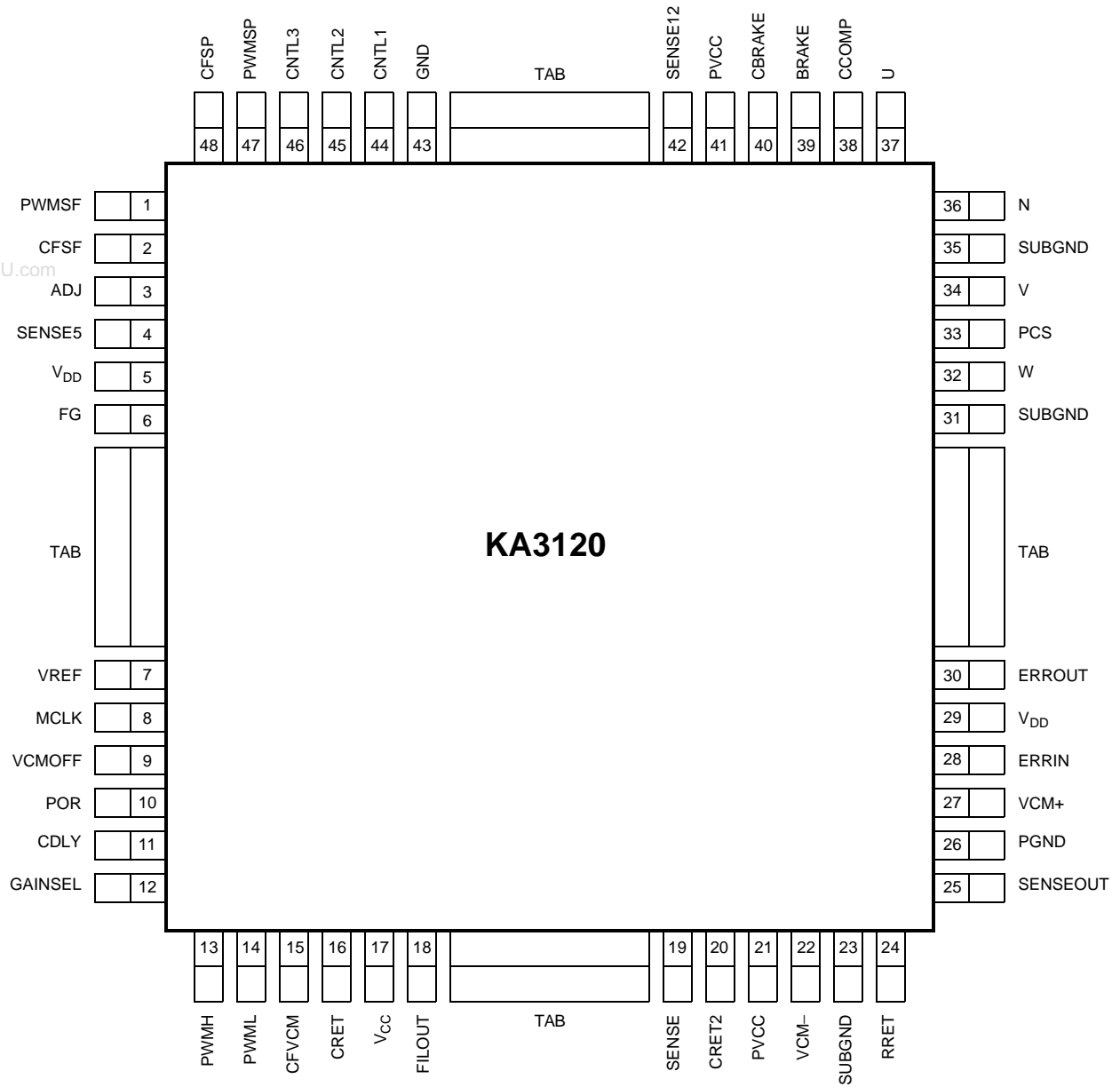
- Hard disk drive (HDD) products

BLOCK DIAGRAM



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PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	PWMSF	I	PWM input for spindle soft switching
2	CFSF	–	Capacitor for spindle PWM soft switching filter
3	ADJ	–	Reference voltage adjustable
4	SENSE5	I	Adjustable threshold voltage to 5V
5	VDD	–	5V power supply
6	FG	O	Frequency generation to spindle speed
7	VREF	O	Voltage reference output for ASIC power
8	MCLK	I	Clock from ASIC for switching
9	VCMOFF	O	VCM output offset monitoring pin
10	POR	O	Power On Reset
11	CDLY	–	Delay capacitor for power on reset
12	GAINSEL	I	VCM Amplifier gain selection
13	PWMH	I	PWM signal input (MSB)
14	PWML	I	PWM signal input (LSB)
15	CFVCM	–	Filter capacitor for VCM PWM control
16	CRET	–	Delay capacitor for retract
17	V _{CC}	–	12V power line
18	FILOUT	O	VCM PWM output
19	SENSE	I	VCM current sense input
20	CRET2	–	Power for VCM retract
21	PVCC	–	12V power line for VCM output
22	VCM(–)	–	VCM negative output
23	SUBGND	–	Ground
24	RRET	I	Adjustable maximum retract current
25	SENSEOUT	O	VCM current sense Amplifier output
26	PGND	–	Ground
27	VCM(+)	–	VCM positive output
28	ERRIN	I	VCM error Amplifier negative input
29	V _{DD}	–	5V power supply
30	ERROUT	O	VCM error Amplifier output
31	SUBGND	–	Ground
32	W	O	Spindle motor W phase output

PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Description
33	PCS	O	Spindle soutput current sensing
34	V	O	Spindle motor V phase output
35	SUBGND	–	Ground
36	N	I	Spindle motor neutral point
37	U	O	Spindle motor U phase output
38	CCOMP	–	Spindle output control compensation
39	BRAKE	O	Dynamic brake
40	CBRAKE	–	Back-EMF charging capacitor for brake power
41	PVCC	–	12V power line for spindle
42	SENSE12	I	Adjustable for threshold voltage to 12V
43	GND	–	Ground
44	CNTL1	I	Control input for spindle and brake
45	CNTL2	I	Control input for start-up clock and soft switching
46	CNTL3	I	Control input for VCM Amplifier & retract
47	PWMSP	I	PWM input for spindle speed control
48	CFSP	–	Filter capacitor for spindle PWM control

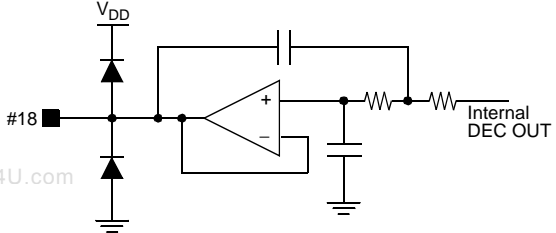
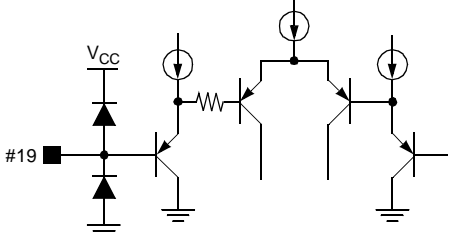
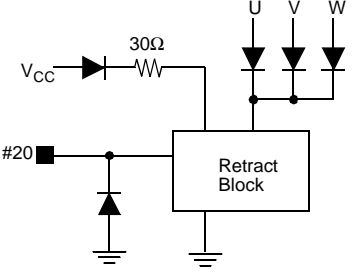
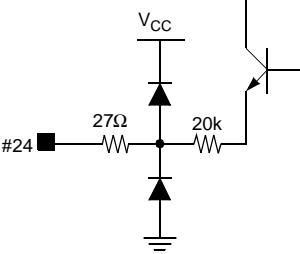
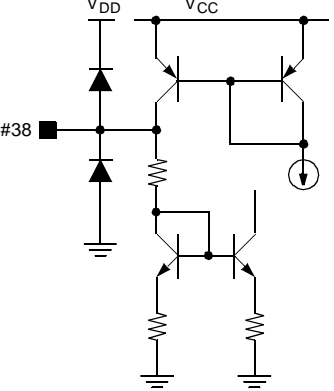
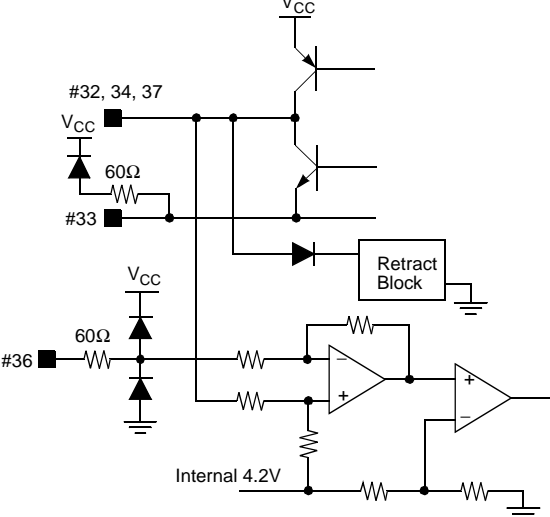
EQUIVALENT CIRCUITS

<p style="text-align: center;">PWM decoder filter input</p>	<p style="text-align: center;">PWM decoder filter Capacitor</p>
<p style="text-align: center;">Regulator part</p>	<p style="text-align: center;">SENSE input</p>
<p style="text-align: center;">FG output</p>	<p style="text-align: center;">MCLK input</p>

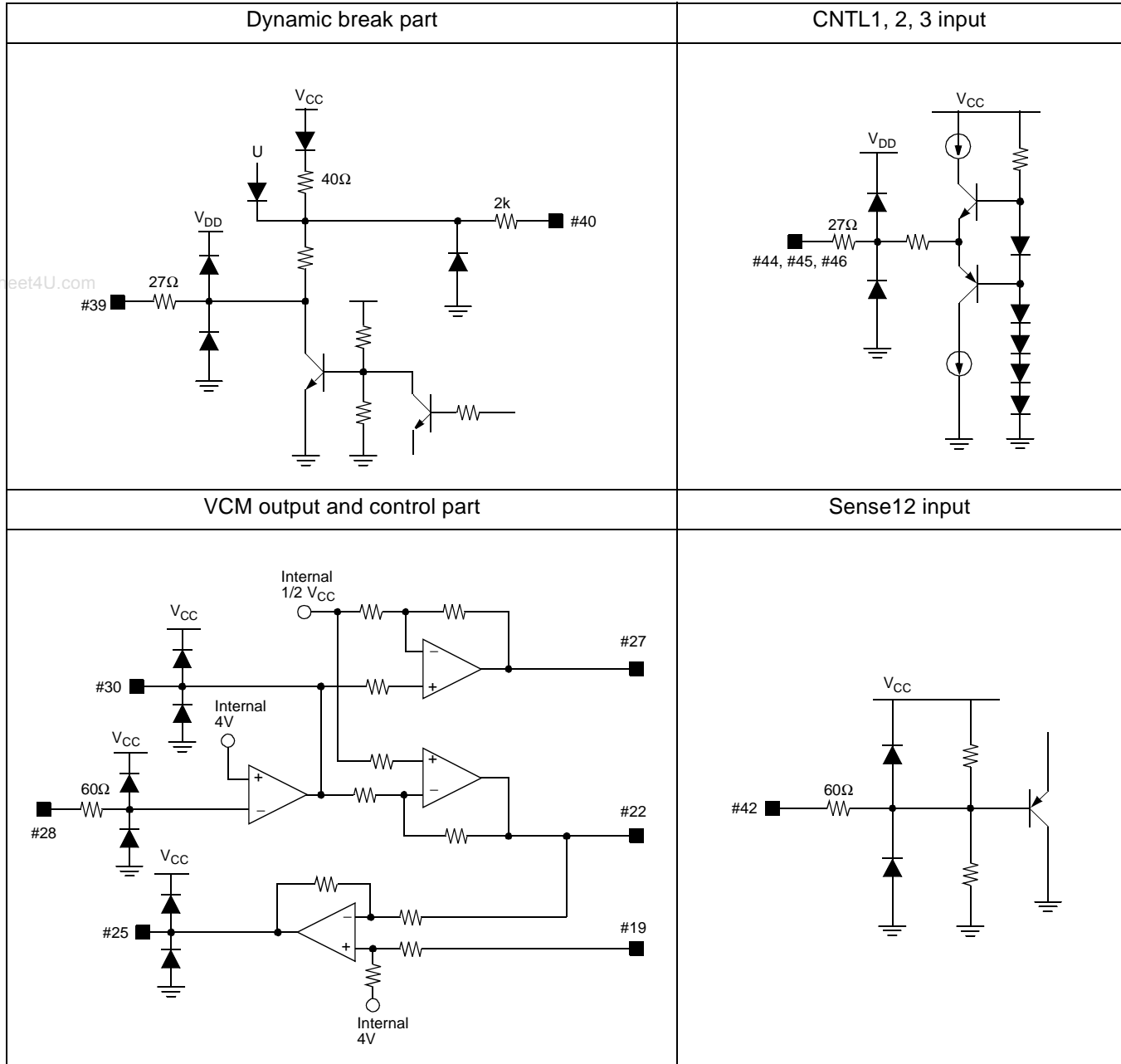
EQUIVALENT CIRCUITS (Continued)

<p>VCM offset compensation output</p>	<p>Power on reset part</p>
<p>VCM gain selection input</p>	<p>VCM PWM high input</p>
<p>VCM PWM low input</p>	<p>VCM PWM filter Capacitor</p>

EQUIVALENT CIRCUITS (Continued)

<p>Filtered VCM PWM command output</p> 	<p>VCM current sense input</p> 
<p>Capacitor for retract power</p> 	<p>Max. retract current set input</p> 
<p>Spindle motor output compensation Capacitor</p>	<p>Spindle motor output and Back EMP sensing part</p>
	

EQUIVALENT CIRCUITS (Continued)

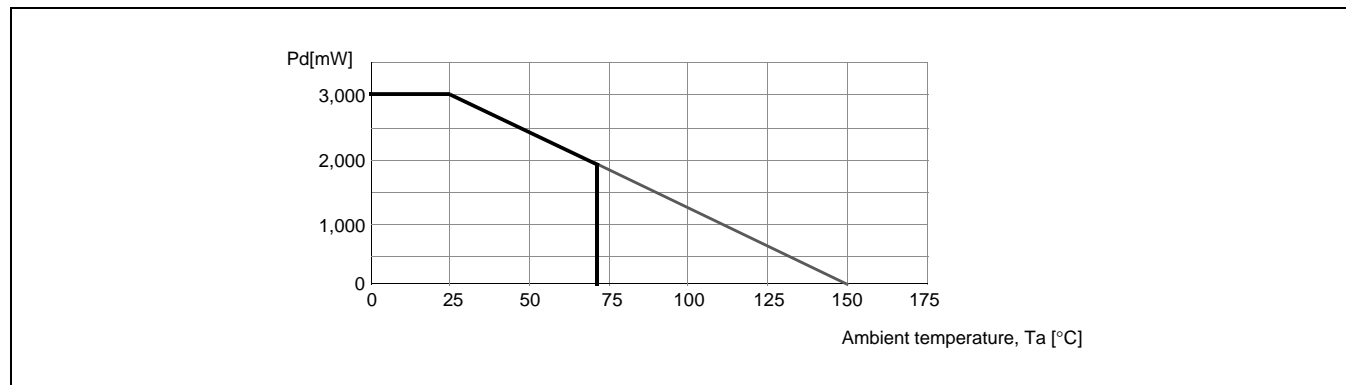


ABSOLUTE MAXIMUM RATING (Ta=25°C)

Characteristics	Symbol	Value	Unit
Maximum signal block supply voltage for 5V line	V_{DDMAX}	6	V
Maximum signal block supply voltage for 12V line	V_{CCMAX}	15	V
Maximum power block supply voltage for 12V line	PV_{CCMAX}	15	V
Maximum output current	I_{OMAX}	2	A
Power dissipation	P_D	3.0 ^{note}	W
Storage temperature	T_{STG}	-55 ~ 125	°C
Maximum junction temperature	T_{JMAX}	150	°C
Operating ambient temperature	T_A	0 ~ 70	°C

NOTE:

- When mounted on 50mm × 50mm × 1mm PCB (Phenolic resin material)
- Power dissipation is reduced 16mW / °C for using above Ta=25°C.
- Do not exceed Pd and SOA.



RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}, PV_{CC2}	10.8	12.0	13.2	V
Supply voltage in logic part	V_{DD}	4.5	5.0	5.5	V

ELECTRICAL CHARACTERISTICS

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
SUPPLY CURRENT						
5V line supply current 1	I _{DD1}	CNTL1=0V	40	50	60	mA
5V line supply current 2	I _{DD2}	–	15	20	25	mA
5V line supply current 3	I _{DD3}	CNTL1=CNTL3=5V	15	20	25	mA
5V line supply current 4	I _{DD4}	CNTL3=0V	15	20	25	mA
12V line supply current 1	I _{CC1}	CNTL1=0V	4	7	15	mA
12V line supply current 2	I _{CC2}	–	4	7	15	mA
12V line supply current 3	I _{CC3}	CNTL1=CNTL3=5V	10	30	50	mA
12V line supply current 4	I _{CC4}	CNTL3=0V	4	7	15	mA
POWER MONITOR						
Threshold voltage1 level for 12V	V _{TH12}	V _{CC} =Sweep, V _{DD} =5V	9.1	9.4	9.8	V
Threshold voltage2 level for 12V	V _{TH12b}	V _{CC} =Sweep, V _{DD} =5V	8.9	9.2	9.6	V
Hysteresis on 12V comparator	V _{HYS12}	V _{CC} =Sweep, V _{DD} =5V	100	200	300	mV
Adjustable pin voltage for 12V	V12	V _{CC} =12V, V _{DD} =5V	3.0	3.2	3.4	V
Threshold voltage level1 for 5V	V _{TH5}	V _{CC} =12V, V _{DD} =Sweep	3.9	4.1	4.4	V
Threshold voltage level2 for 5V	V _{TH5b}	V _{CC} =12V, V _{DD} =Sweep	3.8	4.0	4.3	V
Hysteresis on 5V comparator	V _{HYS5}	V _{CC} =12V, V _{DD} =Sweep	50	100	150	mV
Adjustable pin voltage for 5V	V5	V _{CC} =12V, V _{DD} =5V	2.85	3.0	3.25	V
POWER ON RESET GENERATOR						
Charging current for POR Capacitor	I _{CPOR}	V _{CC} =12V, V _{DD} =5V	-17.0	-14.0	-10.0	μA
POR threshold voltage	V _{THPOR}	CDLY=Sweep	2.3	2.5	2.7	V
Output high voltage	V _{POH}	V _{CC} =12V, V _{DD} =5V	4.5	–	V _{DD}	V
Output low voltage	V _{POL}	V _{CC} =12V, V _{DD} =5V	0	–	0.5	V
Power on reset delay	T _{dPOR}	C _{DLY} =220nF	–	40	–	ms
CONTROL INPUT						
Logic control input 1 MED voltage	V _{CTL10}	CNTL1=2.5V	2.3	2.5	2.7	V
Logic control input 1 MED current	I _{CTL1}	CNTL1=2.5V	-5	0	5	μA
Logic control input 1 HIGH voltage	V _{CTL1H}	CNTL1=Sweep	3.8	4.2	4.6	V
Logic control input 1 HIGH current	I _{CTL1H}	CNTL=5V	60	80	100	μA
Logic control input 1 LOW voltage	V _{CTL1L}	CNTL1=Sweep	0.5	0.8	1.2	V
Logic control input 1 LOW current	I _{CTL1L}	CNTL1=0V	-100	-80	-60	μA
LOGIC CONTROL INPUT2 & 3 SPEC'S ARE EQUAL TO LOGIC CONTROL INPUT1						

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
START-UP HOLD CHECK						
Start-up hold check1	SHM1	–	0	0.2	0.5	V
Start-up hold check2	SHM2	–	0	0.2	0.5	V
START-UP MODE CHECK						
Start-up mode check1	STM1	–	0	0.2	0.5	V
Start-up mode check2	STM2	–	0	0.2	0.5	V
RUNNING MODE CHECK						
BEMF threshold voltage	V _{BTH}	–	65	80	95	mV
FG output high voltage	V _{FGH}	–	4.5	4.8	5.0	V
FG output low voltage	V _{FGL}	–	0	0.2	0.5	V
Running mode check1	RM1	U=V=W=5V, N=100Hz	90	100	110	Hz
Running mode check2	RM2	U=V=W=5V, N=100Hz	90	100	110	Hz
SPINDLE FG GENERATION						
FG frequency	FG	U,V,W=120° shift pulse(1KHz)	2.9	3	3.1	KHz
FG duty	D _{TFG}	U,V,W=120° shift pulse(1KHz)	45	50	55	%
SPINDLE PWM CONTROL						
PWM high level input voltage	V _{SPMH}	–	3.0	–	–	V
PWM low level input voltage	V _{SPML}	–	–	–	2.0	V
High input current at PWMSP	I _{PSP1}	PWMSP=100% duty	85	105	125	μA
CFSP voltage2(100% duty of PWMSP)	V _{SP2}	PWMSP=100% duty	1.4	1.7	1.9	V
Low input current at PWMSP	I _{PSP2}	PWMSP=0% duty	–125	–105	–85	μA
CFSP voltage1(0% duty of PWMSP)	V _{SP1}	PWMSP=0% duty	3.1	3.3	3.5	V
CFSP voltage amplitude	V _{SPD}	–	1.5	1.6	1.8	V
CFSP voltage3 (50% of PWMSP)	V _{SP3}	PWMSP=50% duty	2.4	2.5	2.6	V
CFSP charging current	I _{CFSP1}	PWMSP=0%, CFSP=2.5V	–180	–150	–130	μA
CFSP discharge current	I _{CFSP2}	SPMSP=100%, CFSP=2.5V	130	150	180	μA

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
SPINDLE PWM SOFT SWITCHING						
PWM high level input voltage	V _{SFMH}	–	3.0	–	–	V
PWM low level input voltage	V _{SFML}	–	–	–	2.0	V
High input current at PWMSF	I _{PPF1}	PWMSF=100% duty	85	100	125	μA
CFSF voltage2(100% duty of PWMSF)	V _{SF2}	PWMSF=100% duty	2.65	2.75	2.85	V
Low input current at PWMSF	I _{PSF2}	PWMSF=0% duty	–125	–100	–85	μA
CFSF voltage1(0% duty of PWMSF)	V _{SF1}	PWMSF=0% duty	2.15	2.25	2.35	V
CFSF voltage amplitude	V _{SFD}	–	450	500	550	mV
CFSF voltage3 (50% of PWMSF)	V _{SF3}	PWMSF=50% duty	2.4	2.5	2.6	V
CFSF charging current	I _{CFSF1}	PWMSF=0%, CFSP=2.5V	–110	–90	–70	μA
CFSF discharge current	I _{CFSF2}	SPMSF=100%, CFSP=2.5V	90	110	130	μA
BRAKE						
CBrake output voltage	V _{BC}	–	11.0	11.3	11.5	V
Brake output high voltage	V _{BH}	(Test only)	–	V _{DD}	–	V
Brake output low voltage	V _{BL}	–	0	0.2	0.5	V
SPINDLE OUTPUT						
U saturation voltage_upper5	V _{SU5U}	R _U ,R _V ,R _W =5Ω	0.2	0.3	0.5	V
V saturation voltage_upper5	V _{SU5V}	R _U ,R _V ,R _W =5Ω	0.2	0.3	0.5	V
W saturation voltage_upper5	V _{SU5W}	R _U ,R _V ,R _W =5Ω	0.2	0.3	0.5	V
U saturation voltage_lower5	V _{SV5L}	R _U ,R _V ,R _W =5Ω	0.2	0.3	0.5	V
V saturation voltage_lower5	V _{SU5L}	R _U ,R _V ,R _W =5Ω	0.2	0.3	0.5	V
W saturation voltage_lower5	V _{SU5L}	R _U ,R _V ,R _W =5Ω	0.2	0.3	0.5	V
U output frequency	F _U	CNTL2=12KHz	0.9	1	1.1	KHz
V output frequency	F _V	CNTL2=12KHz	0.9	1	1.1	KHz
W output frequency	F _W	CNTL2=12KHz	0.9	1	1.1	KHz

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
SPINDLE OUTPUT						
U phase high duration time	T _{UH}	CNTL2=12KHz	300	333	360	μs
U phase middle duration time	T _{UM}	CNTL2=12KHz	600	666	720	μs
V phase high duration time	T _{VH}	CNTL2=12KHz	300	333	360	μs
V phase middle duration time	T _{VM}	CNTL2=12KHz	600	666	720	μs
W phase high duration time	T _{WH}	CNTL2=12KHz	300	333	360	μs
W phase middle duration time	T _{WM}	CNTL2=12KHz	600	666	720	μs
Leakage current U upper	I _{ULQU}	–	–1	0	1	μA
Leakage current V upper	I _{VLQU}	–	–1	0	1	μA
Leakage current W upper	I _{WLQU}	–	–1	0	1	μA
Leakage current U lower	I _{ULQL}	–	–1	0	1	μA
Leakage current V lower	I _{VLQL}	–	–1	0	1	μA
Leakage current W lower	I _{WLQL}	–	–1	0	1	μA
U sourcing current 0.2V	I _{OU02}	–	3.0	4.0	5.0	μA
V sourcing current 0.2V	I _{OV02}	–	3.0	4.0	5.0	μA
W sourcing current 0.2V	I _{OW02}	–	3.0	4.0	5.0	μA
Transconductance gain U upper	GM _{UH}	PWMSP=sweep, R _U ,R _V ,R _W =5Ω	0.8	0.9	1.0	A/V
Transconductance gain U lower	GM _{UL}	PWMSP=sweep, R _U ,R _V ,R _W =5Ω	0.8	0.9	1.0	A/V
Transconductance gain V upper	GM _{VH}	PWMSP=sweep, R _U ,R _V ,R _W =5Ω	0.8	0.9	1.0	A/V
Transconductance gain V lower	GM _{VL}	PWMSP=sweep, R _U ,R _V ,R _W =5Ω	0.8	0.9	1.0	A/V
Transconductance gain W upper	GM _{WH}	PWMSP=sweep, R _U ,R _V ,R _W =5Ω	0.8	0.9	1.0	A/V
Transconductance gain W lower	GM _{WL}	PWMSP=sweep, R _U ,R _V ,R _W =5Ω	0.8	0.9	1.0	A/V
CCOMP charging current1	I _{COMP1}	PWMSP=0%	–20	0	20	μA
CCOMP charging current2	I _{COMP2}	PWMSP=50%	–200	–250	–300	μA
CCOMP charging current3	I _{COMP3}	PWMSP=100%	–400	–500	–600	μA

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
COMUTATION CONTROL						
U stair high	V _{USTH}	–	2.85	3.0	3.15	V
U stair middle	V _{USTM}	–	2.35	2.5	2.65	V
U stair low	V _{USTL}	–	1.85	2.0	2.15	V
U stair frequency	F _{UST}	–	0.9	1.0	1.1	KHz
V stair high	V _{VSTH}	–	2.85	3.0	3.15	V
V stair middle	V _{VSTM}	–	2.35	2.5	2.65	V
V stair low	V _{VSTL}	–	1.85	2.0	2.15	V
V stair frequency	F _{VST}	–	0.9	1.0	1.1	KHz
W stair high	V _{WSTH}	–	2.85	3.0	3.15	V
W stair middle	V _{WSTM}	–	2.35	2.5	2.65	V
W stair low	V _{WSTL}	–	1.85	2.0	2.15	V
W stair frequency	F _{WST}	–	0.9	1.0	1.1	KHz
Com high	V _{COMH}	–	2.6	2.75	2.9	V
Com low	V _{COML}	–	2.1	2.25	2.4	V
Com frequency	F _{COM}	–	2.8	3.0	3.2	KHz
COMUTATION CONTROL SOFT						
U stair frequency_soft	F _{USTSF}	–	0.9	1.0	1.1	KHz
V stair frequency_soft	F _{VSTSF}	–	0.9	1.0	1.1	KHz
W stair frequency_soft	F _{WSTSF}	–	0.9	1.0	1.1	KHz
Com frequency_soft	F _{CSF}	–	2.9	3	3.1	KHz
Com high voltage_soft1	V _{CHSF1}	–	2.65	2.75	2.85	V
Com low voltage_soft1	V _{CLSF1}	–	2.15	2.25	2.35	V
Com high voltage_soft2	V _{CHSF1}	–	2.65	2.75	2.85	V
Com low voltage_soft2	V _{CLSF1}	–	2.15	2.25	2.35	V
REGULATOR						
Adjustable PIN voltage	V _{ADJ}	VDD=5V,R3a=15KΩ,R3b=10KΩ	1.2	1.3	1.4	V
Regulator output voltage	V _{REG}	VDD=5V,R3a=15KΩ,R3b=10KΩ	3.1	3.3	3.5	V
Regulator line regulation	R _{LINE}	VDD=sweep	0	0.5	1.0	%
Regulator load regulation	R _{LOAD}	VDD=5V	0	0.5	1.0	%

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
SPINDLE MCLOCK						
High threshold voltage	V _{MH}	–	2.0	1.4	–	V
Low threshold voltage	V _{ML}	–	–	1.4	0.8	V
High input current	I _{MH}	–	15	25	35	μA
High input current	I _{ML}	–	–10	0	10	μA
VCM PWM CONTROL						
High PWMH input current	I _{PWMH1}	PWMH=100%	100	113	130	μA
Low PWMH input current	I _{PWMH2}	PWMH=0%	–130	–113	–100	μA
High PWML input current	I _{PWML1}	PWML=100%	100	113	130	μA
Low PWML input current	I _{PWML2}	PWML=0%	–130	–113	–100	μA
PWMH high level input voltage	V _{PWMH1}	–	3.0	–	–	V
PWMH low level input voltage	V _{PWMH2}	–	–	–	2.0	V
PWML high level input voltage	V _{PWML1}	–	3.0	–	–	V
PWML low level input voltage	V _{PWML2}	–	–130	–113	–100	V
CFVCM voltage1	V _{CFVC1}	PWMH=100%,PWML=100%	5.90	6.06	6.30	V
CFVCM voltage2	V _{CFVC2}	PWMH=100%,PWML=50%	5.80	6.00	6.20	V
CFVCM voltage3	V _{CFVC3}	PWMH=100%,PWML=0%	5.70	5.94	6.10	V
CFVCM voltage4	V _{CFVC4}	PWMH=50%,PWML=100%	3.90	4.06	4.30	V
CFVCM voltage5	V _{CFVC5}	PWMH=50%,PWML=50%	3.80	4.00	4.20	V
CFVCM voltage6	V _{CFVC6}	PWMH=50%,PWML=0%	3.70	3.94	4.10	V
CFVCM voltage7	V _{CFVC7}	PWMH=0%,PWML=100%	1.90	2.06	2.40	V
CFVCM voltage8	V _{CFVC8}	PWMH=0%,PWML=50%	1.80	2.00	2.30	V
CFVCM voltage9	V _{CFVC9}	PWMH=0%,PWML=0%	1.70	1.94	2.20	V
PWM current ratio (VCM)	R _{PWM}	–	30	32	34	
PWMH current variation	I _{VPWM}	–	0.8	1.0	1.2	mA
PWML current variation	I _{VPWM}	–	27	32.3	36	μA
VCM PWM FILTER						
Maximum phase shift	ΔΦ	Measure at 500HZ, CFVCM=10nF	–	–	2	deg
Filter cut-off frequency	F _{CO}	–	–	100	–	μA
Filter attenuation at 1MHz	α _{FILTER}	–	–	70	–	dB

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
VCM REFERENCE VOLTAGE						
VCM reference voltage	V _{REF}	CNTL3=5V	3.8	4.0	4.2	V
VCM ERROR AMPLIFIER						
Amplifier output high	V _{EOH}	–	10.8	11.2	11.5	V
Amplifier output low	V _{EOL}	–	0.5	0.8	1.2	V
Short circuit current	I _{ESC}	–	10	–	–	mA
Input offset voltage	V _{OSE}	–	–15	0	15	mV
Error amplifier open loop gain	A _{VE}	–	–	80	–	dB
Unit gain bandwidth	BG _E	–	–	2.3	–	MHz
VCM SENSE AMPLIFIER						
Amplifier output high	V _{SOH}	–	10.8	11.2	11.5	V
Amplifier output low	V _{SOL}	–	0.5	0.8	1.2	V
Short circuit current	I _{SSC}	–	10	–	–	mA
Input offset voltage	V _{OSE}	–	–15	0	15	mV
Unit gain bandwidth	BG _S	–	–	3.4	–	MHz
Sense amplifier voltage gain1	A _{VS1}	Gain _{sel} =5V	–	24	–	dB
Sense amplifier voltage gain2	A _{VS2}	Gain _{sel} =5V	–	6	–	dB
VCM POWER AMPLIFIER						
Power Amplifier gain1	A _{PO1}	–	24	24.6	25	dB
Power Amplifier gain2	A _{PO2}	–	24	24.6	25	dB
Power Amplifier output high voltage1	V _{POH1}	–	11.5	11.8	12.0	V
Power Amplifier output high voltage2	V _{POH2}	–	11.5	11.8	12.0	V
Power Amplifier output low voltage1	V _{POL1}	–	0	0.2	0.5	V
Power Amplifier output low voltage2	V _{POL2}	–	0	0.2	0.5	V
Input offset voltage	V _{OSE}	–	–15	0	15	mV
Unit gain bandwidth1	BG _{P1}	–	–	2	–	MHz
Unit gain bandwidth2	BG _{P2}	–	–	2	–	MHz
VCM OFFSET COMPARATOR						
Offset comparator high voltage	V _{OCH}	–	4.5	4.8	5.0	V
Offset comparator low voltage	V _{OCL}	–	0	0.2	0.5	V
Offset comparator offset voltage	V _{OCOS}	–	–	0	–	mV
Offset comparator hysteresis	V _{OCHYS}	–	5	10	15	mV

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
VCM AMPLIFIER TOTAL						
VCM offset current	I _{OSVCM}	PWMH=PWML=50% duty	-15	0	15	mA
VCM transconductance gain high	GM _{VH}	Gain _{sel} =0V	0.47	0.50	0.53	A/V
VCM transconductance gain low	GM _{VL}	Gain _{sel} =5V	0.1	0.125	0.15	A/V
VCM+ saturation voltage lower	V _{VMS1}	R _{vcm} =15Ω	-	-	0.5	V
VCM- saturation voltage upper	V _{VMS2}	R _{vcm} =15Ω	-	-	0.5	V
VCM+ saturation voltage upper	V _{VMS3}	R _{vcm} =15Ω	-	-	0.5	V
VCM- saturation voltage lower	V _{VMS4}	R _{vcm} =15Ω	-	-	0.5	V
VCM+ saturation voltage lower	V _{VMS5}	R _{vcm} =15Ω	-	-	0.5	V
VCM- saturation voltage upper	V _{VMS6}	R _{vcm} =15Ω	-	-	0.5	V
VCM+ saturation voltage upper	V _{VMS7}	R _{vcm} =15Ω	-	-	0.5	V
VCM- saturation voltage lower	V _{VMS8}	R _{vcm} =15Ω	-	-	0.5	V
Leakage current power Amplifier1	I _{VCML1}	-	-10	0	10	μA
Leakage current power Amplifier2	I _{VCML2}	-	-10	0	10	μA
RETRACT						
Min. operating voltage of CRET2	V _{CRET2}	CRET2=Sweep	-	3.0	-	V
Source voltage	V _{SRC}	CRET2=5V	0.8	1.0	1.2	V
Sinking saturation voltage	V _{RTSAT}	CRET2=5V	-	-	0.5	V
Retract sinking current1	I _{RCT1}	R _{ret} =8.0KΩ	40	48.2	60	mV
Retract sinking current2	I _{RCT2}	R _{ret} =4.2KΩ	80	91.8	100	mV
Retract sinking current3	I _{RCT3}	R _{ret} =2.7KΩ	130	143	155	mV
Cret charging current1	I _{CRET}	-	90	100	110	μA
Retract power Tr. leakage upper	I _{LRET1}	-	-1	0	1	μA
Retract power Tr. leakage lower	I _{LRET1}	-	-1	0	1	μA
THERMAL SHUT DOWN						
Operating temperature	TSD	-	135	150	165	°C
Thermal hysteresis	T _{HYS}	-	20	30	40	°C

APPLICATION INFORMATION

SPINDLE MOTOR DRIVE PART

The KA3120 is a combination chip consisting of spindle motor and voice coil motor designed for HDD system. According to the spindle conditions, the digital ASIC circuit provides optimum control signals (Start-up, commutation, speed control, and switching mode) to the KA3120.

Detection of the back-EMF (BEMF) of the spindle motor has to be output to an external digital circuit via FG. The MCLK and PWM signals are used to determine the commutation timing and to control the spindle speed, respectively.

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SPINDLE DRIVER

The spindle includes both low and high side drivers (H-bridge) for a three-phase sensorless brushless DC motor. To reduce the saturation voltage, the vertical PNP Tr is used as the high side driver.

FREQUENCY GENERATION (FG)

FG stands for Frequency Generation. It is the out signal toward the digital ASIC.

Representing the current spindle speed frequency, it contains important information about the motor speed and motor spin.

According to the FG frequency, the digital ASIC provides different motor clock signals to the motor drive IC via MCLK and checks the motor speed to send the VCM enable signal via CNTL3.

FG frequency (Hz), motor speed (rpm) and pole number are directly related as shown below in the three phase motor.

$$\text{FG frequency} = \text{motor speed} \times \text{pole number} \times 3 / 120$$

In a typical application,(8 pole motor)

$$\text{FG frequency} = 5400 \times 8 \times 3 / 120 = 1080\text{Hz}$$

$$\text{FG frequency} = \text{Output frequency} \times 3$$

MCLK & MASK

The MCLK is a motor clock used as the standard clock signal for the proper commutation timing of the spindle motor. It is supplied by the ASIC.

As shown in table 1, it has different delay times depending on the mode of the spindle speed. Table 1. MCLK & MASK Delay Time to the Spindle Speed.

Table 1. MCLK & MASK delay time to the spindle speed

	MCLK (Td)	MASK	Switching
Start-up mode	External ASIC	1ms	Hard switching
Acceleration mode	FG(n-1) / 2	FG(n-1) / 4	Hard switching
Running mode	FG(n-1) / 32	344.45µs	Soft switching

After the FG_Edge signal, the MCLK occurs after a half FG_Edge delay time in the acceleration mode and 1/ 32 FG_Edge delay time in the soft switching mode.

MASK

When the coil current is abruptly changed in a short time interval, a spark voltage occurs. This spark voltage mixes with the FG output to give the wrong spindle information to the ASIC. To eliminate the spark voltage from the FG output, the masking block is needed.

$$V_{coil} = -L \frac{di}{dt}$$

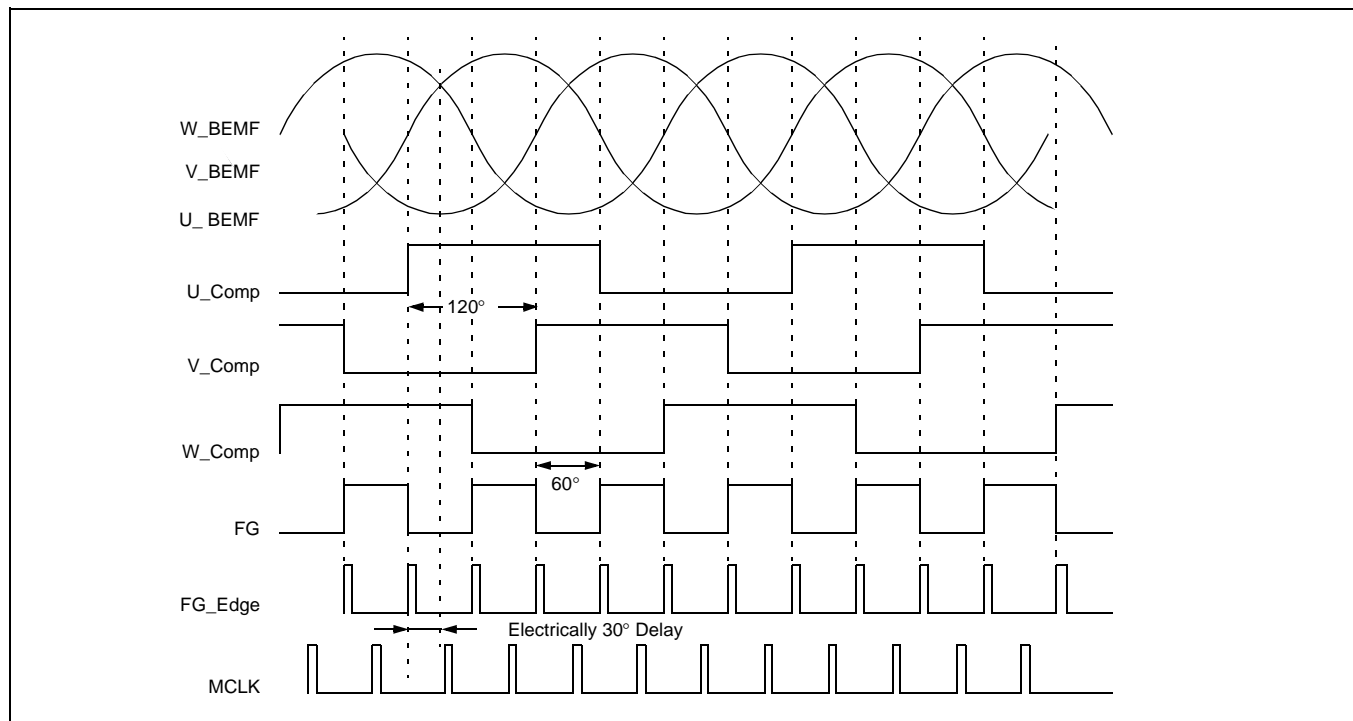


Figure 1. BEM, FG, and MCLK in the acceleration mode

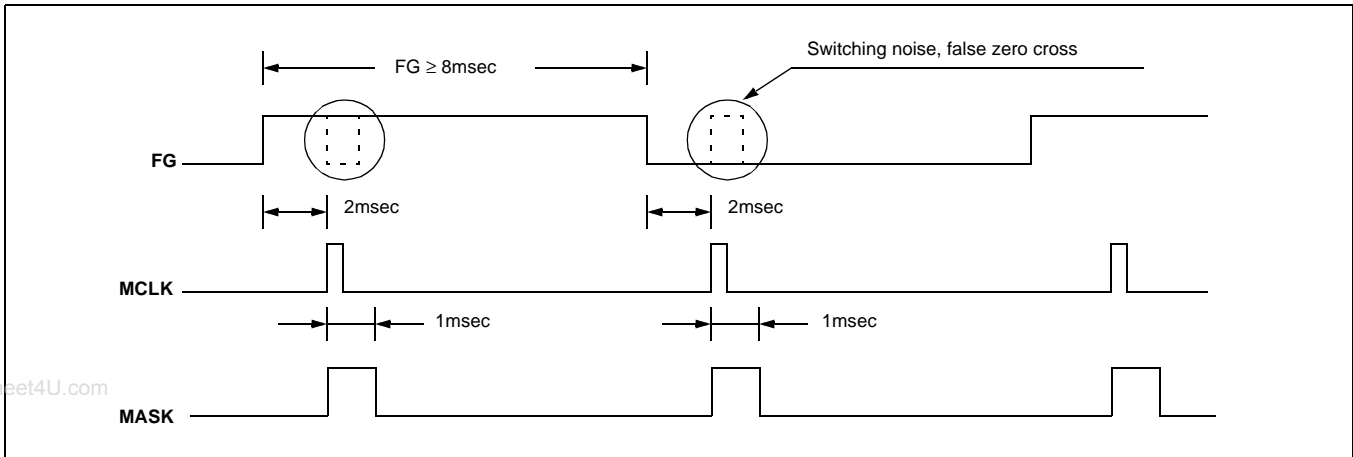


Figure 2. MCLK vs MASK in the start-up mode

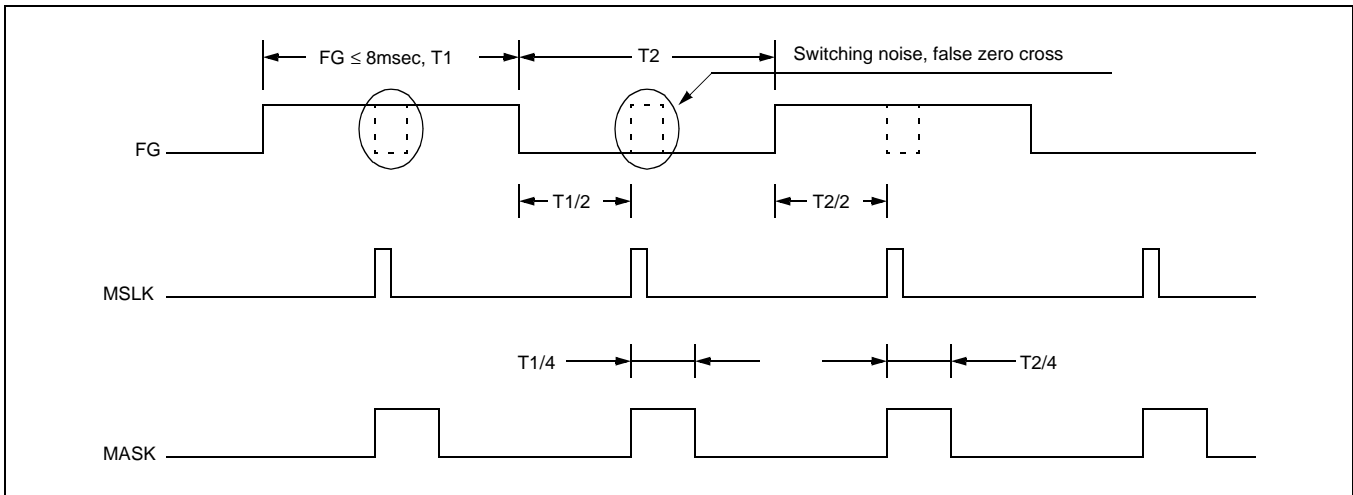


Figure 3. MCLK vs MASK in the acceleration mode

PWMDEC AND SPEED CONTROL

Motor speed is measured by the ASIC via the FG output. The digital ASIC compares FG frequency with the target motor speed and sends the speed compensation signal to the PWMSP input of the KA3120. This PWM signal is internally filtered and is converted into DC voltage through the built-in PWM Decoder Filter. The analog output of the filter depends on the duty of the PWM signal. The filter is a 3rd order, low-pass filter. The first pole location of the filter is determined by the external capacitor connected to pin(48) CFSP.

$$I_{spindle} = (D - 0.1) \cdot \frac{0.625}{R33 (= 0.25)}$$

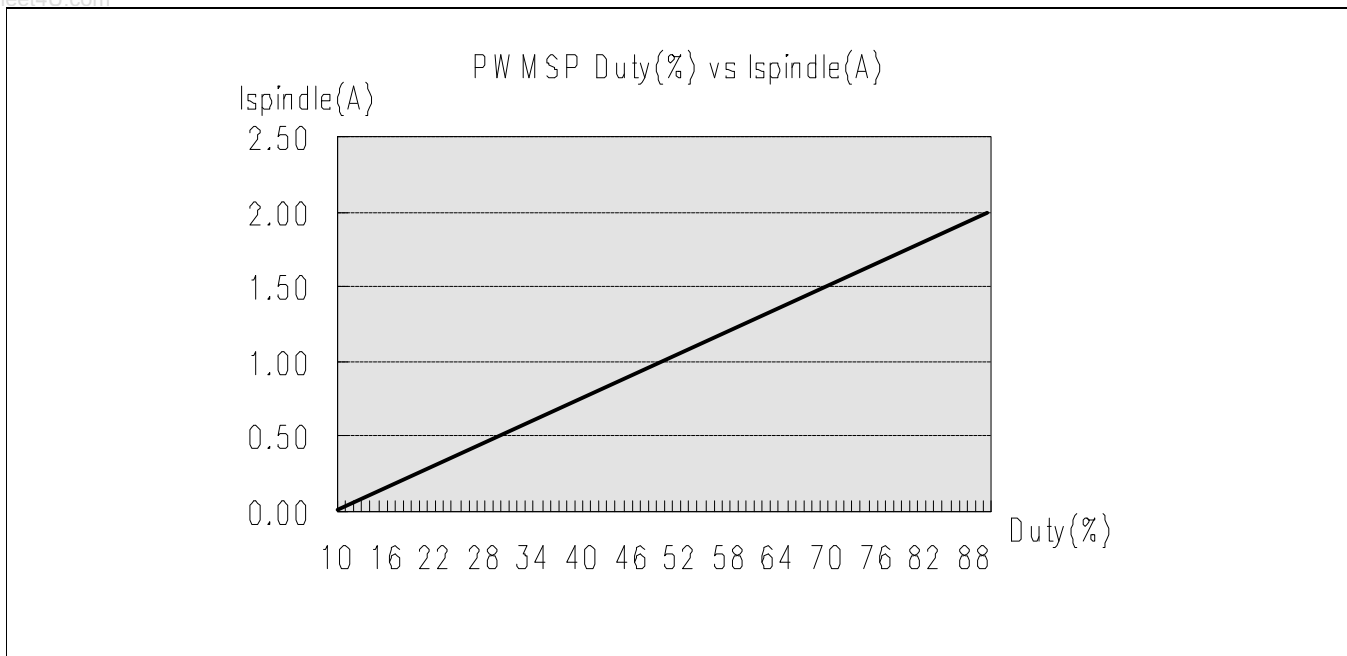


Figure 4. Spindle current vs PWMSP duty variation

START-UP MODE

The BEMF is used in the sensorless BLDC motor driver to determine the rotor position. The detected rotor position is a very important information to control the motor speed and the commutation timing.

At standstill condition, there is no BEMF voltage and no FG output. There is no information about the motor position. However the spindle motor must be started up at standstill.

To drive the spindle at the start-up mode, the digital ASIC sends the spindle enable signal via CNTL1 and supplies the HIGH or OPEN signal in turns via CNTL2 to be used as commutation signal of the spindle motor.

The digital ASIC continuously provides HIGH or OPEN signal until the BEMF generated is enough large to produce the FG signal i.e. the spindle motor can be driven by the self commutation. During a fixed time, if the BEMF generated is too small and the spindle motor is not driven by the self commutation, the ASIC resets all signals sent and retries the spindle.

Table 2. Pin setup truth table

	CNTL1 ⁽¹⁾		CNTL2 ⁽²⁾	CNTL3 ⁽³⁾		GAINSEL	
	SPM driver	Brake	S/W	VCM driver	Retract	SPM driver	VCM gain
High (5V)	1	0	Hard S/W	1	0	Normal	0.125
Open (Floating)	0	0	Hard S/W	0	0	x	x
Low (0V)	0	1	Soft S/W	0	1	Start up ⁽⁴⁾ Hold	0.5

NOTES:

1. CNTL1: Spindle motor control
2. CNTL2: Switching mode control
3. CNTL3; VCM motor control
4. Test only
5. "1": Enable; "0": disable; "S/W": switching

ACCELERATION MODE

When the BEMF detected is enough to be used as the information of motor position, the mode is changed from start-up to acceleration. The ASIC sends the optimum commutation timing signal via MCLK according to the FG input.

By using the BEMF, the spindle is self-commuted at acceleration and running modes. During the motor drive, the spindle motor is commuted at that point which is electrically 30° delayed after the FG_Edge generates.

RUNNING MODE

It is called to the running mode when the spindle motor speed arrives within ± 1% of the target speed. The switching mode, commutation delay time, MCLK delay time (Td) and masking time are changed at the running mode.

The spindle motor speed is controlled by PWM signal within ± 0.01%.

The soft switching using the current slope of the motor may reduce noise, EMI (Electromagnetic Interference) and spark voltage which is generated on the motor coil at the switching.

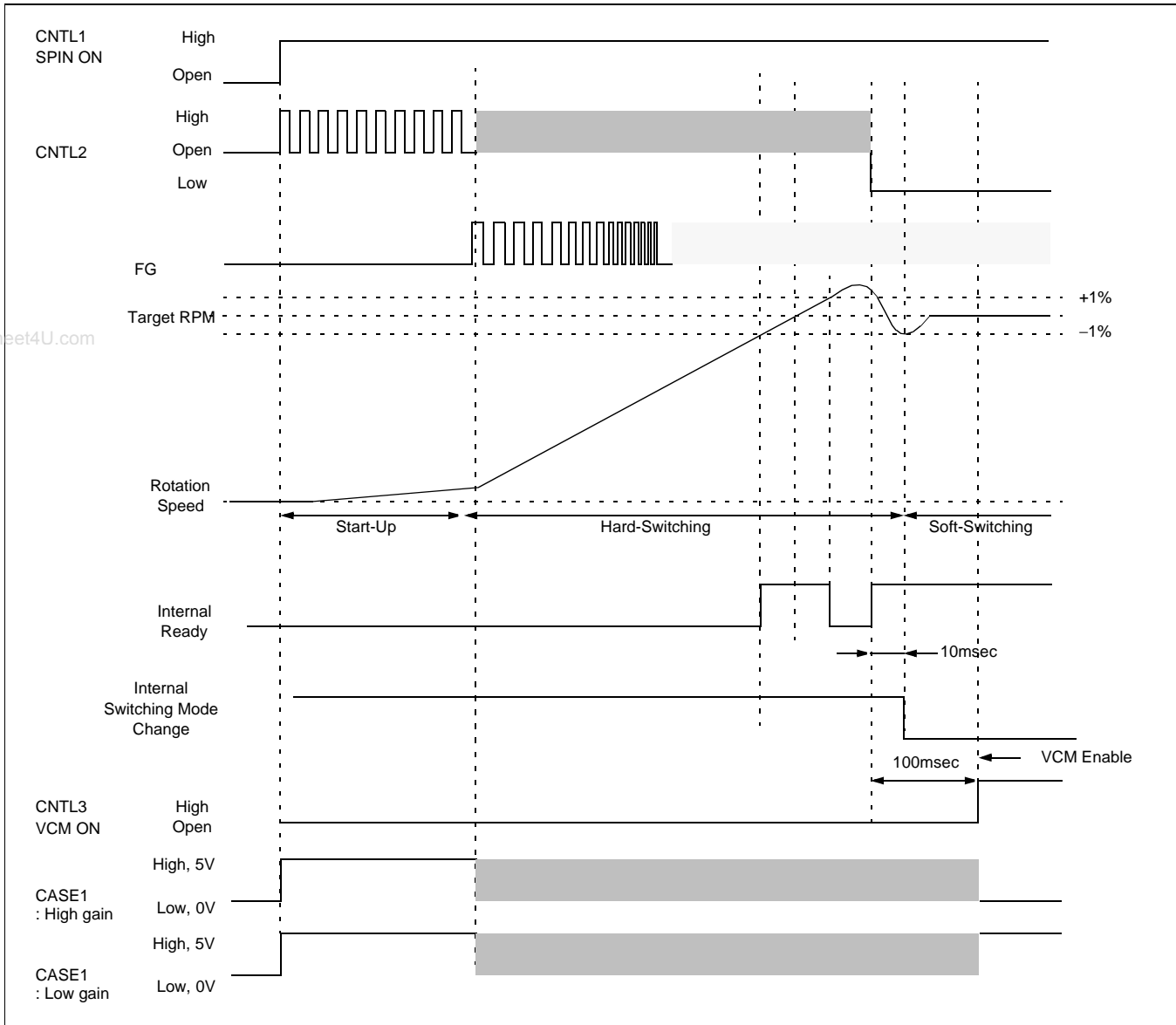


Figure 5. Motor start-up sequence

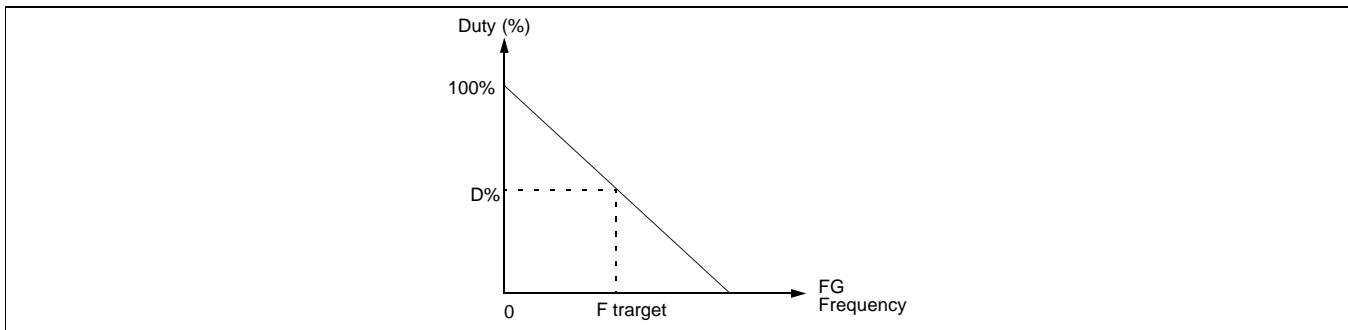


Figure 6. FG vs PWMSP duty variation

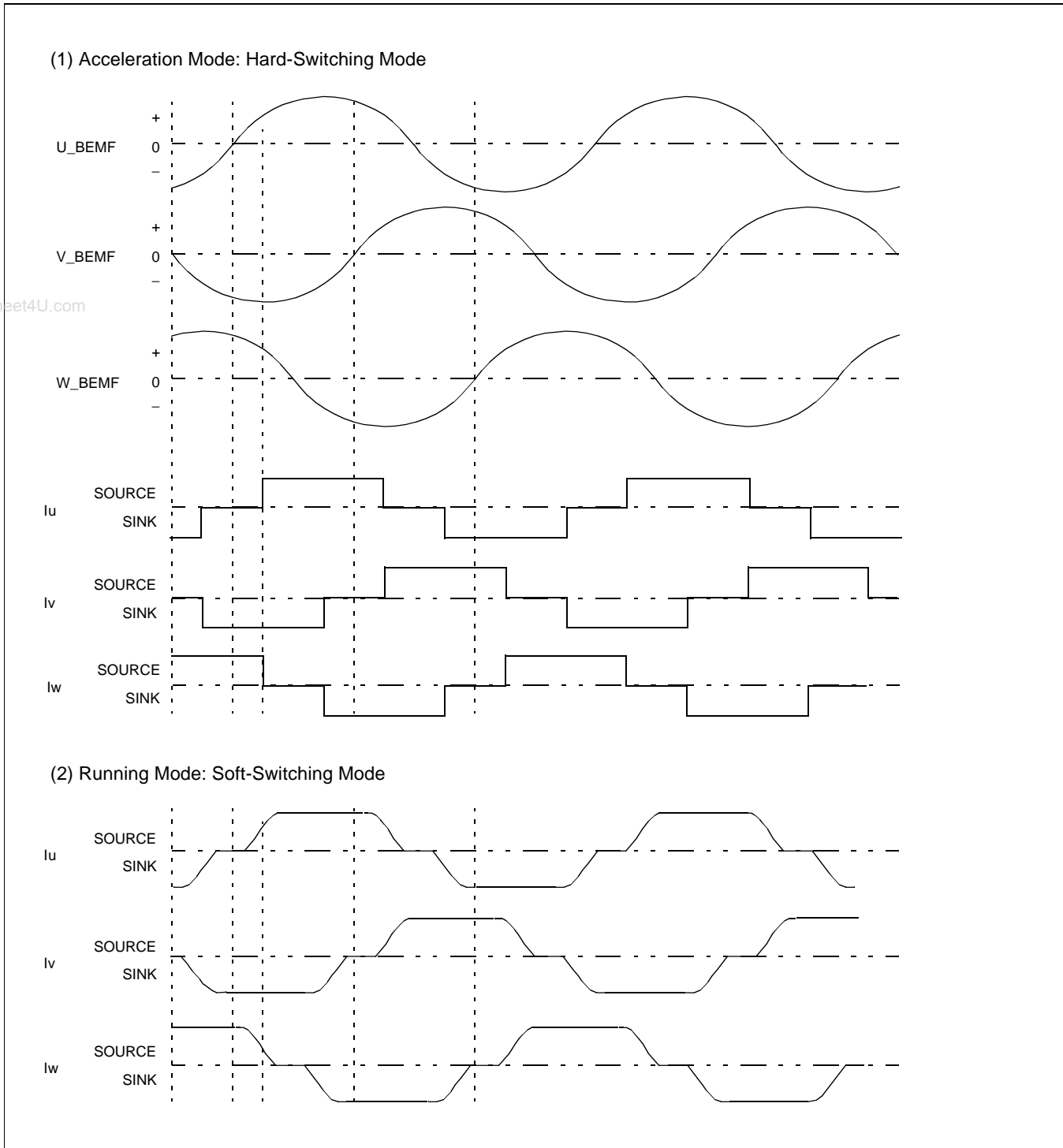


Figure 7. Acceleration and running the spindle motor

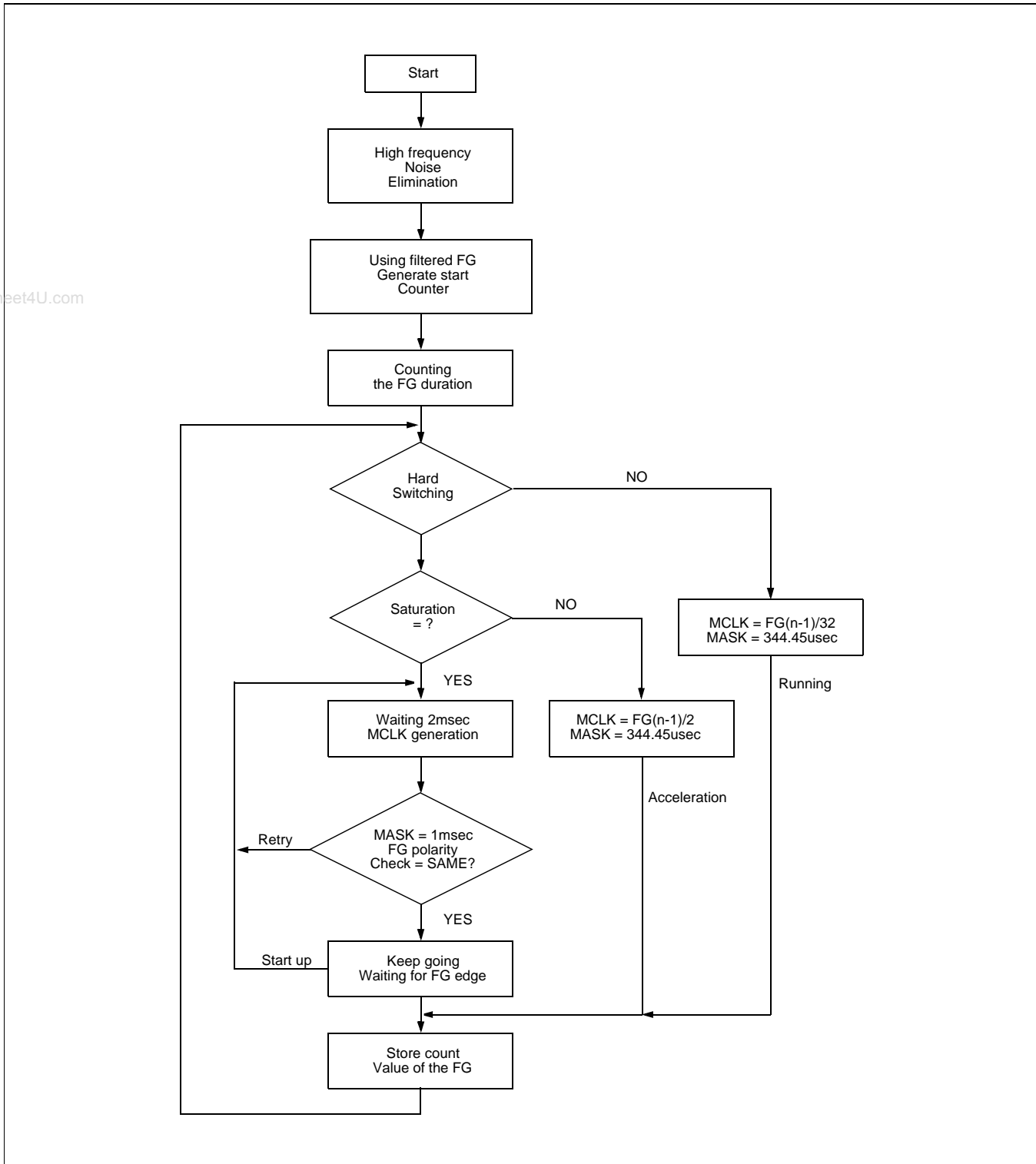


Figure 8. MCLK generation flow chart

VOICE COIL MOTOR

VCM driver

The voice coil motor driver is linear, class AB, H-bridge type driver, and it includes all power transistors. After the VCM is enabled via CNTL3, the VCM current level is controlled by two PWM signals. The input voltage level at pin PWMH weighs, at a maximum, 32 times more than the input voltage at pin PWML. These PWM signals are filtered by an internal second-order low-pass filter and converted into PWMOUT (DC Voltage). The filter PWMOUT depends only on the duty factor and not on the logic level. The PWM Filter's pole is adjustable by pin CFVCM connected to the external capacitor.

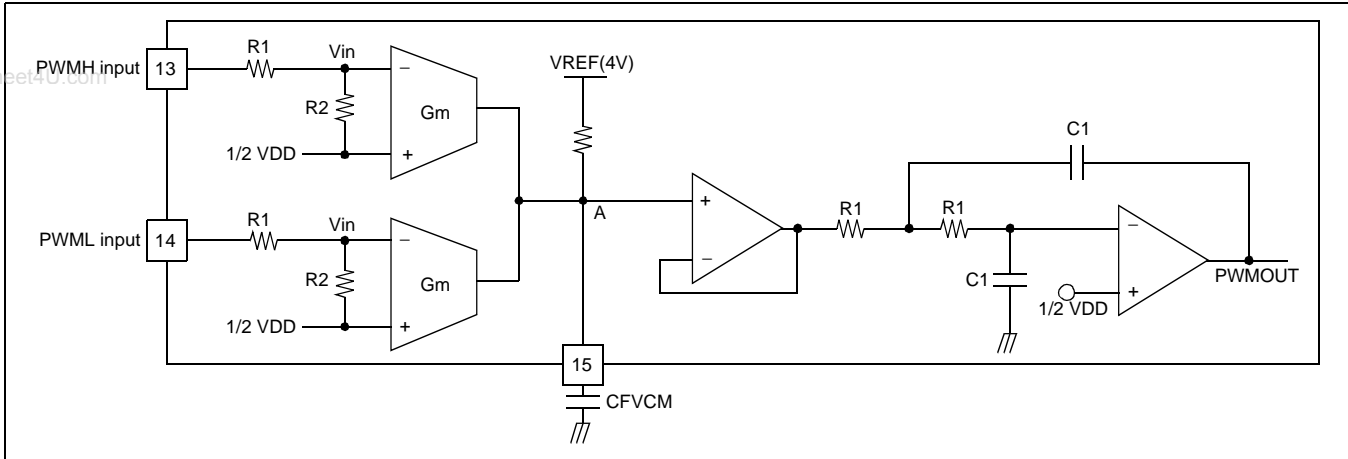


Figure 9. PWM decoder & filter schematic 2

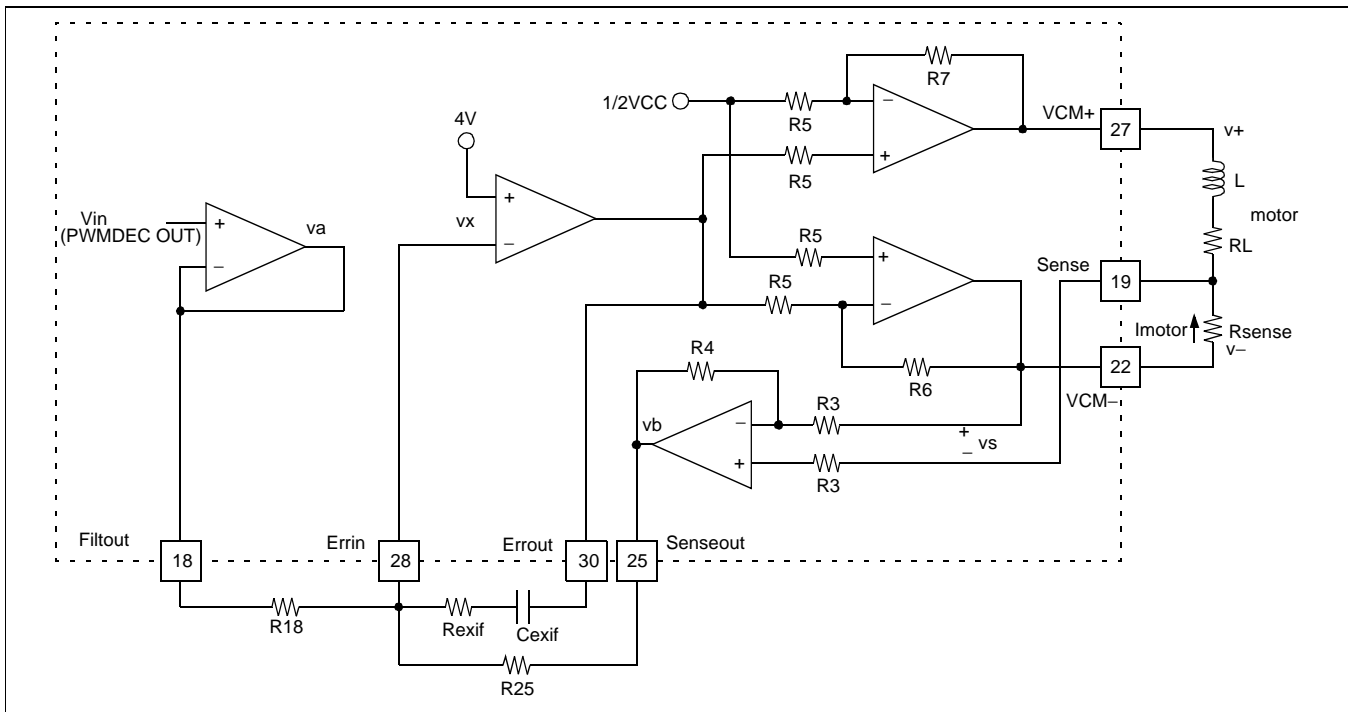


Figure 10. VCM driver schematic

The transconductance of VCM AMPLIFIER gain, G_m , is:

$$G_m = \frac{I_{motor}}{V_{in}} = \frac{2 \cdot A_{error} \cdot A_{power} \cdot R_{25}}{2 \cdot R_{18} \cdot R_{sense} \cdot A_s \cdot A_{error} \cdot A_{power} + (R_{18} + R_{25})(Z_{motor} + R_{sense})}$$

$$G_m = \frac{A_{loop}}{1 + A_{loop}} \left(\frac{R_{25}}{R_{18} R_{sense} A_s} \right)$$

$$A_{loop} = \frac{2 \cdot R_{18} \cdot A_s \cdot A_{error} \cdot A_{power}}{(R_{18} + R_{25})(Z_{motor} + R_{sense})}$$

Therefore $A_{loop} \gg 1$,

$$G_m \cong \frac{R_{25}}{R_{18}} \cdot \frac{1}{R_{sense}} \cdot \frac{1}{A_s}$$

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The transconductance (G_m) can be adjusted by selecting the external components R_{18} , R_{25} and sense resistor R_{sense} .

if $R_{18} = 15k$, $R_{25} = 15k$, $R_{sense} = 1$

GAINSEL = 0(0V), $1 / A_s = 0.5$

$G_m = 0.5$

GAINSEL = 1(5V), $1 / A_s = 0.125$

$G_m = 0.125$

VCM current (I_{motor}) is:

GAINSEL = 0(0V)

$$I_{motor} = 4 \times \left[(PWMH - 0.5) + \frac{1}{32}(PWML - 0.5) \right] \times \frac{R_{25}}{R_{18}} \times \frac{1}{R_{sense}} \times 0.43$$

GAINSEL = 1(5V)

$$I_{motor} = 4 \times \left[(PWMH - 0.5) + \frac{1}{32}(PWML - 0.5) \right] \times \frac{R_{25}}{R_{18}} \times \frac{1}{R_{sense}} \times 0.11$$

Recommended value PWMH(100%) = 1
 $R_{18} = R_{25} = 15k$ PWMH(50%) = 0.5
 $R_{sense} = 1$ PWMH(0%) = 0

RETRACT CIRCUIT

The retract function is the operation where the VCM moves from the data zone to the parking zone when off normal state power and abnormal power interrupt cause the spindle to stop.

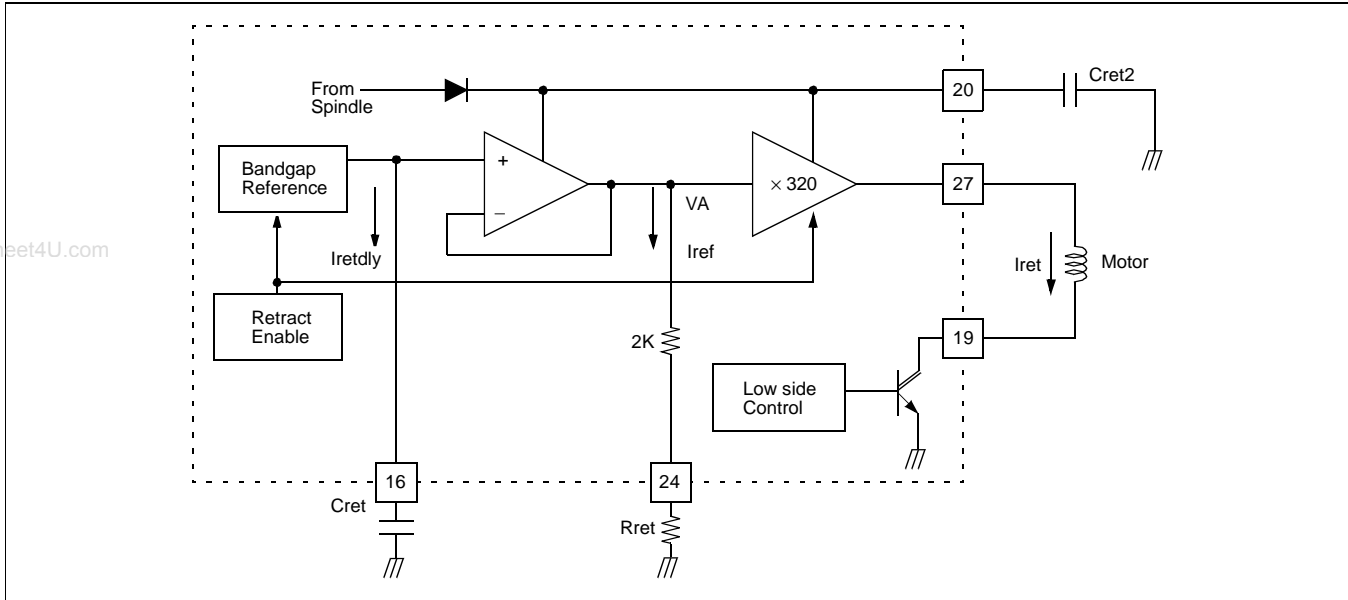


Figure 11. Retract block schematic

$$VA = 2.0V$$

$$I_{ref} = \frac{VA}{R_{ext} + 2k}$$

$$I_{ret} = I_{ref} \times 320$$

$$T_{retdly} = \frac{C_{ret} \times 2.0V}{I_{retdly}(= 100\mu)}$$

POWER MANAGEMENT FEATURES

LOW POWER INTERRUPT:

The low power interrupt operation occurs when the power supply voltage (5V, 12V) level drops below each threshold voltage. The threshold voltage (V_{th}) and time delay (T_{dly}) may be adjustable by the external component value.

$$T_{dly} = CDLY \frac{V_{th}}{I}, (V_{th} = 2.5V, I = 14\mu A)$$

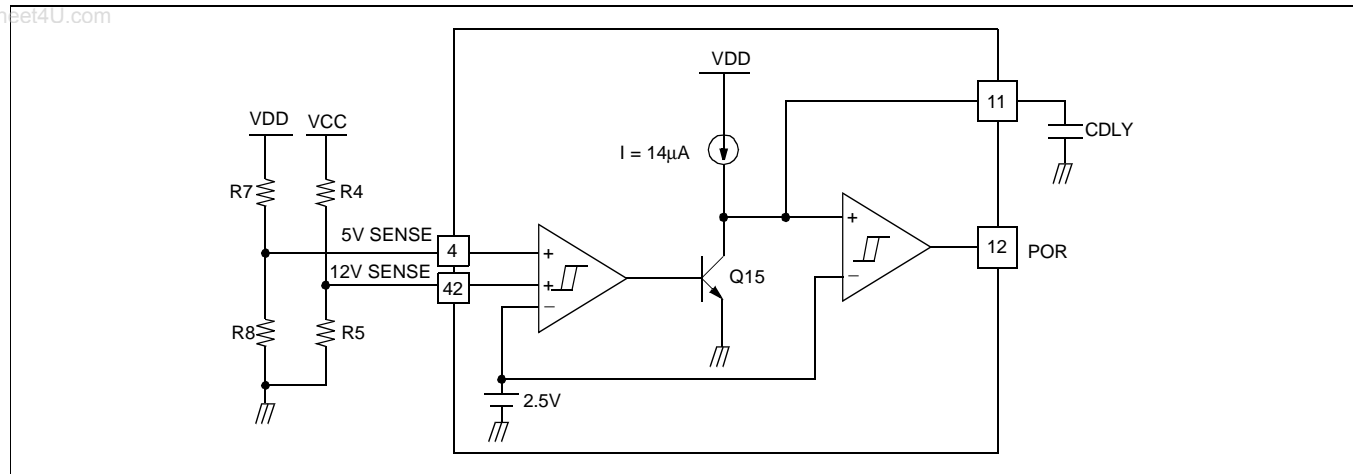


Figure 12. Power on reset block schematic

POWER ON RESET

The power-on reset circuit monitors the voltage level of both +5V and +12V power supplies. The power-on reset circuit disables the spindle out block, the whole VCM block, and the digital ASIC when the power supply voltage level drops below the reference voltage.

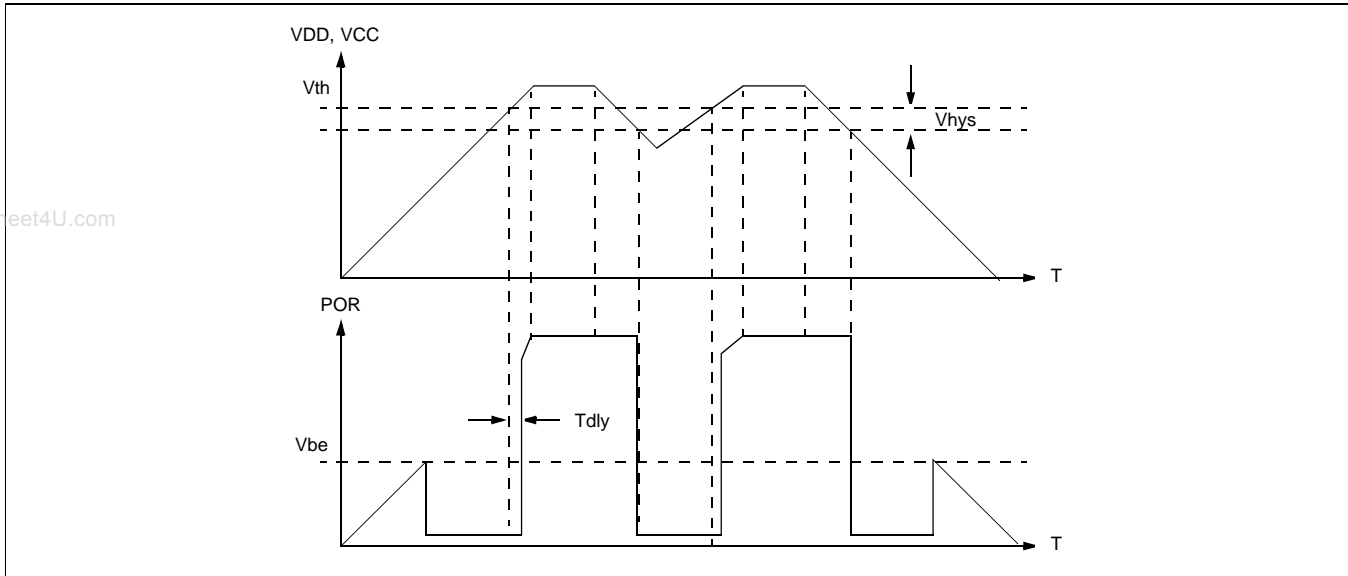


Figure 13. Power on reset function

$$V_{hys} = 4.2mV$$

$$V_{DD}; V_{hys}(5V) = \frac{R4 + R5}{R5} \times V_{hys}$$

$$V_{DD}; V_{hys}(12V) = \frac{R7 + R8}{R8} \times V_{hys}$$

Default (pin4, pin42 : not connected)

$$V_{DD}, th \cong 4.1V$$

$$V_{CC}, th \cong 9.4V$$

REGULATOR

The KA3120 includes the regulator block which supplies power of the digital ASIC. It consists of the bias block, the band gap reference, the error amp and the external NPN power Tr. The regulator voltage can be adjusted by the external resistor, R3a, R3b.

$$V_{reg} = V_{ref} \left(1 + \frac{R_{3a}}{R_{3b}} \right), V_{ref} = 1.3V$$

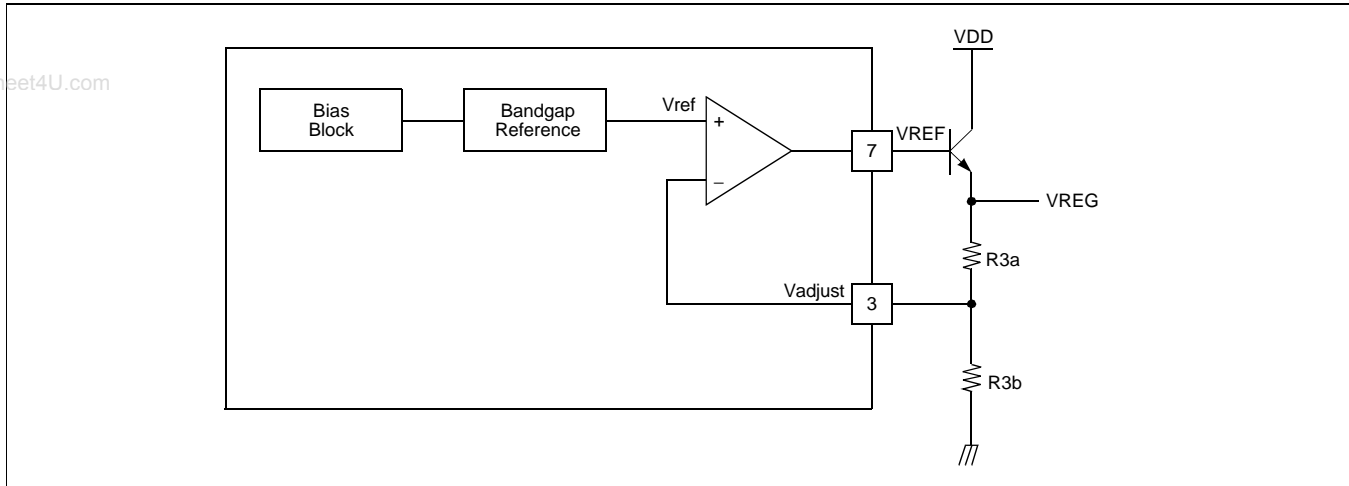


Figure 14. low drop regulator schematic

if R3a = 15k, R3b = 10k

$$V_{reg} = V_{ref} \left(1 + \frac{R_{3a}}{R_{3b}} \right) = 1.3 \times \left(1 + \frac{15k}{10k} \right) = 3.25V$$

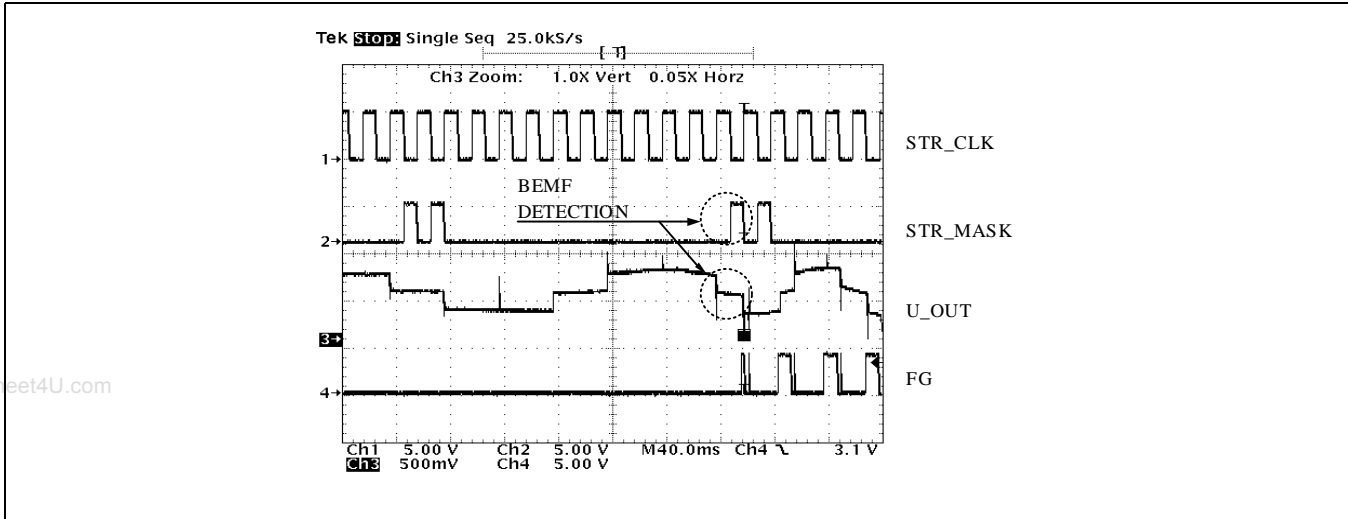


Figure 15. Start-up mode

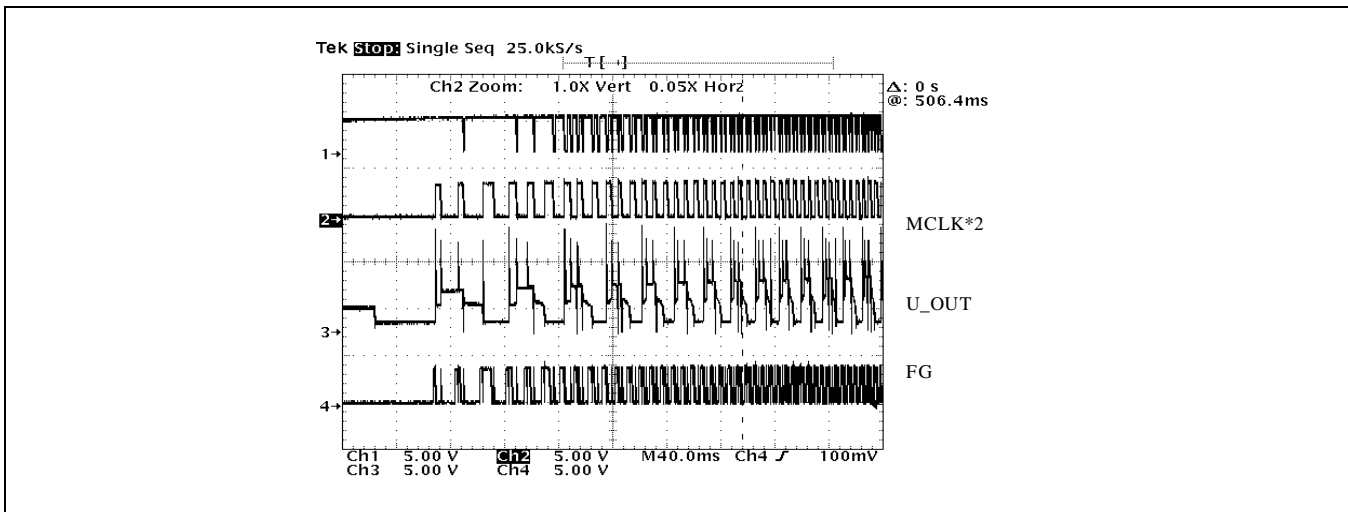


Figure 16. Acceleration mode 1

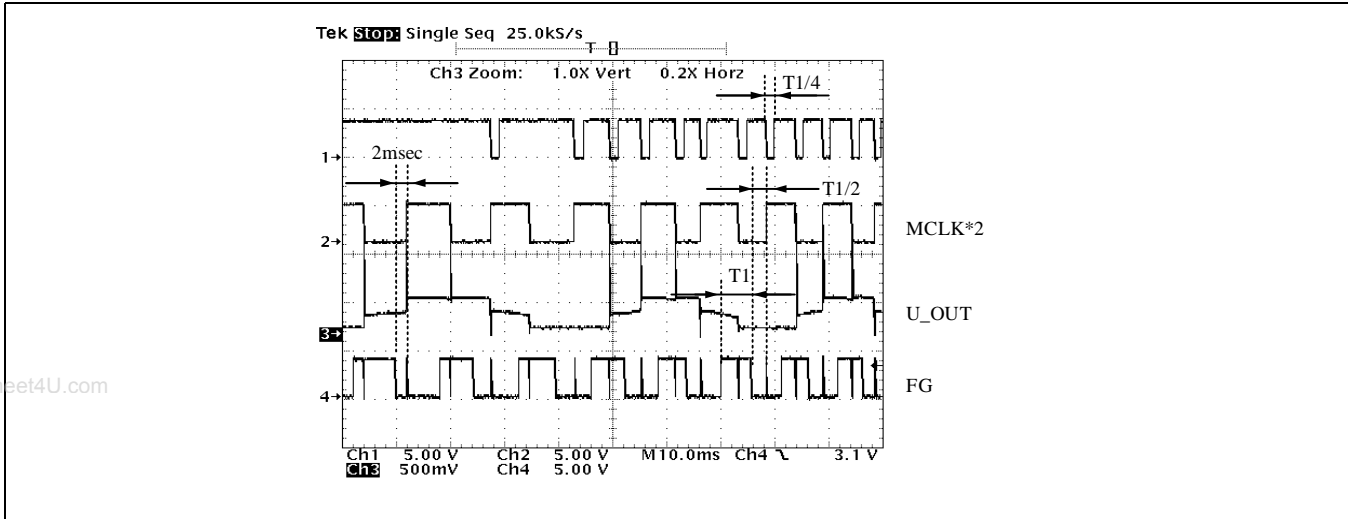


Figure 17. Acceleration mode 2

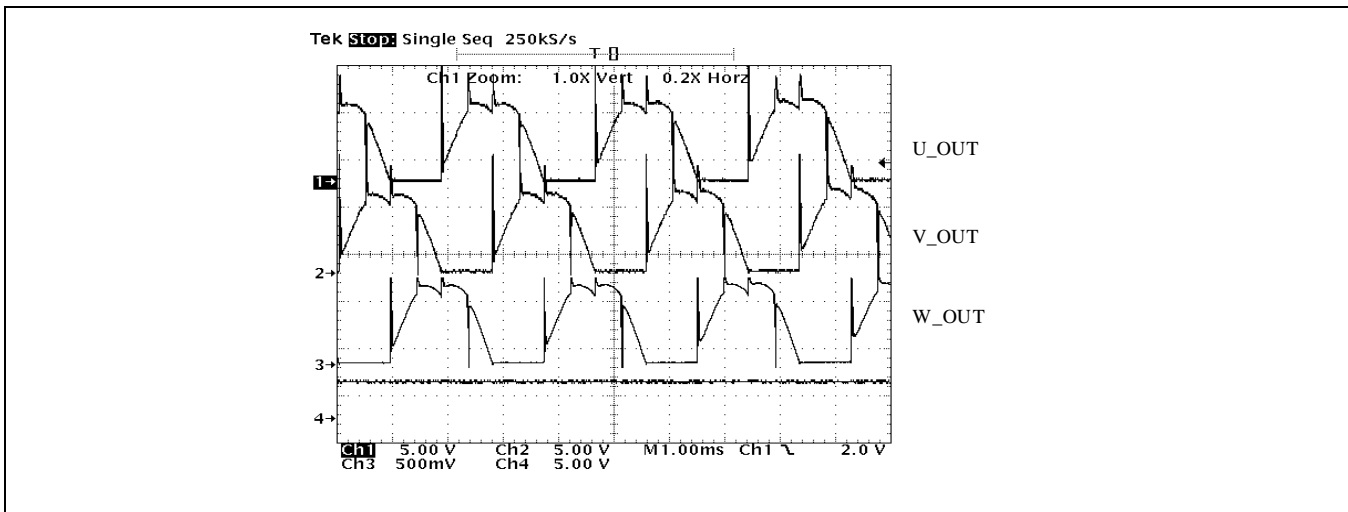


Figure 18. Output in hard-switching mode

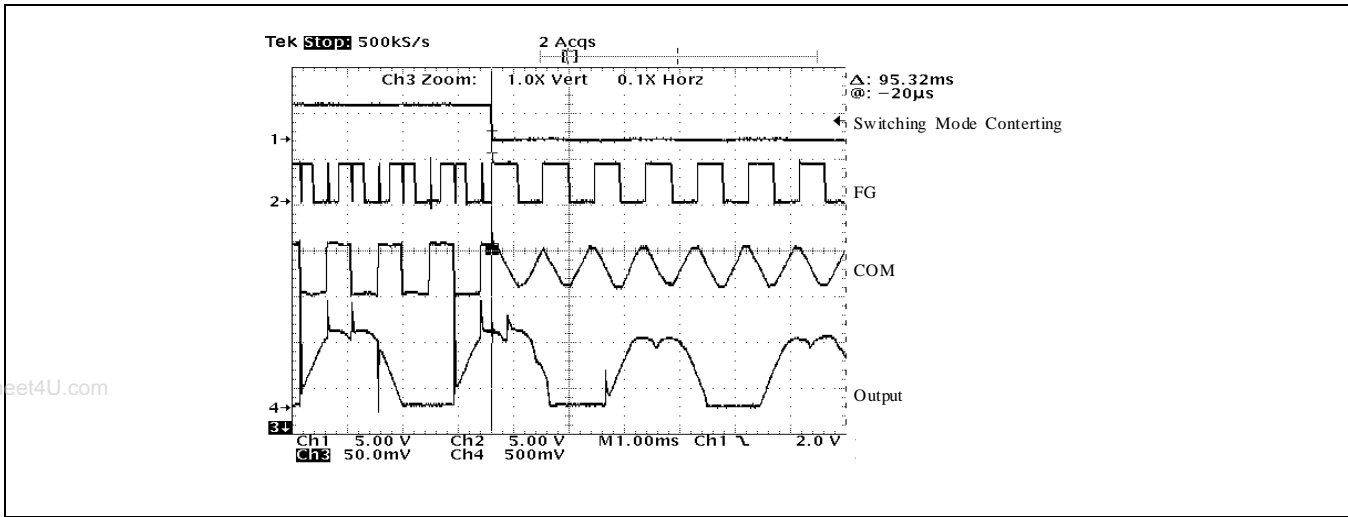


Figure 19. Switching mode converting

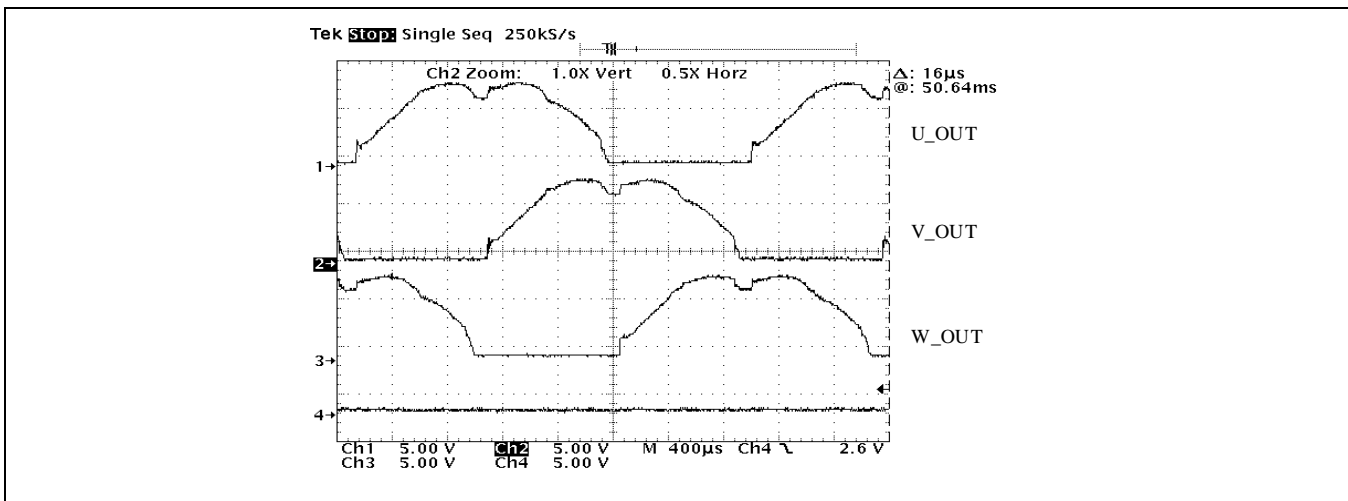


Figure 20. Soft-switching mode

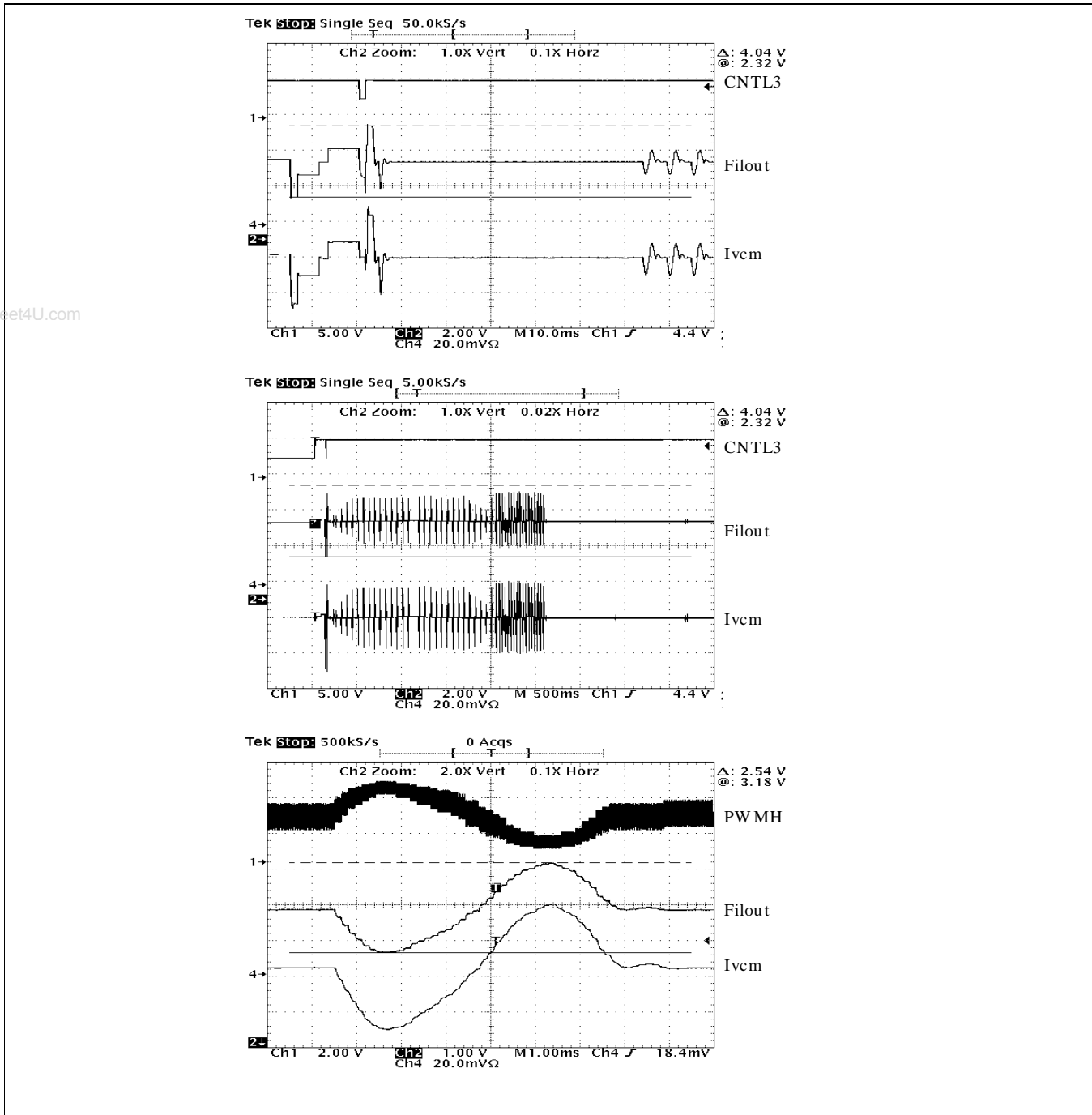


Figure 21. VCM recalibration flow

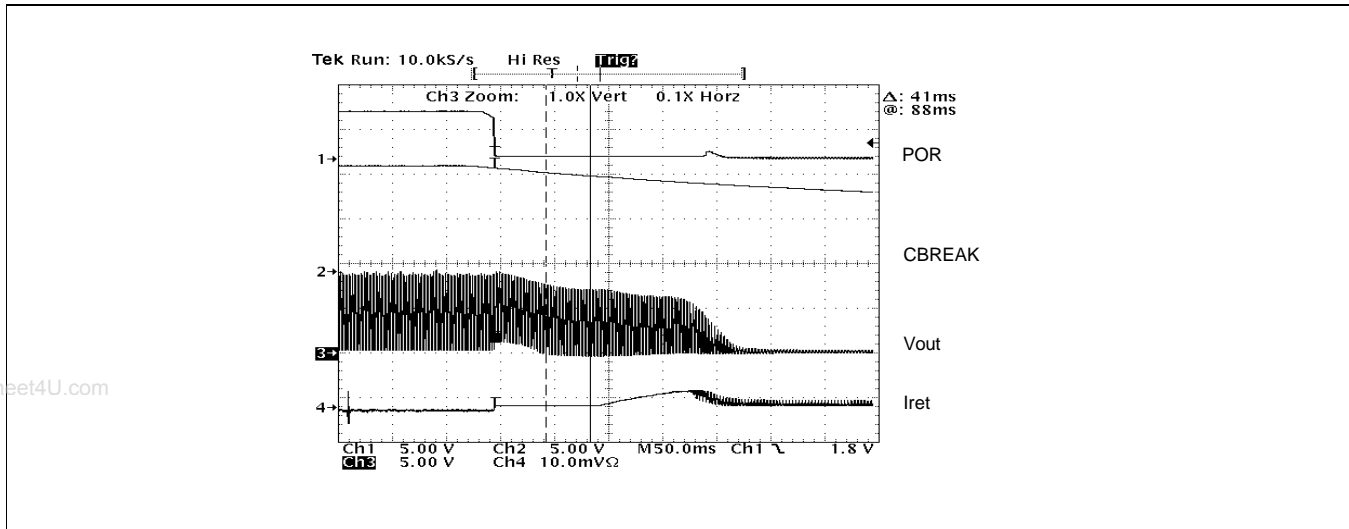
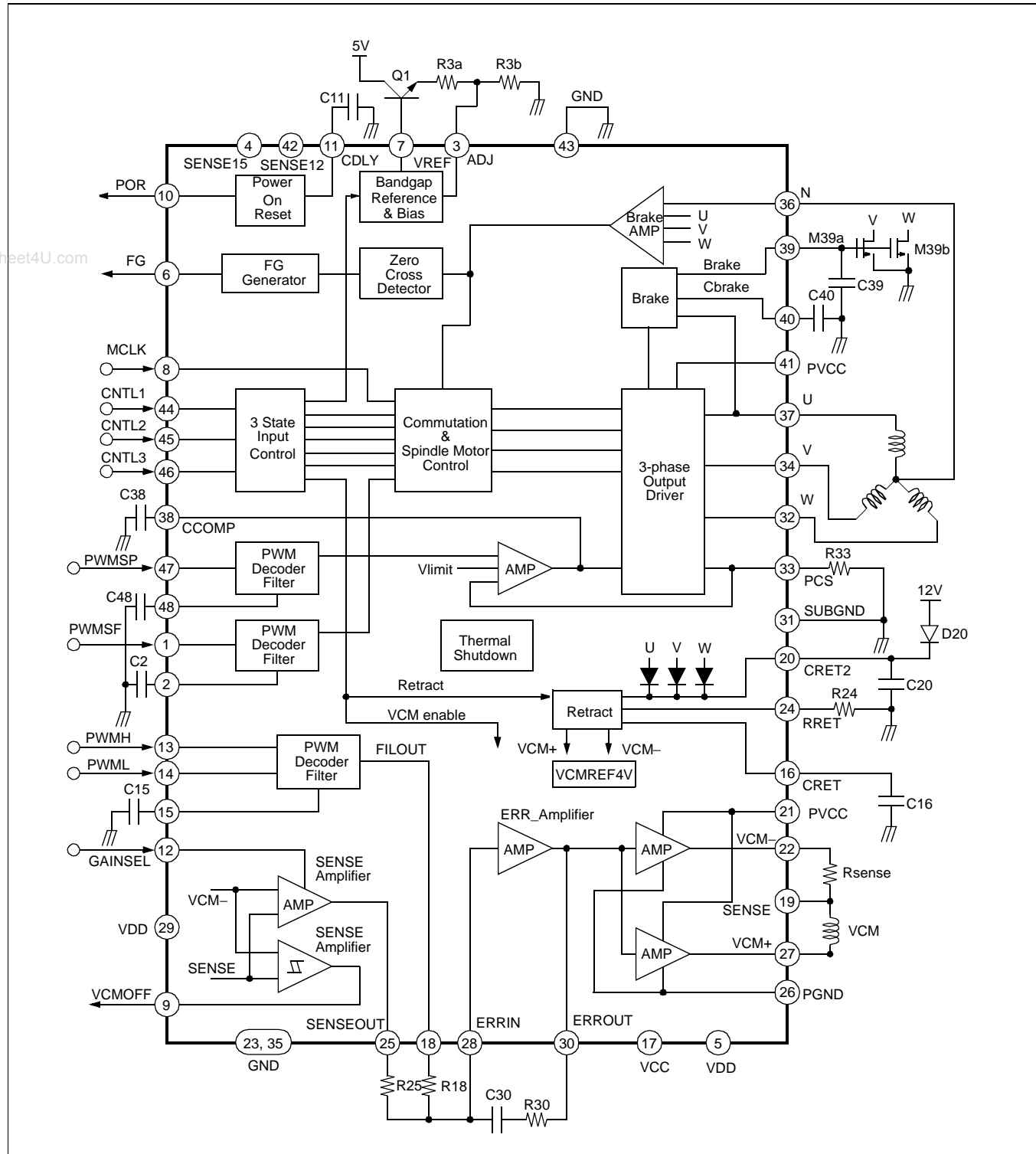
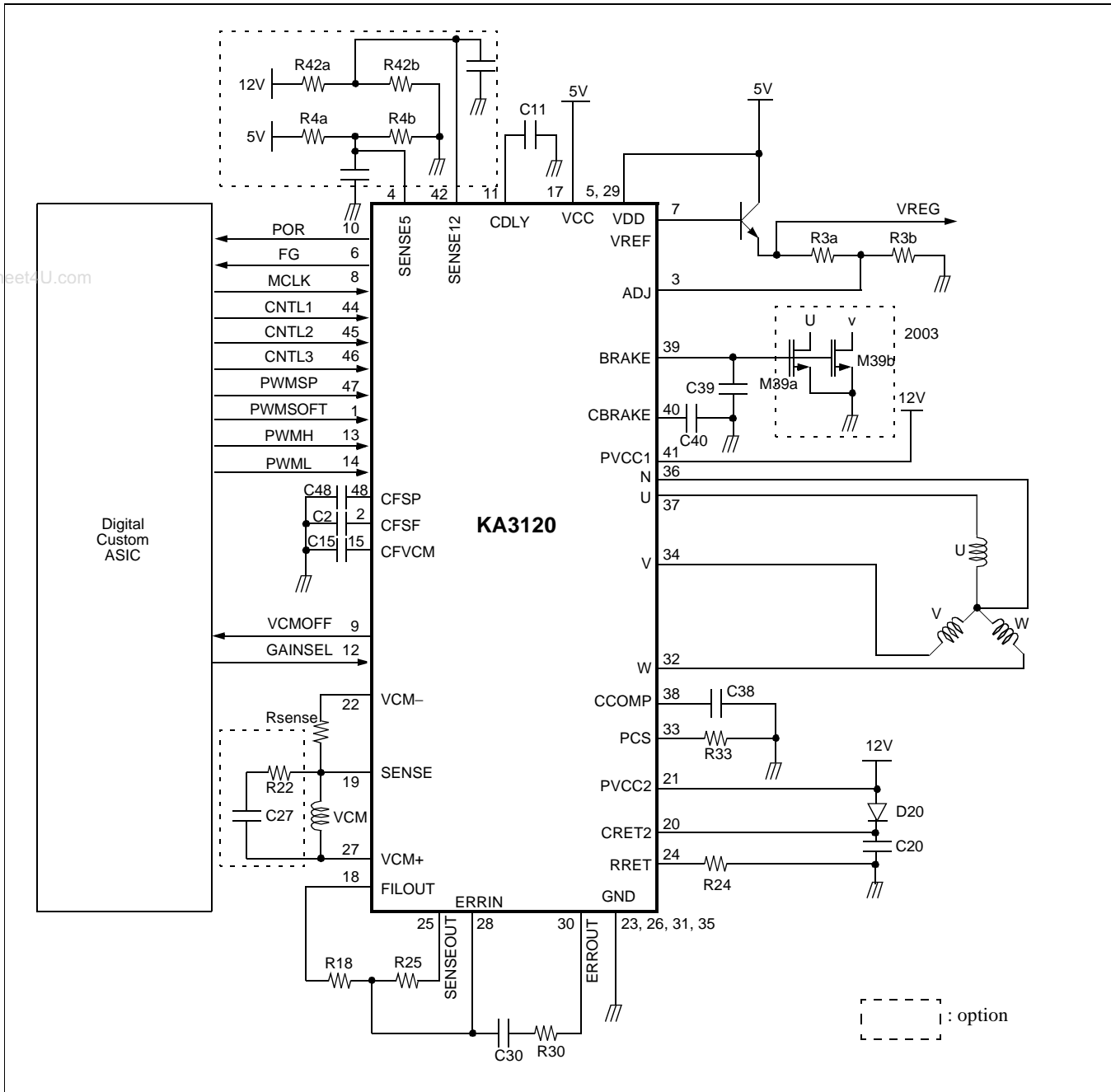


Figure 22. Retract & break at power off

TYPICAL APPLICATION CIRCUIT



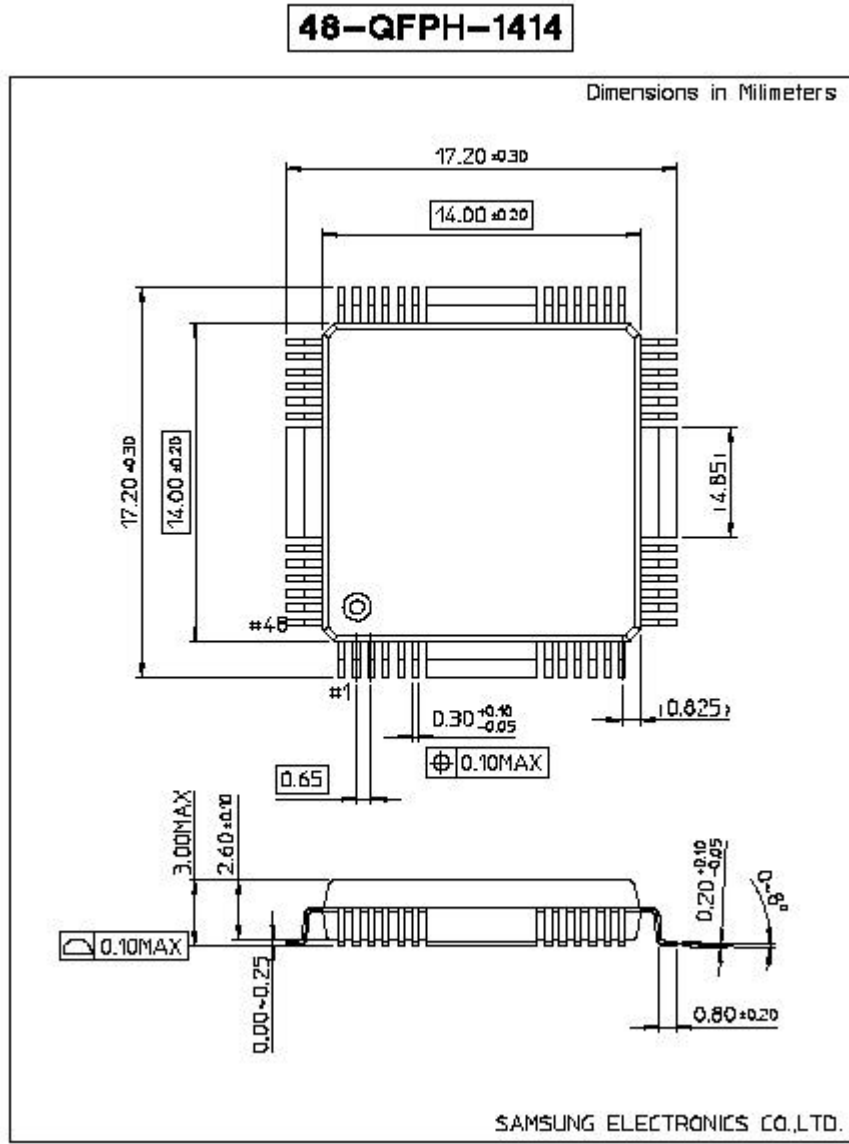
APPLICATION CIRCUIT



COMPONENT VALUE

Part No.	Value	Type	Part No.	Value	Type	Part No.	Value	Type
R18	15k	1/4W	C2	10n	Ceramic	Q1	KSH29	D-PAK
R24	2.2k	1/4W	C11	47n	Ceramic	M39a	SSD2003	8SOP
R22	Option	1/4W	C15	10n	Ceramic	M39b		
R25	15k	1/4W	C16	1 μ	Ceramic	D20	RB4110	Schottky Diode
R30	1k	1/4W	C20	224n	Ceramic	-	-	-
Rsense	1	1W	C27	1 μ	Ceramic	-	-	-
R33	0.25	1W	C30	1.2n	Ceramic	-	-	-
R4A	Option	1/4W	C38	150n	Ceramic	-	-	-
R4B	Option	1/4W	C40	220n	Ceramic	-	-	-
R42A	Option	1/4W	C48	10n	Ceramic	-	-	-
R42B	Option	1/4W	C39	Option	Ceramic	-	-	-

PACKAGE DIMENSION



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