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Micropower Synchronous Buck-Boost DC/DC Converter

FEATURES

- **Single Inductor**
- **Fixed Frequency Operation with Battery Voltages Above, Below or Equal to the Output**
- **Synchronous Rectification: Up to 96% Efficiency**
- **40μA Quiescent Current in Burst Mode® Operation**
- **Up to 600mA Continuous Output Current**
- No Schottky Diodes Required (V_{OUT} < 4.3V)
- V_{OUT} Disconnected from V_{IN} During Shutdown
- 2.5V to 5.5V Input and Output Range
- Programmable Oscillator Frequency from 300kHz to 2MHz
- Synchronizable Oscillator
- Burst Mode Enable Control
- 5 μA Shutdown Current
- Small Thermally Enhanced 10-Pin MSOP and (3mm × 3mm) DFN Packages

APPLICATIONS

- Palmtop Computers
- Handheld Instruments
- MP3 Players
- Digital Cameras

DESCRIPTION

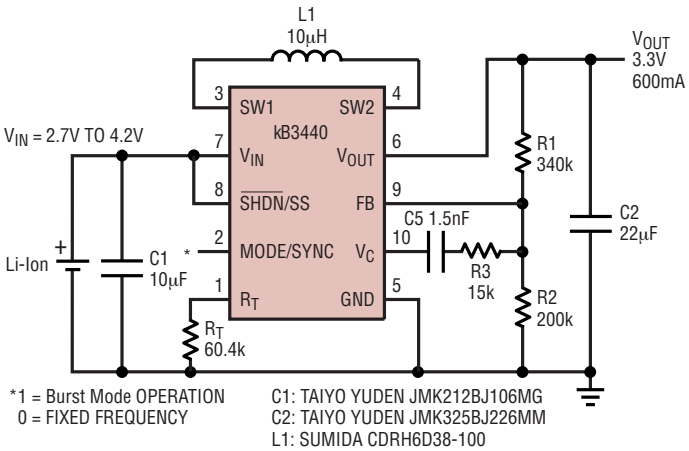
The kB3440 is a high efficiency, fixed frequency, Buck-Boost DC/DC converter that operates from input voltages above, below or equal to the output voltage. The topology incorporated in the IC provides a continuous transfer function through all operating modes, making the product ideal for single lithium-ion, multicell alkaline or NiMH applications where the output voltage is within the battery voltage range.

The device includes two 0.19Ω N-channel MOSFET switches and two 0.22Ω P-channel switches. Switching frequencies up to 2MHz are programmed with an external resistor and the oscillator can be synchronized to an external clock. Quiescent current is only 40μA in Burst Mode operation, maximizing battery life in portable applications. Burst Mode operation is user controlled and can be enabled by driving the MODE/SYNC pin high. If the MODE/SYNC pin has either a clock or is driven low, then fixed frequency switching is enabled.

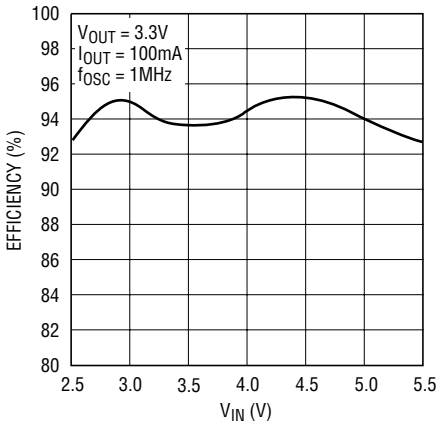
Other features include a 1μA shutdown, soft-start control, thermal shutdown and current limit. The kB3440 is available in the 10-pin thermally enhanced MSOP and (3mm × 3mm) DFN packages.

TYPICAL APPLICATION

Li-Ion to 3.3V at 600mA Buck-Boost Converter



Efficiency vs V_{IN}



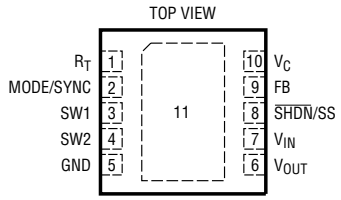
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, V_{OUT} Voltage ..... –0.3V to 6V
SW1, SW2 Voltage ..... –0.3V to 6V
V_C, R_T, FB, $\overline{SHDN}$/SS,
MODE/SYNC Voltage ..... –0.3V to 6V

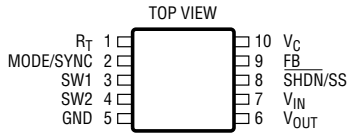
Operating Temperature Range (Note 2) .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACAGE/ORDER INFORMATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
EXPOSED PAD (PIN 11) IS GND
MUST BE SOLDERED TO PCB
T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3°C/W

ORDER PART NUMBER
kB3440EDD
DD PART MARKING
XXXX



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C,
θ_{JA} = 130°C/W 1 LAYER BOARD
θ_{JA} = 100°C/W 4 LAYER BOARD
θ_{JC} = 45°C/W

ORDER PART NUMBER
kB3440EMS
MS PART MARKING
HX-AA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} = 3.6V, R_T = 60k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Start-Up Voltage		●		2.4	2.5	V
Input Operating Range		●	2.5		5.5	V
Output Voltage Adjust Range		●	2.5		5.5	V
Feedback Voltage		●	1.196	1.22	1.244	V
Feedback Input Current	V_{FB} = 1.22V			1	50	nA
Quiescent Current, Burst Mode Operation	V_C = 0V, MODE/SYNC = 3V (Note 3)			40	50	μA
Quiescent Current, Shutdown	$\overline{SHDN}$ = 0V, Not Including Switch Leakage			0.1	1	μA
Quiescent Current, Active	V_C = 0V, MODE/SYNC = 0V (Note 3)			2800	4000	μA
NMOS Switch Leakage	Switches B and C			0.1	5	μA
PMOS Switch Leakage	Switches A and D			0.1	10	μA
NMOS Switch On Resistance	Switches B and C			0.19		Ω
PMOS Switch On Resistance	Switches A and D			0.22		Ω
Input Current Limit		●	1			A
Maximum Duty Cycle	Boost (% Switch C On) Buck (% Switch A On)	● ●	55 100	75		% %
Minimum Duty Cycle		●			0	%
Frequency Accuracy		●	0.8	1	1.2	MHz
MODE/SYNC Threshold			0.4		2	V
MODE/SYNC Input Current	$V_{MODE/SYNC}$ = 5.5V			0.01	1	μA
Error Amp AVOL				90		dB
Error Amp Source Current				15		μA
Error Amp Sink Current				380		μA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} = 3.6V, R_T = 60k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$/SS Threshold	When IC is Enabled When EA is at Maximum Boost Duty Cycle	●	0.4	1 2.2	1.5	V V
$\overline{SHDN}$/SS Input Current	$V_{\overline{SHDN}}$ = 5.5V			0.01	1	µA

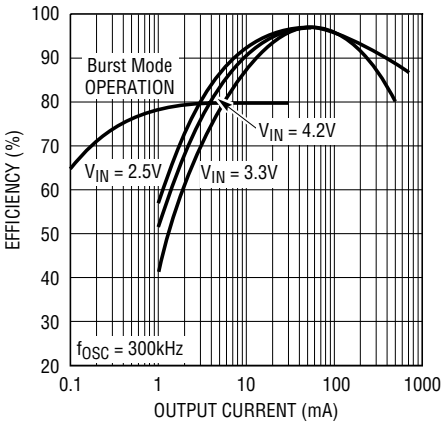
Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: The kB3440E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

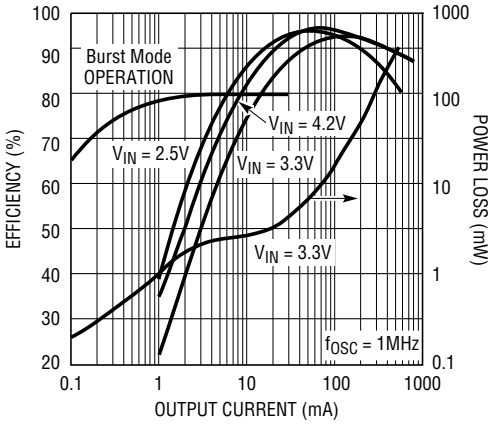
Note 3: Current measurements are performed when the outputs are not switching.

TYPICAL PERFORMANCE CHARACTERISTICS

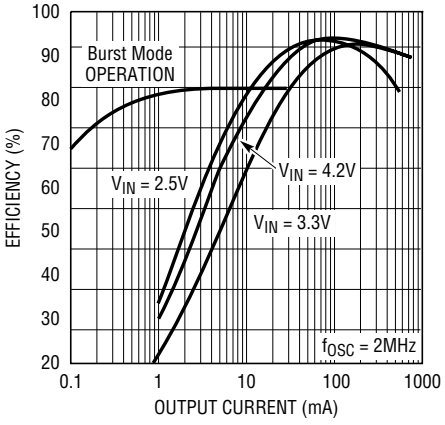
Li-Ion to 3.3V Efficiency (f_{OSC} = 300kHz)



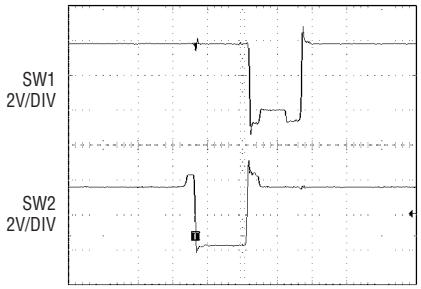
Li-Ion to 3.3V Efficiency, Power Loss (f_{OSC} = 1MHz)



Li-Ion to 3.3V Efficiency (f_{OSC} = 2MHz)

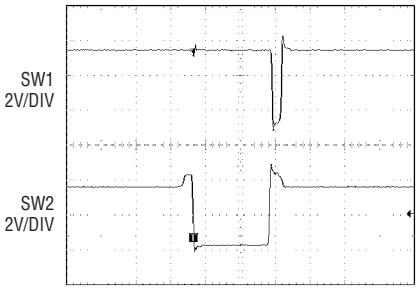


Switch Pins During Buck/Boost



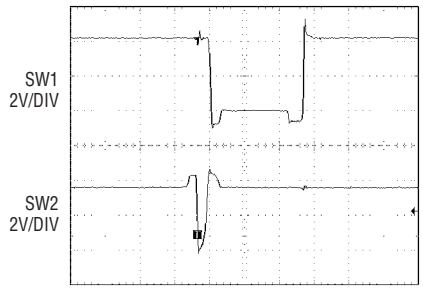
V_{IN} = 3.78V 50ns/DIV
V_{OUT} = 3.3V
I_{OUT} = 250mA

Switch Pins on the Edge of Buck/Boost and Approaching Boost



V_{IN} = 3.42V 50ns/DIV
V_{OUT} = 3.3V
I_{OUT} = 250mA

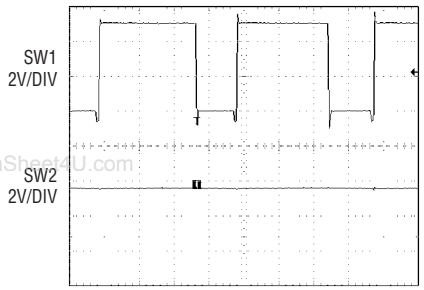
Switch Pins on the Edge of Buck/Boost and Approaching Buck



V_{IN} = 4.15V 50ns/DIV
V_{OUT} = 3.3V
I_{OUT} = 250mA

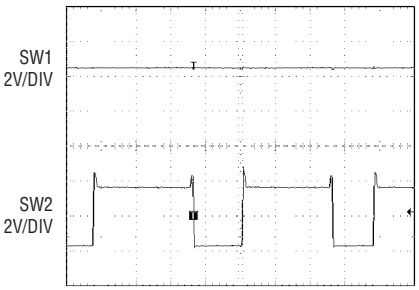
TYPICAL PERFORMANCE CHARACTERISTICS

Switch Pins in Buck Mode



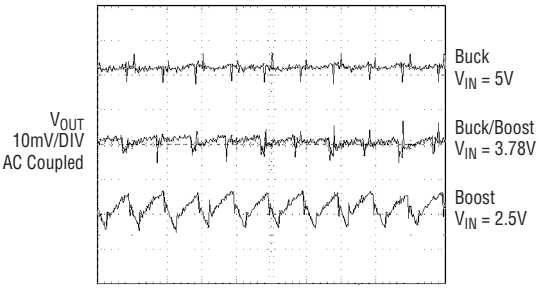
V_{IN} = 5V
V_{OUT} = 3.3V
I_{OUT} = 250mA
250ns/DIV

Switch Pins in Boost Mode



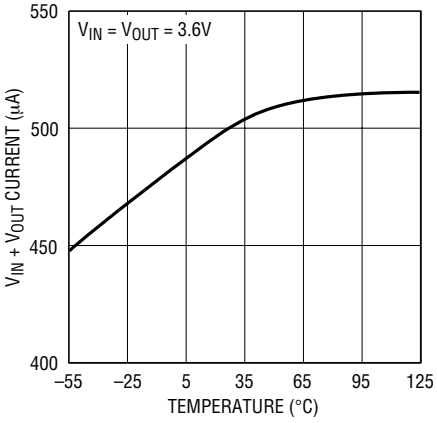
V_{IN} = 2.5V
V_{OUT} = 3.3V
I_{OUT} = 250mA
250ns/DIV

V_{OUT} Ripple During Buck, Buck/Boost and Boost Modes

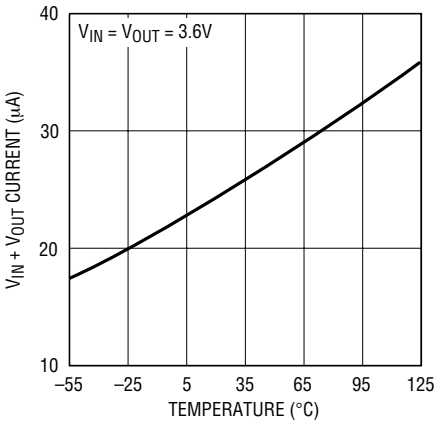


L = 10µH
C_{OUT} = 22µF
I_{OUT} = 250mA
f_{OSC} = 1MHz
1µs/DIV

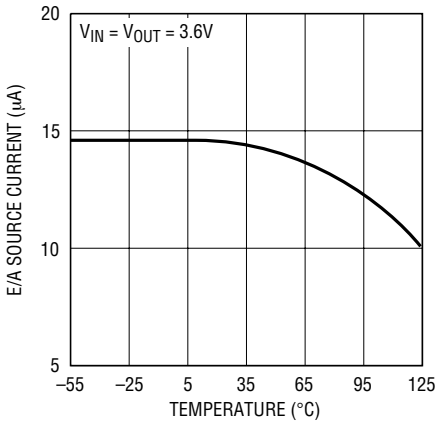
Active Quiescent Current



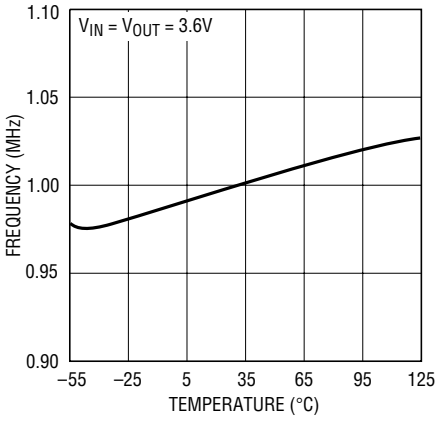
Burst Mode Quiescent Current



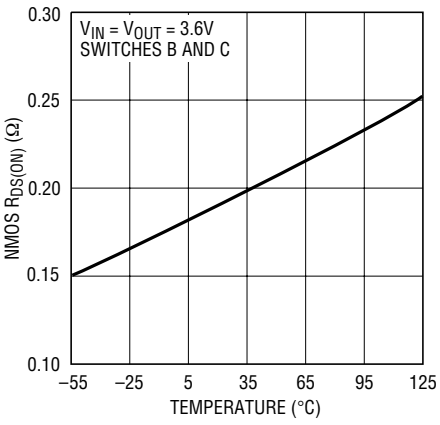
Error Amp Source Current



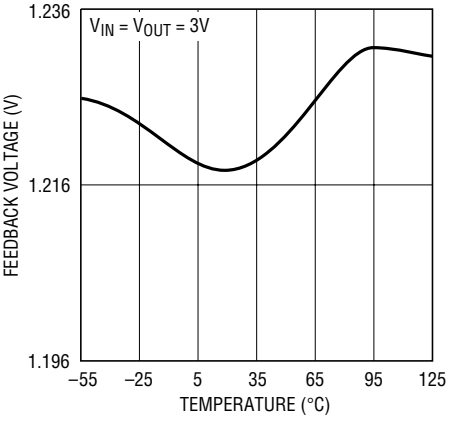
Output Frequency



NMOS $R_{DS(ON)}$

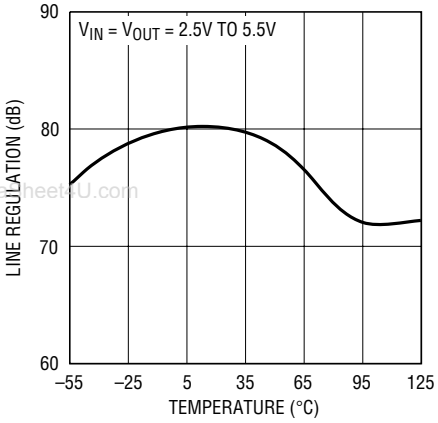


Feedback Voltage

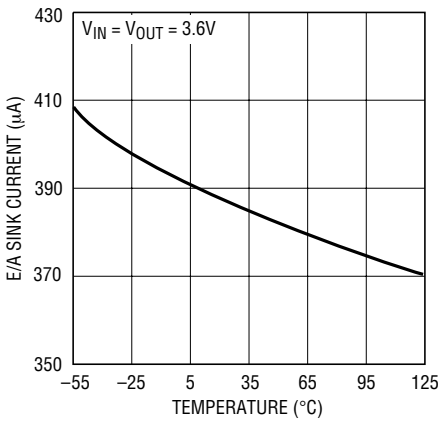


TYPICAL PERFORMANCE CHARACTERISTICS

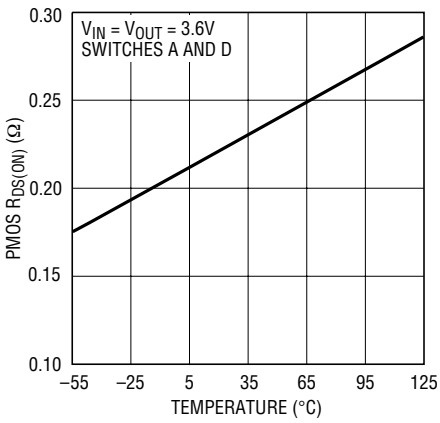
Feedback Voltage Line Regulation



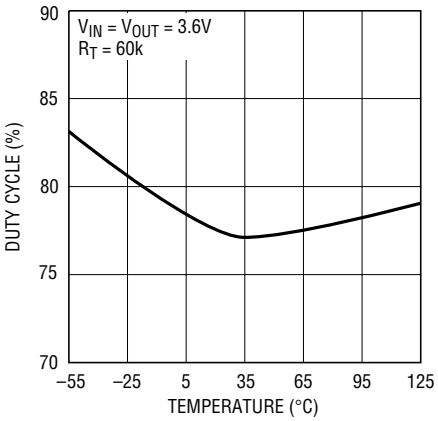
Error Amp Sink Current



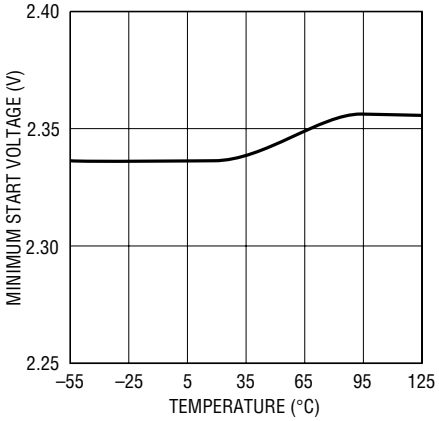
PMOS $R_{DS(ON)}$



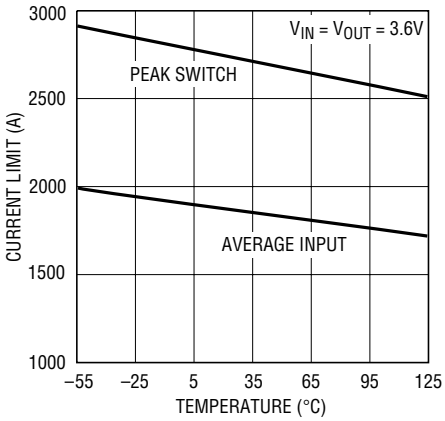
Boost Max Duty Cycle



Minimum Start Voltage



Current Limit



PIN FUNCTIONS

R_T (Pin 1): Timing Resistor to Program the Oscillator Frequency. The programming frequency range is 300kHz to 2MHz.

$$f_{OSC} = \frac{6 \bullet 10^{10}}{R_T} Hz$$

MODE/SYNC (Pin 2): MODE/SYNC = External CLK : Synchronization of the internal oscillator. A clock frequency of twice the desired switching frequency and with a pulse width between 100ns and 2μs is applied. The oscillator free running frequency is set slower than the desired synchronized switching frequency to guarantee sync. The oscillator R_T component value required is given by:

$$R_T = \frac{8 \bullet 10^{10}}{f_{SW}}$$

where f_{SW} = desired synchronized switching frequency.

SW1 (Pin 3): Switch Pin Where the Internal Switches A and B are Connected. Connect inductor from SW1 to SW2. An optional Schottky diode can be connected from SW1 to ground. Minimize trace length to keep EMI down.

SW2 (Pin 4): Switch Pin Where the Internal Switches C and D are Connected. For applications with output voltages over 4.3V, a Schottky diode is required from SW2 to V_{OUT} to ensure the SW pin does not exhibit excess voltage.

GND (Pin 5): Signal and Power Ground for the IC.

V_{OUT} (Pin 6): Output of the Synchronous Rectifier. A filter capacitor is placed from V_{OUT} to GND.

V_{IN} (Pin 7): Input Supply Pin. Internal V_{CC} for the IC. A ceramic bypass capacitor as close to the V_{IN} pin and GND (Pin 5) is required.

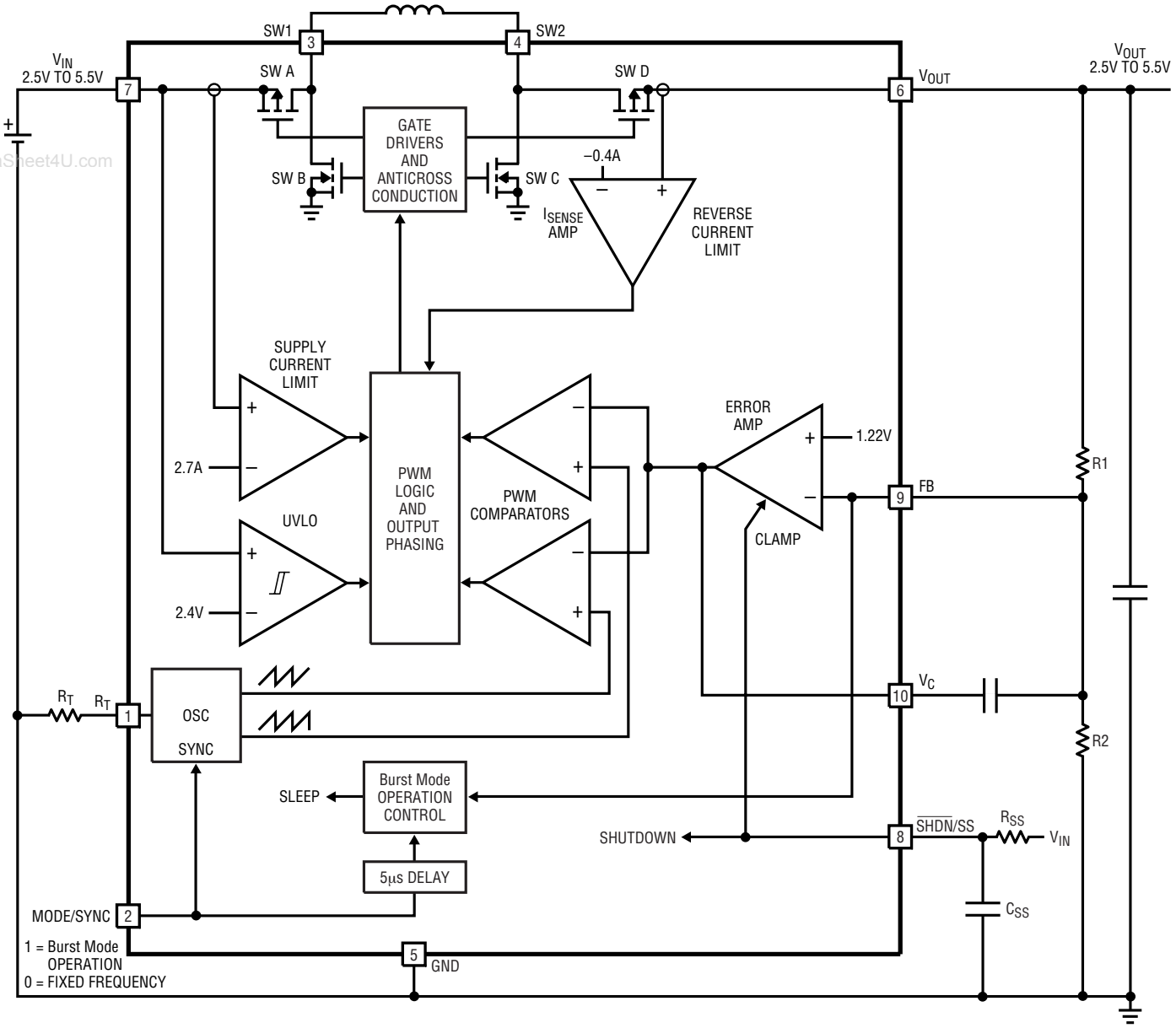
$\overline{SHDN}$/SS (Pin 8): Combined Soft-Start and Shutdown. Grounding this pin shuts down the IC. Tie to >1.5V to enable the IC and >2.5V to ensure the error amp is not clamped from soft-start. An RC from the shutdown command signal to this pin will provide a soft-start function by limiting the rise time of the V_C pin.

FB (Pin 9): Feedback Pin. Connect resistor divider tap here. The output voltage can be adjusted from 2.5V to 5.5V. The feedback reference voltage is typically 1.22V.

V_C (Pin 10): Error Amp Output. A frequency compensation network is connected from this pin to the FB pin to compensate the loop. See the section “Compensating the Feedback Loop” for guidelines.

Exposed Pad (Pin 11, DFN Package Only): Ground. This pin must be soldered to the PCB and electrically connected to ground.

SIMPLIFIED BLOC DIAGRAM



OPERATION

The kB3440 provides high efficiency, low noise power for applications such as portable instrumentation. The Kingbor Technology allows input voltages above, below or equal to the output voltage by properly phasing the output switches. The error amp output voltage on the V_C pin determines the output duty cycle of the switches. Since the V_C pin is a filtered signal, it provides rejection of frequencies from well below the switching frequency. The low $R_{DS(ON)}$, low gate charge synchronous switches provide high frequency pulse width modulation control at high efficiency. Schottky diodes across the synchronous switch D and synchronous switch B are not required, but provide a lower drop during the break-before-make time (typically 15ns). The addition of the Schottky diodes will improve peak efficiency by typically 1% to 2% at 600kHz. High efficiency is achieved at light loads when Burst Mode operation is entered and when the IC's quiescent current is a low 25μA.

LOW NOISE FIXED FREQUENCY OPERATION

Oscillator

The frequency of operation is user programmable and is set through a resistor from the R_T pin to ground where:

$$f = \left(\frac{6e10}{R_T}\right) Hz$$

An internally trimmed timing capacitor resides inside the IC. The oscillator can be synchronized with an external clock applied to the MODE/SYNC pin. A clock frequency of twice the desired switching frequency and with a pulse width between 100ns and 2μs is applied. The oscillator R_T component value required is given by:

$$R_T = \frac{8 \bullet 10^{10}}{f_{SW}}$$

where f_{SW} = desired synchronized switching frequency.

For example to achieve a 1.2MHz synchronized switching frequency the applied clock frequency to the MODE/SYNC pin is set to 2.4MHz and the timing resistor, R_T, is set to 66.5k (closest 1% value).

Error Amp

The error amplifier is a voltage mode amplifier. The loop compensation components are configured around the amplifier to provide loop compensation for the converter. The $\overline{SHDN}$/SS pin will clamp the error amp output, V_C, to provide a soft-start function.

Supply Current Limit

The current limit amplifier will shut PMOS switch A off once the current exceeds 2.7A typical. The current amplifier delay to output is typically 50ns.

Reverse Current Limit

The reverse current limit amplifier monitors the inductor current from the output through switch D. Once a negative inductor current exceeds –400mA typical, the IC will shut off switch D.

Output Switch Control

Figure 1 shows a simplified diagram of how the four internal switches are connected to the inductor, V_{IN}, V_{OUT} and GND. Figure 2 shows the regions of operation for the kB3440 as a function of the internal control voltage, V_{CI}. The V_{CI} voltage is a level shifted voltage from the output of the error amp (V_C pin) (see Figure 5). The output switches are properly phased so the transfer between operation modes is continuous, filtered and transparent to the user. When V_{IN} approaches V_{OUT} the Buck/Boost region is reached where the conduction time of the four switch region is typically 150ns. Referring to Figures 1 and 2, the various regions of operation will now be described.

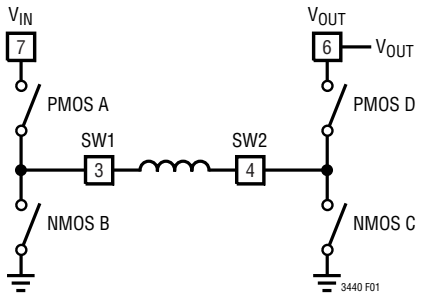


Figure 1. Simplified Diagram of Output Switches

OPERATION

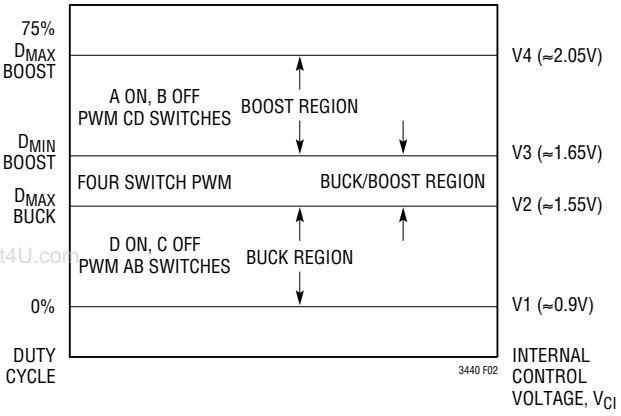


Figure 2. Switch Control vs Internal Control Voltage, V_{CI}

Buck Region ($V_{IN} > V_{OUT}$)

Switch D is always on and switch C is always off during this mode. When the internal control voltage, V_{CI}, is above voltage V1, output A begins to switch. During the off time of switch A, synchronous switch B turns on for the remainder of the time. Switches A and B will alternate similar to a typical synchronous buck regulator. As the control voltage increases, the duty cycle of switch A increases until the maximum duty cycle of the converter in Buck mode reaches D_{MAX_BUCK}, given by:

$$D_{MAX\_BUCK} = 100 - D4_{SW}\ \%$$

where $D4_{SW}$ = duty cycle % of the four switch range.

$$D4_{SW} = (150ns \bullet f) \bullet 100\ \%$$

where f = operating frequency, Hz.

Beyond this point the "four switch," or Buck/Boost region is reached.

Buck/Boost or Four Switch ($V_{IN} \sim V_{OUT}$)

When the internal control voltage, V_{CI}, is above voltage V2, switch pair AD remain on for duty cycle D_{MAX_BUCK}, and the switch pair AC begins to phase in. As switch pair AC phases in, switch pair BD phases out accordingly. When the V_{CI} voltage reaches the edge of the Buck/Boost range, at voltage V3, the AC switch pair completely phase out the BD pair, and the boost phase begins at duty cycle $D4_{SW}$.

The input voltage, V_{IN}, where the four switch region begins is given by:

$$V_{IN} = \frac{V_{OUT}}{1 - (150ns \bullet f)} V$$

The point at which the four switch region ends is given by:

$$V_{IN} = V_{OUT}(1 - D) = V_{OUT}(1 - 150ns \bullet f)\ V$$

Boost Region ($V_{IN} < V_{OUT}$)

Switch A is always on and switch B is always off during this mode. When the internal control voltage, V_{CI}, is above voltage V3, switch pair CD will alternately switch to provide a boosted output voltage. This operation is typical to a synchronous boost regulator. The maximum duty cycle of the converter is limited to 75% typical and is reached when V_{CI} is above V4.

Burst Mode Operation

Burst Mode operation is when the IC delivers energy to the output until it is regulated and then goes into a sleep mode where the outputs are off and the IC is consuming only 40μA. In this mode the output ripple has a variable frequency component that depends upon load current.

During the period where the device is delivering energy to the output, the peak current will be equal to 400mA typical and the inductor current will terminate at zero current for each cycle. In this mode the maximum average output current is given by:

$$I_{OUT(MAX)BURST} \approx \frac{0.1 \bullet V_{IN}}{V_{OUT} + V_{IN}} A$$

Burst Mode operation is user controlled, by driving the MODE/SYNC pin high to enable and low to disable.

The peak efficiency during Burst Mode operation is less than the peak efficiency during fixed frequency because the part enters full-time 4-switch mode (when servicing the output) with discontinuous inductor current as illustrated in Figures 3 and 4. During Burst Mode operation, the control loop is nonlinear and cannot utilize the control

OPERATION

voltage from the error amp to determine the control mode, therefore full-time 4-switch mode is required to maintain the Buck/Boost function. The efficiency below 1mA becomes dominated primarily by the quiescent current and not the peak efficiency. The equation is given by:

$$\text{Efficiency Burst} \approx \frac{(\eta bm) \bullet I_{LOAD}}{25\mu A + I_{LOAD}}$$

where (ηbm) is typically 79% during Burst Mode operation for an ESR of the inductor of 50mΩ. For 200mΩ of inductor ESR, the peak efficiency (ηbm) drops to 75%.

Burst Mode Operation to Fixed Frequency Transient Response

When transitioning from Burst Mode operation to fixed frequency, the system exhibits a transient since the modes of operation have changed. For most systems this transient is acceptable, but the application may have stringent input current and/or output voltage requirements that dictate a broad-band voltage loop to minimize the transient. Lowering the DC gain of the loop will facilitate the task (10M FB to V_C) at the expense of DC load regulation. Type 3 compensation is also recommended to broad band the loop and roll off past the two pole response of the LC of the converter (see Closing the Feedback Loop).

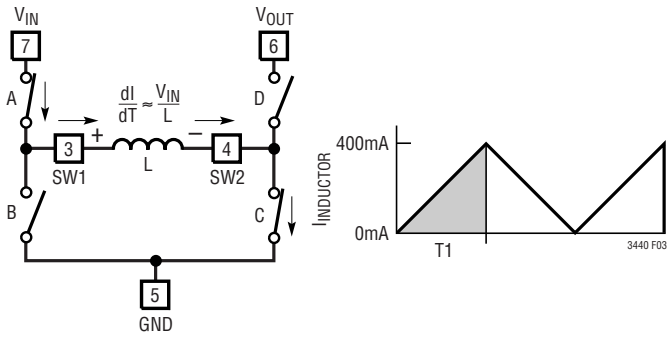


Figure 3. Inductor Charge Cycle During Burst Mode Operation

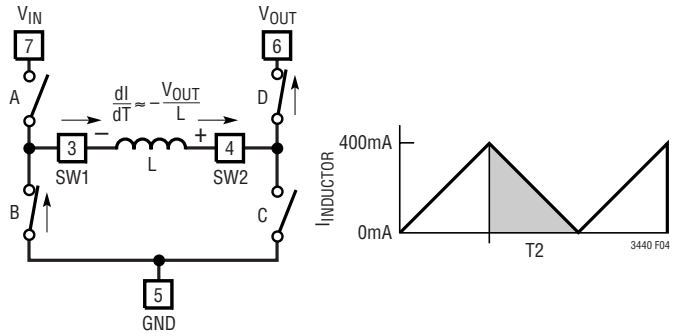


Figure 4. Inductor Discharge Cycle During Burst Mode Operation

OPERATION

SOFT-START

The soft-start function is combined with shutdown. When the SHDN/SS pin is brought above typically 1V, the IC is enabled but the EA duty cycle is clamped from the V_C pin.

A detailed diagram of this function is shown in Figure 5. The components R_{SS} and C_{SS} provide a slow ramping voltage on the SHDN/SS pin to provide a soft-start function.

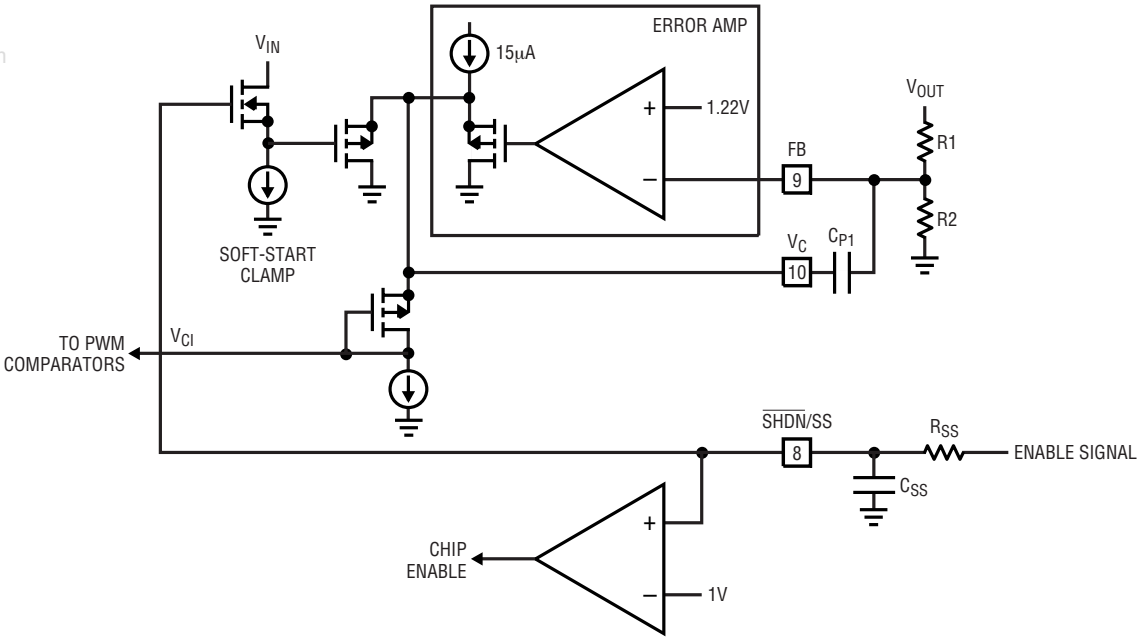


Figure 5. Soft-Start Circuitry

APPLICATIONS INFORMATION

COMPONENT SELECTION

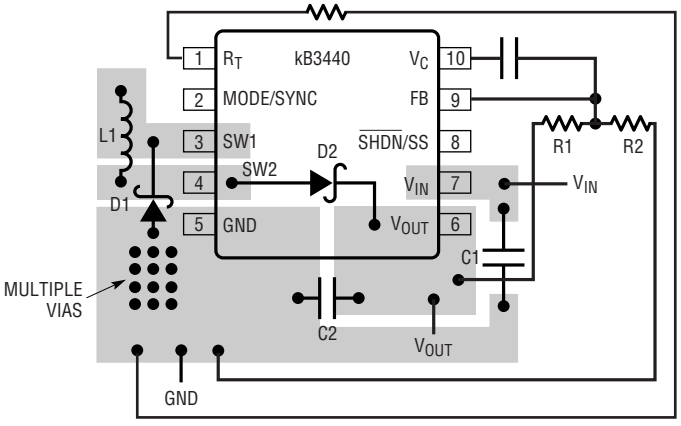


Figure 6. Recommended Component Placement. Traces Carrying High Current are Direct. Trace Area at FB and V_C Pins are Kept Low. Lead Length to Battery Should be Kept Short

Inductor Selection

The high frequency operation of the kB3440 allows the use of small surface mount inductors. The inductor current ripple is typically set to 20% to 40% of the maximum inductor current. For a given ripple the inductance terms are given as follows:

$$L > \frac{V_{IN(MIN)}^{2} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{f \bullet I_{OUT(MAX)} \bullet Ripple \bullet V_{OUT}^{2}}\ \mu H,$$

$$L > \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right)}{f \bullet I_{OUT(MAX)} \bullet Ripple \bullet V_{IN(MAX)}}\ \mu H$$

where f = operating frequency, MHz

APPLICATIONS INFORMATION

Ripple = allowable inductor current ripple (e.g., 0.2 = 20%)

$V_{IN(MIN)}$ = minimum input voltage, V

$V_{IN(MAX)}$ = maximum input voltage, V

V_{OUT} = output voltage, V

$I_{OUT(MAX)}$ = maximum output load current

For high efficiency, choose an inductor with a high frequency core material, such as ferrite, to reduce core loses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors usually do not have enough core to support the peak inductor currents in the 1A to 2A region. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor. See Table 1 for suggested components and Table 2 for a list of component suppliers.

Table 1. Inductor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
Coilcraft	(847) 639-6400	(847) 639-1469	www.coilcraft.com
Coiltronics	(561) 241-7876	(561) 241-9339	www.coiltronics.com
Murata	USA: (814) 237-1431 (800) 831-9172	USA: (814) 238-0490	www.murata.com
Sumida	USA: (847) 956-0666 Japan: 81(3) 3607-5111	 (847) 956-0702 81(3) 3607-5144	www.japanlink.com/ sumida

Output Capacitor Selection

The bulk value of the capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The steady state ripple due to charge is given by:

$$\%Ripple\_Boost = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right) \bullet 100}{C_{OUT} \bullet V_{OUT}^2 \bullet f}\%$$

$$\%Ripple\_Buck = \frac{I_{OUT(MAX)} \bullet \left(V_{IN(MAX)} - V_{OUT}\right) \bullet 100}{C_{OUT} \bullet V_{IN(MAX)} \bullet V_{OUT} \bullet f}\%$$

where C_{OUT} = output filter capacitor, F

The output capacitance is usually many times larger in order to handle the transient response of the converter. For a rule of thumb, the ratio of the operating frequency to the unity-gain bandwidth of the converter is the amount the output capacitance will have to increase from the above calculations in order to maintain the desired transient response.

The other component of ripple is due to the ESR (equivalent series resistance) of the output capacitor. Low ESR capacitors should be used to minimize output voltage ripple. For surface mount applications, Taiyo Yuden ceramic capacitors, AVX TPS series tantalum capacitors or Sanyo POSCAP are recommended.

Input Capacitor Selection

Since the V_{IN} pin is the supply voltage for the IC it is recommended to place at least a 4.7μF, low ESR bypass capacitor.

Table 2. Capacitor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
AVX	(803) 448-9411	(803) 448-1943	www.avxcorp.com
Sanyo	(619) 661-6322	(619) 661-1055	www.sanyovideo.com
Taiyo Yuden	(408) 573-4150	(408) 573-4159	www.t-yuden.com

Optional Schottky Diodes

To achieve a 1%-2% efficiency improvement above 50mW, Schottky diodes can be added across synchronous switches B (SW1 to GND) and D (SW2 to V_{OUT}). The Schottky diodes will provide a lower voltage drop during the break-before-make time (typically 15ns) of the NMOS to PMOS transition. General purpose diodes such as a 1N914 are not recommended due to the slow recovery times and will compromise efficiency. If desired a large Schottky diode, such as an MBRM120T3, can be used from SW2 to V_{OUT}. A low capacitance Schottky diode is recommended from GND to SW1 such as a Phillips PMEG2010EA or equivalent.

APPLICATIONS INFORMATION

Output Voltage > 4.3V

A Schottky diode from SW to V_{OUT} is required for output voltages over 4.3V. The diode must be located as close to the pins as possible in order to reduce the peak voltage on SW2 due to the parasitic lead and trace inductance.

Input Voltage > 4.5V

For applications with input voltages above 4.5V which could exhibit an overload or short-circuit condition, a 2Ω/1nF series snubber is required between the SW1 pin and GND. A Schottky diode such as the Phillips PMEG2010EA or equivalent from SW1 to V_{IN} should also be added as close to the pins as possible. For the higher input voltages V_{IN} bypassing becomes more critical, therefore, a ceramic bypass capacitor as close to the V_{IN} and GND pins as possible is also required.

Operating Frequency Selection

There are several considerations in selecting the operating frequency of the converter. The first is, what are the sensitive frequency bands that cannot tolerate any spectral noise? For example, in products incorporating RF communications, the 455kHz IF frequency is sensitive to any noise, therefore switching above 600kHz is desired. Some communications have sensitivity to 1.1MHz and in that case a 2MHz converter frequency may be employed.

Other considerations are the physical size of the converter and efficiency. As the operating frequency goes up, the inductor and filter capacitors go down in value and size. The trade off is in efficiency since the switching losses due to gate charge are going up proportional with frequency.

Additional quiescent current due to the output switches GATE charge is given by:

Buck: $500e^{-12} \bullet V_{IN} \bullet F$

Boost: $250e^{-12} \bullet (V_{IN} + V_{OUT}) \bullet F$

Buck/Boost: $F \bullet (750e^{-12} \bullet V_{IN} + 250e^{-12} \bullet V_{OUT})$

where F = switching frequency

Closing the Feedback Loop

The kB3440 incorporates voltage mode PWM control. The control to output gain varies with operation region (Buck, Boost, Buck-Boost), but is usually no greater than 15. The output filter exhibits a double pole response is given by:

$$f_{FILTER\_POLE} = \frac{1}{2 \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}} \text{ Hz (in Buck mode)}$$

$$f_{FILTER\_POLE} = \frac{V_{IN}}{2\pi \bullet \sqrt{L \bullet V_{OUT}}} \text{ Hz (in Boost mode)}$$

where C_{OUT} is the output filter capacitor.

The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}} \text{Hz}$$

where R_{ESR} is the capacitor equivalent series resistance.

A troublesome feature in Boost mode is the right-half plane zero (RHP), and is given by:

$$f_{RHPZ} = \frac{V_{IN}^{2}}{2 \bullet \pi \bullet I_{OUT} \bullet L \bullet V_{OUT}} \text{Hz}$$

The loop gain is typically rolled off before the RHP zero frequency.

A simple Type I compensation network can be incorporated to stabilize the loop but at a cost of reduced bandwidth and slower transient response. To ensure proper phase margin, the loop requires to be crossed over a decade before the LC double pole.

The unity-gain frequency of the error amplifier with the Type I compensation is given by:

$$f_{UG} = \frac{1}{2 \bullet \pi \bullet R1 \bullet CP1} \text{Hz}$$

Most applications demand an improved transient response to allow a smaller output filter capacitor. To achieve a higher bandwidth, Type III compensation is required. Two zeros are required to compensate for the double-pole response.

APPLICATIONS INFORMATION

$$f_{POLE1} \approx \frac{1}{2 \bullet \pi \bullet 32e^3 \bullet R1 \bullet C_{P1}} Hz$$

Which is extremely close to DC

$$f_{ZERO1} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{P1}} Hz$$

$$f_{ZERO2} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{Z1}} Hz$$

$$f_{POLE2} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{P2}} Hz$$

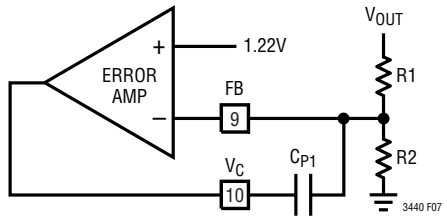


Figure 7. Error Amplifier with Type I Compensation

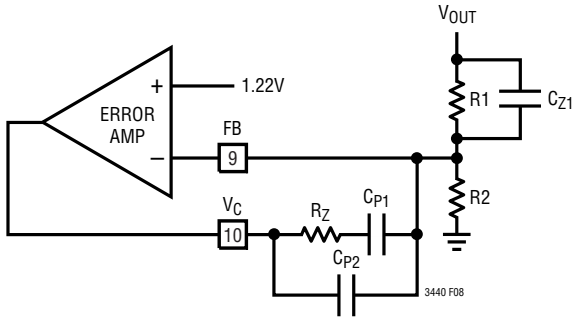


Figure 8. Error Amplifier with Type III Compensation

Short-Circuit Improvements

The kB3440 is current limited to 2.7A peak to protect the IC from damage. At input voltages above 4.5V a current limit condition may produce undesirable voltages to the IC due to the series inductance of the package, as well as the traces and external components. Following the recommendations for output voltage >4.3V and input voltage >4.5V will improve this condition. Additional short-circuit protection can be accomplished with some external circuitry.

In an overload or short-circuit condition the kB3440 voltage loop opens and the error amp control voltage on the V_C pin slams to the upper clamp level. This condition forces boost mode operation in order to attempt to provide more output voltage and the IC hits a peak switch current limit of 2.7A. When switch current limit is reached switches B and D turn on for the remainder of the cycle to reverse the volts • seconds on the inductor. Although this prevents current run away, this condition produces four switch operation producing a current foldback characteristic and the average input current drops. The IC is trimmed to guarantee greater than 1A average input current to meet the maximum load demand, but in a short-circuit or overload condition the foldback characteristic will occur producing higher peak switch currents. To minimize this affect during this condition the following circuits can be utilized.

Restart Circuit

For a sustained short-circuit the circuit in Figure 9 will force a soft-start condition. The only design constraint is that R2/C2 time constant must be longer than the soft-start components R1/C1 to ensure start-up.

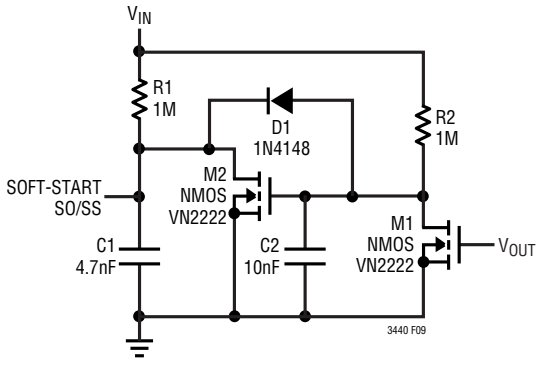


Figure 9. Soft-Start Reset Circuitry for a Sustained Short-Circuit

APPLICATIONS INFORMATION

Simple Average Input Current Control

A simple average current limit circuit is shown in Figure 10. Once the input current of the IC is above approximately 1A, Q1 will start sourcing current into the FB pin and lower the output voltage to maintain the average input current. Since the voltage loop is utilized to perform average current limit, the voltage control loop is maintained and the V_C voltage does not slam. The averaging function of current comes from the fact that voltage loop compensation is also used with this circuit.

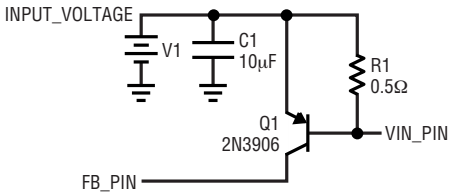
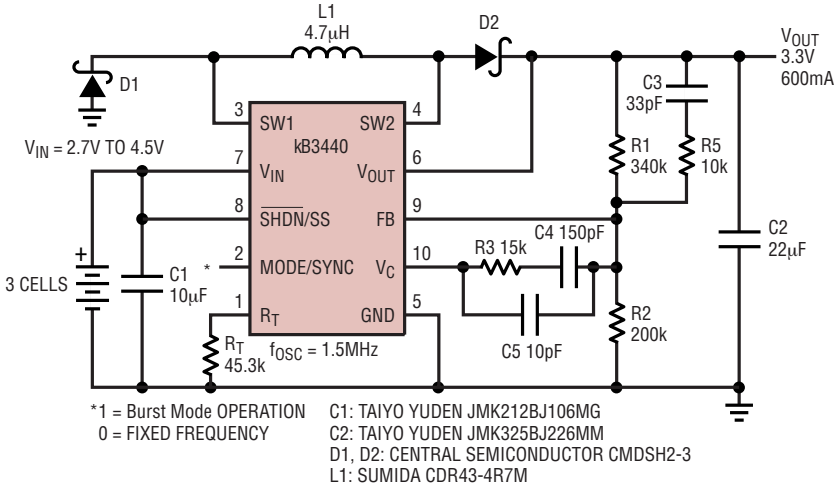


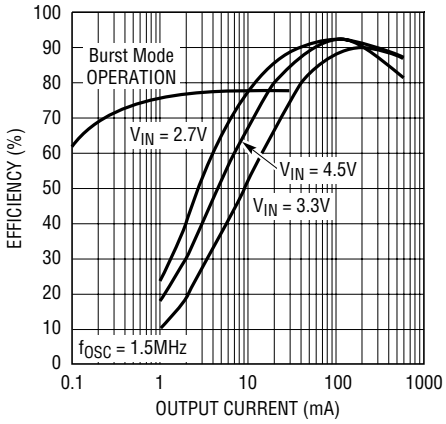
Figure 10. Simple Input Current Control Utilizing the Voltage Loop

TYPICAL APPLICATION

3-Cell to 3.3V at 600mA Converter

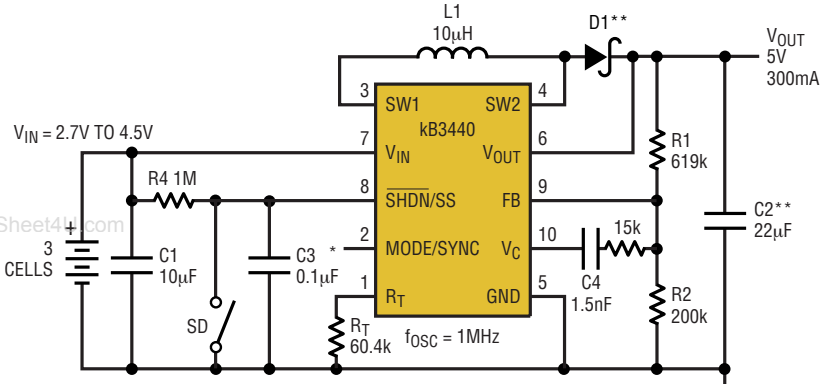


3-Cell to 3.3V Efficiency



TYPICAL APPLICATION

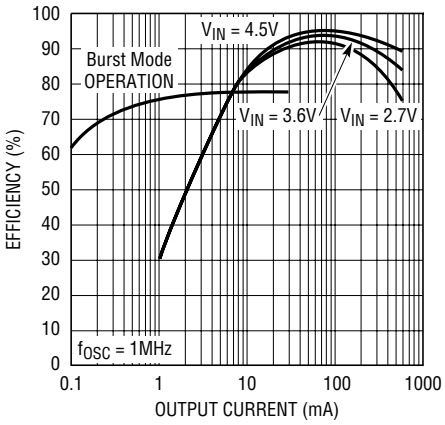
3-Cell to 5V Boost Converter with Output Disconnect



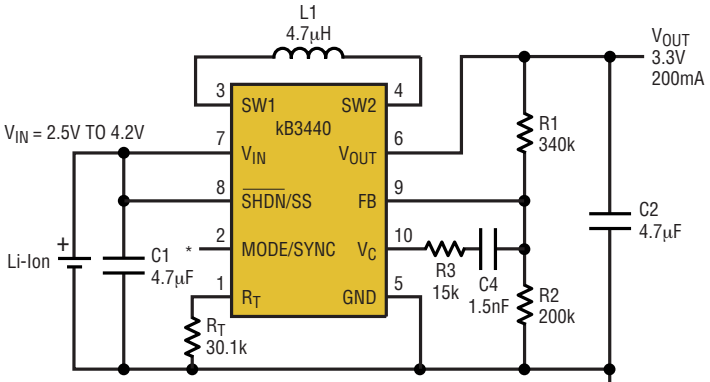
*1 = Burst Mode OPERATION
0 = FIXED FREQUENCY
** LOCATE COMPONENTS AS CLOSE TO IC AS POSSIBLE

C1: TAIYO YUDEN JMK212BJ106MG
C2: TAIYO YUDEN JMK325BJ226MM
D1: ON SEMICONDUCTOR MBRM120T3
L1: SUMIDA CDRH4D28-100

3-Cell to 5V Boost Efficiency



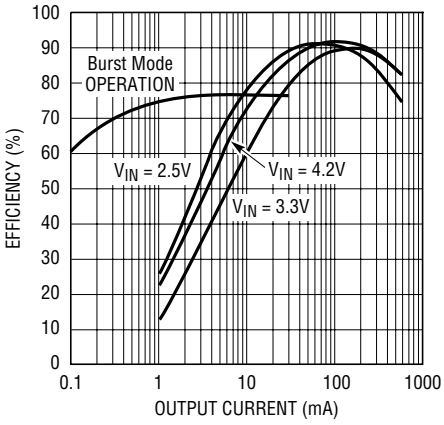
Low Profile (<1.1mm) Li-Ion to 3.3V at 200mA Converter



*1 = Burst Mode OPERATION
0 = FIXED FREQUENCY
fOSC = 2MHz

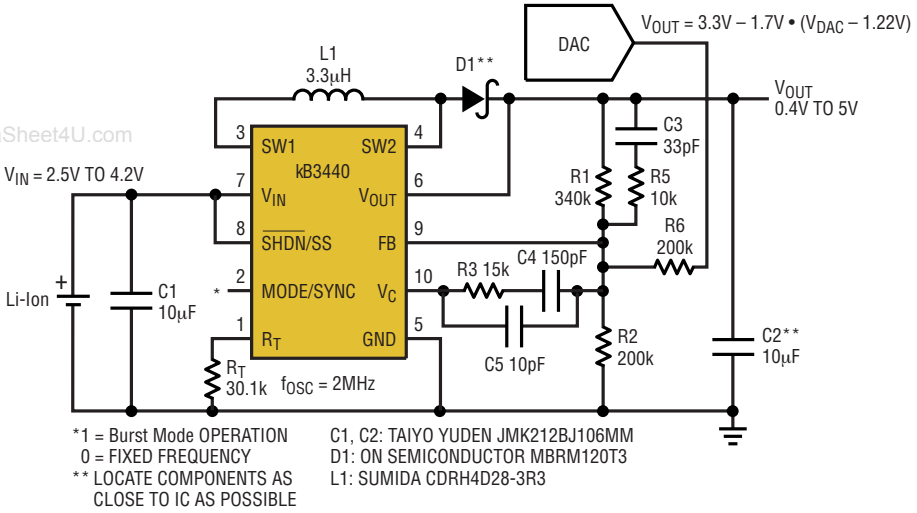
C1: TAIYO YUDEN JMK212BJ475MG
C2: TAIYO YUDEN JMK212BJ475MG
L1: COILCRAFT LPO1704-472M

Efficiency



TYPICAL APPLICATION

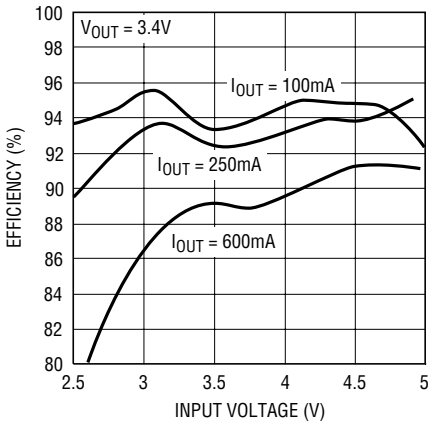
WCDMA Power Amp Power Supply with Dynamic Voltage Control



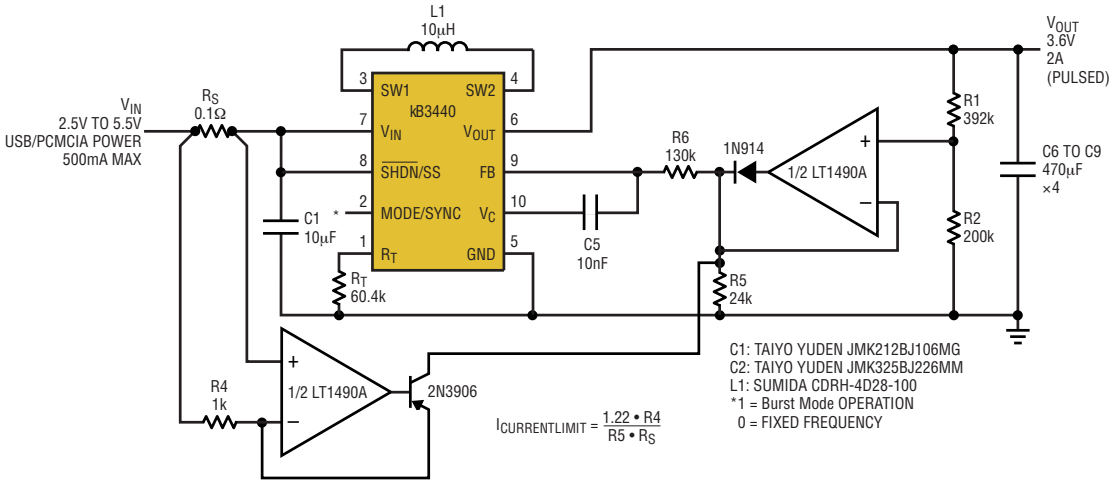
*1 = Burst Mode OPERATION
0 = FIXED FREQUENCY
** LOCATE COMPONENTS AS CLOSE TO IC AS POSSIBLE

C1, C2: TAIYO YUDEN JMK212BJ106MM
D1: ON SEMICONDUCTOR MBRM120T3
L1: SUMIDA CDRH4D28-3R3

Efficiency of the WCDMA Power Amp Power Supply



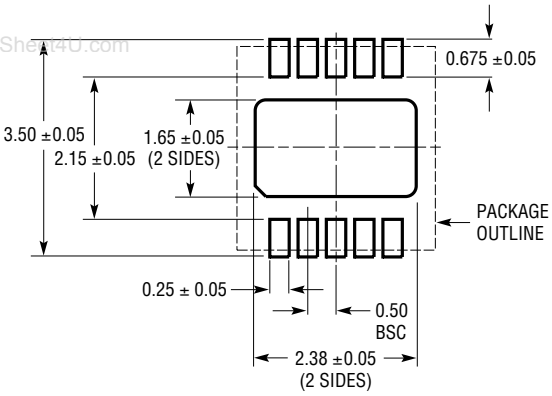
GSM Modem Powered from USB or PCMCIA with 500mA Input Current Limit



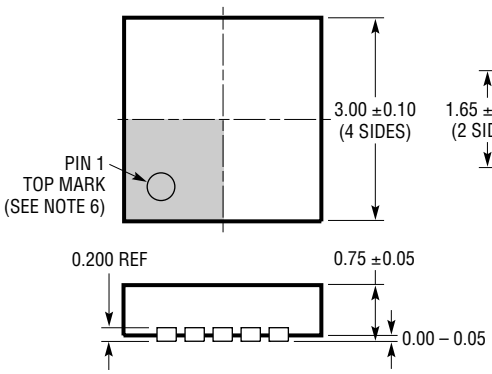
C1: TAIYO YUDEN JMK212BJ106MG
C2: TAIYO YUDEN JMK325BJ226MM
L1: SUMIDA CDRH-4D28-100
*1 = Burst Mode OPERATION
0 = FIXED FREQUENCY

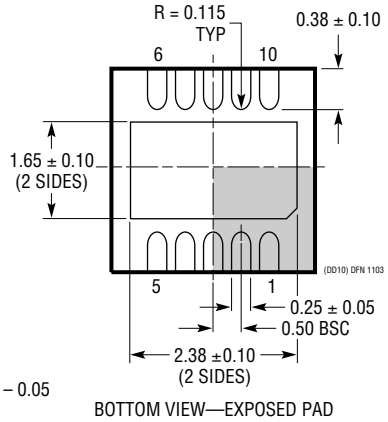
PACAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



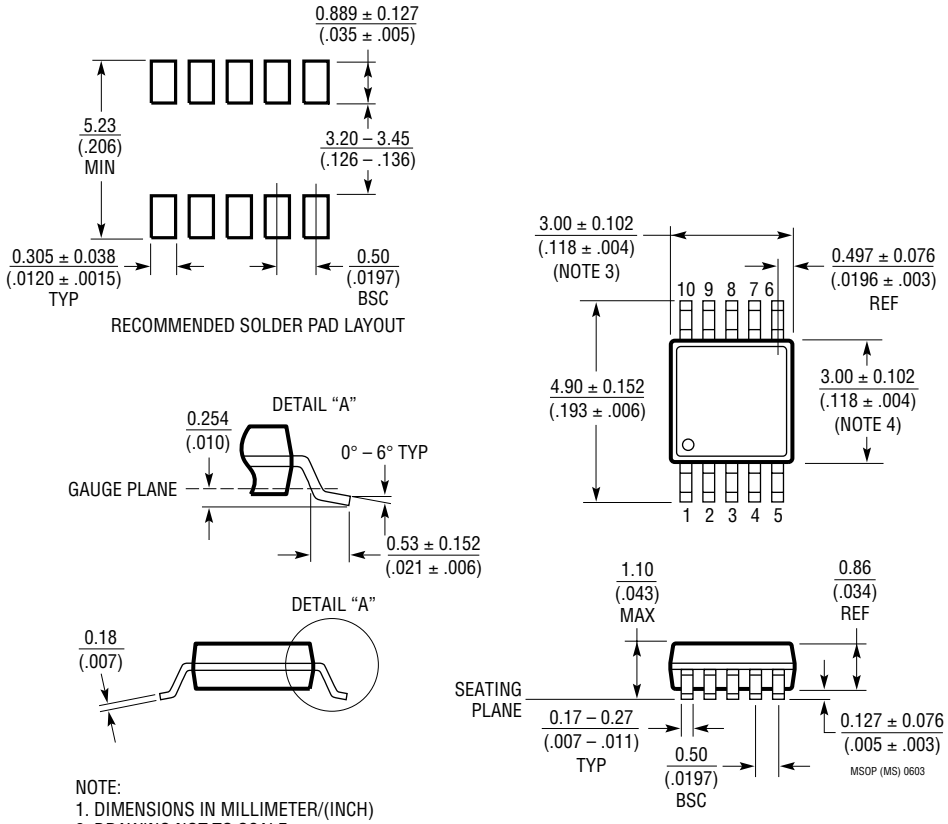


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE KB WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACAGE DESCRIPTION

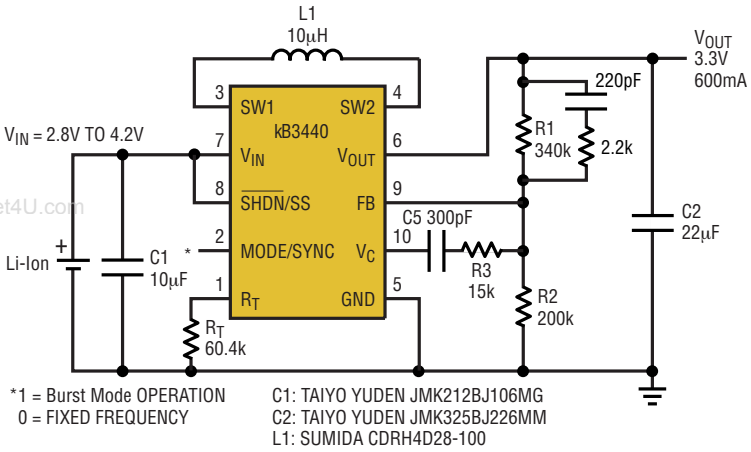
MS Package
10-Lead Plastic MSOP



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Li-Ion to 3.3V at 600mA Buck-Boost Converter



Efficiency