KBC1102

Legacy Free Mobile KBC with SFI, ADC and DAC with SMSC SentinelAlert!™

PRODUCT FEATURES

Data Brief

- 3.3V Operation with 5V Tolerant Buffers
- ACPI 1.0b/2.0 and PC99a/PC2001 Compliant
- LPC Interface with Clock Run Support
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - 15 Direct IRQs
  - ACPI SCI Interface
  - nSMI
  - Shadowed write only registers
- LPC/Firmware Hub Host Flash Interface
  - Single Byte FWH Memory Read and FWH Memory Write Support
  - FWH ID Support
  - 16MB FWH Flash and Register Addressing, 128K Legacy BIOS Addressing
  - Single Byte LPC Memory Read and LPC Memory Write Support
- Serial Peripheral Interface (SPI)
  - Dual Ported Controller with Keeper Circuit
- 8 MByte Shared FlashROM Interface (SFI)
  - 8051/Host CPU Hardware Arbitrated Interface
  - 0.5 - 8MB - Host System BIOS & 8051 Keyboard
  - 8051 64KB Code Space Accessible as Separate 32KB Pages in Flash
  - Low-Power Flash Access Modes
  - 8051-Programmable Flash Access Protection
    - Read/Write/No-Access Protection
    - Variable Bank Sizes
- Host Flash Address Redirection for Recovery
- Serial Flash Programming Interface
- Two Power Planes
  - Low Standby Current in Sleep Mode
  - Main powered blocks power supplied by standby power plane and controlled by power management signals
- 3-Port ACPI Embedded Controller Interface
- Configuration Register Set
  - Compatible with ISA Plug-and-Play Standard (Version 1.0a)
  - Four Pin Selectable Addressing Options
  - 8051-Programmable Base Address
- High-Performance Embedded 8051 Keyboard and System Controller
  - Provides System Power Management
  - System Watch Dog Timer (WDT)
  - 8042 Style Host Interface Relocatable to 480 Different Base I/O Addresses
  - Supports Interrupt and Polling Access
  - Interrupt Accelerator
  - 512 Bytes Data RAM
  - 2 Kilobytes Scratch ROM/RAM
  - On-Chip Memory-Mapped Control Registers
  - Up to 18x8 Keyboard Scan Matrix
  - Two 16 Bit Timer/Counters
  - Eleven 8051 Interrupt Sources
  - Thirty-Two 8-Bit, Host/8051 Mailbox Registers
  - Thirty-six Maskable Hardware Wake-Up Events
  - Fast GATEA20
  - Fast CPU_RESET
  - Multiple Clock Sources and Operating Frequencies up to 32MHz
  - IDLE and SLEEP Modes
  - Low Power Fail-Safe Ring Oscillator ±10% Accuracy
  - Hibernation Timer with programmable wake-up from 0.5ms to 128 minutes
  - 8051-Driven 16550A UART
    - 16-Byte Send/Receive FIFOs
    - External Baud Clock Option
  - Power-Fail Status Register
- Battery Backed Resources
  - 32KHz clock generator
  - 1 Week Wakeup timer
- Two 8584-Style SMBus Controllers
  - 8051 Host Interface Logic Allows Master or Slave Operation
  - Controllers are Fully Operational on Standby Power
  - One Controller with one Port

- Three independent Hardware Driven PS/2 Ports
  - Fully functional on Main and/or Suspend Power
  - PS/2 edge Wake Capable
  - Wake on specific mouse protocol
  - Wake on specific keyboard protocol
- 92 General Purpose I/O Pins
- Four Programmable Pulse-Width Modulator Outputs
  - Multiple clock Sources and Independent Clock Rates
  - 8 Bit Duty Cycle Granularity
- Three Fan Tachometer Inputs
- Four Programmable 16-bit Counter/Timers
- Direct Battery Management with SMSC SentinelAlert!
  - Analog to Digital Converter with
    - 8 channels, 8b/10b conversion
    - 20ms conversion time for 8 channels
  - Digital to Analog Converter with SMSC SentinelAlert!
    - 3 channels, 8b conversion
    - 1.5ms conversion time for 3 channels
  - 2-GPIO's with SMSC SentinelAlert!
  - 2-Single pin SMSC BudgetBus Sensor Interface Ports
  - HW_PROTECT# output thermal event indication
- MCU Serial Debug Port
- Integrated Standby Power Reset Generator
- 156 Pin DQFN Green, Lead-Free Package

ORDER NUMBER(S): KBC1102-AJZS FOR 156 PIN, DQFN PACKAGE (GREEN, LEAD-FREE)

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General Description

The KBC1102 is an integrated Keyboard/System Management Controller which incorporates a high-performance 8051 Micro-Controller, an LPC Bus Interface which provides a Firmware Hub Interface and integrated Super I/O/LPC Resources. The KBC1102 is powered by two separate supply planes (VCC1, VCC0) to provide “instant on” and sophisticated system power management functions. The KBC1102 power control circuitry supports multiple low power-down modes.

The KBC1102 incorporates a Direct Battery Management (DBM) with SMSC SentinelAlert! accessible by the 8051. Together with external remote temperature sensor(s) can provide complete Analog Monitoring & Control System. The KBC1102 DBM includes an 8 channel ADC, a 3 channel DAC with SMSC SentinelAlert! and up to 2 SMSC SentinelAlert! GPIO's, two channel one-pin Temperature Sensor Communication Links, and a hardware protect output that requires no programming or 8051 intervention to operate.

The KBC1102 incorporates a Standby Power Reset Generator (RESGEN) which monitors the VCC1 power input and generates the internal VCC1 power on reset for the KBC1102. The KBC1102 also outputs VCC1RST# which can be used to reset the Flash memory on the Shared Flash Interface (SFI).

Package Outline

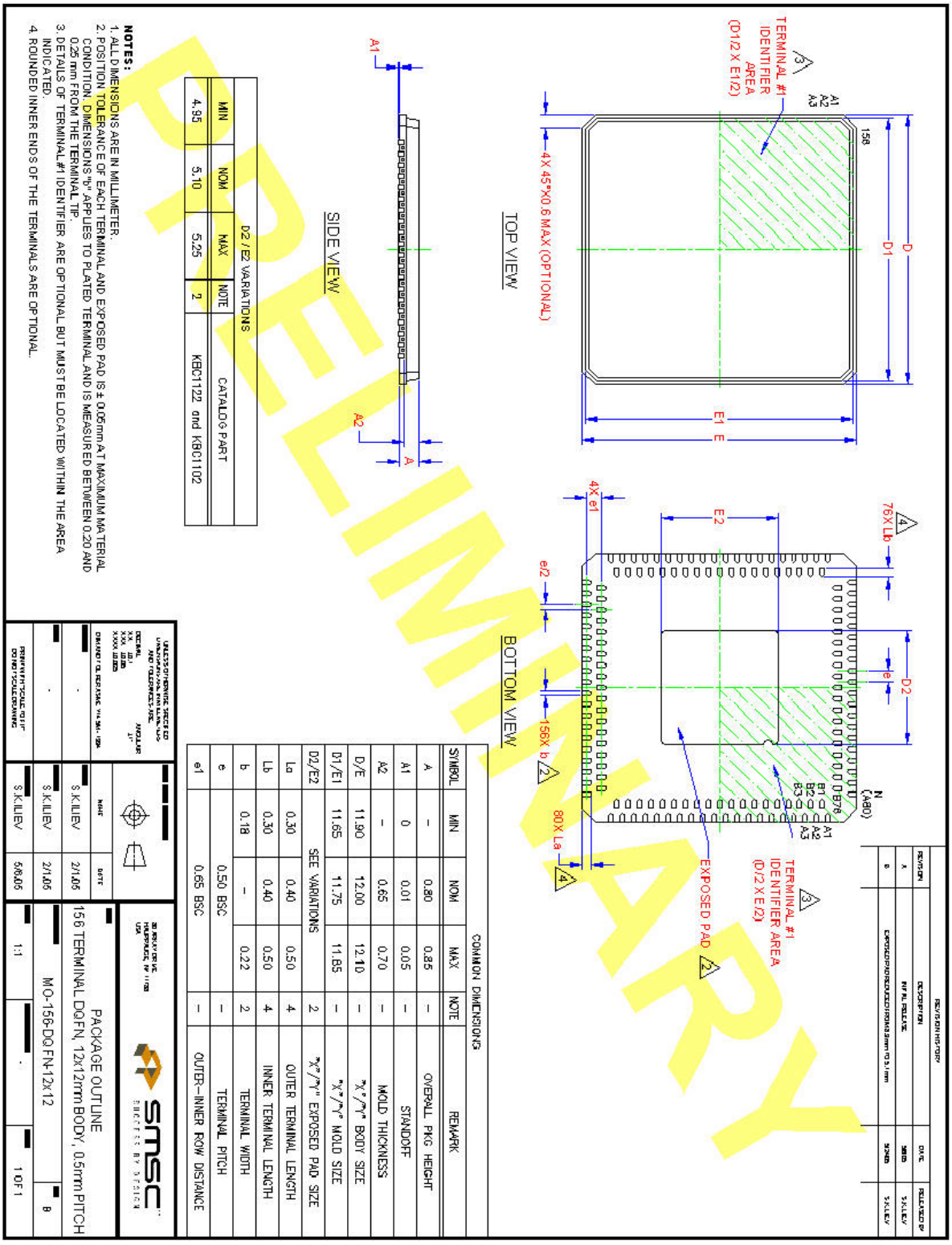

Figure 1 156 Pin DQFN Package Outline