

**SPECIFICATION
FOR
LCD Module
KD026LQTMA008**

MODULE:	KD026LQTMA008
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2017.04.22

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

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常 备 库 存	长 期 供 货	支持小量	品 种 齐 全	
Stock For Sale	Long Time supply	NO MOQ	In Full Range	

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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 2.6" TFT-LCD contains 320x240 pixels, and can display up to 65K/262K colors.

* Features

- Low Input Voltage: 3.3V(TYP)
- Display Colors of TFT LCD: 65K/262K colors
- Interface: 8/9/16/18Bit MCU Interface
3/4SPI+16/18Bit RGB Interface
3-line/4-line Serial Interface

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	52.80(H)*39.60 (V) (2.6inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	320(RGB)*240	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.165(H)*0.165(V)	mm	-
Viewing angle	6:00	o'clock	-
Controller IC	ILI9342C	-	-
Display mode	Transmissive/ Normally White	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		60.30		mm	-
	Vertical(V)		51.15		mm	-
	Depth(D)		2.60		mm	-
Weight			TBD		g	-

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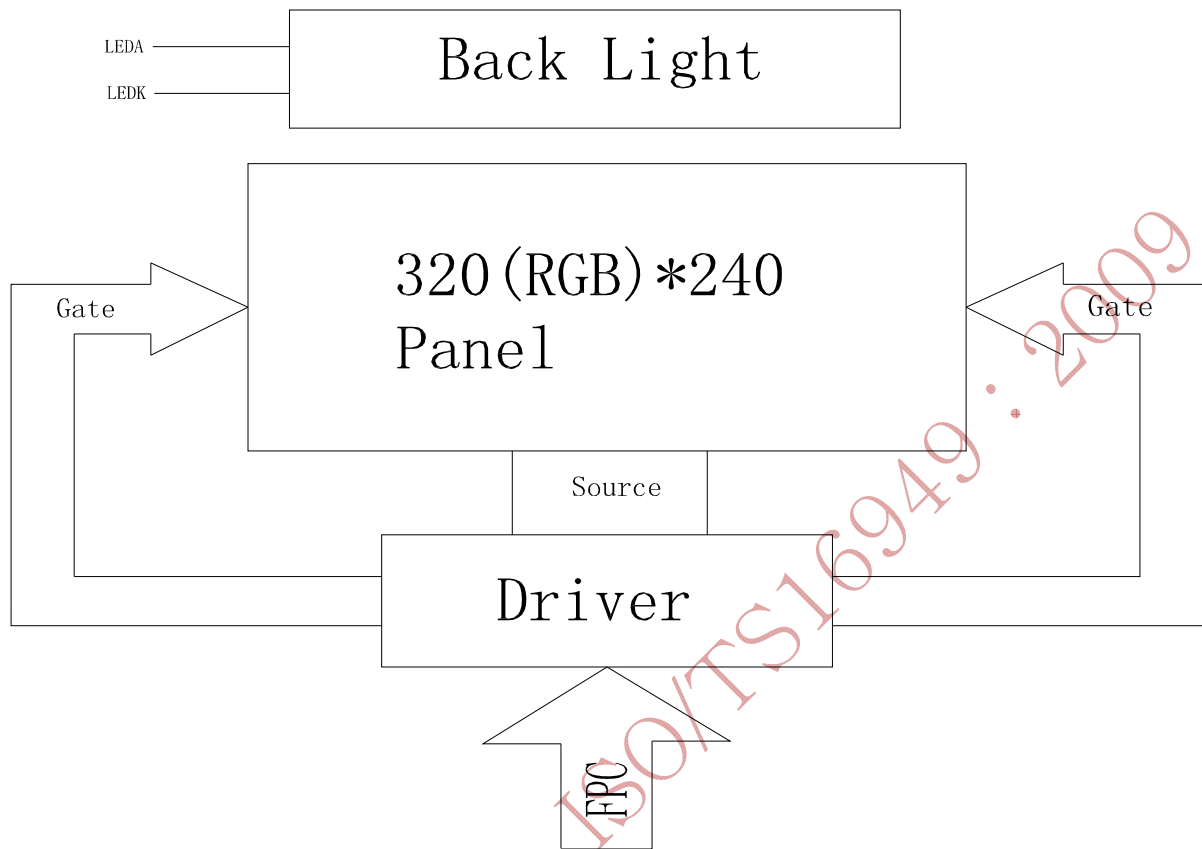
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Long Time supply

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NO MOQ

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1. Block Diagram



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3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O																																								
1	GND	Ground.	P																																								
2	GND	Ground.	P																																								
3	IOVCC	Supply voltage(1.65-3.3V)	P																																								
4	VCI	Supply voltage(3.3V).	P																																								
5	IM3	<table><tr><th colspan="5">Interface Selection</th></tr><tr><th>IM3</th><th>IM2</th><th>IM0</th><th>Interface type</th><th>DB Pin in use</th></tr><tr><td>0</td><td>0</td><td>0</td><td>DBI Tyb_ 8-bit interface</td><td>DB7-DB0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>DBI Tyb_ 16-bit interface</td><td>DB15-DB0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>DBI Tyb_ 9-bit interface</td><td>DB8-DB0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>DBI Tyb_ 18-bit interface</td><td>DB17-DB0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>3-Wire 9 BIT data serial interface.</td><td>SDA SCL CS</td></tr><tr><td>1</td><td>1</td><td>1</td><td>4-Wire 8 BIT data serial interface</td><td>SDA SCL CS RS</td></tr></table>	Interface Selection					IM3	IM2	IM0	Interface type	DB Pin in use	0	0	0	DBI Tyb_ 8-bit interface	DB7-DB0	0	1	0	DBI Tyb_ 16-bit interface	DB15-DB0	0	0	1	DBI Tyb_ 9-bit interface	DB8-DB0	0	1	1	DBI Tyb_ 18-bit interface	DB17-DB0	1	0	1	3-Wire 9 BIT data serial interface.	SDA SCL CS	1	1	1	4-Wire 8 BIT data serial interface	SDA SCL CS RS	I
Interface Selection																																											
IM3	IM2		IM0	Interface type	DB Pin in use																																						
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1	1	1	4-Wire 8 BIT data serial interface	SDA SCL CS RS																																							
6	IM2		I																																								
7	IM0		I																																								
8	SDA	Serial input signal.The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VCI or GND.	I																																								
9	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I																																								
10	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use	I																																								
11	DOTCLK	Dot clock signal for RGB interface operation Fix this pin at VCI or GND when not in use.	I																																								
12	ENABLE	Data enable signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I																																								
13	RD	Serves as a read signal and MCU read data at the rising edge. fix this pin at VCI or GND when not in use.	I																																								
14	WR(SPI-RS)	(WR): Serves as a write signal and writes data at the rising edge. 4-line system (RS): Serves as command or parameter select. Fix to IOVCC or GND level when not in use.	I																																								
15	RS(SPI-SCL)	This pin is used to select “Data or Command” in the parallel interface. When RS = '1', data is selected.	I																																								

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		When RS = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. If not used, this pin should be connected to IOVCC or GND. RS_SCL1 is equal to RS(SCL).	
16	CS	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only. CSX1 is equal to CSX.	I
17	RESET	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low. RESX1 is equal to RESX.	I
18-35	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode Fix to GND level when not in use	I/O
36	LEDK1	Cathode pin OF backlight	P
37	LEDK2	Cathode pin OF backlight	P
38	LEDK3	Cathode pin OF backlight	P
39	LEDK4	Cathode pin OF backlight	P
40	LEDA	Anode pin of backlight	P
41	XR	Touch panel Right Glass Terminal	A/D
42	YU	Touch panel Top Film Terminal	A/D
43	XL	Touch panel LIFT Glass Terminal	A/D
44	YD	Touch panel Bottom Film Terminal	A/D
45	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

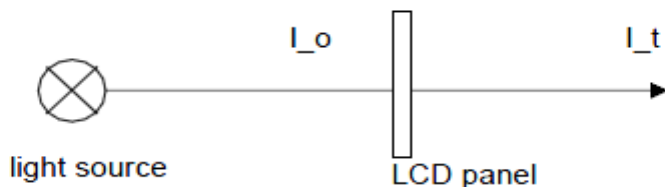
Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$ Normal viewing angle	--	300	--	msec	
Response time	Rising	T_R+T_F		--	35	50		
	Falling			--				
Color gamut		S(%)		--	58	--	%	
Color Filter Chromaticity	White	W_X		0.27	0.310	0.35		
		W_Y		0.296	0.336	0.376		
	Red	R_X		0.601	0.621	0.641		
		R_Y		0.342	0.363	0.383		
	Green	G_X		0.324	0.344	0.364		
		G_Y		0.588	0.608	0.628		
	Blue	B_X		0.130	0.150	0.170		
		B_Y		0.055	0.075	0.095		
Viewing angle	Hor.	Θ_{21}	CR>10	--	15	--	deg	
		Θ_{22}		--	35	--		
	Ver.	Θ_{12}		--	45	--		
		Θ_{11}		--	45	--		
Option View Direction		6"Clock						



4.2 Definitions and measuring methods■ Measuring surrounding: dark room

[1] Transmittance (T%)

The transmittance of the panel including polarizers is measured without electrical driving.



The Transmittance is defined as:

$$Tr = \frac{I_t}{I_o} \times 100\%$$

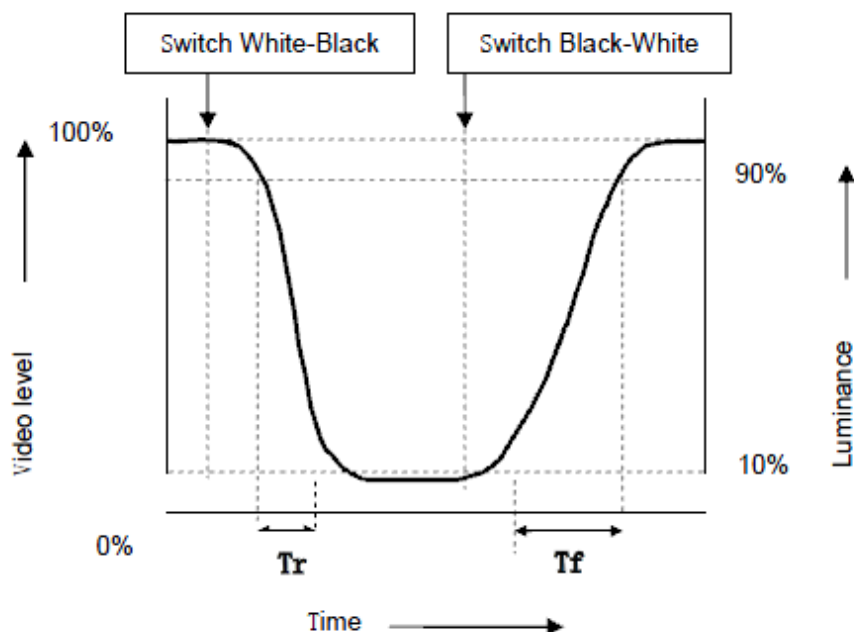
here,

I_o : the brightness of the light source.

I_t : the brightness after panel transmission.

[2] Response Time(Tr 、 Tf)

The rise time ' Tr ' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time ' Tf ' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



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The contrast ratio (Cr), measured on a module, is the ratio between the luminance (L_w) in a full white area ($R=G=B=1$) and the luminance (L_d) in a dark area ($R=G=B=0$):

$$Cr = \frac{L_w}{L_d}$$

θ: Viewing Angle
Reference Point: ASIC at 6 O'clock direction

Normal $\theta = 0^\circ$

θ₂₁ θ₂₂

θ₁₂ θ₁₁

3 O'clock

12 O'clock

6 O'clock

9 O'clock

ISO9000

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[5] Definition of color gamut

Measuring machine: CFT-01. NTSC'S Primaries: R(x,y,Y)、 G(x,y,Y)、 B(x,y,Y).

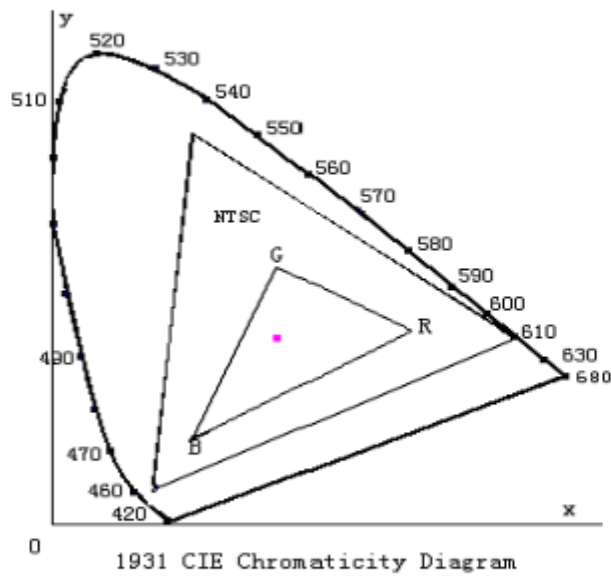


Fig. 1931 CIE chromaticity diagram

$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

ISO9001 : 2008

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5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCI	-0.3	4.2	V
Digital interface supply Voltage	IOVCC	-0.3	3.3	V
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	2.8	3.3	V	
Digital interface supply Voltage	IOVCC	1.65	1.8	3.3	V	
Normal mode Current consumption	IDD	--	3	--	mA	
Level input voltage	V _{IH}	0.7IOVCC		IOVCC	V	
	V _{IL}	GND		0.3IOVCC	V	
Level output voltage	V _{OH}	0.8IOVCC		IOVCC	V	
	V _{OL}	GND		0.2IOVCC	V	

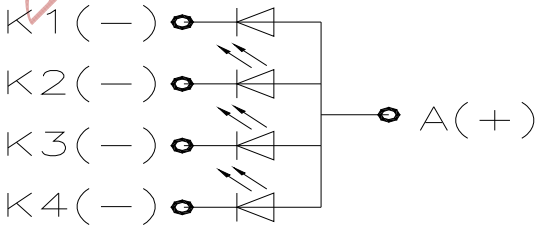
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 4chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I _F	70	80	--	mA	
Forward Voltage	V _F	--	3.2	--	V	
LCM Luminance	L _V	300	--	--	cd/m ²	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:
Ta=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

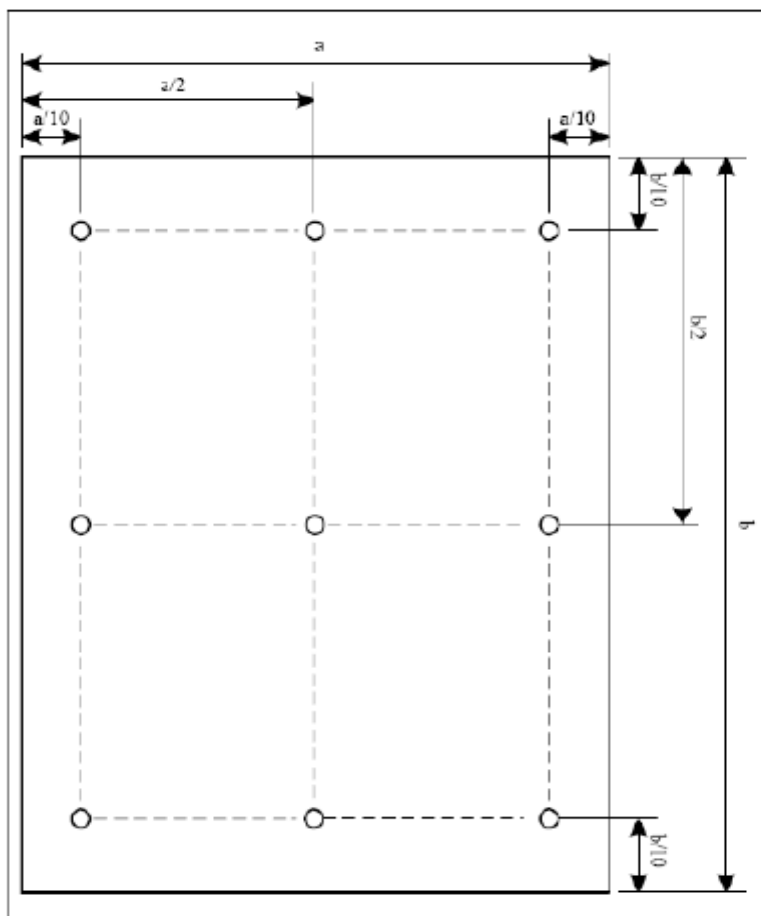
Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at
Ta=25℃ and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA. The
constant current driving method is suggested.



BLU CIRCUIT DIAGRAM



NOTE 3: Luminance Uniformity of these 9 points is defined as below:



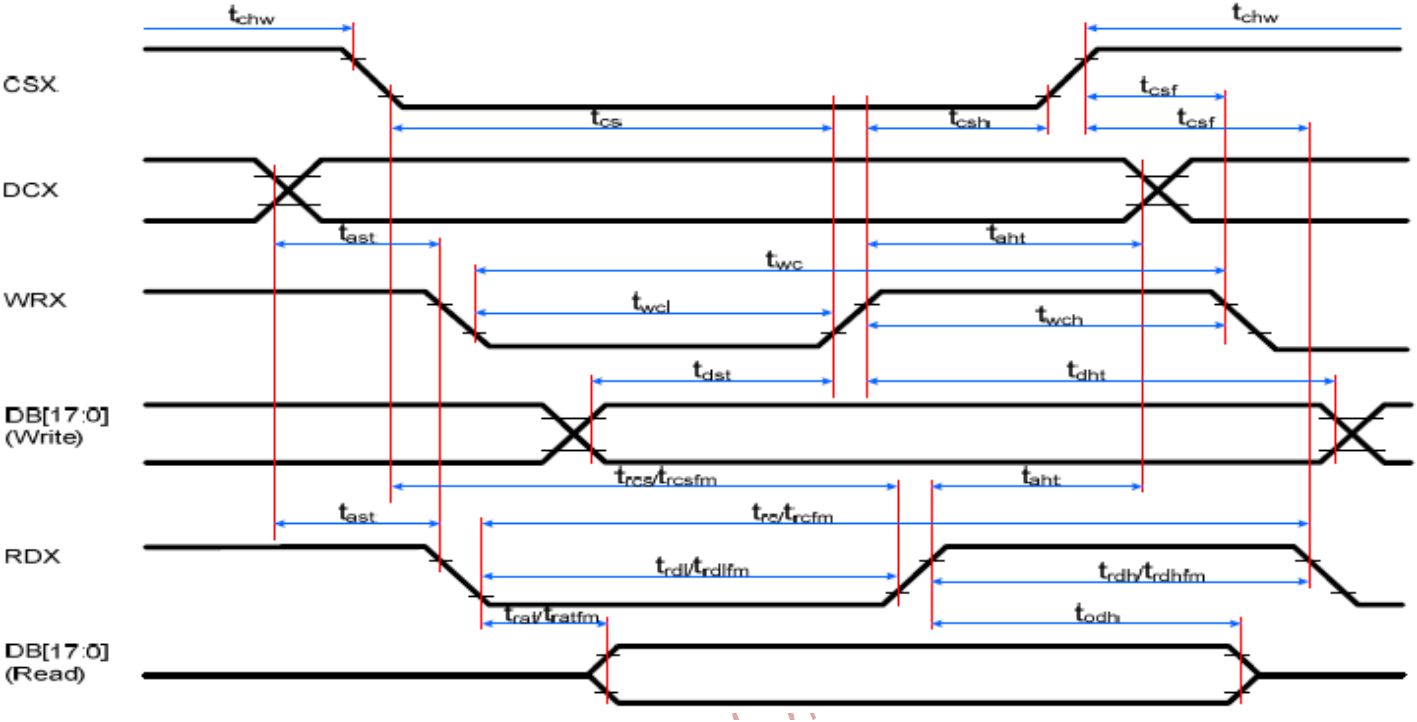
$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

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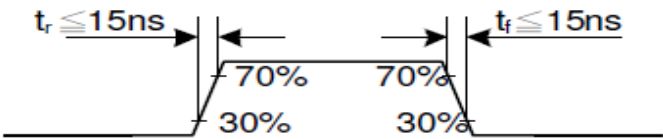
6. AC Characteristic

6.1 Display Parallel 8/9/16/18-bit Interface Timing Characteristics (8080 system)



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t _{ast}	Address setup time	0	-	ns	
	t _{ah}	Address hold time (Write/Read)	10	-	ns	
CSX	t _{chw}	CSX "H" pulse width	0	-	ns	
	t _{cs}	Chip Select setup time (Write)	15	-	ns	
	t _{rcs}	Chip Select setup time (Read ID)	45	-	ns	
	t _{rcsfm}	Chip Select setup time (Read FM)	355	-	ns	
	t _{csf}	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t _{wc}	Write cycle	66	-	ns	
	t _{wrh}	Write Control pulse H duration	15	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
RDX (FM)	t _{rcfm}	Read Cycle (FM)	450	-	ns	
	t _{rdhfm}	Read Control H duration (FM)	90	-	ns	
	t _{rdlfm}	Read Control L duration (FM)	355	-	ns	
RDX (ID)	t _{rc}	Read cycle (ID)	160	-	ns	
	t _{rdh}	Read Control pulse H duration	90	-	ns	
	t _{rdl}	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dht}	Write data hold time	10	-	ns	
	t _{rat}	Read access time	-	40	ns	
	t _{ratfm}	Read access time	-	340	ns	
	t _{trod}	Read output disable time	20	80	ns	

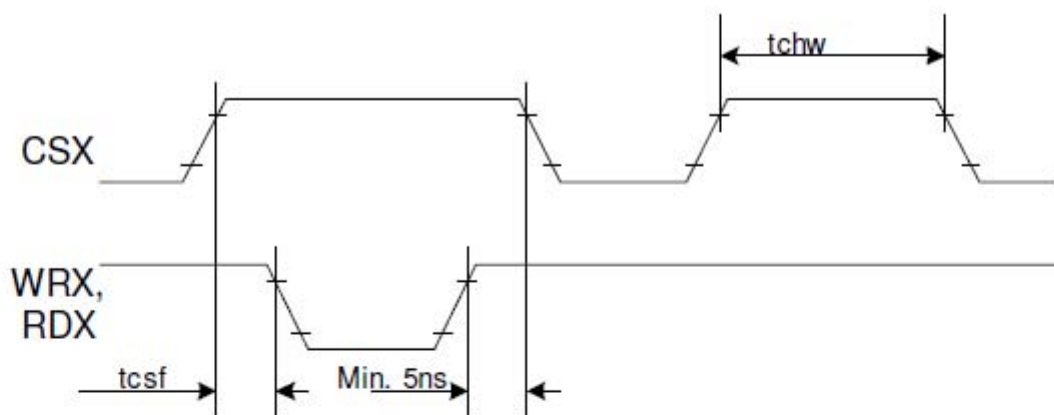
Note: Ta = -30 to 70 °C, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, GND=0V.



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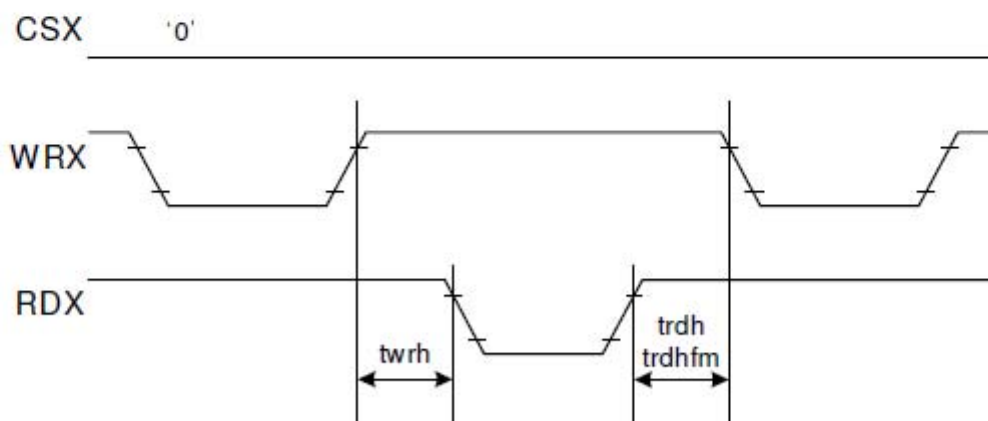


CSX timins :



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:

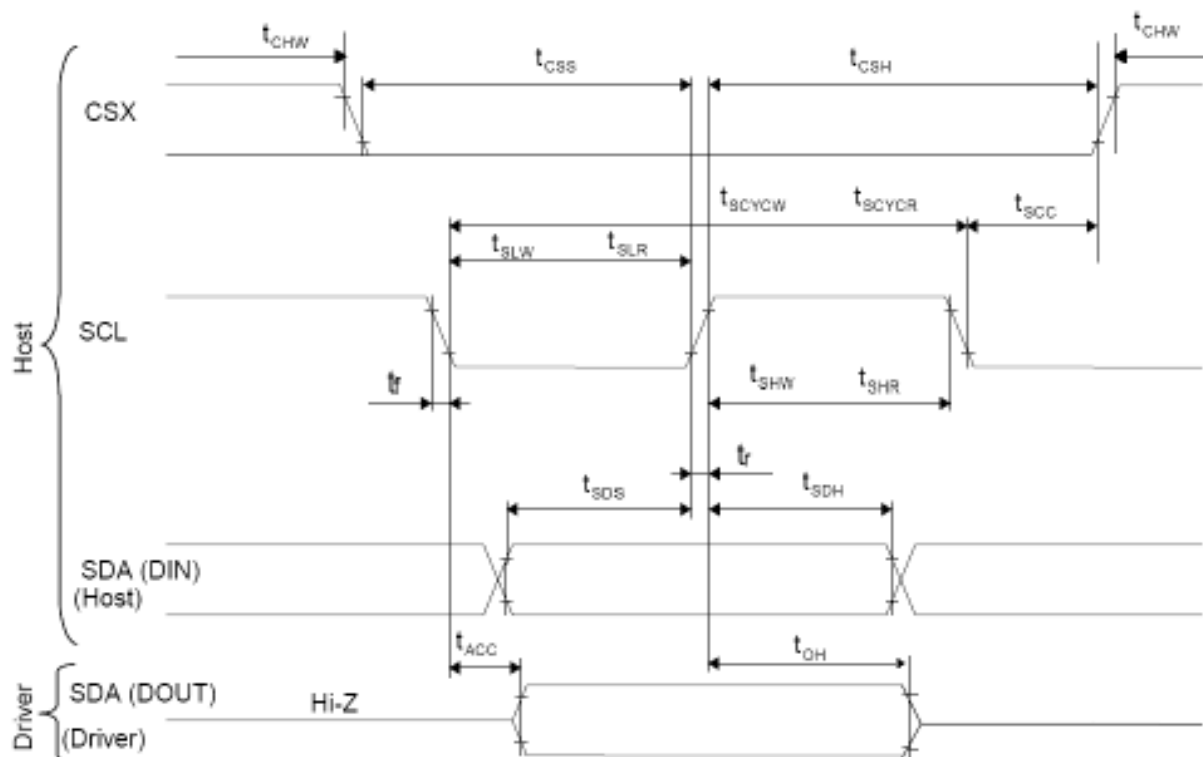


Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

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常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

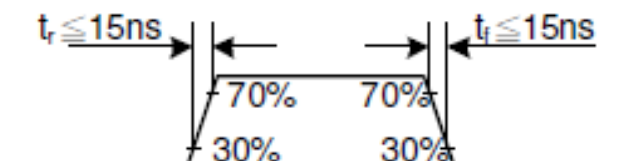


6.2 Display Serial Interface Timing Characteristics (3-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	35	-	ns	
	tslw	SCL "L" Pulse Width (Write)	35	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	15	50	ns	
CSX	tsc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time(write)	30	-	ns	
	tcs		30	-	ns	

Note: $T_a = 25\text{ }^{\circ}\text{C}$, $IOVCC=1.65\text{V to }2.8\text{V}$, $VCI=2.6\text{V to }3.3\text{V}$, $AGND=GND=0\text{V}$



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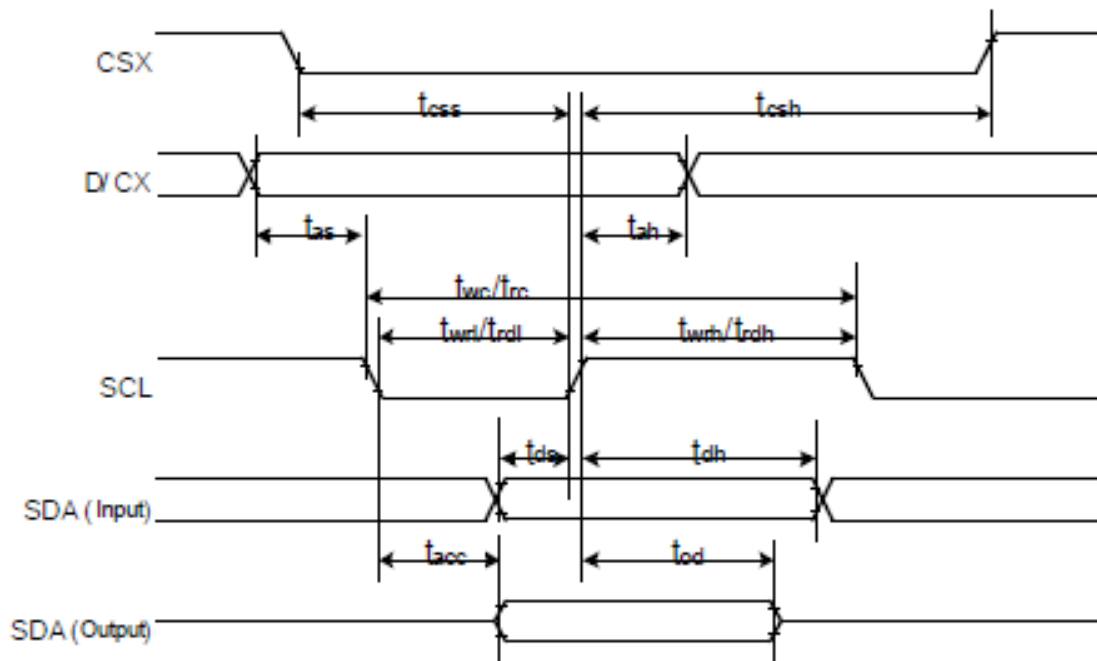
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支持小量
NO MOQ

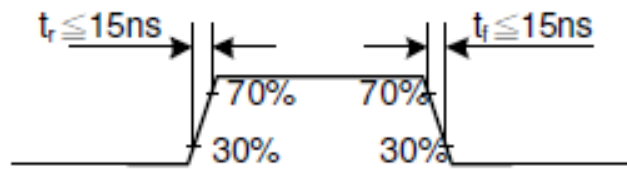
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6.3Display Serial Interface Timing Characteristics (4-line SPI system)

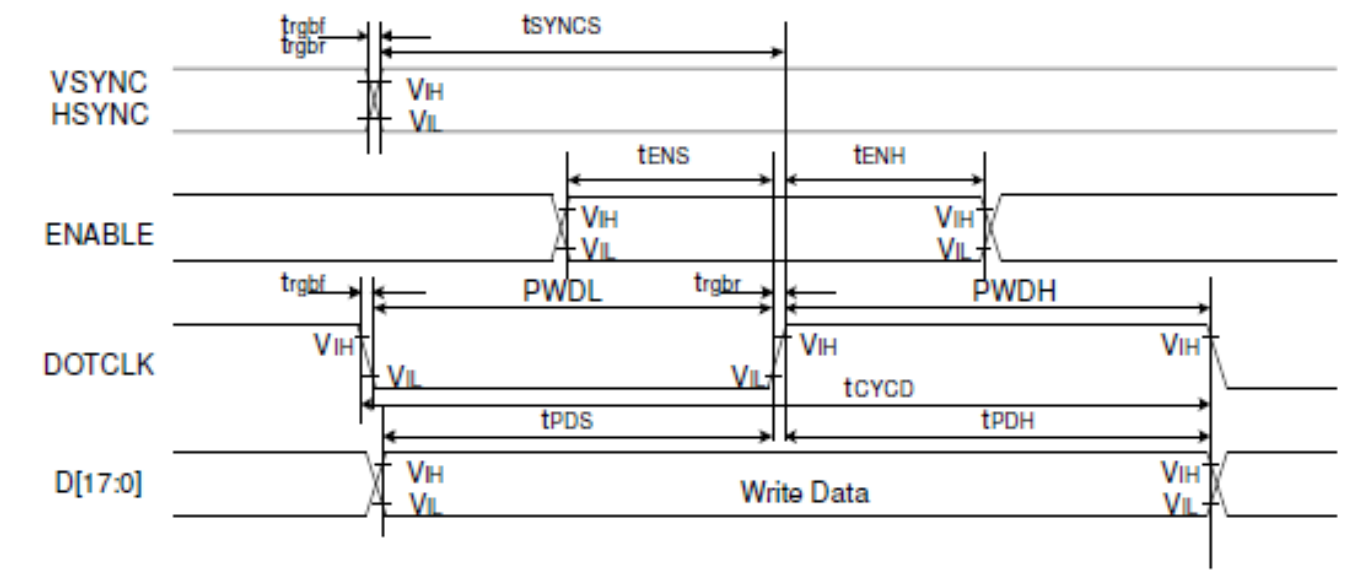


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{css}	Chip select time (Write)	30	-	ns	
	t_{csh}	Chip select hold time (write)	30	-	ns	
SCL	t_{wc}	Serial clock cycle (Write)	100	-	ns	
	t_{wrh}	SCL "H" pulse width (Write)	35	-	ns	
	t_{wrl}	SCL "L" pulse width (Write)	35	-	ns	
	t_{rc}	Serial clock cycle (Read)	150	-	ns	
	t_{rdh}	SCL "H" pulse width (Read)	60	-	ns	
	t_{rdl}	SCL "L" pulse width (Read)	60	-	ns	
D/CX	t_{as}	D/CX setup time	10	-		
	t_{ah}	D/CX hold time (Write / Read)	10	-		
SDA (Input)	t_{ds}	Data setup time (Write)	30	-	ns	
	t_{dh}	Data hold time (Write)	30	-	ns	
SDA (Output)	t_{acc}	Access time (Read)	-	50	ns	For maximum CL=30pF
	t_{od}	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: $T_a = 25\text{ }^{\circ}\text{C}$, $IOVCC=1.65\text{V to }2.8\text{V}$, $VCI=2.6\text{V to }3.3\text{V}$, $AGND=GND=0\text{V}$

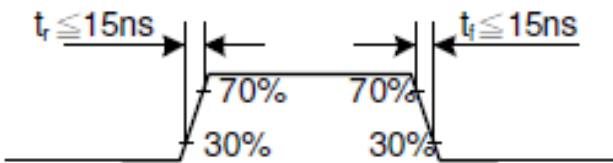


6.4 Parallel 16/18BIT RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	tSYNCS	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	tSYNCH	VSYNC/HSYNC hold time	15	-	ns	
DE	tENS	DE setup time	15	-	ns	
	tENH	DE hold time	15	-	ns	
D[17:0]	tPOS	Data setup time	15	-	ns	
	tPOH	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	33	-	ns	
	PWDL	DOTCLK low-level period	33	-	ns	
	tCYCD	DOTCLK cycle time(18 bit)	100	-	ns	
	tRGBR, tRGBF	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	tSYNCS	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	tSYNCH	VSYNC/HSYNC hold time	15	-	ns	
DE	tENS	DE setup time	15	-	ns	
	tENH	DE hold time	15	-	ns	
D[17:0]	tPOS	Data setup time	15	-	ns	
	tPOH	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	25	-	ns	
	PWDL	DOTCLK low-level pulse period	25	-	ns	
	tCYCD	DOTCLK cycle time	50	-	ns	
	tRGBR, tRGBF	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

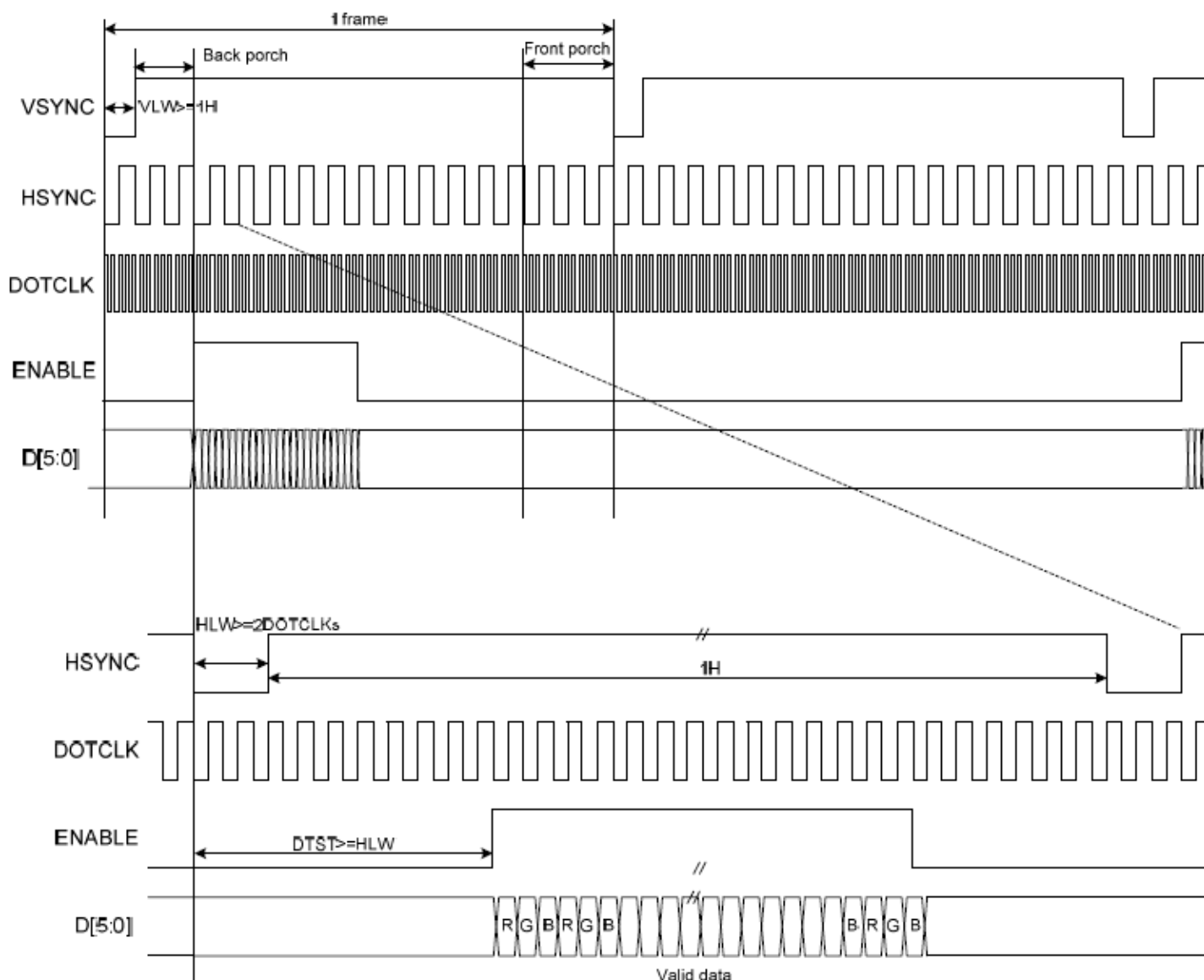
Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, AGND=GND=0V





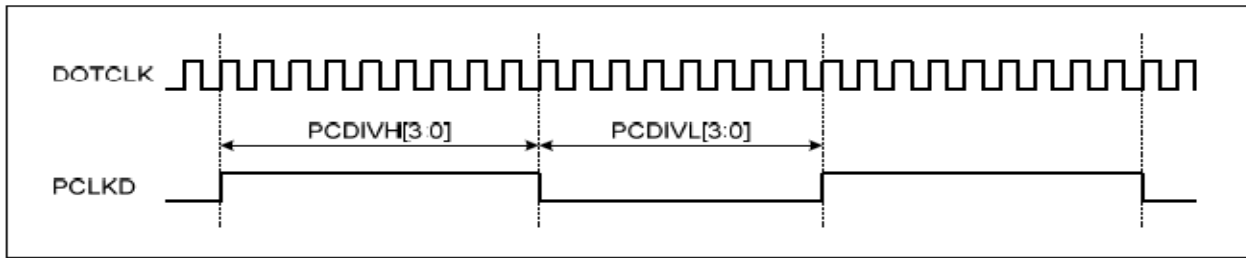
6.5 RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.

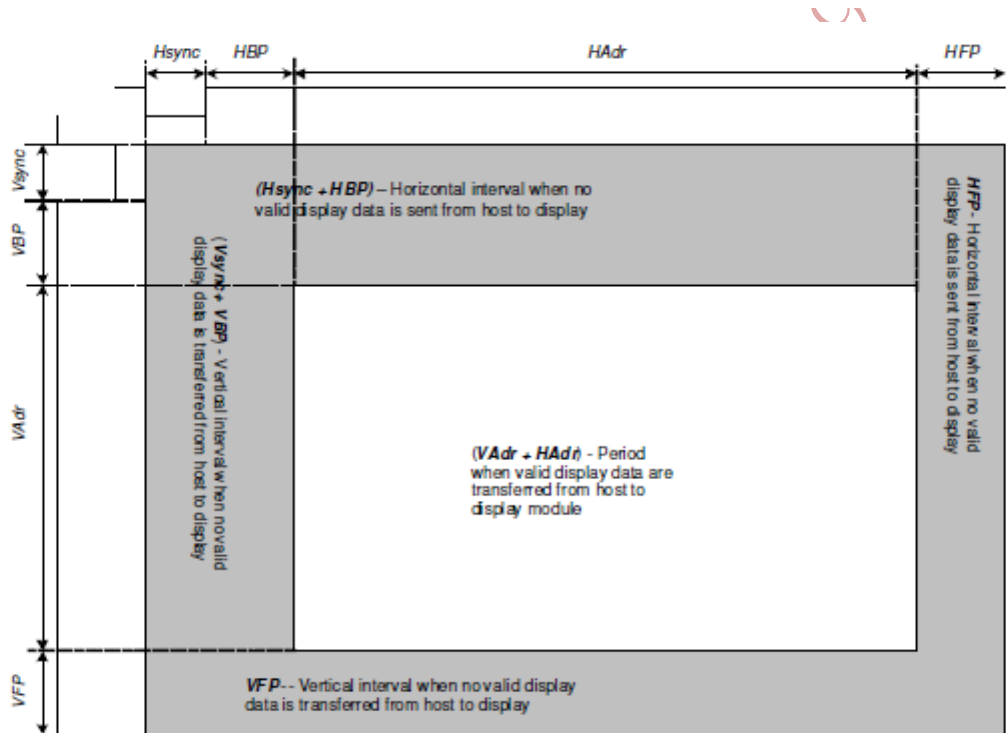


VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time

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常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	



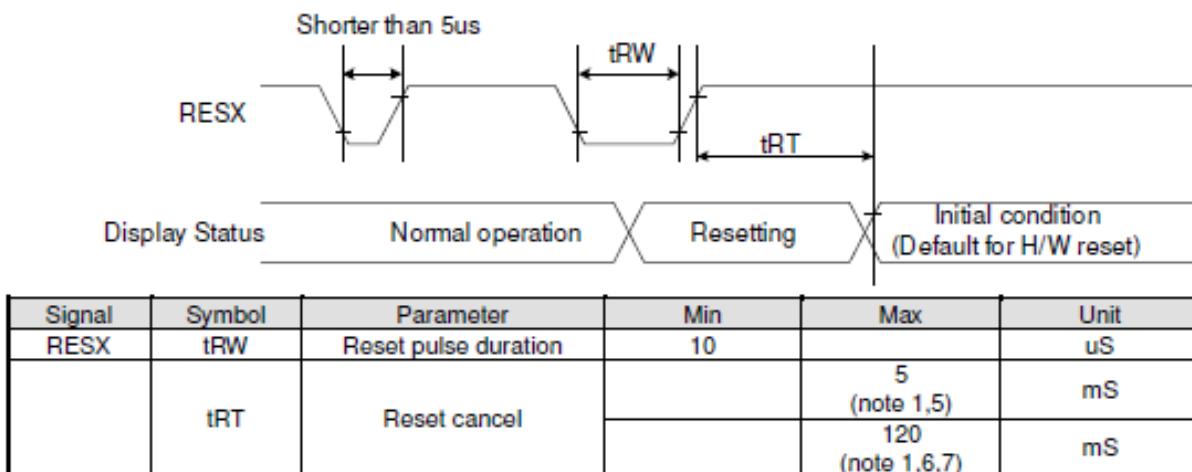
- Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.
- Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.
- Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.
- Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Back Porch(By pass mode)*	HBP(BP)		58	68	200	DOTCLK
Horizontal Address	HAdr		-	320	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	240	-	Line
Vertical Front Porch	VFP		3	4	-	Line



6.6 Reset Timing Characteristics



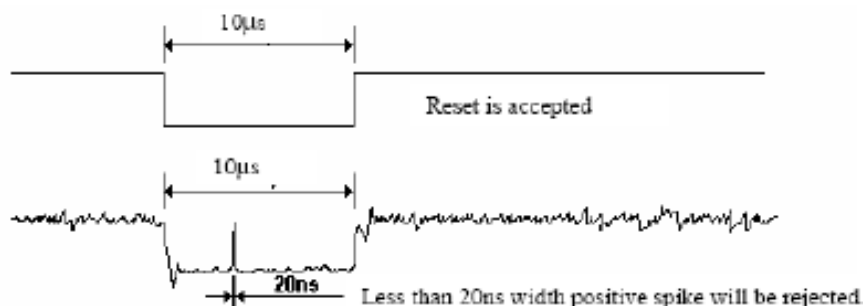
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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常备库存
Stock For Sale

长期供货
Long Time supply

支持小量
NO MOQ

品种齐全
In Full Range

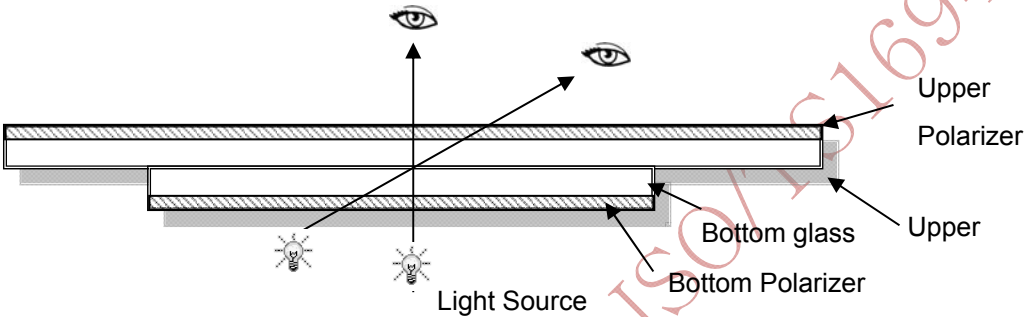
7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

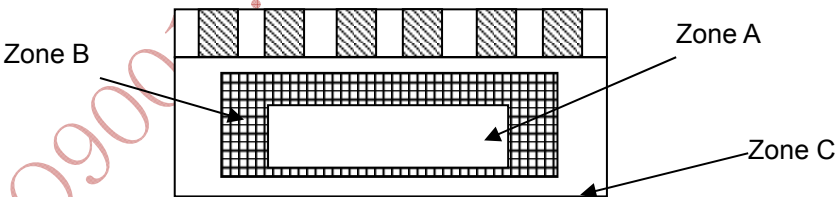
7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

- Temperature : 25±5℃
- Humidity : 65%±10%RH
- Viewing Angle : Normal viewing Angle.
- Illumination: Single fluorescent lamp (300 to 700Lux)
- Viewing distance:30-50cm



7.1.2 Definition



- Zone A : Effective Viewing Area(Character or Digit can be seen)
- Zone B : Viewing Area except Zone A
- Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

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7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

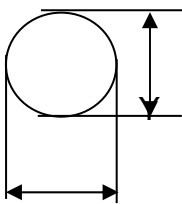
Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

7.1.4 Criteria (Visual)

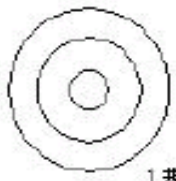
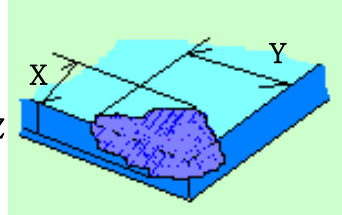
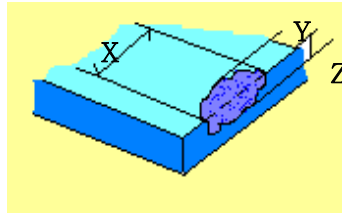
Number	Items	Criteria(mm)
1.0 LCD Crack/Broken <		

Number	Items	Criteria (mm)																									
2.0	Spot defect  X Φ=(X+Y)/2	① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)																									
		<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Accep able Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.30</td><td colspan="2">Ignore</td><td rowspan="4">Ignor</td></tr><tr><td>0.20<Φ≤0.3</td><td colspan="2">3(distance ≥ 10mm)</td></tr><tr><td>0.25<Φ≤0.35</td><td colspan="2">2</td></tr><tr><td>Φ > 0.4</td><td colspan="2">0</td></tr></table>	Zone Size (mm)	Accep able Qty			A	B	C	Φ≤0.30	Ignore		Ignor	0.20<Φ≤0.3	3(distance ≥ 10mm)		0.25<Φ≤0.35	2		Φ > 0.4	0						
		Zone Size (mm)		Accep able Qty																							
			A	B	C																						
		Φ≤0.30	Ignore		Ignor																						
		0.20<Φ≤0.3	3(distance ≥ 10mm)																								
		0.25<Φ≤0.35	2																								
		Φ > 0.4	0																								
		②Dim spot (LCD/TP/Polarizer dim dot, light leakage、dark spot)																									
		<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.3</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>0.2<Φ≤0.3</td><td colspan="2">3(distance ≥ 10mm)</td></tr><tr><td>0.25<Φ≤0.35</td><td colspan="2">2</td></tr><tr><td>Φ > 0.4</td><td colspan="2">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.3	Ignore		Ignore	0.2<Φ≤0.3	3(distance ≥ 10mm)		0.25<Φ≤0.35	2		Φ > 0.4	0						
		Zone Size (mm)		Acceptable Qty																							
			A	B	C																						
		Φ≤0.3	Ignore		Ignore																						
		0.2<Φ≤0.3	3(distance ≥ 10mm)																								
		0.25<Φ≤0.35	2																								
		Φ > 0.4	0																								
		③ Polarizer accidented spot																									
	<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.3</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>0.25<Φ≤0.5</td><td colspan="2">2(distance ≥ 10mm)</td></tr><tr><td>Φ>0.5</td><td colspan="2">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.3	Ignore		Ignore	0.25<Φ≤0.5	2(distance ≥ 10mm)		Φ>0.5	0										
	Zone Size (mm)		Acceptable Qty																								
		A	B	C																							
	Φ≤0.3	Ignore		Ignore																							
0.25<Φ≤0.5	2(distance ≥ 10mm)																										
Φ>0.5	0																										
Line defect (LCD/TP /Polarizer black/white line, scratch, stain)	<table><tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.05</td><td>Igno e</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>0.04<W≤0.07</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr><tr><td>0.06<W≤0.09</td><td>L≤2.0</td><td colspan="2">N≤2</td></tr><tr><td>0.09<W</td><td colspan="4">Define as spot defect</td></tr></table>	Width(mm)	Length(mm)	Acceptable Qty			A	B	C	Φ≤0.05	Igno e	Ignore		Ignore	0.04<W≤0.07	L≤3.0	N≤2		0.06<W≤0.09	L≤2.0	N≤2		0.09<W	Define as spot defect			
	Width(mm)			Length(mm)	Acceptable Qty																						
		A	B		C																						
	Φ≤0.05	Igno e	Ignore		Ignore																						
	0.04<W≤0.07	L≤3.0	N≤2																								
	0.06<W≤0.09	L≤2.0	N≤2																								
	0.09<W	Define as spot defect																									



3.0	Polarizer Bubble				
		Zone Size (mm)		Acceptable Qty	
				A	B
		$\Phi \leq 0.2$	Ignore		Ignore
		$0.2 < \Phi \leq 0.4$	3(distance ≥ 10 m)		
		$0.4 < \Phi \leq 0.6$	2		
		$0.6 < \Phi$	0		
4.0	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.			

		TP bubble/ accidented spot	<table><tr><th rowspan="2">Size Φ(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi \leq 0.3$</td><td colspan="3">Ignore</td></tr><tr><td>$0.25 < \Phi \leq 0.3$</td><td colspan="3">3 (distance $\geq$</td></tr><tr><td>$0.25 < \Phi \leq 0.35$</td><td colspan="3">2</td></tr><tr><td>$0.4 < \Phi$</td><td colspan="3">0</td></tr></table>			Size Φ (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.3$	Ignore			$0.25 < \Phi \leq 0.3$	3 (distance $\geq$			$0.25 < \Phi \leq 0.35$	2			$0.4 < \Phi$	0		
Size Φ (mm)	Acceptable Qty																											
	A		B	C																								
$\Phi \leq 0.3$	Ignore																											
$0.25 < \Phi \leq 0.3$	3 (distance $\geq$																											
$0.25 < \Phi \leq 0.35$	2																											
$0.4 < \Phi$	0																											
Assembly deflection			beyond the edge of backlight $\leq 0.15\text{mm}$																									

5.0	TP Related	Newton Ring	Newton Ring area>1/3 TP area NG			 1 规律性				
			Newton Ring area≤1/3 TP area OK				 2 非规律性			
					 似牛顿环					
		TP corner broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thicknes</td></tr></table>	X	Y	Z	X≤3.0mm	Y≤3.0mm	Z<LCD thicknes	
X	Y	Z								
X≤3.0mm	Y≤3.0mm	Z<LCD thicknes								
TP edge broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤6.0mm</td><td>Y≤2.0mm</td><td>Z<LCD thicknes</td></tr></table>	X	Y	Z	X≤6.0mm	Y≤2.0mm	Z<LCD thicknes			
X	Y	Z								
X≤6.0mm	Y≤2.0mm	Z<LCD thicknes								

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

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8. Reliability Test Result

8.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70℃90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	-30℃, 96HR	3ea	pass	-
ESD test	150pF, 330Ω, ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point	3ea	pass	
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

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				品种齐全 In Full Range

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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				品种齐全 In Full Range



10. Packing

---TBD-----

ISO9001 : 2008 ISO/TS16949 : 2009

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常 备 库 存 Stock For Sale		长 期 供 货 Long Time supply		支 持 小 量 NO MOQ
				品 种 齐 全 In Full Range