

**SPECIFICATION
FOR
LCD Module
KD035FM-07**

MODULE:	KD035FM-07
CUSTOMER:	

REV	DESCRIPTION	DATE
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PREPARED BY		
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APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		



Revision History

[illegible]

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General Description

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 3.5" TFT-LCD contains 320x480 pixels, and can display up to 65K/262K colors.

* Features

- Low Input Voltage: 2.8V~3.3V(TYP)
- Display Colors of TFT LCD: 65K/262K colors
- Interface: 8-bits, 9-bits, 16-bits, 18-bits MCU interface.
6-bits, 16-bits, 18-bits RGB interface with graphic controller.
3-line/4-line serial interface.

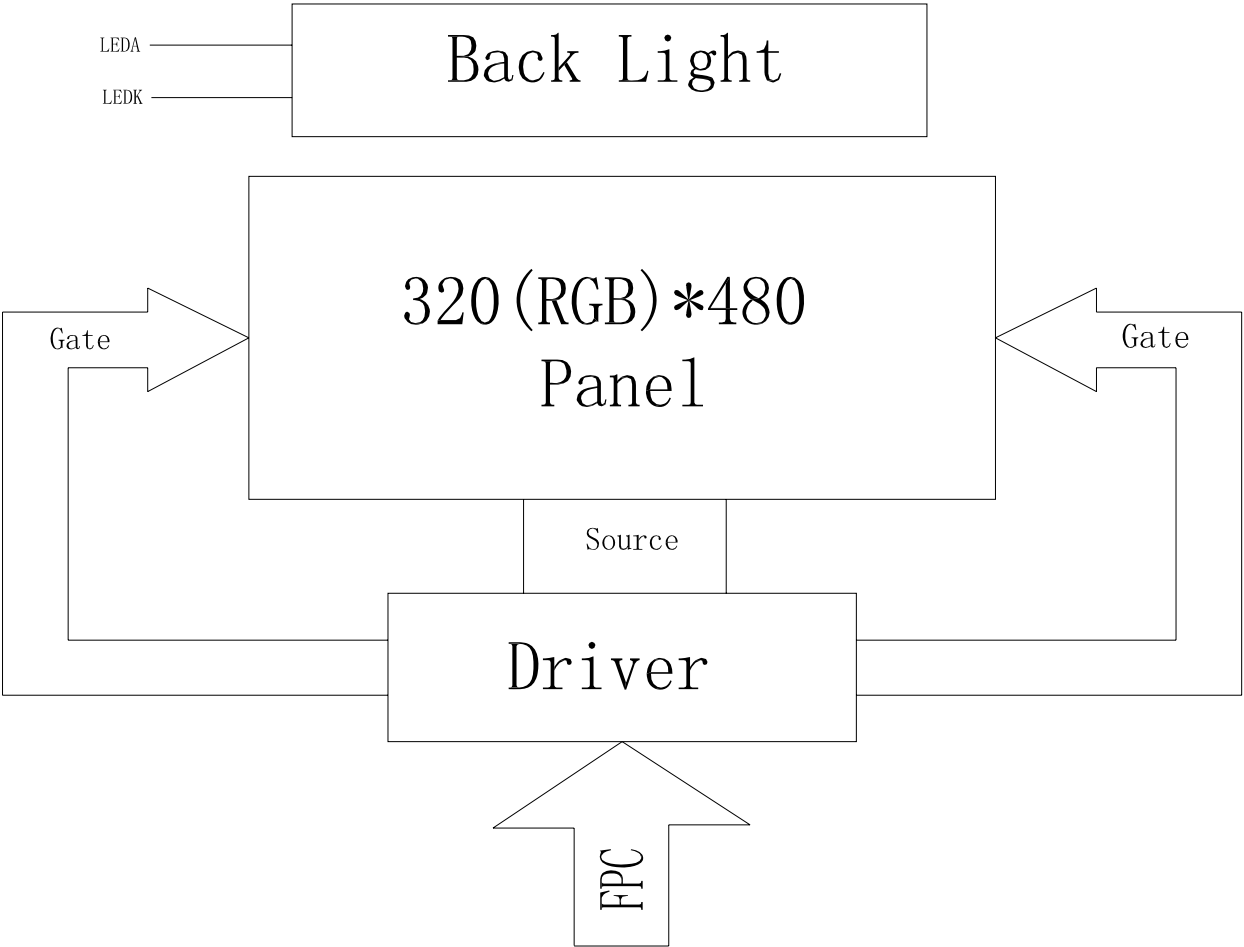
General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	48.96(H)*73.44(V) (3.5inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262k	colors	-
Number of pixels	320(RGB)*480	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.153(H)*0.153(V)	mm	-
Viewing angle	ALL	o'clock	-
Controller IC	ILI9486L	-	-
Display mode	Transmissive/Normally Black	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		54.58		mm	-
	Vertical(V)		83.57		mm	-
	Depth(D)		2.1		mm	-
Weight			TBD		g	-

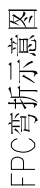


1. Block Diagram





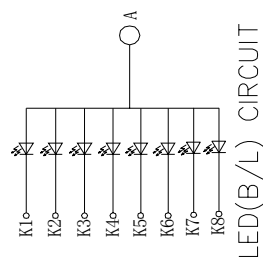
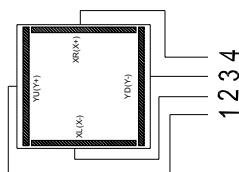
NO.	Ph Name	Ph Name
1	GND	1
2	VCI	2
3	VCI	3
4	IM0	4
5	IM1	5
6	IM2	6
7	RESX	7
8	YSYNIC	8
9	HSYNIC	9
10	PLCK	10
11	DE	11
12	DBT7/R5	12
13	DBT6/R5	13
14	DBT6/R5	14
15	DBT6/R5	15
16	DBT4/R2	16
17	DBT1/R0 Lsb	17
18	DBT1/R5 Lsb	18
19	DBT0/G4	19
20	DBR0/G2	20
21	DBR0/G2	21
22	DBR7/G1	22
23	DBR6/G0 Lsb	23
24	DBR5/G6 Lsb	24
25	DBR4/B4	25
26	DBR3/B3	26
27	DBR2/B2	27
28	DBR1/B1	28
29	DBR0/B0 Lsb	29
30	GND	30
31	DOIT	31
32	DIN_SDA	32
33	ROX	33
34	WRX_SCL	34
35	DOX	35
36	CSX	36
37	LEDA	37
38	LEDK1	38
39	LEDK2	39
40	LEDK3	40
41	LEDK4	41
42	LEDK5	42
43	LEDK6	43
44	LEDK7	44
45	LEDK8	45
46	XRNC	46
47	YU(NC)	47
48	XU(NC)	48
49	YU(NC)	49
50	GND	50



DB2	DB1	DB0	Interface type	DB Pin in use
0	0	0	DB1 T ₀ , 10-bit interface	DB17-DB80
0	0	1	DB1 T ₀ , 9-bit interface	DB88-DB80
0	1	0	DB1 T ₀ , 10-bit interface	DB15-DB80
0	1	1	DB1 T ₀ , 8-bit interface	DB7-DB80
1	0	1	5-Fire 9 BIT data serial interface	SD1 SCL CS
1	1	1	4-Fire 8 BIT data serial interface	SD1 SCL CS RS

NOTE:

1. If not use PIN, fix to the GND , VCI or NC.
2. If use RGB interface must select serial interface



LED(B/L) CIRCUIT

7. BACK LIGHT: LED WHITE, 8 LED, 120–160mA, $3.2V \pm 0.3V$

- NOTES:
1. DISPLAY TYPE: 3.5", TFT-LCD, 262K COLORS
 2. DISPLAY MODE: NORMALLY BLACK
 3. VIEWING DIRECTION: ALL
 4. DRIVER IC: ILI9486L (COG)
 5. VCI: 2.5–3.3V
 6. OPERATING TEMP: –20°C TO 70°C
STORAGE TEMP: –30°C TO 80°C
 7. BACK LIGHT: LED WHITE, 8 LED, 120–160mA,
 8. RoHS COMPLIANT.

1234		深圳市柯达科电子科技有限公司 Shenzhen Startek Electronic Technology Co.,Ltd		TOLERANCE(公差) TOLERANCE X.X±0.3 OTHERS X.XX±0.2 SPECIFIED		DRAWING NAME Drawn Checked		KD035FM-07	
Rev	Revision content description	Date							
A	FIRST	2012/07/06				Unit			
B	配合光亮	2012/07/14				mm			
								Approve	
						Scale 1:1		Page 1/1	

3. Input terminal Pin Assignment

Pin NO.	Symbol	Function	I/O
1.	GND	Ground.	P
2	VCI	Analog power supply, 3.3V.	P
3	VCI	Analog power supply, 3.3V	P
4	IM0	Select Interface mode signal.	I
5	IM1		
6	IM2		
7	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.	I
8	VSYNC	Frame synchronizing signal for DPI I/F mode. If not use, please connect to GND.	I
9	HSYNC	Frame synchronizing signal for DPI I/F mode. If not use, please connect to GND.	I
10	PCLK	Pixel clock signal for DPI I/F mode. If not use, please connect to VCI.	I
11	DE	A DATA ENABLE signal for DPI I/F mode. If not use, please connect to GND.	I
12-29	DB17-DB0	Data bus PINS. 18-bit bi-directional data bus. 8-bit bus: use DB7-DB0 9-bit bus: use DB8-DB0 16-bit bus: use DB15DB0 18-bit bus: use DB17-DB0 When Operation in MIPI DPI interface mode, it is an 18-bit bus RGB data bus. 6-bit bus: use DB5-DB0 16-bit bus: use DB15-DB0 18-bit bus: use DB17-DB0 If not used PINS, please must connect to GND.	I/O
30	GND	Ground.	P
31	DOUT	Serial data output pin in serial bus system interface. If not used, please open this pin.	O



32	DINI_SDA	Serial data input pin or input/output pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal. If not used, please connect to GND.	I
33	RDX	DBI Type-B: Serves as a read signal and read data at the low level. If not use, please connect to IOVCC.	I
34	WRX_SCL	DBI Type-B: Serves as a write signal and write data at the low level. DBI Type-C: it serves as SCL (Serial Clock). If not use, please connect to GND.	I
35	DCX	Data / Command Selection pin If not use, please connect to GND.	I
36	CSX	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed. If not use, please connect to GND.	I
37	LEDA	Anode pin of backlight.	P
38-45	LEDK1-LEDK8	Cathode pin of backlight.	P
46	XR	Touch panel Right Glass Terminal.	A/D
47	YD	Touch panel Bottom Film Terminal.	A/D
48	XL	Touch panel LEFT Glass Terminal.	A/D
49	YU	Touch panel Top Film Terminal.	A/D
50	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
*1) Threshold Voltage	Vsat	3.7	3.8	3.9	V	Fig.2
	Vth	1.9	2.0	2.1	V	
*1) Transmittance	T(%)	3.86	4.40	-	%	Fig.1
*1) Contrast Ratio	C/R	400	500	-		
*1) Response Time	Tr+Tf	-	35	50	msec	Fig.3
*2) CIE Color Coordinate	Rx	0.640	0.660	0.680		
	Ry	0.297	0.317	0.337		
	Gx	0.240	0.260	0.280		
	Gy	0.555	0.575	0.595		
	Bx	0.121	0.141	0.161		
	By	0.055	0.075	0.095		
	Wx	0.275	0.295	0.315		
	Wy	0.297	0.317	0.337		
*1) Viewing Angle	Θ_l	-	80	-	Degree	C/R>10 Fig.4
	Θ_r	-	80	-		
	Θ_u	-	80	-		
	Θ_d	-	80	-		

4.2 Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : 25±2℃
- 15min. warm-up time

4.3 Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

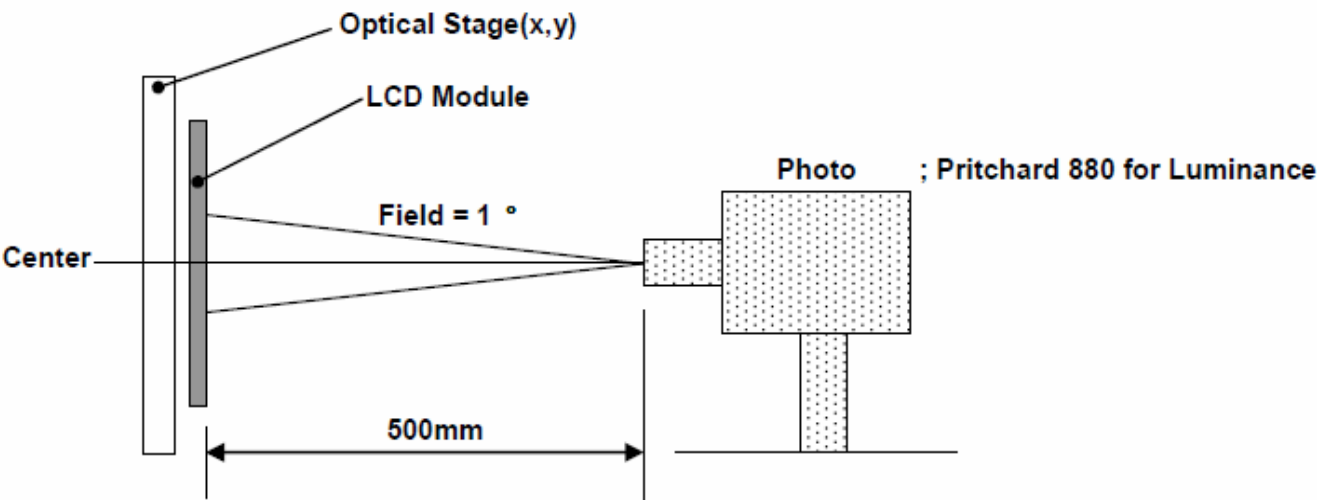
- Notes :
1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$
 2. Surface luminance is the center point across the TFT-LCD surface 240 mm from the surface with all pixels displaying white. For more information see FIG 1.
 3. Response time is the time required for the display to transition from black to white(Rise Time, Tr) and from white to black(Falling Time, Tf). For additional information see FIG 3.
 4. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the TFT-LCD surface. For more information see FIG 4.
 5. Optimum contrast is obtained by adjusting the TFT-LCD Threshold voltage(Vth & Vsat)

FIG. 1 Optical Characteristic Measurement Equipment and Method

Pritchard 880 System

[Test Equipment Set Up]



- Measuring Condition ;
 - Measuring surroundings : Dark Room
 - Measuring temperature : T_a=25℃
 - Adjust operating voltage to get optimum contrast at the center of the display.
 - Measured value at the center point of LCD panel after more than 30 minutes while backlight turning on.

5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	4.2	V
Digital interface supply Voltage	VDDIO	-0.3	VDD	V
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

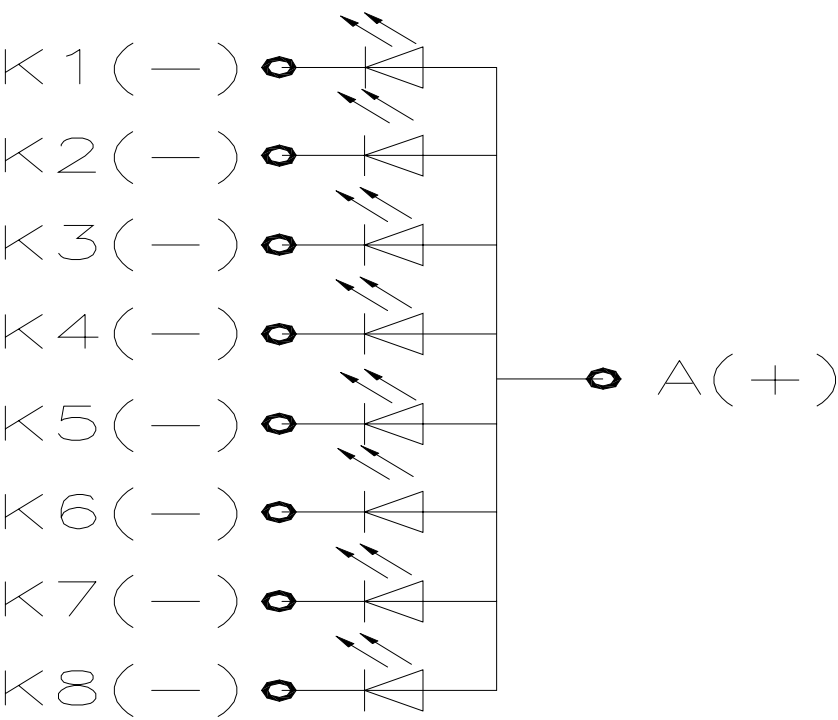
5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.6	3.3	4.2	V	--
Digital interface supply Voltage	VDDIO	1.65	3.3	4.2	V	--
Normal mode Current consumption	IDD	--	10	--	mA	--
Level input voltage	V _{IH}	0.7VDDIO	--	VDDIO	V	--
	V _{IL}	GND	--	0.3VDDIO	V	--
Level output voltage	V _{OH}	0.8VDDIO	--	VDDIO	V	--
	V _{OL}	GND	--	0.2VDDIO	V	--

5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 8chips White LED

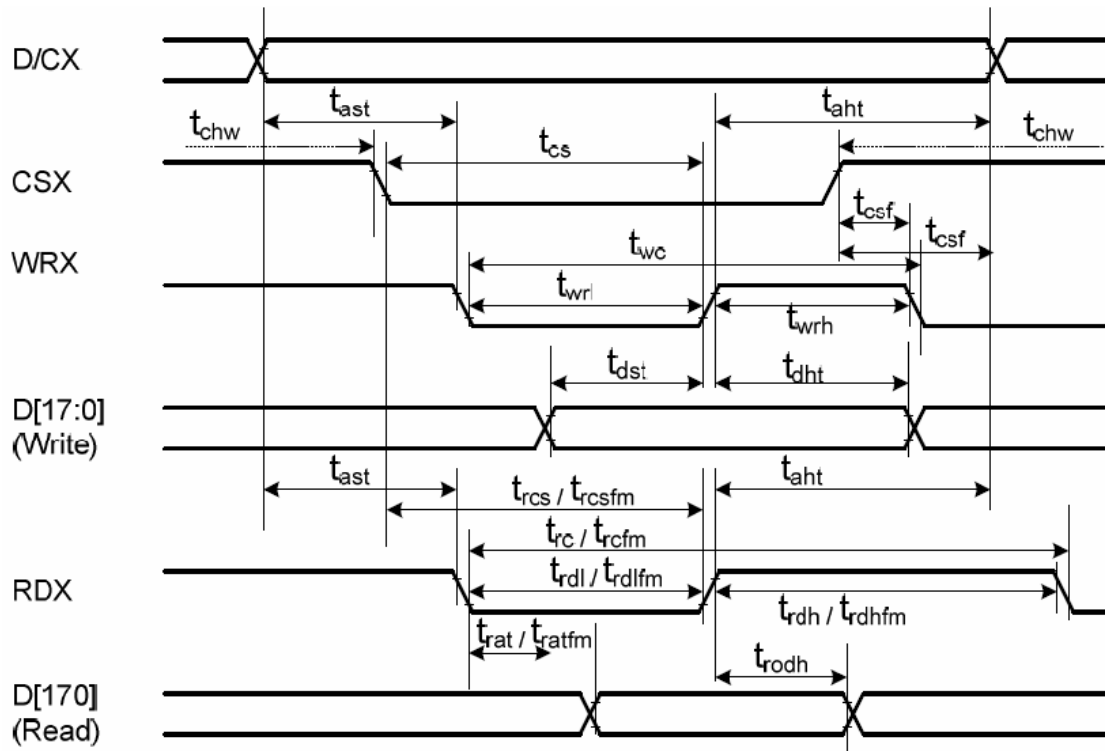
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I _F	120	160	-	mA	
Forward Voltage	V _F	2.9	3.2	3.4	V	-
LCM Luminance	L _V	400	-	-	cd/m ²	IF=160mA
Uniformity	AVg	80	-	-	%	-



BLU C I R C U I T D I A G R A M

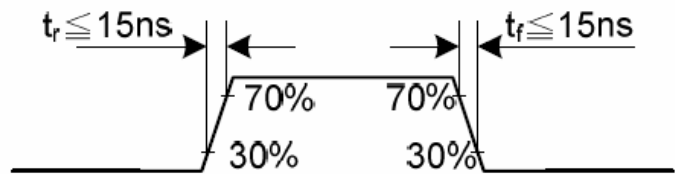
6. AC Characteristic

6.1 DBI Type B (18/16/9/8 bit) Interface Timing Characteristics(8080-series)

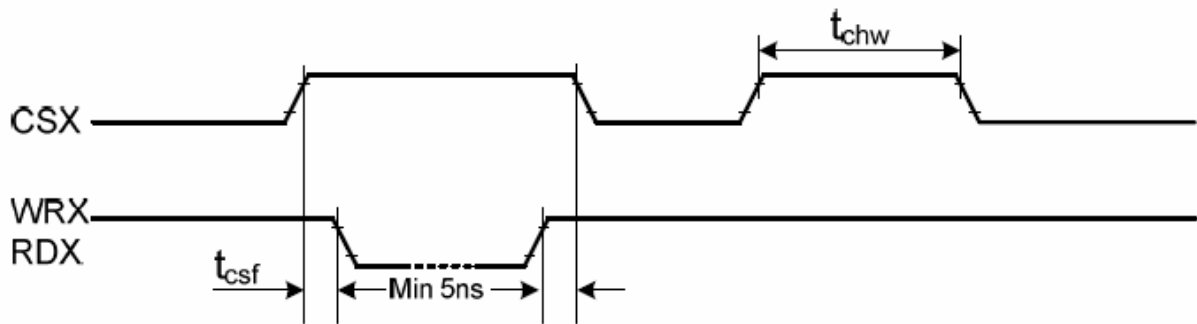


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	taht	Address hold time (Write/Read)	0	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
WRX	twc	Write cycle	50	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB[17:0], DB[15:0], DB[8:0] DB[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

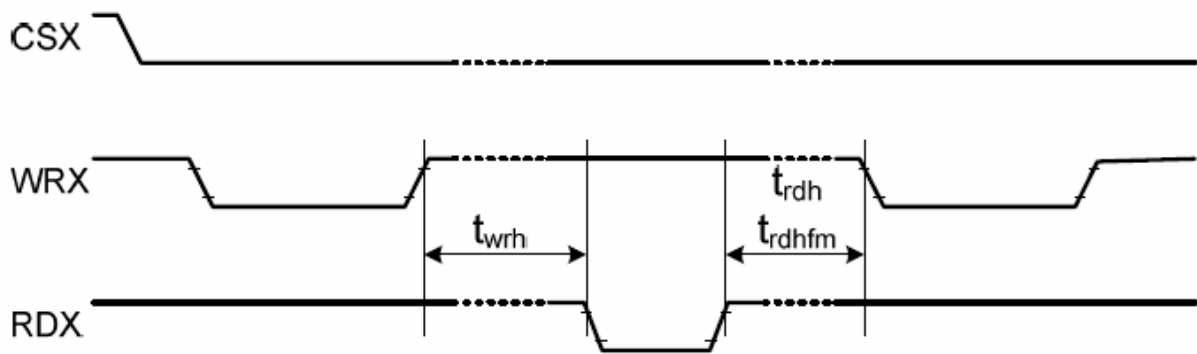
Note: (1) $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $IOVCC=1.65\text{V}$ to 3.6V , $VCI=2.5\text{V}$ to 3.6V , $AGND=DGND=0\text{V}$



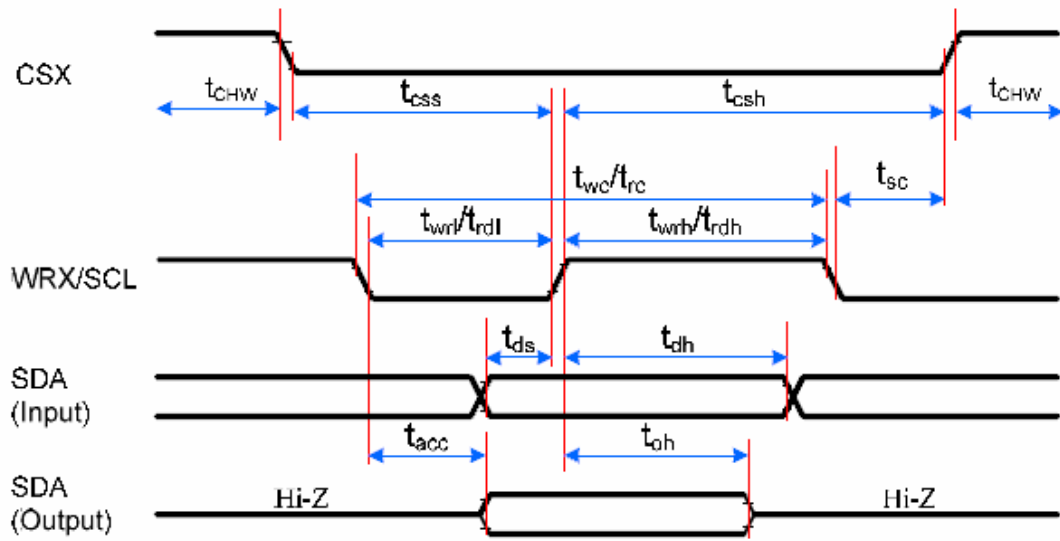
(2) Logic high and low levels are specified as 30% and 70% of $IOVCC$ for input signals.



(3) Logic high and low levels are specified as 30% and 70% of $IOVCC$ for input signals.

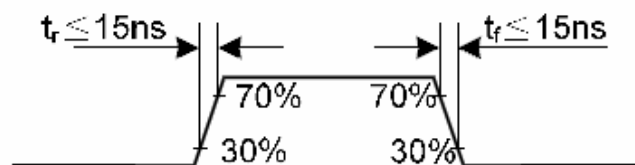


6.2 Display Serial Interface Timing Characteristics (3-line SPI system)

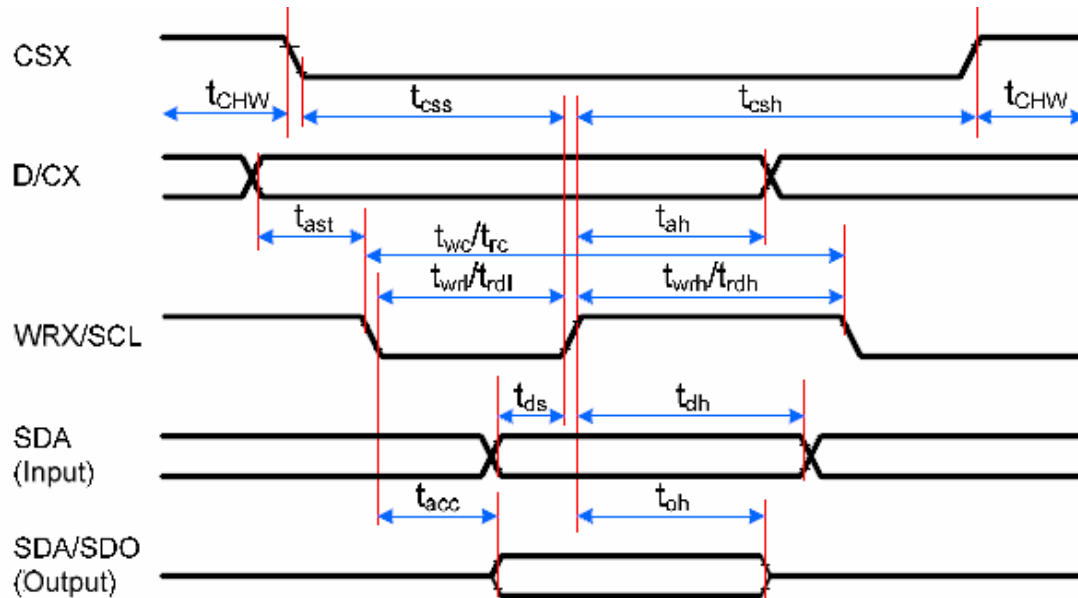


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchwh	CSX H Pulse Width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
	twrl	SCL L Pulse Width (Write)	15	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: $T_a = -30$ to 70 °C, $I_{OVCC} = 1.65V$ to $3.6V$, $V_{CI} = 2.5V$ to $3.6V$, $AGND = DGND = 0V$, $T = 10 \pm 0.5ns$



6.3 Display Serial Interface Timing Characteristics (4-line SPI system)



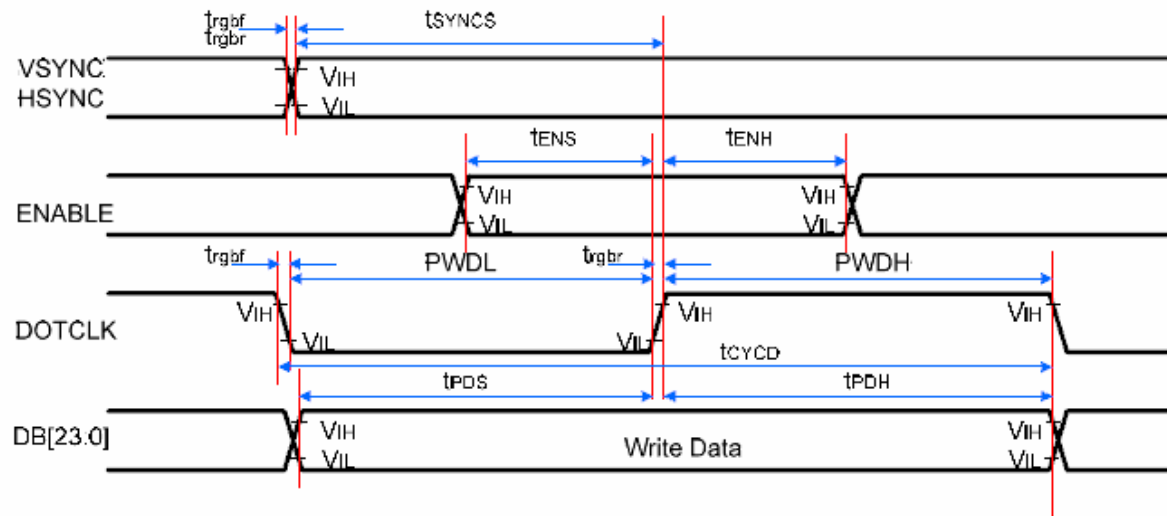
Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{css}	Chip select time (Write)	15	-	ns	
	t_{csh}	Chip select hold time (Read)	15	-	ns	
	t_{CHW}	CS H pulse width	40	-	ns	
SCL	t_{wc}	Serial clock cycle (Write)	50	-	ns	
	t_{wrh}	SCL H pulse width (Write)	10	-	ns	
	t_{wrl}	SCL L pulse width (Write)	10	-	ns	
	t_{rc}	Serial clock cycle (Read)	150	-	ns	
	t_{rdh}	SCL H pulse width (Read)	60	-	ns	
	t_{rdl}	SCL L pulse width (Read)	60	-	ns	
D/CX	t_{as}	D/CX setup time	10	-	ns	
	t_{ah}	D/CX hold time (Write/Read)	10	-	ns	
SDA (Input)	t_{ds}	Data setup time (Write)	10	-	ns	
	t_{dh}	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	t_{acc}	Access time (Read)	10	50	ns	For maximum $C_L=30pF$
	t_{od}	Output disable time (Read)	15	50	ns	For minimum $C_L=8pF$

Notes:

1. $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $I_{OVCC} = 1.65\text{V}$ to 3.3V , $V_{CI} = 2.5\text{V}$ to 3.3V , $AGND = DGND = 0\text{V}$, $T = 10\pm 0.5\text{ns}$.
2. Does not include signal rising and falling times.

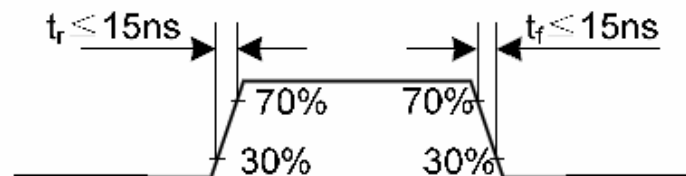


6.4 Parallel RGB Interface Timing Characteristics



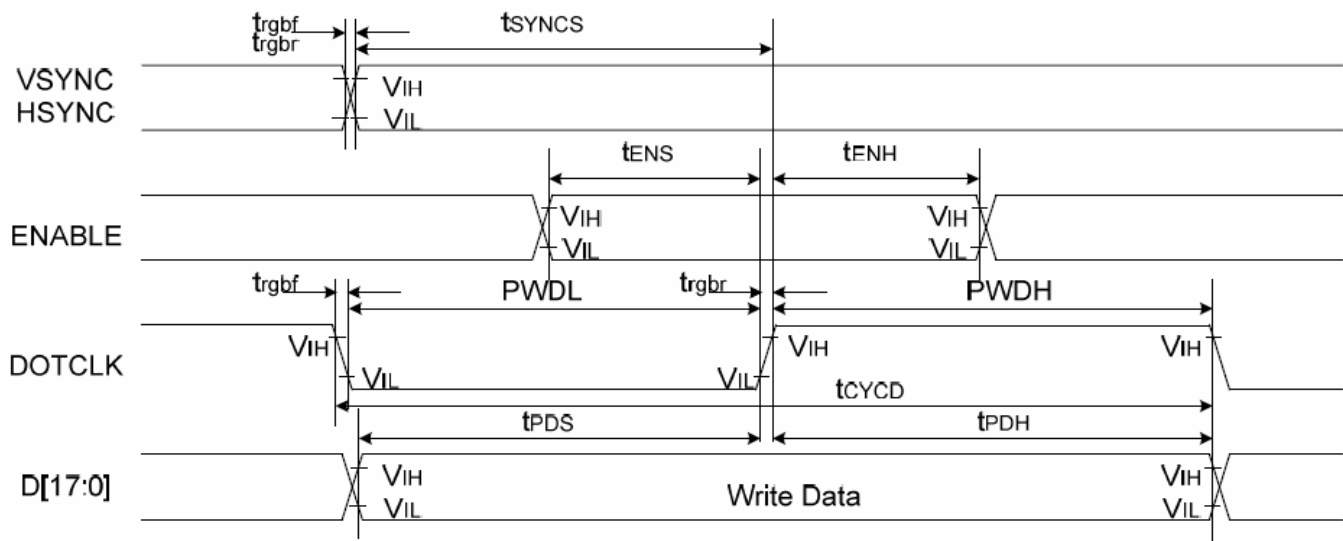
Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	16-/18-/24-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB [23:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	20	-	ns	
	PWDL	DOTCLK low-level period	20	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{RGBF}, t_{RGBR}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	

Note: $T_a = -30$ to 70°C , $IOVCC = 1.65\text{V}$ to 3.3V , $VCI = 2.5\text{V}$ to 3.3V , $AGND = DGND = 0\text{V}$



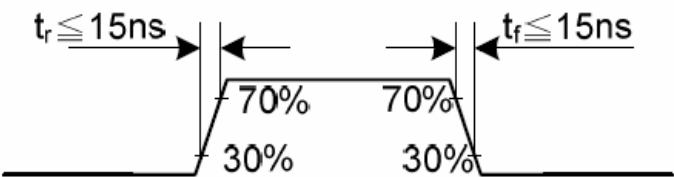


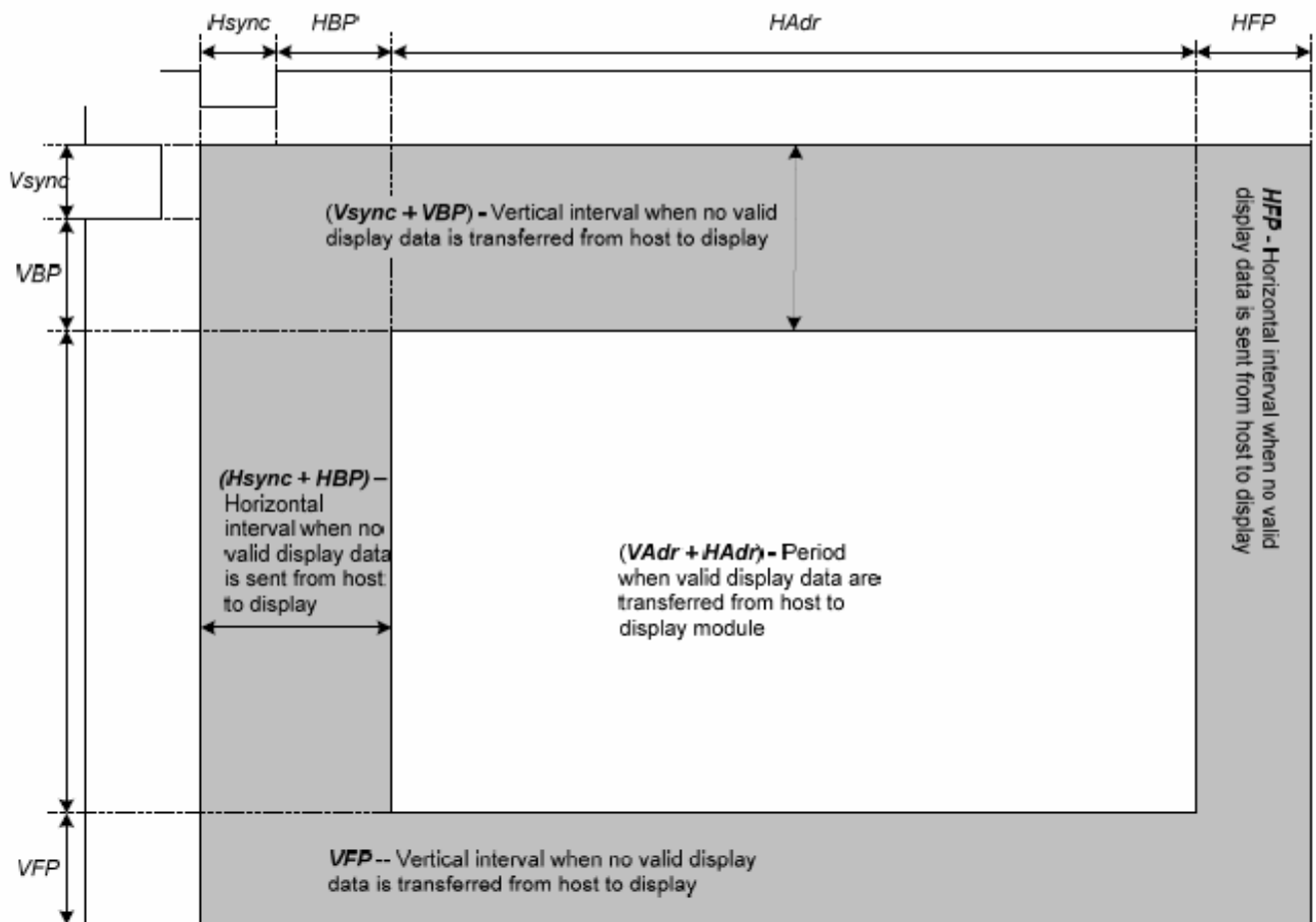
6.5 Parallel 18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	66	-	ns	
	t_{rgbbr}, t_{rgbfr}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	

Note: $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $IOVCC=1.65\text{V}$ to 3.6V , $VCI=2.5\text{V}$ to 3.3V , $AGND=DGND=0\text{V}$



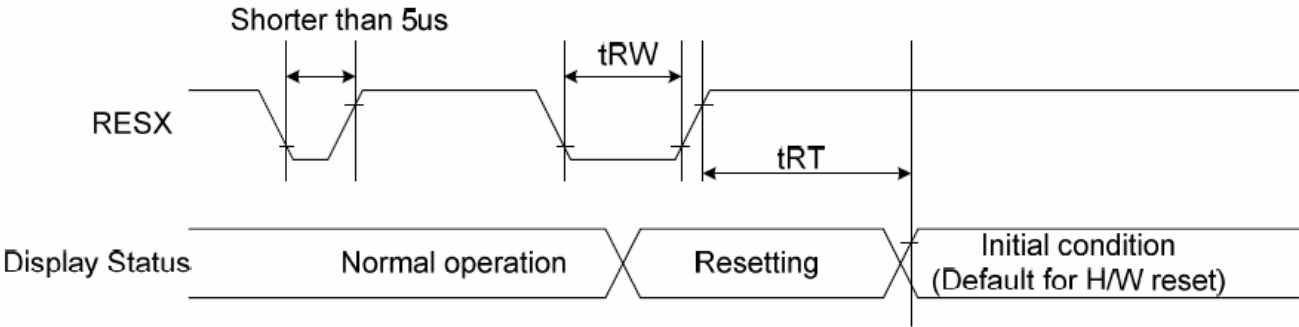


Parameters	Symbols	Min.	Typ.	Max.	Units
PCLK Cycle	PCLK _{CYC}	100	80	66.6	ns
Horizontal Synchronization	Hsync	3	3	-	PCLK
Horizontal Back Porch	HBP	3	3	-	PCLK
Horizontal Address	HAdr	-	320	-	PCLK
Horizontal Front Porch	HFP	3	3	-	PCLK
Vertical Synchronization	Vsync	2	2	-	Line
Vertical Back Porch	VBP	2	2	-	Line
Vertical Address	VAdr	-	480	-	Line
Vertical Front Porch	VFP	2	2	-	Line
Vertical Frequency(*)		50	60	80	Hz
Horizontal Frequency(*)		-	33	-	KHz
PCLK Frequency(*)		10	12.5	15	MHz

Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

6.5 RESET Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

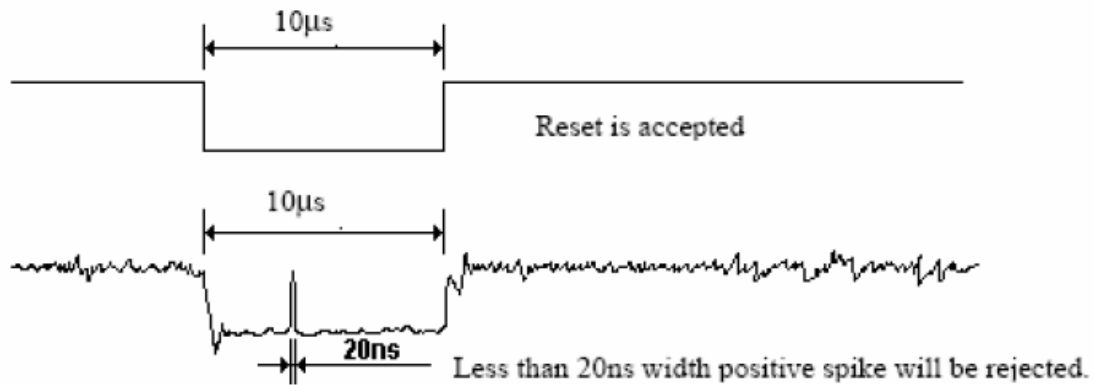
Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts



Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

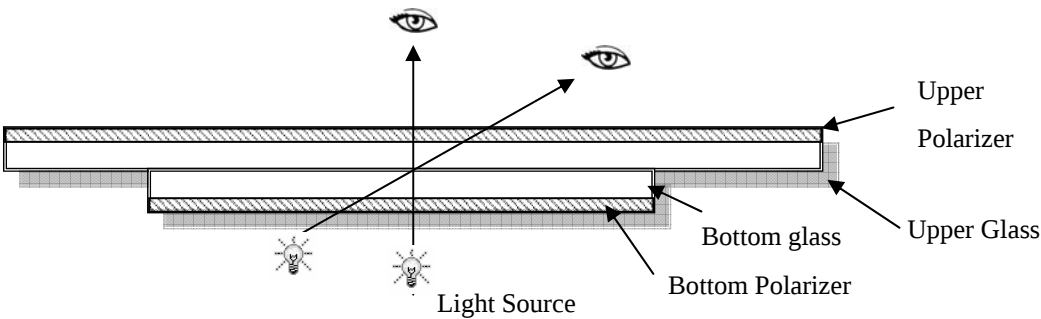
7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

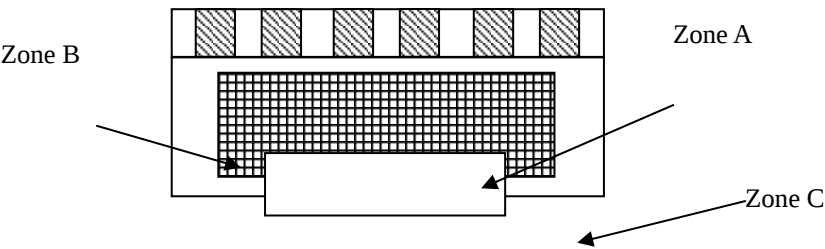
7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

- Temperature : 25±5℃
- Humidity : 65%±10%RH
- Viewing Angle : Normal viewing Angle.
- Illumination: Single fluorescent lamp (300 to 700Lux)
- Viewing distance:30-50cm



7.1.2 Definition



- Zone A : Effective Viewing Area(Character or Digit can be seen)
- Zone B : Viewing Area except Zone A
- Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

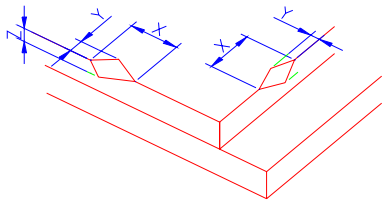
AQL:

Major defect	Minor defect
0.65	1.5

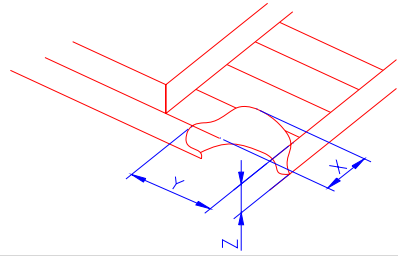
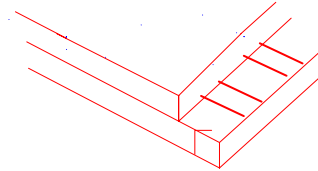
LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

7.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken	(1) The edge of LCD broken	 <table> <tr> <th>X</th><th>Y</th><th>Z</th></tr> <tr> <td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr> </table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
X	Y	Z						
≤3.0mm	<Inner border line of the seal	≤T						
NOTE: X: Length Y: Width Z: Height L: Length of ITO,								



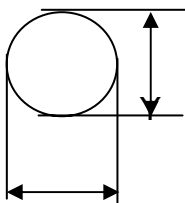
T: Height of LCD	(2)LCD corner broken	 <table border="1" data-bbox="914 546 1327 647"><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T
X	Y	Z						
≤3.0mm	≤L	≤T						
	(3) LCD crack	 Crack Not allowed						

Number	Items	Criteria (mm)
--------	-------	---------------



2.0

Spot defect



X

$$\Phi = (X + Y) / 2$$

① light dot (LCD/TP/Polarizer black/white spot, light dot, pinhole, dent, stain)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.10$	Ignore		Ignore
$0.10 < \Phi \leq 0.15$	3(distance $\geq 10\text{mm}$)		
$0.15 < \Phi \leq 0.2$	1		
$0.2 < \Phi$	0		

② Dim spot (LCD/TP/Polarizer dim dot, light leakage, dark spot)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.1$	Ignore		Ignore
$0.1 < \Phi \leq 0.2$	2(distance $\geq 10\text{mm}$)		
$0.2 < \Phi \leq 0.3$	1		
$\Phi > 0.3$	0		

③ Polarizer accidented spot

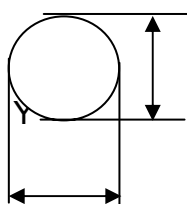
Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		Ignore
$0.2 < \Phi \leq 0.5$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.5$	0		

Line defect
(LCD/TP
/Polarizer
black/white
line, scratch,
stain)

Width(mm)	Length(mm)	Acceptable Qty		
		A	B	C
$\Phi\leq0.03$	Ignore	Ignore		Ignore
$0.03<W\leq0.05$	$L\leq3.0$	$N\leq2$		
$0.05<W\leq0.08$	$L\leq2.0$	$N\leq2$		
$0.08<W$	Define as spot defect			



Items	Criteria (mm)
Spot defect	</

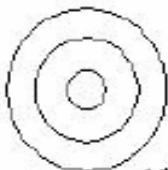
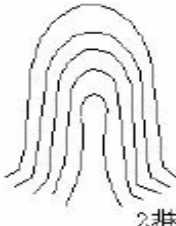
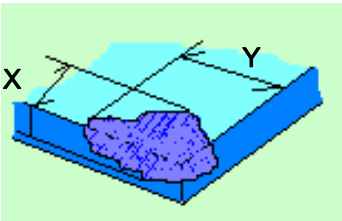
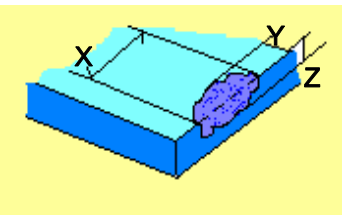


X

$$\Phi = (X + Y) / 2$$



	Line defect (LCD/TP /Polarizer black/white line, scratch, stain)	<table><tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi\leq0.03$</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>$0.03<W\leq0.05$</td><td>$L\leq3.0$</td><td colspan="2">$N\leq2$</td></tr><tr><td>$0.05<W\leq0.08$</td><td>$L\leq2.0$</td><td colspan="2">$N\leq2$</td></tr><tr><td>$0.08<W$</td><td colspan="4">Define as spot defect</td></tr></table>					Width(mm)	Length(mm)	Acceptable Qty			A	B	C	$\Phi\leq0.03$	Ignore	Ignore		Ignore	$0.03<W\leq0.05$	$L\leq3.0$	$N\leq2$		$0.05<W\leq0.08$	$L\leq2.0$	$N\leq2$		$0.08<W$	Define as spot defect			
Width(mm)	Length(mm)	Acceptable Qty																														
		A	B	C																												
$\Phi\leq0.03$	Ignore	Ignore		Ignore																												
$0.03<W\leq0.05$	$L\leq3.0$	$N\leq2$																														
$0.05<W\leq0.08$	$L\leq2.0$	$N\leq2$																														
$0.08<W$	Define as spot defect																															
	Polarizer Bubble	<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi\leq0.2$</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>$0.2<\Phi\leq0.4$</td><td colspan="2">2(distance $\geq 10\text{mm}$)</td></tr><tr><td>$0.4<\Phi\leq0.6$</td><td colspan="2">1</td></tr><tr><td>$0.6<\Phi$</td><td colspan="2">0</td></tr></table>					Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi\leq0.2$	Ignore		Ignore	$0.2<\Phi\leq0.4$	2(distance $\geq 10\text{mm}$)		$0.4<\Phi\leq0.6$	1		$0.6<\Phi$	0							
Zone Size (mm)	Acceptable Qty																															
	A	B	C																													
$\Phi\leq0.2$	Ignore		Ignore																													
$0.2<\Phi\leq0.4$	2(distance $\geq 10\text{mm}$)																															
$0.4<\Phi\leq0.6$	1																															
$0.6<\Phi$	0																															
	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.																														
		TP bubble/ accident spot	<table><tr><th rowspan="2">Size $\Phi(\text{mm})$</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi\leq0.1$</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>$0.1<\Phi\leq0.2$</td><td colspan="2">2 (distance $\geq 10\text{mm}$)</td></tr><tr><td>$0.2<\Phi\leq0.3$</td><td colspan="2">1</td></tr><tr><td>$0.3<\Phi$</td><td colspan="2">0</td></tr></table>				Size $\Phi(\text{mm})$	Acceptable Qty			A	B	C	$\Phi\leq0.1$	Ignore		Ignore	$0.1<\Phi\leq0.2$	2 (distance $\geq 10\text{mm}$)		$0.2<\Phi\leq0.3$	1		$0.3<\Phi$	0							
Size $\Phi(\text{mm})$	Acceptable Qty																															
	A	B	C																													
$\Phi\leq0.1$	Ignore		Ignore																													
$0.1<\Phi\leq0.2$	2 (distance $\geq 10\text{mm}$)																															
$0.2<\Phi\leq0.3$	1																															
$0.3<\Phi$	0																															
		Assembly deflection	beyond the edge of backlight $\leq0.15\text{mm}$																													

5.0	TP Related				 1 规律性			
		Newton Ring	Newton Ring area>1/3 TP area	NG	 2 非规律性			
			Newton Ring area≤1/3 TP area	OK				
						 似牛顿环		
TP corner broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thickness</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	X≤3.0mm	Y≤3.0mm	Z<LCD thickness	
X	Y	Z						
X≤3.0mm	Y≤3.0mm	Z<LCD thickness						
TP edge broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤6.0mm</td><td>Y≤2.0mm</td><td>Z<LCD thickness</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	X≤6.0mm	Y≤2.0mm	Z<LCD thickness	
X	Y	Z						
X≤6.0mm	Y≤2.0mm	Z<LCD thickness						



Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

8. Reliability Test Result

8.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	60℃, 90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	- 30℃, 96HR	3ea	pass	-
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the “Power ON” condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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10.Packing

---TBD----

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