SPECIFICATION
FOR
LCD Module
KD050FM-1

MODULE:	**KD050FM-1**
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2015.01.20

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Data	Rev. No.	Page	Summary
2015.01.13	V1.0	ALL	FIRST ISSUE

Contents

General Description

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 5.0'TFT-LCD contains 480x854 pixels, and can display up to 65K/262K/16.74M colors.

* Features

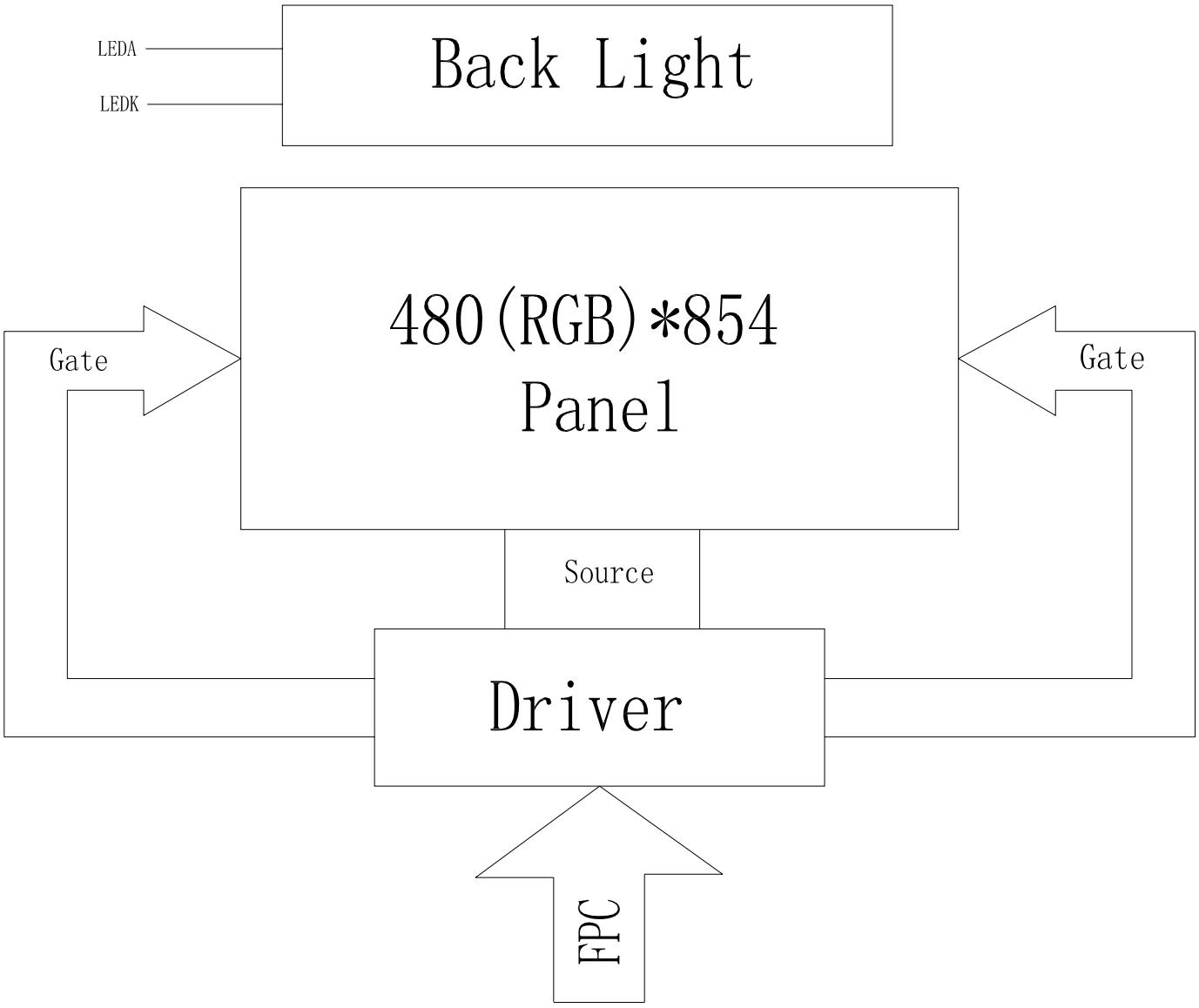
-Low Input Voltage: 3.3V(TYP)
-Display Colors of TFT LCD: 65K/262K/16.7M colors
-Interface: 3-SPI+16/18/24-bits RGB interface.

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	61.56(H)*109.5255(V) (5.0inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K/16.7M	colors	-
Number of pixels	480(RGB)*854	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.12825(H)*0.12825(V)	mm	-
Viewing angle	ALL	o'clock	-
Controller IC	ILI9806E	-	-
Display mode	Transmissive/Normally Black	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

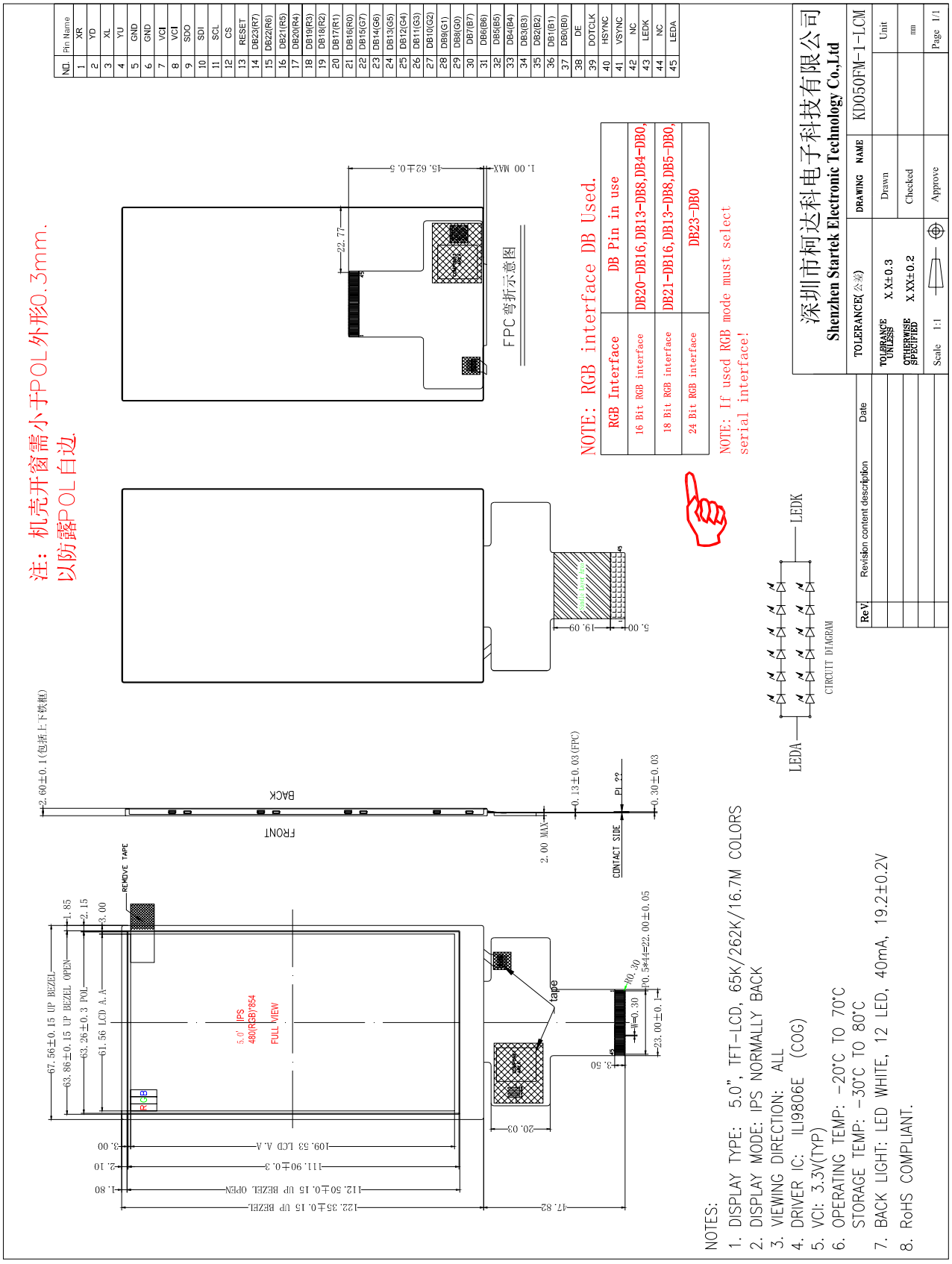
* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		67.56		mm	-
	Vertical(V)		122.35		mm	-
	Depth(D)		2.6		mm	-
Weight			TBD		g	-

1. Block Diagram



2. Outline dimension



3. Input terminal Pin Assignment

Pin NO.	Symbol	Function	I/O
1	XR(NC)	Touch panel Right Glass Terminal	A/D
2	YD(NC)	Touch panel Bottom Film Terminal	A/D
3	XL(NC)	Touch panel LIFT Glass Terminal	A/D
4	YU(NC)	Touch panel Top Film Terminal	A/D
5	GND	Ground.	P
6	GND	Ground.	P
7	VCI	Supply voltage (3.3V).	P
8	VCI	Supply voltage (3.3V).	P
9	SDO	SPI interface output pin.-The data is output on the falling edge of the SCL signal.-If not used, let this pin open.	O
10	SDI	Data lane in 1 data lane serial interface. The data is latched on the rising edge of the SCL signal.	I
11	SCL	This pin is used to select “Data or Command” in the parallel interface. When D/CX = ’1’, data is selected. When D/CX = ’0’, command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4- wire 8-bit serial data interface. fix this pin at VCI or GND when not in use.	I
12	CS	Chip select input pin (“Low” enable). fix this pin at VCI or GND when not in use.	I
13	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.	I
14-37	DB23-DB0	24-bit parallel bi-directional data bus for MCU system and RGB interface mode .Fix to GND level when not in use	I/O
38	DE	Data enable signal for RGB interface peration. fix this pin at VCI or GND when not in use.	I

39	DOTCLK	Dot clock signal for RGB interface operation. Fix this pin at VCI or GND when not in use.	I
40	HSYNC	Line synchronizing signal for RGB interface o peration. fix this pin at VCI or GND when not in use.	I
41	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
42	NC		
43	LEDK	Cathode pin of backlight.	P
44	NC		
45	LEDA	Anode pin of backlight.	P

4. LCD Optical Characteristics

4.1 Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance 1lux and temperature = 25 2℃) with the equipment of Luminance meter system (Goniometer system and TOPCON BM-5) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0 . We refer to θØ=0 (=θ3) as the 3 o‟clock direction (the "right"), θØ=90 (= θ12) as the 12 o‟clock direction ("upward"), θØ=180 (= θ9) as the 9 o‟clock direction ("left") and θØ=270(= θ6) as the 6 o‟clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed.

Optimum viewing angle direction is 6 ‟clock.

4.2 Optical Specifications

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	-	80	-	Deg.	Note 1
		Θ_9		-	80	-	Deg.	
	Vertical	Θ_{12}		-	80	-	Deg.	
		Θ_6		-	80	-	Deg.	
Contrast ratio		CR	Θ = 0°	-	800	-		Note 2
Transmittance		Tr		-	4.5	-	%	Base on C Light Note 3
White Chromaticity		x_w		-	0.298	-		Note 4 CF Glass Base on C Light
		y_w		-	0.328	-		
Reproduction of color (C light)	Red	R_x		-	0.659	-		
		R_y		-	0.322	-		
	Green	G_x		-	0.290	-		
		G_y		-	0.588	-		
	Blue	B_x		-	0.134	-		
		B_y		-	0.124	-		
Response Time (Rising + Falling)		$T_r + T_f$	Ta= 25° C Θ = 0°	-	30	35	ms	Note 5

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer

4. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

5. The electro-optical response time measurements shall be made as FIGURE 3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

Figure 1. The Definition of Vth & Vsat

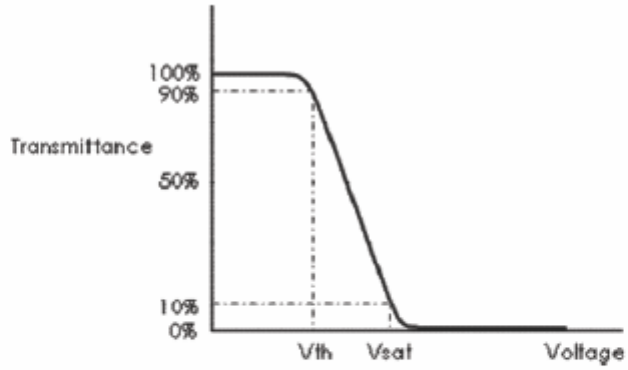


Figure 2. Measurement Set Up

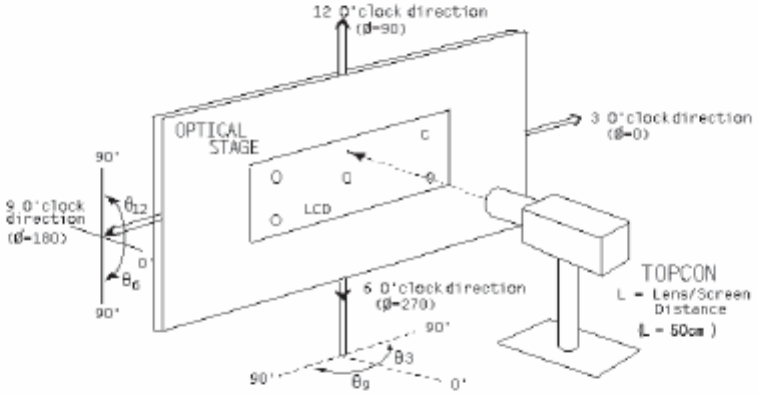
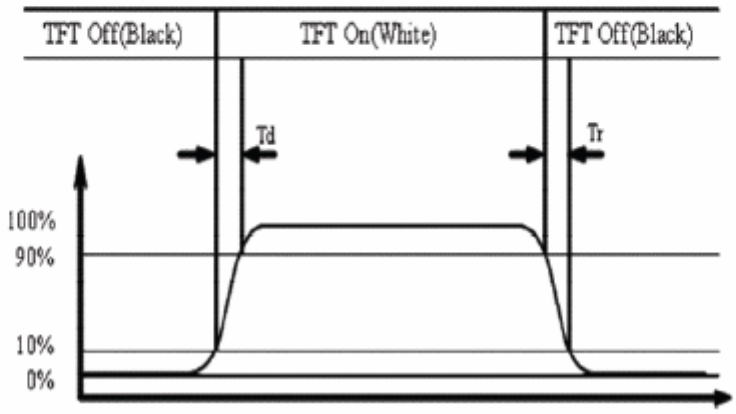


Figure 3. Response Time Testing



5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	5.0	**V**
Digital interface supple Voltage	VDDIO	-0.3	4.0	**V**
Operating temperature	T_{OP}	-20	+70	℃
Storage temperature	T_{ST}	-30	+80	℃

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	3.0	3.3	4.2	V	--
Digital interface supple Voltage	VDDIO	1.65	3.3	4.2	V	--
Normal mode Current consumption	IDD	--	30	--	mA	--
Level input voltage	V_{IH}	$0.7V_{DDIO}$	--	V_{DDIO}	V	--
	V_{IL}	GND	--	$0.3V_{DDIO}$	V	--
Level output voltage	V_{OH}	V_{DDIO}-0.4	--	--	V	--
	V_{OL}	GND	--	GND+0.4	V	--

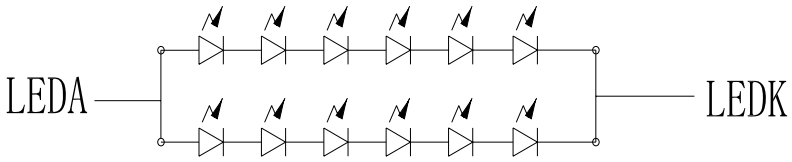
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 12 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	30	40	--	mA	--
Forward Voltage	V_F	--	19.2	--	V	--
LCM Luminance	L_V	450	500	--	cd/m2	I_F=40mA
LED life time	Hr	50000			Hour	Note1,2
Uniformity	AVg	80	--	--	%	--

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

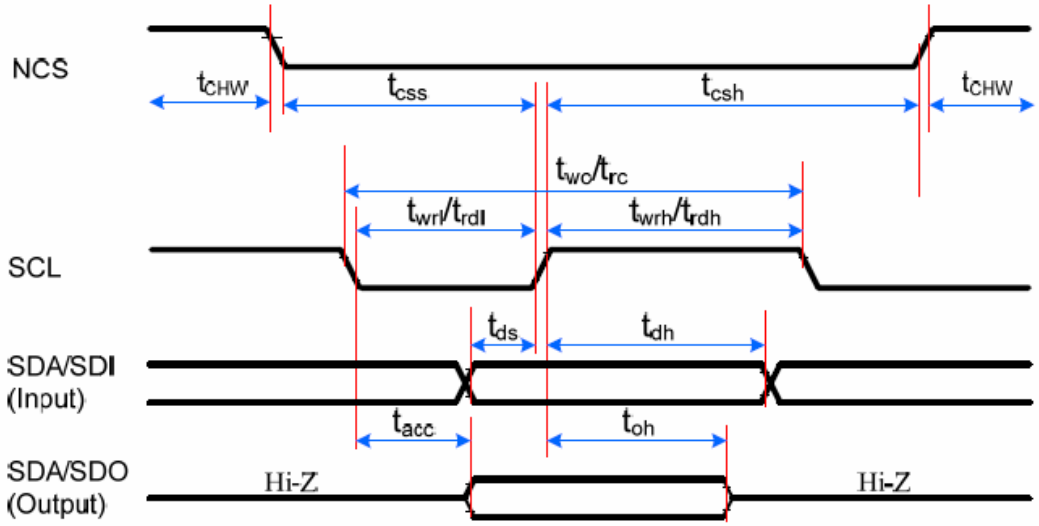
Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.



CIRCUIT DIAGRAM

6. AC Characteristic

6.1 Display Serial Interface Timing Characteristics (3-line SPI system)

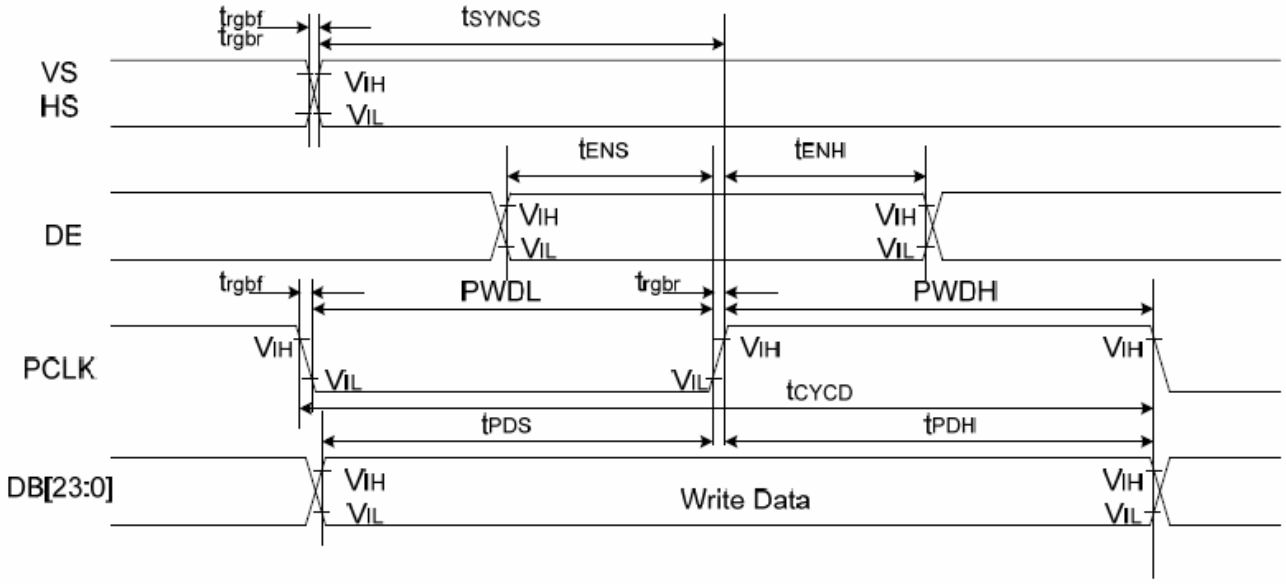


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tcHW	CS "H" pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	30	-	ns	
	twrh	SCL "H" pulse width (Write)	10	-	ns	
	twrl	SCL "L" pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	100	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	100	ns	For minimum CL=8pF
SDA/SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	

Note:

1. Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, T=10+/-0.5ns.
2. Does not include signal rise and fall times.

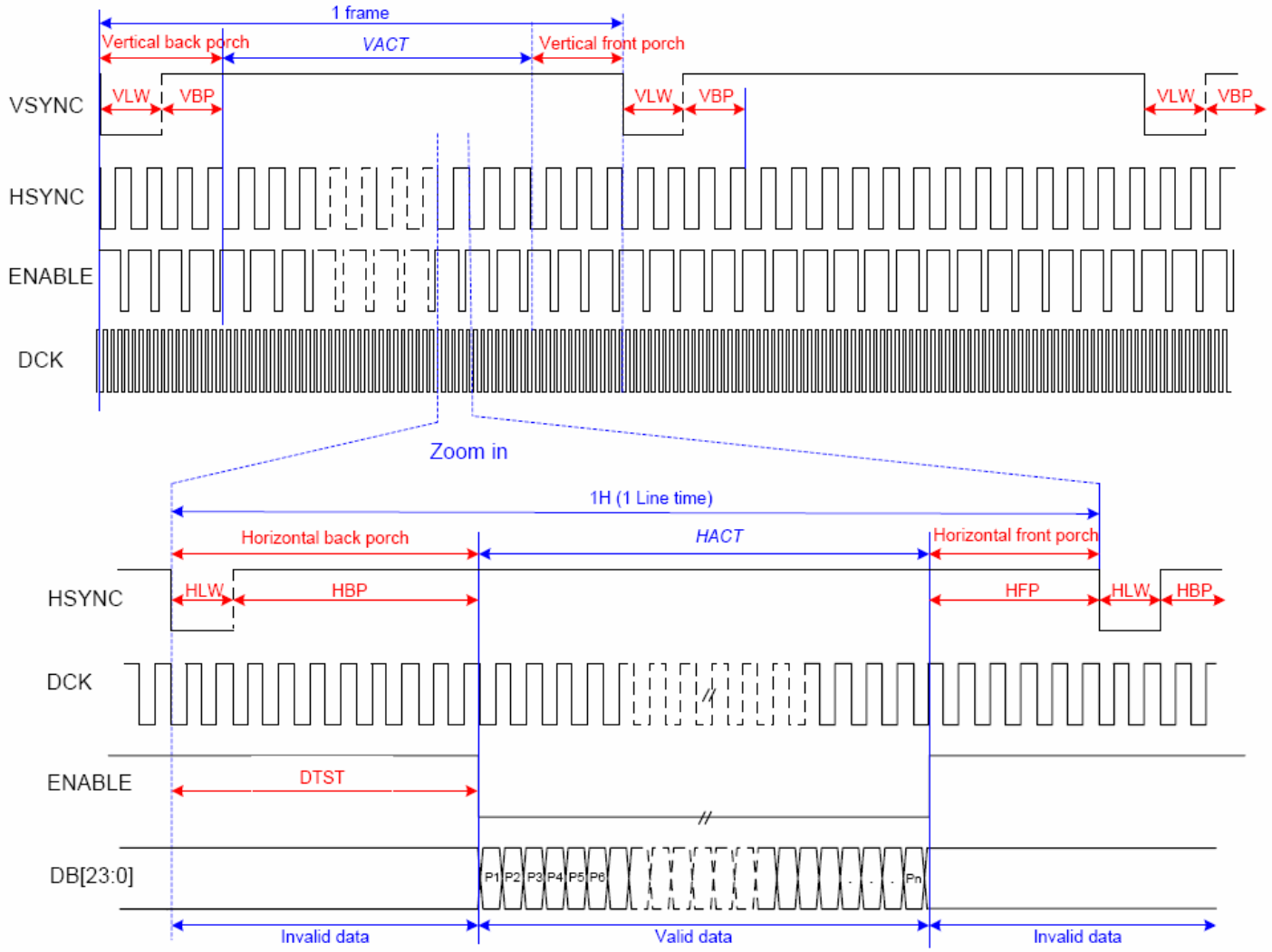
6.2 Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VS/ HS	t_{SYNCS}	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	t_{SYNCH}	VS/HS hold time	5	-	ns	
DE	t_{ENS}	DE setup time	5	-	ns	
	t_{ENH}	DE hold time	5	-	ns	
DB[23:0]	t_{POS}	Data setup time	5	-	ns	
	t_{PDH}	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	13	-	ns	
	PWDL	PCLK low-level period	13	-	ns	
	t_{CYCD}	PCLK cycle time	28	-	ns	
	t_{rgbr} , t_{rgbf}	PCLK,HS,VS rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, DGND=0V

6.3 DPI Interface Timing



VLW : VSYNC Low pulse Width
HLW : HSYNC Low pulse Width
DTST : Data Transfer Startup Time
Pn : pixel 1, pixel 2…, pixel n.

Parameter	Symbols	Condition	Min.	Typ.	Max.	Units
Frame Rate	FR		54		66	fps
Horizontal Low Pulse width	HLW		1		-	DOTCLK
Horizontal Back Porch	HBP		2		126	DOTCLK
Horizontal Address	HACT			480		DOTCLK
Horizontal Front Porch	HFP		2		-	DOTCLK
Vertical Low Pulse width	VLW		1		126	Line
Vertical Back Porch	VBP		1		126	Line
Vertical Address	VACT				864	Line
Vertical Front Porch	VFP		1		255	Line
Data Clock	DCLK		16.6		41.7	MHz

6.4 Reset input timing

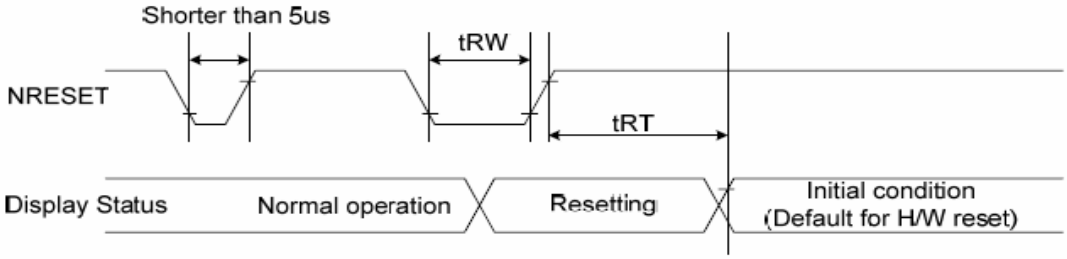


Figure 102 Reset Timing

Table 41 Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5(note 1,5)	ms
				120 (note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 43.

Table 42 Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

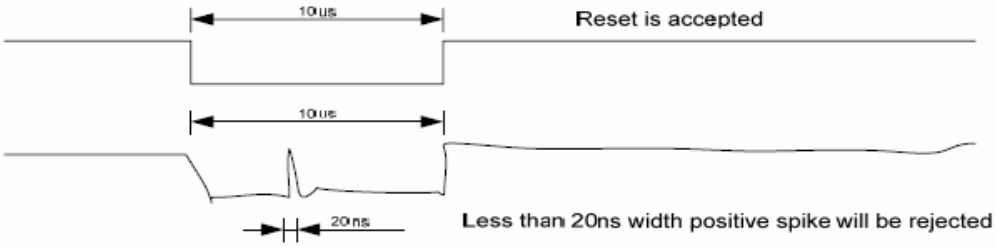


Figure 103 Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

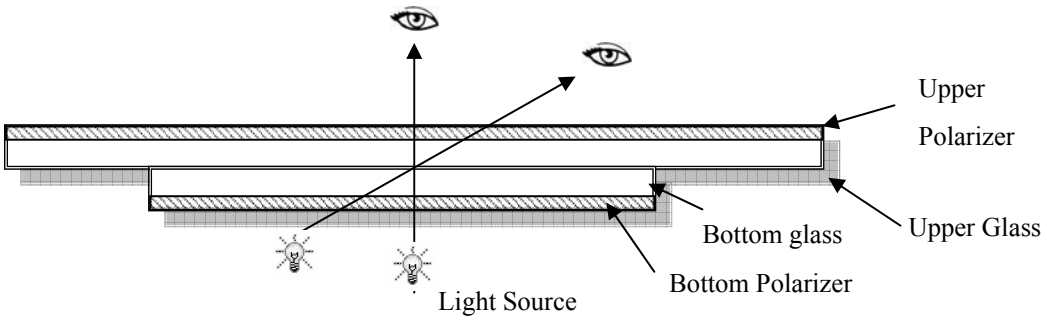
Temperature : 25±5℃

Humidity : 65%±10%RH

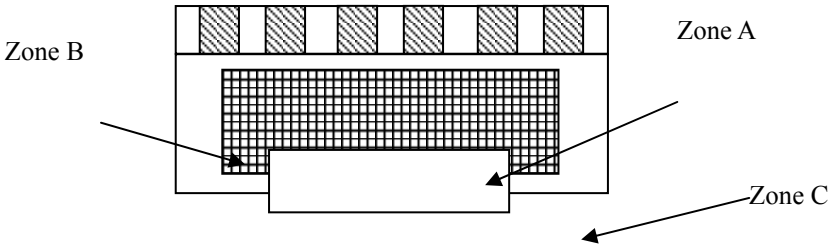
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

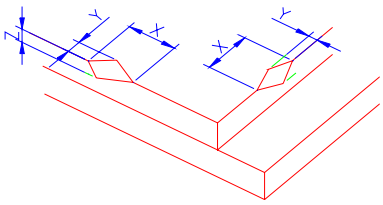
Major defect	Minor defect
0.65	1.5

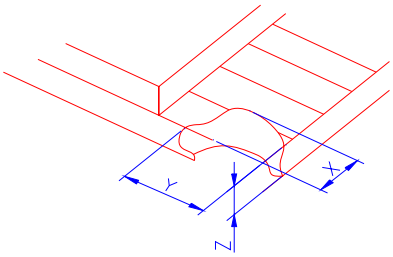
LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

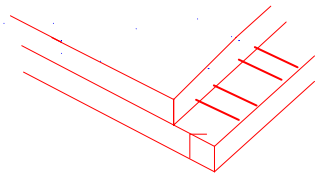
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

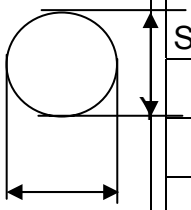
7.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr>
<td>1.0 LCD Crack/Broken

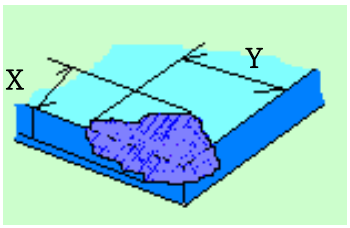
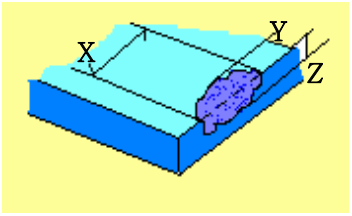
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,</td>
<td>(1) The edge of LCD broken</td>
<td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr>
</table>
</td>
</tr>
</table>

<table>
<tr><td rowspan="2">T: Height of LCD</td><td>(2)LCD corner broken</td><td> 

<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

<table>
<tr><th>Number</th><th>Items</th><th>Criteria (mm)</th></tr>
<tr><td>2.0</td><td>Spot defect
 
X
Φ=(X+Y)/2</td><td>
① light dot（LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain）
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.10</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.15<Φ≤0.2</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.2<Φ≤0.3</td><td colspan="2">1</td></tr>
<tr><td>0.3<Φ</td><td colspan="2">0</td></tr>
</table>
②Dim spot（LCD/TP/Polarizer dim dot, light leakage、dark spot）
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.15<Φ≤0.2</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>0.2<Φ≤0.3</td><td colspan="2">1</td></tr>
<tr><td>Φ＞0.3</td><td colspan="2">0</td></tr>
</table>
③ Polarizer accidented spot
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.2<Φ≤0.5</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>Φ>0.5</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td></td><td>Line defect (LCD/TP /Polarizer black/white line, scratch, stain)</td><td>
<table>
<tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.05</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.05<W≤0.08</td><td>L≤2.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td>3.0</td><td>Polarizer Bubble</td><td>
<table>
<tr><td rowspan="2">Zone
Size (mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.2<Φ≤0.4</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>0.4<Φ≤0.6</td><td colspan="2">1</td></tr>
<tr><td>0.6<Φ</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>4.0</td><td>SMT</td><td>According to IPC-A-610C class Ⅱ standard . Function defect and missing part are major defect ,the others are minor defect.</td></tr>
<tr><td></td><td></td><td>TP bubble/ accidented spot</td><td>
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.2</td><td colspan="2">2（distance≧10mm）</td></tr>
<tr><td>0.2<Φ≤0.3</td><td colspan="2">1</td></tr>
<tr><td>0.3<Φ</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td></td><td></td><td>Assembly deflection</td><td>beyond the edge of backlight ≤0.15mm</td></tr>
</table>

<table>
<tr>
<td rowspan="3">5.0</td>
<td rowspan="3">TP Related</td>
<td>Newton Ring</td>
<td>Newton Ring area>1/3 TP area NG
Newton Ring area≤1/3 TP area OK</td>
<td> 
</td>
</tr>
<tr>
<td>TP corner broken
X：length
Y：width
Z：height</td>
<td>
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thickness</td></tr>
</table>
*
Circuitry broken is not allowed.
</td>
<td> 
</td>
</tr>
<tr>
<td>TP edge broken
X：length
Y：width
Z：height</td>
<td>
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>X≤6.0mm</td><td>Y≤2.0mm</td><td>Z<LCD thickness</td></tr>
</table>
* Circuitry broken is not allowed.
</td>
<td> 
</td>
</tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

8. Reliability Test Result

8.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	60℃, 90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	－30℃, 96HR	3ea	pass	-
ESD test	150pF, 330Ω , ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point	3ea	pass	
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66㎝(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

10.Packing

---TBD----