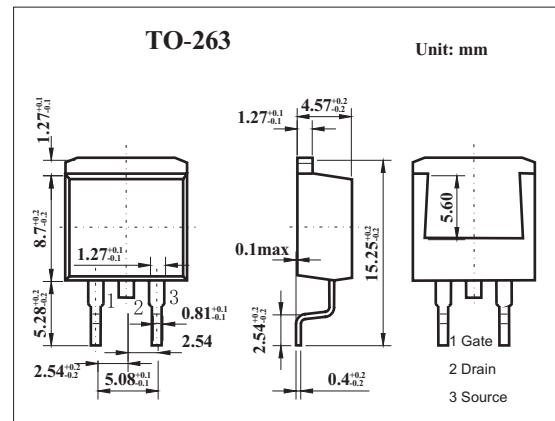
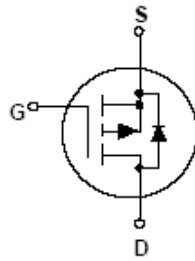


P-Channel 2.5V Specified Enhancement Mode Field Effect Transistor

KDB4020P(FDB4020P)

■ Features

- -16 A, -20 V. $R_{DS(on)} = 0.08 \Omega$ @ $V_{GS} = -4.5$ V
 $R_{DS(on)} = 0.11 \Omega$ @ $V_{GS} = -2.5$ V.
- Critical DC electrical parameters specified at elevated temperature.
- High density cell design for extremely low $R_{DS(on)}$.



■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain to source voltage	V_{DS}	-20	V
Gate to source voltage	V_{GS}	± 8	V
Drain current $T_c=25^\circ\text{C}$	I_D	-16	A
Drain current-pulsed	I_{DP}	-48	A
Power dissipation	P_D	37.5	W
Derate above 25°C		0.25	W/ $^\circ\text{C}$
Thermal Resistance, Junction-to- Case	$R_{\theta JC}$	4	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	40	$^\circ\text{C}/\text{W}$
Channel temperature	T_{ch}	175	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +175	$^\circ\text{C}$

KDB4020P(FDB4020P)

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Drain to source breakdown voltage	V _{DSS}	I _D =250μA, V _{GS} =0V	-20			V
Drain cut-off current	I _{BSS}	V _{DS} =-16V, V _{GS} =0, T _C =25°C			-1	μA
Gate leakage current	I _{GSS}	V _{GS} =±8V, V _{DS} =0V			±100	nA
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-0.4	-0.58	-1	V
Drain to source on-state resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-8A		0.068	0.08	Ω
		V _{GS} =-4.5V, I _D =-8A, T _J =125°C		0.098	0.13	
		V _{GS} =-2.5V, I _D =-7A		0.096	0.110	
On-State Drain Current	I _{D(on)}	V _{GS} = -4.5 V, V _{DS} = -5 V	-20			A
Forward Transconductance	g _{FS}	V _{DS} = -5 V, I _D = -8 A		14		S
Input capacitance	C _{iss}			665		pF
Output capacitance	C _{oss}	V _{DS} =-10V, V _{GS} =0, f=1MHZ		270		pF
Reverse transfer capacitance	C _{rss}			70		pF
Total Gate Charge	Q _g	V _{DS} = -5 V,		9.5	13	nC
Gate-Source Charge	Q _{gs}	I _D = -16 A, V _{GS} = -4.5 V *		1.3		nC
Gate-Drain Charge	Q _{gd}			2.2		nC
Turn-on delay time	t _{on}			8	16	ns
Rise time	t _r	V _{DD} = -5 V, I _D = -1 A,		24	38	ns
Turn-off delay time	t _{off}	V _{GS} = -4.5 V, R _{GEN} = 6 Ω*		50	80	ns
Fall time	t _f			29	45	ns
Maximum Continuous Drain-Source Diode Forward Current	I _S				-16	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				-48	A
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = -16 A *			-1.2	V

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%