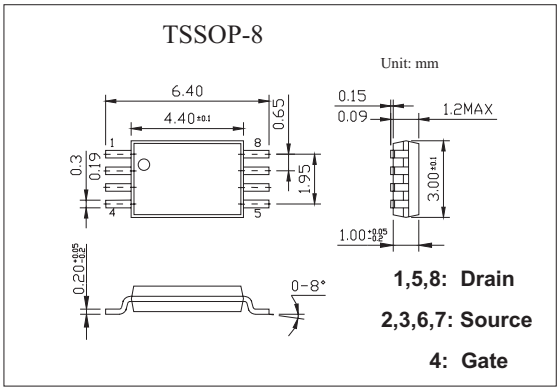
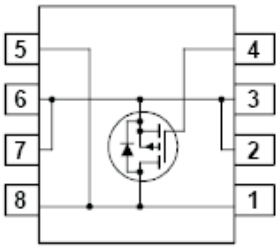
P-Channel 1.8V Specified PowerTrench MOSFET

KDW258P

■ Features

- -9 A, -12 V. $R_{DS(ON)}$ = 11mΩ @ V_{GS} = -4.5 V
  $R_{DS(ON)}$ = 14mΩ @ V_{GS} =-2.5V
  $R_{DS(ON)}$ = 20mΩ @ V_{GS} =-1.8V
- Rds ratings for use with 1.8 V logic
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low gate charge
- Low profile TSSOP-8 package





■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	-12	V
Gate to Source Voltage	V_{GS}	±8	V
Drain Current Continuous (Note 1)	I_D	-9	A
Drain Current Pulsed		-50	A
Power Dissipation for Single Operation (Note 1a)	P_D	1.3	W
Power Dissipation for Single Operation (Note 1b)		0.6	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	℃
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	87	℃/W
Thermal Resistance Junction to Ambient (Note 1b)	$R_{\theta JA}$	114	℃/W

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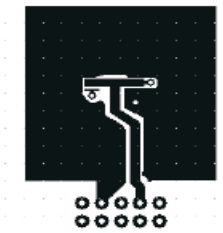
■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = -250 μA	-12			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = -250 μA, Referenced to 25℃		-3		mV/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -10 V, V_{GS} = 0 V			-1	μA
Gate-Body Leakage, Forward	I_{GSSF}	V_{GS} = 8V, V_{DS} = 0 V			100	nA
Gate-Body Leakage, Reverse	I_{GSSR}	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
Gate Threshold Voltage(Not 2)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 μA	-0.4	-0.6	-1.5	V
Gate Threshold Voltage Temperature Coefficient(Not 2)	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = -250 μA, Referenced to 25℃		3		mV/℃
Static Drain-Source On-Resistance(Not 2)	$R_{DS(on)}$	V_{GS} = -4.5 V, I_D =-9 A		8.6	11	mΩ
		V_{GS} = -2.5 V, I_D = -8 A		10.6	14	
		V_{GS} = -1.8 V, I_D = -6.5 A		13.8	20	
		V_{GS} = -4.5 V, I_D =-9 A,TJ = 125℃		11.2	14	
On-State Drain Current	$I_{D(on)}$	V_{GS} = -4.5 V, V_{DS} = -5V	-50			A
Forward Transconductance	g_{FS}	V_{DS} = -5 V, I_D = -9A		50		S
Input Capacitance	C_{iss}	V_{DS} = -5 V, V_{GS} = 0 V,f = 1.0 MHz		5049		pF
Output Capacitance	C_{oss}			1943		pF
Reverse Transfer Capacitance	C_{rss}			1226		pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -6 V, I_D = -1 A,V_{GS} = -4.5 V, R_{GEN} = 6 Ω (Note 2)		17	31	ns
Turn-On Rise Time	t_r			23	37	ns
Turn-Off Delay Time	$t_{d(off)}$			201	322	ns
Turn-Off Fall Time	t_f			148	237	ns
Total Gate Charge	Q_g	V_{DS} = -6 V, I_D =-9 A,V_{GS}=-4.5V(Note 2)		61	73	nC
Gate-Source Charge	Q_{gs}			8		nC
Gate-Drain Charge	Q_{gd}			16		nC
Maximum Continuous Drain-Source Diode Forward Current	I_S				-1.25	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, Is = -1.25A (Not 2)		-0.6	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 87°C/W when mounted on a 1in² pad of 2 oz copper.

b) 114°C/W when mounted on a minimum pad of 2 oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

■ Marking

Marking	258P