			SPEC. No.	TQ3C-8EACO	-E1DKA06-01
			DATE	May 1'	7, 2005
SPEC					
	FO	R :			
	<u> </u>	<u>HG062H</u> V	′1 A H − G O	0	
		C O N T E N T	Ś		
<ol> <li>Application</li> <li>Construction</li> <li>Mechanical S</li> <li>Absolute Max</li> <li>Electrical C</li> <li>Optical Char</li> <li>Circuit Bloc</li> <li>Interface Si</li> <li>Interface Ti</li> <li>Data and Scr</li> <li>Input Timing</li> <li>Supply Volta</li> <li>Backlight Ch</li> <li>Lot Number I</li> <li>Warranty</li> <li>Precautions</li> <li>Reliability</li> <li>Outline Draw</li> </ol>	pecifications imum Ratings characteristics acteristics k Diagram gnals ming Chart een c Characterist ge Sequence C aracteristics dentification for Use Data / Enviro	s ics ondition		Ssued Date: MAY, 2 Stering Kydler Ayato LCD I DCERA CORPORA GOSHIMA HAYATO D DIVISION	Ra Division
	ification is Syocera before		ange without	notice.	
Original	Designed by	:Engineering	Dept.	Confirmed by	y :QA Dept.
Issue Data	Prepared	Checked	Approved	Checked	Approved
November 25, 2003	4. Jamazaki	S. Oshita	M.Fujitani	y. yoshita	RHOJAN

## Caution

- 1. This Kyocera LCD module has been specifically designed for use only in electronic devices in the areas of audio control, office automation, industrial control, home appliances, etc. The modules should not be used in applications where module failure could result in physical harm or loss of life, and Kyocera expressly disclaims any and all liability relating in any way to the use of the module in such applications.
- 2. Customer agrees to indemnify, defend and hold Kyocera harmless from and against any and all actions, claims, losses, damages, liabilities, awards, costs, and expenses, including legal fees, resulting from or arising out of Customer's use, or sale for use, of Kyocera modules in applications.
- 3. Kyocera shall have the right, which Customer hereby acknowledges, to immediately scrap or destroy tooling for Kyocera modules for which no Purchase Orders have been received from the Customer in a two-year period.

		Design	ed by:	Engineering D	lept.	Confirmed by: QA Dept.			
Date		Prepared		Checked Approved		Chec <b>k</b> ed	Approved		
May 17,	2005	y. Yamajaki		S. Oshita	M.F.Jitani	Gegosli Ja	A Hayanto		
Rev. No.	Date		Page		Descriptio	ons			
01	May 17	, 2005	1	1. Applicati ∼Add comme	on nt ″[RoHS Co	ompliance』 "			
			2	3. Mechanica ∼Change "D ∼"Mass" D	l Specificatio ot size″0.0 elete()	$\begin{array}{l} \text{ons} \\ 067 \times 0.221 \rightarrow \end{array}$	0.057×0.211		
			4	5-1. VDD = 5 $\sim$ Delete () $\sim$ Add Frame		X 150 Hz″			
			5	5-2. VDD = 3 $\sim$ Delete () $\sim$ Add Frame		X 150 Hz″			
			6	6. Optical C ~Delete()	characteristics	;			
			9	6-10. Measur $\sim$ Delete	6-10. Measurement method of reflectance ~Delete				
			11	7-1. Power supply $\sim$ Change "Vcont" (+0.8V $\sim$ +2.8V) $\rightarrow$ (+1.2V $\sim$ +2.4V)					
			12	8-1. LCD ~Change LC ~08-6210-	CD connector 020-340-800″-	→ ″08-6210-02	0-340-800+″		
				8-2. CFL ∼Add Recom ″SM02-(8.	mended matchir 0)B-BHS-1-TB(L	ng connector F)(SN) (JST)	"		
			19	13. Backligh ∼Delete ()	t Characterist	ics			
			20	14. Lot Numb ∼Change″Y	er Identificat 'EAR", "CODE"	ion			
			21	<pre>16-1. Installation of the LCD</pre>					
			23	18. Outline ∼Change Dr					

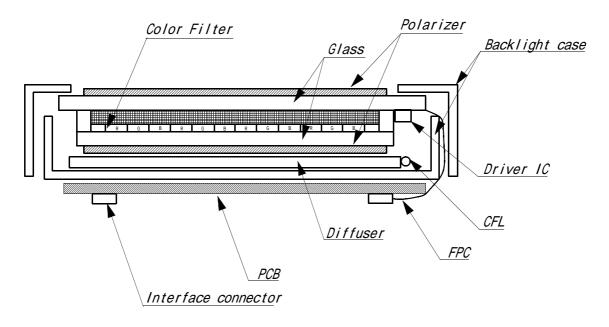
Revision Record

## 1. Application

This data sheet defines the specification for a  $(640 \times R.G.B) \times 240 \text{ dot}$ , STN Transflective color dot matrix type Liquid Crystal Display with CFL backlight. <sup>P</sup>RoHS Compliance<sub>2</sub>

#### 2. Construction and Outline

$(640 \times R.G.B) \times 240$ c	dots, COG type LCD with CFL backlight.
Backlight system	: Side-edge type CFL (1 tube).
Inverter	: Option. Recommended Inverter : PH-BLC08-K2(HITACHI MEDIA ELECTRONICS) or Equivalent.
Polarizer	: Glare treatment.
Additional circuit	: Bias voltage circuit, Randomizing circuit, DC-DC converter



This drawing is showing conception only.

## 3. Mechanical Specifications

ITEM	SPECIFICATION	UNIT
Outline dimensions	174.2 (W) × 73.4 (H) × 7.6 (D) (PCB and components not included.) Refer outline drawing in detail	mm
Effective viewing area	149.8 (W) × 57.4 (H)	mm
Dot number	(640×R.G.B) (₩) × 240 (H)	Dots
Dot size	0.057 (W) × 0.211 (H)	mm
Dot pitch	0.077 (W) × 0.231 (H)	mm
Display color *1	White *2	-
Base color *1	Black *2	-
Mass	135	g

\*1 Due to the characteristics of the LC material, the color vary with environmental temperature.

\*2 Negative-type display Display data "H" :R.G.B Dots ON : White Display data "L" :R.G.B Dots OFF : Black

#### 4. Absolute Maximum Ratings

#### 4-1. Electrical absolute maximum ratings

ITEM	SYMBOL	MIN.	MAX.	UNIT
Supply voltage for logic	VDD	0	6.0	V
Supply voltage for LCD driving	VCONT	0	VDD	V
Input signal voltage *1	Vin	0	VDD	V
FRM frequency	fFRM	-	150	Hz

\*1 Input signal : CP, LOAD, FRM, DISP, D0~D7

#### 4-2. Environmental absolute maximum ratings

ITEM		SYMBOL	MIN	MAX	UNIT
Operating temperature	*1	Тор	0	50	
Storage temperature	*2	Tsto	-20	60	
Operating humidity	*3	Нор	10	*4	%RH
Storage humidity	*3	Нsтo	10	*4	%RH
Vibration		-	*5	*5	-
Shock		-	*6	*6	-

\*1 LCD's display quality shall not be guaranteed at the temperature range of : below 0 and upper 40 .

\*2 Temp. = -20 < 48 h , Temp = 60 < 168 h Store LCD panel at normal temperature/humidity. Keep it free from vibration and shock. LCD panel that is kept at low or high temperature for a long time can be defective due to the other conditions, even if the temperature satisfies standard. (Please refers to 16. Precautions for use as detail)

\*3 Non-condensation.

\*4 Temp. 40 , 85% RH Max.

```
Temp. > 40 , Absolute Humidity shall be less than 85%RH at 40 .
```

```
*5
```

Frequency	10~55 Hz	Converted to acceleration value :
Vibration width	0.15 mm	$(0.3 \sim 9 \text{ m/s}^2)$
Interval	10-55-10 Hz	1 minute

2 hours in each direction X/Y/Z (6 hours as total) EIAJ ED-2531

```
*6 Acceleration: 490m/s<sup>2</sup>
Pulse width : 11 ms
3 times in each direction : ±X/±Y/±Z.
EIAJ ED-2531
```

#### 5. Electrical Characteristics

5-1.	VDD=5.0V
• • •	100-0.01

5-1. VD=5.0V			VDD =	+5.0V ± 5%	, Temp. = $0^{-1}$	~ 50
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage for logic	VDD	-	4.75	5.00	5.25	V
LCD driving voltage *1	Vop=	0	1.20	-	-	V
	VCONT	25	1.30	1.80	2.30	V
		50	-	-	2.40	V
Input voltage	Vin	"H" level	0.8VDD	-	VDD	V
(FRM,LOAD,CP,DISP,D0~D7)		"L" level	0	-	0.2VDD	V
Input current	lin	Input signal	-100	-	100	μA
Rush current for logic	Irush	When rush current happens		3.0A(Peak) × 1ms		
Clock frequency	f cp	-	4.03	4.32	10.00	MHz
Frame frequency *2	f <sub>FRM</sub>	-	70	75	150	Hz
Current consumption for logic	IDD	*3	-	40	60	mA
Power consumption	Pdisp		-	200	300	mW

\*1 Maximum contrast ratio is obtained by adjusting the LCD supply voltage (Vop = VCONT) for driving LCD.

- \*2 In consideration of display quality, it is recommended that frame frequency is set in the range of 70-80Hz. When you have to use higher frame and clock frequencies, confirm the LCD's performance and quality prior to finalizing the frequency values: Generally, as frame and clock frequencies become higher current consumption will get bigger and display quality will be degraded.
- \*3 Display high frequency pattern, ( see below ). Vop = VCONT, f FRM = 75 Hz, fcp = 4.32MHz, Temp. = 25 Pattern:

1 2 3 4 5 6 \_\_\_\_\_ 1920(dot) 1 2 3 : 239 240 (dot)

#### 5-2. VDD=3.3V

VDD	=	+3.3V	±	0.3V,	Temp.	=	0~50
-----	---	-------	---	-------	-------	---	------

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage for logic	VDD	-	3.0	3.3	3.6	V
LCD driving voltage *1	Vop=	0	1.20	-	-	V
	VCONT	25	1.30	1.80	2.30	V
		50	-	-	2.40	V
	Vin	"H" level	0.8VDD	-	VDD	V
(FRM,LOAD,CP,DISP,D0~D7)		"L" level	0	-	0.2VDD	V
Input current	lin	Input signal	-100	-	100	μA
Rush current for logic	Irush	When rush current happens	3.0A(Peak) × 1ms			
Clock frequency	f cp	-	4.03	4.32	10.00	MHz
Frame frequency *2	f <sub>FRM</sub>	-	70	75	150	Hz
Current consumption for logic	IDD	*3	-	55	83	mA
Power consumption	Pdisp		-	182	274	mW

\*1 Maximum contrast ratio is obtained by adjusting the LCD supply voltage (Vop= VCONT) for driving LCD.

\*2 In consideration of display quality, it is recommended that frame frequency is set in the range of 70-80Hz. When you have to use higher frame and clock frequencies, confirm the LCD's performance and quality prior to finalizing the frequency values: Generally, as frame and clock frequencies become higher current consumption will get bigger and display quality will be degraded.

\*3 Display high frequency pattern, ( see below ). Vop = VCONT , f FRM = 75 Hz , fcp = 4.32MHz, Temp. = 25 Pattern:

> 1 2 3 4 5 6 \_\_\_\_\_ 1920(dot) 1 2 3 : 239 240 (dot)

#### 6 . Optical Characteristics

#### 6-1. Reflective mode

Measuring Spot = 6mm , Temp. = 25

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Response	Rise	Tr	= =0 °	-	190	290	ms
time	Down	Td	= =0 °	-	180	280	ms
Contrast rat	io	CR	= =0 °	5.0	10.0	-	-
Reflectance			-	15.0	30.0	-	%

Optimum contrast is obtained by adjusting the LCD driving voltage(Vop) while at the viewing angle of  $= 0^{\circ}$ .

#### 6-2. Transmissive mode

Temp.	= 25	,
-------	------	---

ITE	Λ	SYMBOL	COND	ITION	MIN.	TYP.	MAX.	UNIT
Response	Rise	Tr	=	=0 °	-	190	290	ms
time	Down	Td	=	=0 °	-	180	280	ms
Viewing angle	e range			Upper	-	30	-	-1
			00 0	Lower	-	20	-	deg.
			CR 2	Left	-	45	-	
				Right	-	45	-	deg.
Contrast rati	Contrast ratio		=	=0 °	10.0	20.0	-	-
Brightness	Brightness		IL=5.0mA		35	55	-	cd/m <sup>2</sup>
Chromaticity	Red	x		=0 °	0.35	0.40	0.45	
coordinates		у	=	=0 5	0.22	0.27	0.32	
	Green	x		0.0	0.22	0.27	0.32	
		у	=	=0 °	0.30	0.35	0.40	
	Blue	x		0.9	0.15	0.20	0.25	-
		у	=	=0 °	0.16	0.21	0.26	
	White	x		0.9	0.23	0.28	0.33	
		у	=	=0 °	0.24	0.29	0.34	

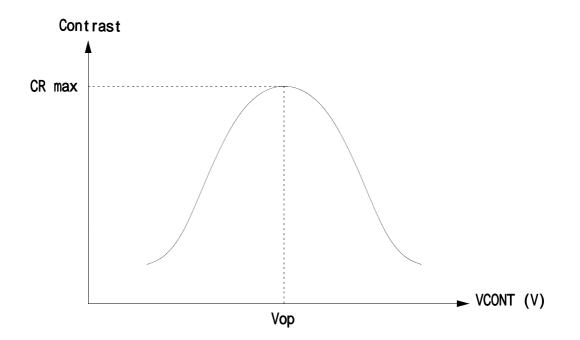
Optimum contrast is obtained by adjusting the LCD driving voltage(Vop) while at the viewing angle of  $= = 0^{\circ}$ .

6-3. Definition of Reflectance

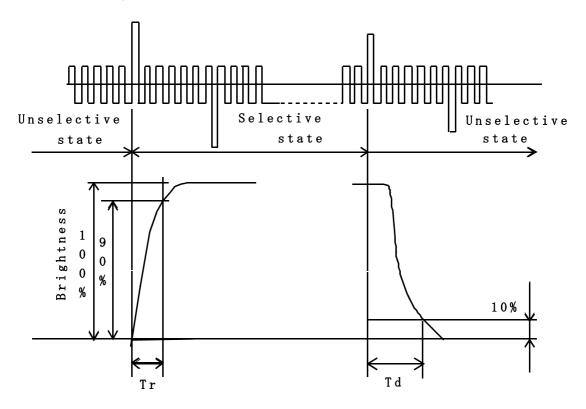
6-4. Definition of Contrast (Reflective Mode)

6-5. Definition of Contrast (Transmissive Mode)

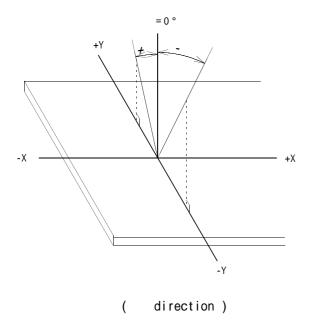
6-6. Definition of Vop

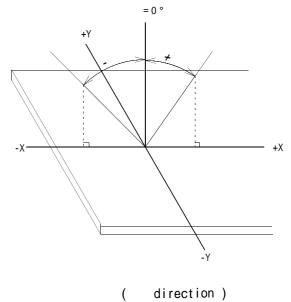


6-7. Definition of response time



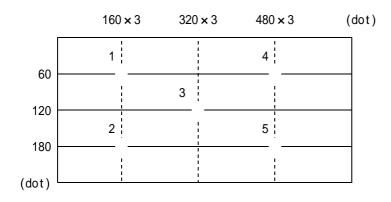
6-8. Definition of viewing angle





direction )

#### 6-9. Measuring points

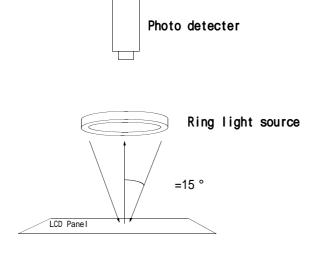


- 1) Rating is defined as the average brightness inside the viewing area.
- 2) 30 minutes after CFL is turned on. (Ambient Temp.= 25 )
- 3) The inverter should meet the eccentric conditions;

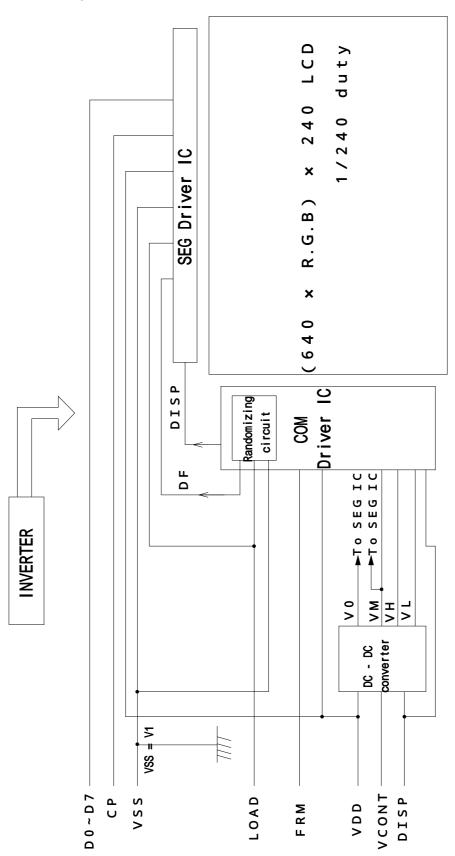
-Sine, symmetric waveform without spike in positive and negative.

4) Measuring Inverter ; PH-BLC08-K2(HITACHI MEDIA ELECTRONICS)

#### 6-10. Measurement method of reflectance (Reflectance)

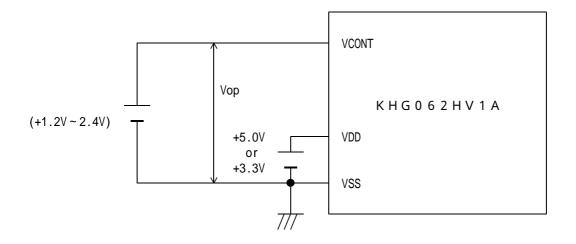


## 7. Circuit Block Diagram



- 10 -

## 7-1. Power supply



## 8. Interface signals

## 8-1. LCD

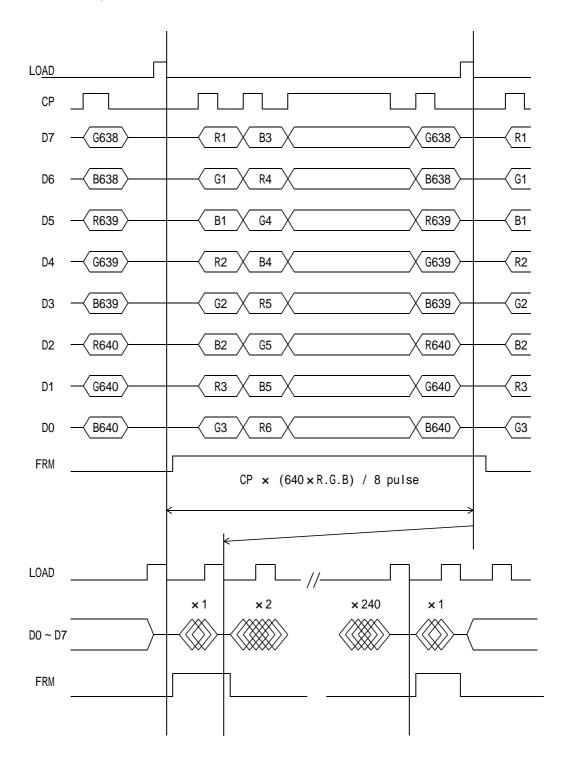
PIN	SYMBOL	DESCRIPTION	LEVEL
1	FRM	Synchronous signal for driving scanning line	Н
2	LOAD	Data signal latch clock	H L
3	CP	Data signal shift clock	H L
4	DISP	Display control signal	H(ON),L(OFF)
5	VDD	Power supply for logic	
6	VSS	GND	
7	VCONT	LCD adjust voltage	
8	D7		
9	D6		
10	D5		
11	D4	Display data	H(ON),L(OFF)
12	D3		
13	D2		
14	D1		
15	DO		
16	VDD	Power supply for logic	-
17	VDD		
18	VSS	GND	
19	VSS		-
20	VSS		

LCD connector : 08-6210-020-340-800+ (ELCO) Recommended matching connector : 0.5mm pitch FFC or FPC

#### 8-2. CFL

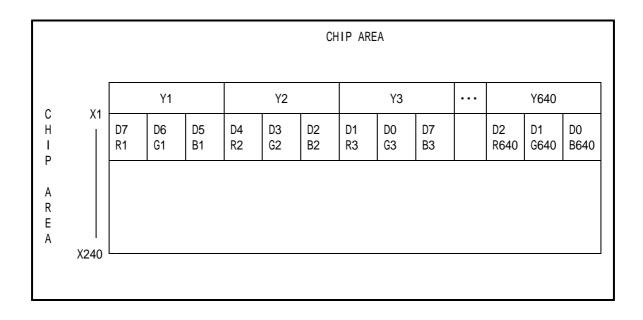
PIN	SYMBOL	DESCRIPTION		
1	HOT	Inverter output high voltage side		
2	NC			
3	COLD	Inverter output low voltage side		
LCD side c Recommende	connector d matching con	: BHR-03VS-1 (JST) nector : SM02-(8.0)B-BHS-1 (JST) : SM02-(8.0)B-BHS-1-TB(LF)(SN) (JST) ••• (Re	oHS)	

## 9 . Interface Timing Chart



- \* The cycle of load signal should be stable and continuously applied without interruption.
- \* The above-mentioned timing chart shows a reference to set up a LCD module, not an electrical rating.

## 10. Data and Screen



# t rCP t f CP tWCLH tWCLL tCCL СР tDS t DH DATA tCDLD СР 1st last 1st tLDCR tWLPH t LCL LOAD tWLPL tr t f tFS t FH FRM

## 1 1. Input Timing Characteristics

## 11-1. Switching characteristics (VDD=5.0V)

SYMBOL	MIN.	MAX.	UNIT
tCCL	100	-	ns
tWCLH	30	-	ns
tWCLL	30	-	ns
t rCP	-	15	ns
t f CP	-	15	ns
tDS	25	-	ns
t DH	25	-	ns
tWLPH	40	-	ns
tWLPL	400	-	ns
tLCL	500	-	ns
tCDLD	60	-	ns
t LDCR	60	-	ns
tr	-	20	ns
tf	-	20	ns
tFS	120	-	ns
tFH	30	-	ns
	t CCL tWCLH tWCLL trCP tfCP tDS tDH tWLPH tWLPH tWLPL tLCL tCDLD tLDCR tr tf	t CCL       100         t WCLH       30         t WCLL       30         t rCP       -         t fCP       -         t fCP       -         t DS       25         t DH       25         t WLPH       40         t WLPL       400         t LCL       500         t CDLD       60         t r       -         t f       -         t f       -         t f       -         t f       -         t f       -         t f       -         t f       -	t CCL         100         -           t WCLH         30         -           t WCLL         30         -           t WCLL         30         -           t T CP         -         15           t f CP         -         15           t DS         25         -           t DH         25         -           t WLPH         40         -           t WLPL         400         -           t LCL         500         -           t LCL         60         -           t LDCR         60         -           t f         -         20           t f         -         20           t FS         120         -

Input Characteristics ; VDD = +5.0V  $\pm$  5%, Temp. = 0~50

\*1 CP Cycle is adjust so that FRM signal is 75Hz.

\*2 LOAD Cycle is constant.

## 11-2. Switching characteristics (VDD=3.3V)

ITEM	SYMBOL	MIN.	MAX.	UNIT
CP Cycle *1	tCCL	100	-	ns
CP "H" Pulse Width	tWCLH	40	-	ns
CP "L" Pulse Width	tWCLL	40	-	ns
CP Rise Up Time	t r CP	-	20	ns
CP Fall Down Time	t f CP	-	20	ns
Data Set Up Time	tDS	35	-	ns
Data Hold Time	t DH	35	-	ns
LOAD "H" Pulse Width	tWLPH	50	-	ns
LOAD "L" Pulse Width	tWLPL	400	-	ns
LOAD Cycle *2	tLCL	500	-	ns
CP Down LOAD Down Delay Time	tCDLD	60	-	ns
LOAD Down CP Rise Delay Time	t LDCR	80	-	ns
Input Signal Rise Up Time	tr	-	20	ns
Input Signal Fall Down Time	tf	-	20	ns
FRM Data Set Up Time	tFS	120	-	ns
FRM Data Hold Time	tFH	30	-	ns

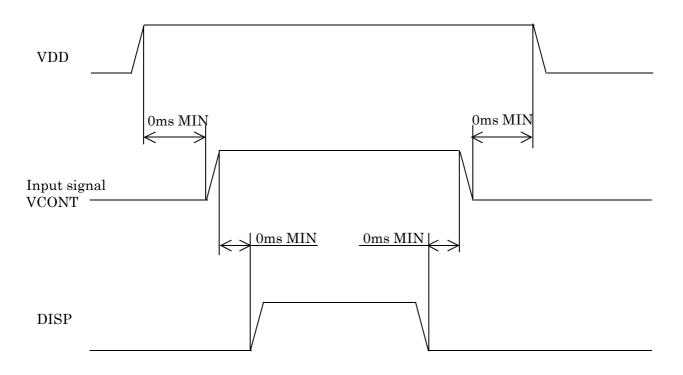
Input Characteristics ; VDD = +3.3V  $\pm$  0.3V, Temp. = 0~50

\*1 CP Cycle is adjust so that FRM signal is 75Hz.

\*2 LOAD Cycle is constant.

#### 1 2. Supply Voltage Sequence Condition

<u>DO NOT</u> apply DC voltage to the LCD panel. DC voltage induce irreversible electrochemical reactions and reduce LCD life. Always follow the power supply ON/OFF sequence of VDD first, input signal second, VCONT third and finally DISP. This will prevent DC driving of the LCD or CMOS LSI latch up as shown below.



- \* Input signal : CP,LOAD,FRM,VCONT,D0~D7 Each signal(CP,LOAD,FRM)is constant
- \* The above sequence should be designed as to keep each normal figure on condition that liquid crystal module is loaded on your system.
- \* Control the supply voltage sequence not to float all signal line when the LCD panel is driving.

#### 1 3. Backlight Characteristics

Temp.= 25

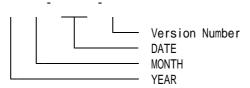
ITEM	SYMBOL	MIN.	TYP.	MAX.	NOTE
Starting	VS	-	-	965 Vrms.	0
discharge Voltage *1	vo	-	-	645 Vrms.	25
Discharging tube current *2,*3	IL	2.0 mArms.	5.0 mArms.	6.0 mArms.	-
Discharging tube voltage	VL	-	395 Vrms.	-	-
Operating life *4 (IL=5.0 mArms.)	Т	36,000 h	54,000 h	-	-
Operating frequency	F	40 kHz	-	100 kHz	-

- \*1 The Non-load output voltage (VS) of the inverter should be designed to have some margin, because VS may increase due to the leak current which may be caused by wiring of CFL cables. (Reference value: 1255 Vrms MIN.)
- \*2 We recommend that you should set the discharging tube current at lower than typical value so as to prevent the heat accumulation of CFL tube from deteriorating a performance of the LCD.
- \*3 Do not apply more than 6.0mA discharging tube current. Because CFL maybe broken due to over current.
- \*4 When the illuminance or quantity of light has decreased to 50 % of the initial value. Average life time of CFL will be decreased when LCD is operating at lower and higher temperature.
- \* The inverter should meet the eccentric conditions ; sine, symmetric waveform without spike in positive and negative.

#### 14. Lot Number Identification

The lot number shall be indicated on the back of the backlight case of each LCD.

KHG062HV1AH-G00-



YEAR	2005	2006	2007	2008	2009	2010
CODE	5	6	7	8	9	0
MONTH	JAN.	FEB.	MAR.	APR.	MAY	JUN.
CODE	1	2	3	4	5	6
MONTH	JUL.	AUG.	SEP.	OCT.	NOV.	DEC.
CODE	7	8	9	Х	Y	Z

#### 1 5 . Warranty

#### 15-1. Incoming inspection

Please inspect the LCD within one month after your receipt.

#### 15-2. Production Warranty

Kyocera warrants its LCDs for a period of 12 months after receipt by the purchaser, and within the limits specified. Kyocera shall, by mutual agreement, replace or rework defective LCDs that are shown to be Kyocera's responsibility.

#### 1 6 . Precautions for use

16-1. Installation of the LCD

- 1. LCD hole(right side) are not connected with GND, but the LCD is structured to have GND connection available to protect against noise. We recommend to connect customer's frame GND to LCD frame in order to stabilize the display performance.
- 2. A transparent protection plate shall be added to protect the LCD and its polarizers.
- 3. The LCD shall be installed so that there is no pressure on the LSI chips.
- 4. The LCD shall be installed flat, without twisting or bending.
- 5. The display window size should be the same as the effective viewing area.
- 6. In case you use outside frame of effective viewing area as outward appearance of your product, unevenness of its outward appearance is out of guarantee.
- 7. Do not pull the CFL lead wires and do not bend the root of the wires. Housing should be designed to protect CFL lead wires from external stress.
- 8. This Kyocera LCD module has been specifically designed for use in general electronic devices, but not for use in a special environment such as usage in an active gas. Hence, when the LCD is supposed to be used in a special environment, evaluate the LCD thoroughly beforehand and do not expose the LCD to chemicals such as an active gas.
- 16-2. Static Electricity
- 1. Since CMOS ICs are mounted directly onto the LCD glass, protection from static electricity is required. Operation should wear ground straps.

16-3. LCD Operation

- 1. The LCD shall be operated within the limits specified. Operation at values outside of these limits may shorten life, and/or harm display images.
- 2. Adjust "LCD driving voltage" to obtain optimum viewing angle and contrast.
- 3. Operation of the LCD at temperature below the limit specified may cause image degradation and/or bubbles.

It may also change the characteristics of the liquid crystal.

This phenomenon may not recover. The LCD shall be operated within the temperature limits specified.

16-4. Storage

- 1. The LCD shall be stored within the temperature and humidity limits specified. Store in a dark area, and protected the LCD from direct sunlight or fluorescent light.
- 2. Always store the LCD so that it is free from external pressure onto it.

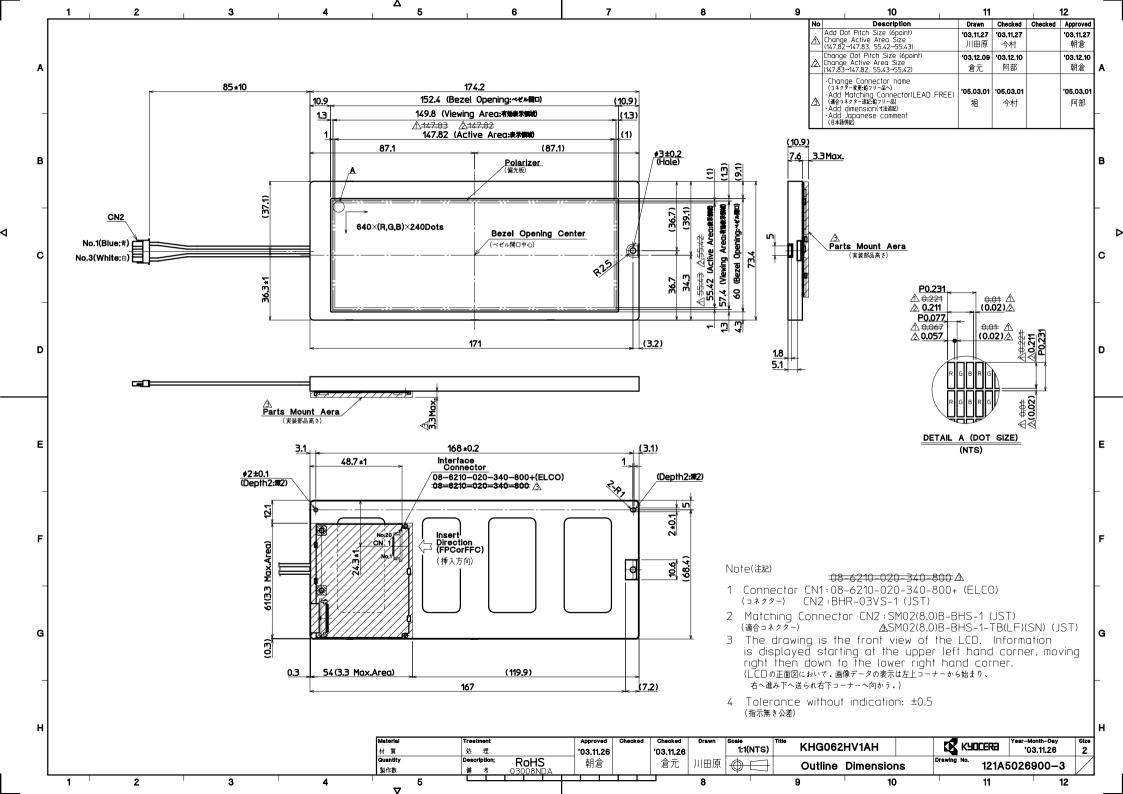
16-5. Screen Surface

- 1. DO NOT store in a high humidity environment for extended periods. Image degradation, bubbles, and/or peeling off of polarizer may result.
- 2. The front polarizer is easily scratched or damaged. Prevent touching it with
- any hard material, and from being pushed or rubbed.
- 3. The LCD screen may be cleaned with a soft cloth or cotton pad. Methanol, or Isopropyl Alcohol may be used, but insure that all solvent residue is removed.
- 4. Water may cause damage or discoloration of the polarizer. Clean any condensation or moisture from any source immediately.
- 5. Always keep the LCD free from condensation during testing. Condensation may permanently spot or stain the polarizers.
- 6. Please do not use solid-base image pattern for long hours because a temporary afterimage may appear. We recommend to use screen saver etc. in cases where a solid-base image pattern must be used.
- 7. Liquid crystal may leak when the module is broken. Be careful not to let the fluid go into your eyes and mouth. In the case the fluid touches your body, rinse it off right away with water and soap.

## 17. Reliability Data / Environmental Test

TEST ITEM	TEST CONDITION	TEST TIME	RESULT
High Temp. Atmosphere	70	240 h	Display Quality : No defect Display Function : No defect Current Consumption : No defect
Low Temp. Atmosphere	-20	240 h	Low Temp. Bubble : None Solid Crystallization of Liquid Crystal : None Display Quality : No defect Display Function : No defect Current Consumption : No defect
High Temp. Humidity Atmosphere	40 90%RH	240 h	Display Quality : No defect Display Function : No defect Peel-off of Organic Sealing : None Current Consumption : No defect
Temp. Cycle	-20 0.5 h R.T. 0.5 h 70 0.5 h	10 cycles	Display Quality : No defect Display Function : No defect Peel-off of Organic Sealing : None Bubble on Cell : None
High Temp. Operation	50 Vop	500 h	Display Quality : No defect Current Consumption : No defect
Point Activation life	Polyacetal stylus (RO.8) Hitting force 3N Hitting speed 2 time/s	one million times	Display Quality : No defect Current Consumption : No defect

- \* Each test item uses a test LCD only once. The tested LCD is not used in any other tests.
- $^{\ast}$  The LCD is tested in circumstances in which there is no condensation.
- \* The tested LCD is inspected after 24 hours of storage at room temperature and room humidity after each test is finished.
- \* The reliability test is not an out-going inspection.
- \* The results of the reliability test are for your reference purpose only. The reliability test is conducted only to examine the LCD's capability.



			SPEC.No.	TQ3C-8EACO	-E2DKA06-00
			DATE	November	25, 2003
	FO	R :			
	<u>10</u>				
<u>K Y O</u>	CERA IN	N S P E C T I	ON STAN	NDARD	
ŋ	YPE :	KHG062H	IV1AH-G	0 0	
-					
				CERA CORPORAT OSHIMA HAYAT(	
				DIVISION	
				[	
Original		by :Engineeri			by :QA Dept.
Issue Data	Prepared	Checked	Approved	Checked	Approved
November 25, 2003	W. Yomo	M.Frittani	H. Chno	y. Joshita	S.Hayashi

Revision Record

D		Design	ed by:	Engineering D	ept.	Confirmed by:	QA Dept.
Date		Prepa	red	Checked	Approved	Checked	Approved
Rev. No.	Date		Page		Descriptio	ns	

# Visuals specification

1)Note

Item	Note			
General	<ol> <li>When defects specified in this Inspection Standards are inspected, operating voltage(Vop) shall be set at the level where optimized contrast is available. Display quality is applied up to effective viewing area. (Bi-Level INSPECTION)</li> </ol>			
	<ul><li>2. This inspection standard about the image quality sh applied to any defect within the effective viewing and shall not be applicable to outside of the area.</li><li>3. Should any defects which are not specified in this standard happen, additional standard shall be deter by mutual agreement between customer and Kyocera.</li></ul>			
	4. Inspection conditions			
	Luminance: 500 Lux minimum .Inspection distance: 300 mm (from the sample)Temperature: $25 \pm 5 \ C$ Direction: right above			
Definition of Inspection item	Pinhole, Bright spot Black spot, Scratch Foreign particle	The color of a small area is different from the remainder. The phenomenon does not change with voltage.		
	Contrast variation	The color of a small area is different from the remainder. The phenomenon changes with voltage.		
	Polarizer ( Scratch, Bubble, Dent )	Scratch, Bubble and Dent in the polarizer which can be observed in on / off state.		

2)Standard

Inspection item	Judgement standard					
Pinhole, Bright spot Black spot, Foreign particle		م ب	d = ( a +	b ) / 2		
	Category Size	(mm)	Acceptab	ole number		
	$\begin{array}{c c} A \\ A \\ d \leq 0.2 \end{array}$		neglected			
	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		5			
		d ≦ 0.5		3		
	D 0.5 <	d		0		
Scratch,Foreign particle			W K			
	Width (mm)	Len	gth (mm)	Acceptable No.		
	A $W \leq 0.03$			neglected		
	В		$L \leq 2.0$	neglected		
	$\begin{array}{c c} C \\ \hline \end{array} 0.03 < \mathbb{W} \leq 0.1 \end{array}$		$L \leq 4.0$	3		
	D D	4.0 <	< L	0		
	$E \qquad 0.1 < W$			According to Circular		
Contrast variation	CategorySizeAB0.5 <	$d \leq 0.5$ $d \leq 0.7$	neg	b ) / 2 Dle number glected 3 0		

Inspection item		Judgement standard					
Polarizer ( Scratch, Bubble, Dent )	(1) Scratch W L						
	Widt	h (mm) L	ength (mm)	Acceptable No.			
	A	$W \leq 0.1$		neglected			
	B C 0.1 <	< W < 0.2	L ≦ 5.0	neglected			
		5.0	< L	0			
	D 0.3 <	< W	_	0			
	d = (a + b) / 2						
	Category	Size (mm)	Acceptab	le number			
	А	$d \leq 0.$	2 neg	neglected			
	В	$0.2 < d \leq 0.$	3	5			
	С	$0.3 < d \leq 0.$	5	3			
	D $0.5 < d 0$						