

1. Description

The KIA50N06 is three-terminal silicon device with current conduction capability of about 50A, fast switching speed. Low on-state resistance, breakdown voltage rating of 60V, and max threshold voltages of 4 volt. It is mainly suitable electronic ballast, and low power switching

2. Features

$R_{DS(ON)}=23m\Omega@V_{GS}=10V$.

Ultra low gate charge (typical 30nC)

Low reverse transfer capacitance

Fast switching capability

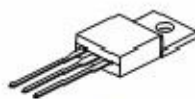
100% avalanche energy specified

Improved dv/dt capability

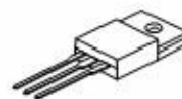
3. Pin configuration



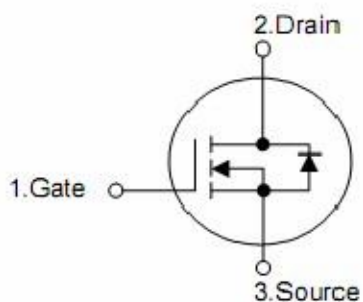
TO-252



TO-220



TO-220F



Pin	Function
1	Gate
2	Drain
3	Source

6. Absolute maximum ratings

Parameter	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	60V	
Gate to source voltage	V_{GS}	$\pm 20V$	
Continuous drain current		$T_J = 25^\circ C$ I_D	50A
		$T_J = 100^\circ C$ I_D	35A
Drain current pulsed (note1)	I_{DM}	200A	
Single pulsed avalanche energy (note2)	E_{AS}	480mJ	
Repetitive avalanche energy (note1)	E_{AR}	13mJ	
Peak diode recovery dv/dt (note3)	dv/dt	7V/ns	
Total power dissipation ($T_J = 25^\circ C$)	P_D	130W	
Derating factor above 25 °C	CP_D	0.9W/°C	
Operating junction temperature	T_J	-55 ~ +150°C	
Storage temperature	T_{STG}	-55 ~ +150°C	
Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.			
Absolute maximum ratings are stress ratings only and functional device operation is not implied.			

3. Thermal resistance

Parameter	Symbol	Typ	Max	Units
Thermal resistance, junction-to-case	θ_{JC}		1.15	°C/W
Thermal resistance, case-to-sink	θ_{CS}			°C/W
Thermal resistance, junction-to-ambient	θ_{JA}	0.5		°C/W
			62.5	

7. Electrical characteristics

(T_J=25°C, unless otherwise notes)

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA		60		V
Breakdown voltage temperature coefficient	ΔBV _{DSS} /ΔT _J	I _D =250μA, referenced to 25 °C		0.07		V/°C
Drain-source leakage current	I _{DSS}	V _{DS} =60V, V _{GS} =0V			1	μA
		V _{DS} =48V, T _c =125 °C			1	μA
Gate-source leakage current	I _{GSS}	V _{GS} =20V, V _{DS} =0V			100	nA
		V _{GS} =-20V, V _{DS} =0V			-100	nA
Gate-source leakage Reverse						
On characteristics						
Gate threshold voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA		2.0	4.0	V
Static drain-source on-state resistance	R _{DS(ON)}	V _{GS} =10V, I _D =25A		18	23	mΩ
Dynamic characteristics						
Input capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1MHz		900	1220	pF
Output capacitance	C _{OSS}			430	550	pF
Reverse transfer capacitance	C _{RSS}			80	100	pF
Switching characteristics						
Turn-on delay time	t _{D(ON)}	V _{DD} =30V, I _D =25A, R _G =50Ω (note4,5)		40	60	ns
Rise time	t _r			100	200	ns
Turn-off delay time	t _{D(OFF)}			90	180	ns
Fall time	t _f			80	160	ns
Total gate charge	Q _G			30	40	nC
Gate-source charge	Q _{GS}	V _{DS} =48V, V _{GS} =10V, I _D =50A (note4,5)		9.6		nC
Gate-drain charge (miller charge)	Q _{GD}			10		nC
Source-drain diode ratings and characteristics						
Diode forward voltage	V _{SD}	V _{GS} =0V, I _S =50A			1.5	V
Continuous source current	I _S	Integral reverse p-n junction diode in the MOSFET			50	A
					200	A
Pulsed source current	I _{SM}					
Reverse recovery time	t _{RR}	V _{GS} =0V, I _S =50A		54		ns
				81		μC

dI_F/dt=100A/μs(note4) Reverse recovery charge Q_{RR}

- Note: 1. repetitive rating: pulse width limited by junction temperature
 2. L=5.6mH, I_{AS}=50A, V_{DD}=25V, R_G=0Ω, starting T_J=25°C
 3. I_{SD}<50A, di/dt<300A/μs, V_{DD}<BV_{DSS}, starting T_J=25 °C
 4. Pulse test: pulse width<300μs, duty cycle<2% –
 5. Essentially independent of operating temperature

8. Test circuits and waveforms

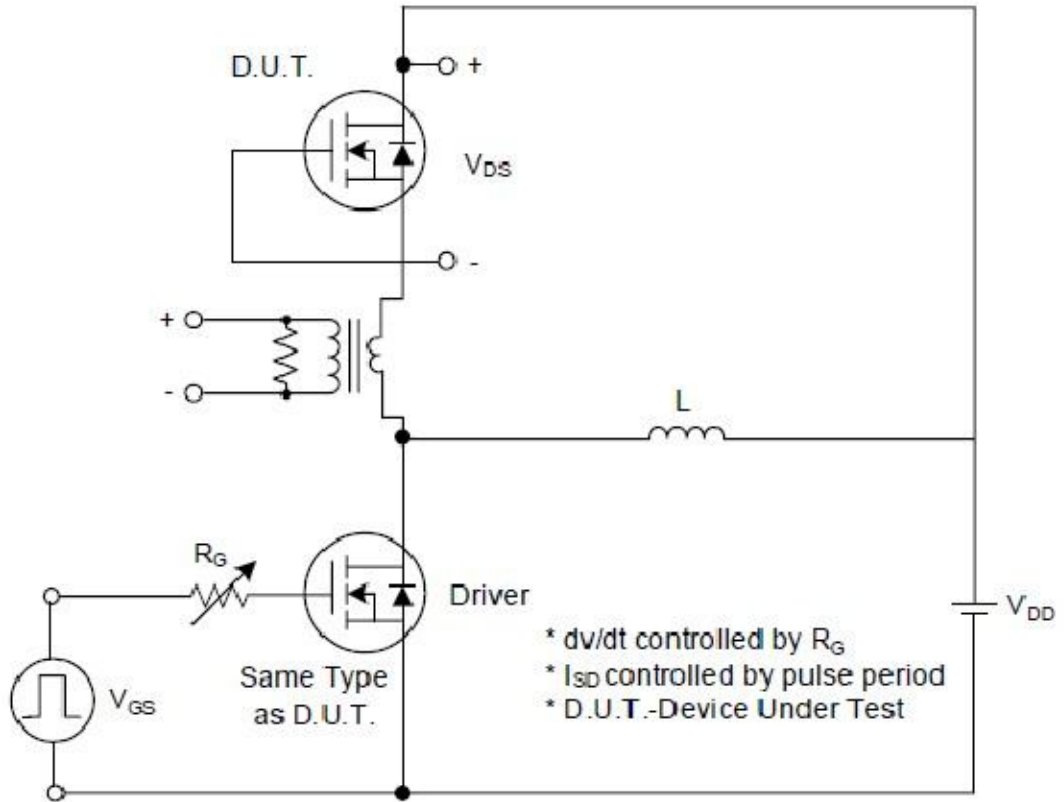


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

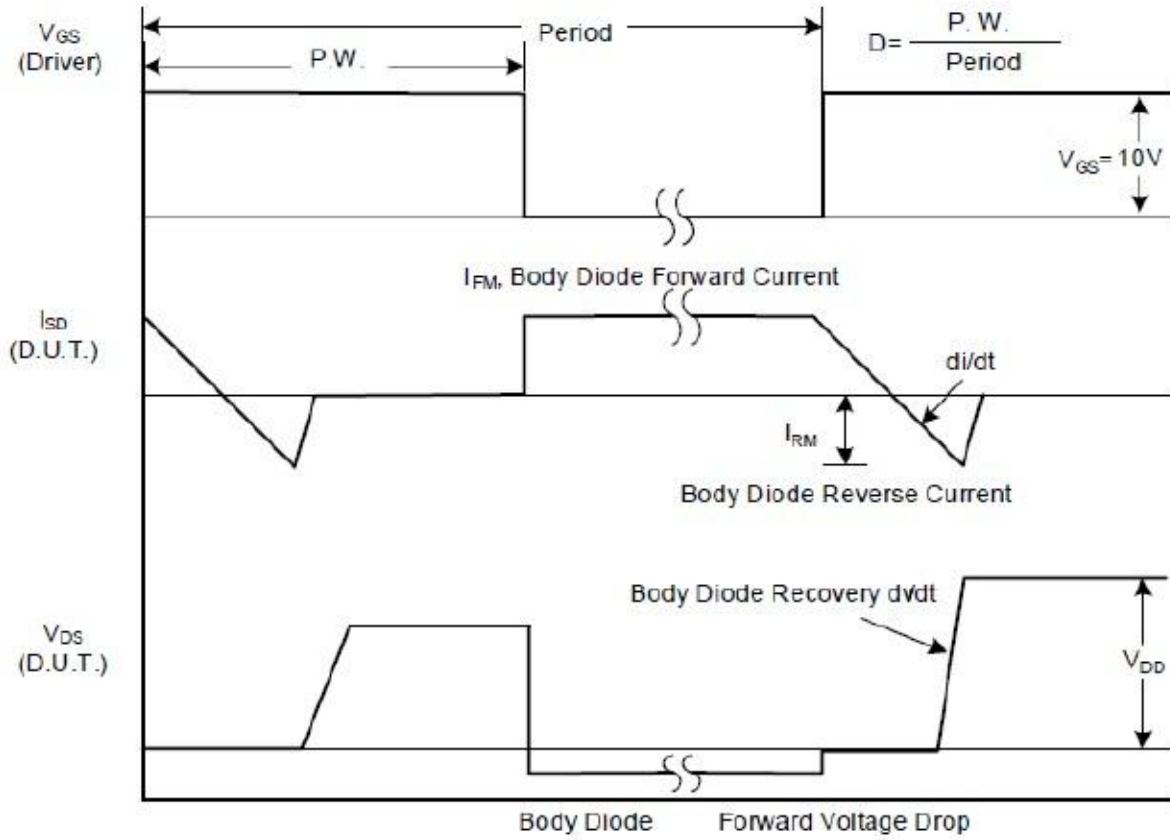


Fig. 1B Peak Diode Recovery dv/dt Waveforms

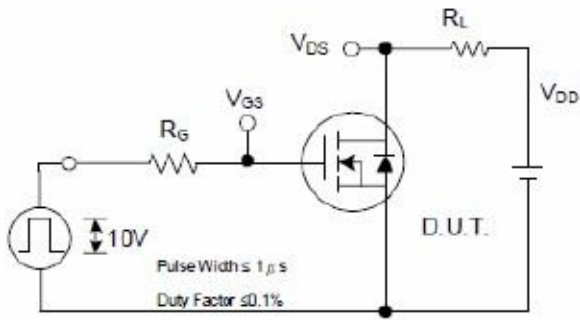


Fig. 2A Switching Test Circuit

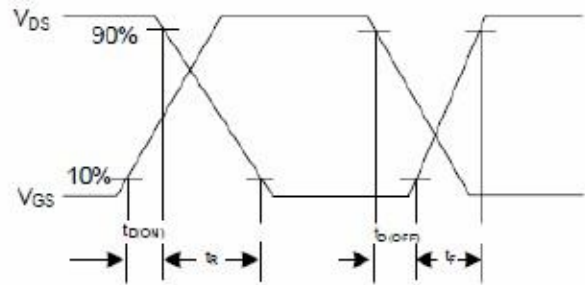


Fig. 2B Switching Waveforms

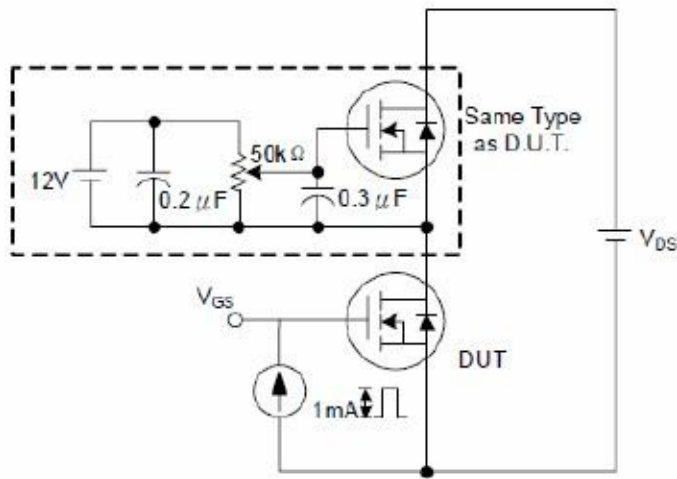


Fig. 3A Gate Charge Test Circuit

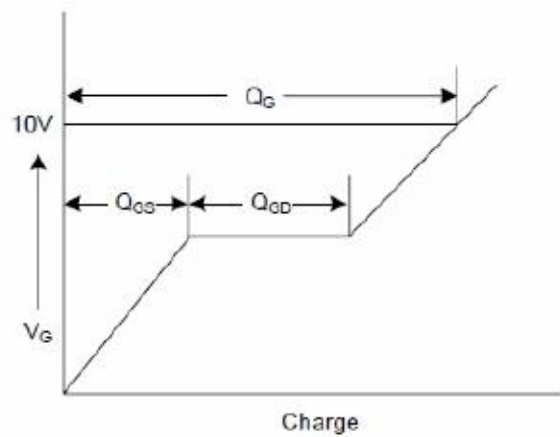


Fig. 3B Gate Charge Waveform

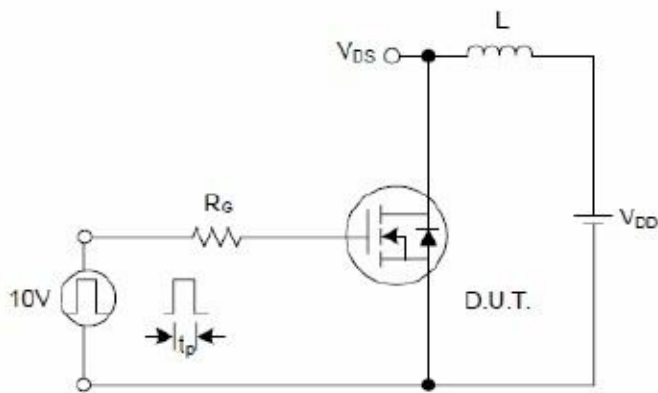


Fig. 4A Unclamped Inductive Switching Test Circuit

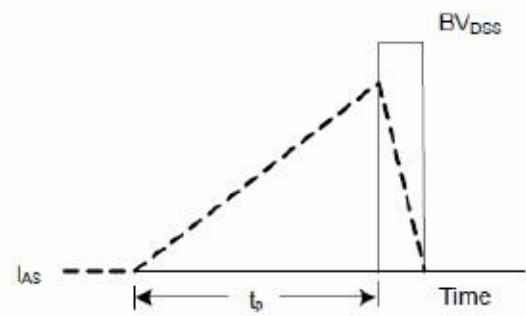


Fig. 4B Unclamped Inductive Switching Waveforms

9. Typical characteristics

