KL5KUSB220

USB2.0 to 100 Ethernet Controller

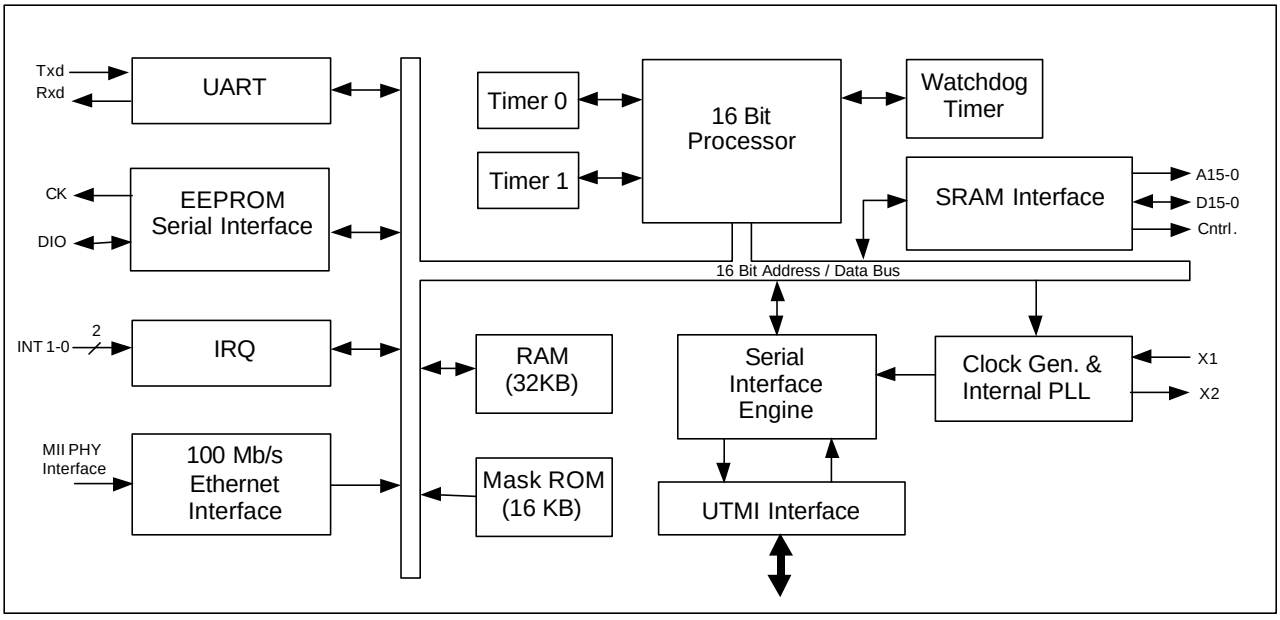
General Description

The Kawasaki KL5KUSB220 Controller used in conjunction with the KL5KUSB200/201 USB2.0 transceiver is a unique solution to interface peripheral devices to the Universal Serial Bus 2.0 (USB2.0) and 100Base-T Ethernet. The KL5KUSB220 has been specifically designed to provide a simple solution to communicate with Ethernet applications accomplished by its highly integrated functionality. The USB controller consists of a central 16-bit processor, mask ROM, RAM buffer, clock generator, Ethernet interface, UART, IRQ, Watchdog Timer, Serial interface, External and Memory Interface. The SIE (Serial Interface Engine) is fully compatible with the USB2.0 specification. Our powerful internal processor enables Remote NDIS (Network Drive) which gives compatibility with next generation operating systems and faster data transfer. This USB to Ethernet controller is ideal for LAN (Local Area Network), HAN (Home Area Network), Cable Modem, Set Top Boxes, or Mobile Networking applications.

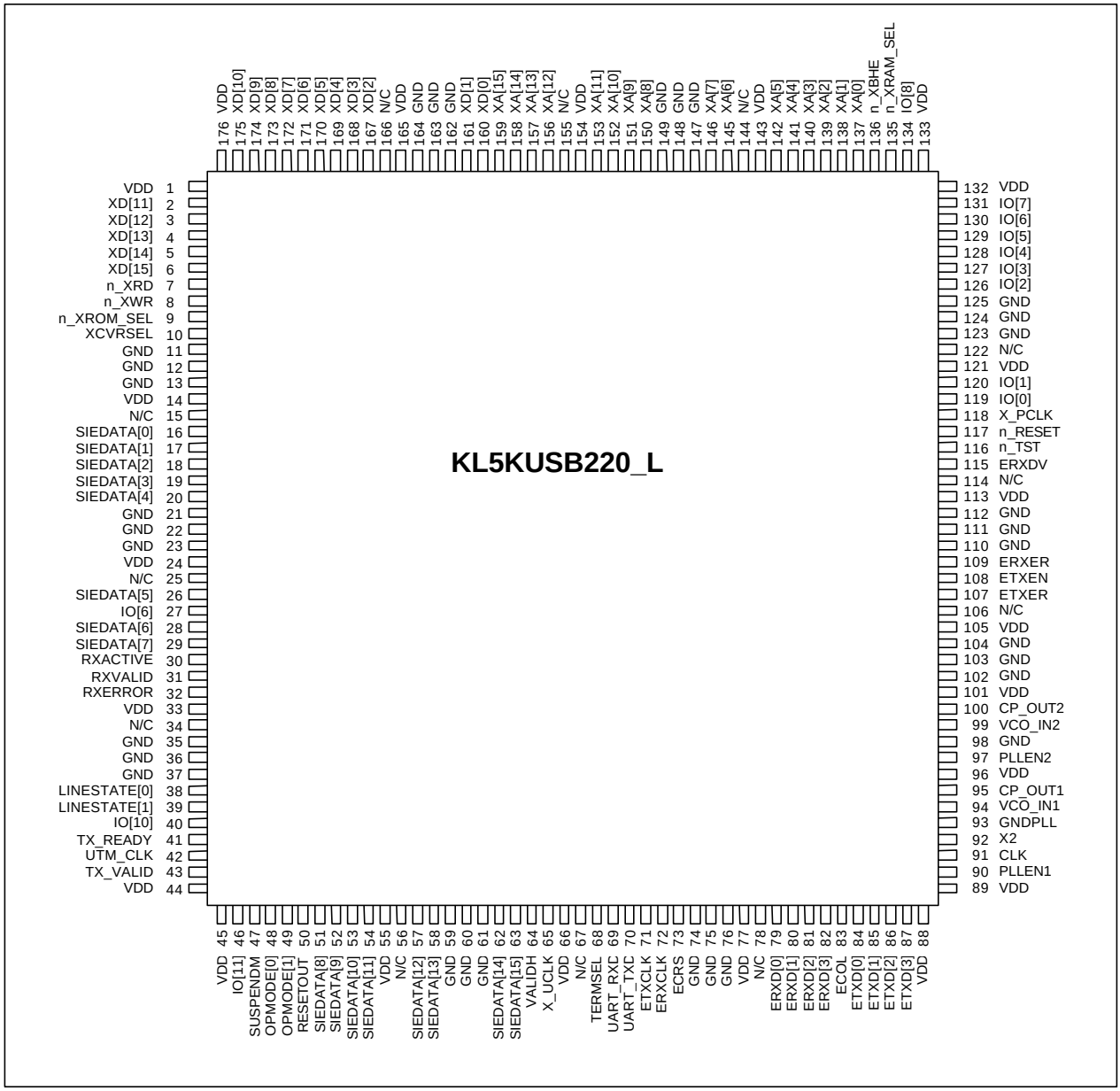
Features

- Advanced 16 Bit processor for USB transaction processing and control data processing
- 100Base-T compatibility
- USB interface version 2.0 compliant
- SIE (Serial Interface Engine)
- Internal Clock Generation - Utilizes low cost external 12MHz crystal circuitry
- MII Physical Layer interface
- 32KB Internal RAM buffer
- Remote NDIS for faster data transfer.
- Fully IEEE compliant 100 Mbit/sec Ethernet MAC Layer. Interfaces serially of an external ENDEC PHY.
- UART
- External memory interface
- 176 LQFP package
- Serial Interface for external EEPROM

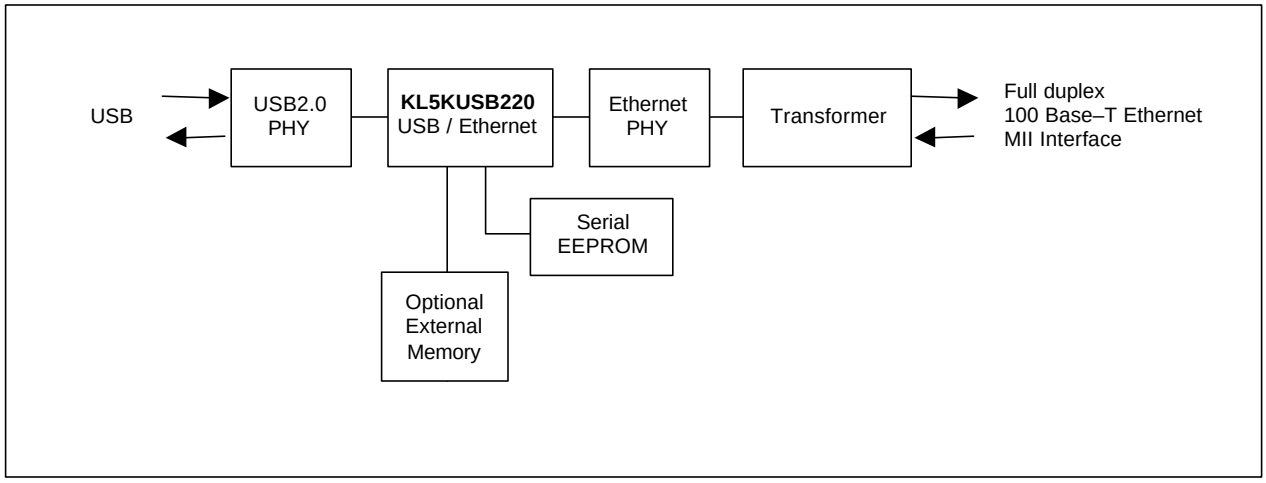
Block Diagram



Pin Diagram 176LQFP



KL5KUSB220 Application Block Diagram



Pin Description

Pin # LQFP	I/O	Pin Name	Description
1	PWR	VDD	VDD
2	I/O	XD[11]	External data 11
3	I/O	XD[12]	External data 12
4	I/O	XD[13]	External data 13
5	I/O	XD[14]	External data 14
6	I/O	XD[15]	External data 15
7	OUT	n_XRD	External memory read, active low.
8	OUT	n_XWR	External memory write, active low.
9	OUT	n_XROM_SEL	External ROM CS.
10	OUT	XCVRSEL	USB Transceiver select, HS/LS.
11	GND	GND	
12	GND	GND	
13	GND	GND	
14	VDD	VDD	
15	N/C	N/C	
16	I/O	SIEDATA[0]	USB data 0.
17	I/O	SIEDATA[1]	USB data 1.
18	I/O	SIEDATA[2]	USB data 2.
19	I/O	SIEDATA[3]	USB data 3.
20	I/O	SIEDATA[4]	USB data 4.
21	GND	GND	
22	GND	GND	
23	GND	GND	

Pin # LQFP	I/O	Pin Name	Description
24	VDD	VDD	
25	N/C	N/C	
26	I/O	SIEDATA[5]	USB data 5.
27	I/O	IO[9]	GPIO 9
28	I/O	SIEDATA[6]	USB data 6.
29	I/O	SIEDATA[7]	USB data 7.
30	IN	RXACTIVE	USB receive active.
31	IN	RXVALID	USB receive data valid.
32	IN	RXERROR	USB receive error
33	VDD	VDD	
34	N/C	N/C	
35	GND	GND	
36	GND	GND	
37	GND	GND	
38	IN	LINESTATE[0]	USB Vp line
39	IN	LINESTATE[1]	USB Vm line
40	I/O	IO[10]	GPIO 10
41	IN	TX_READY	USB transceiver ready for Tx data.
42	IN	UTM_CLK	USB transceiver clock.
43	OUT	TX_VALID	USB Tx data valid for transmission.
44	VDD	VDD	
45	VDD	VDD	
46	I/O	IO[11]	GPIO 11
47	OUT	SUSPENDM	USB suspend.
48	OUT	OPMODE[0]	USB transceiver opmode0.
49	OUT	OPMODE[1]	USB transceiver opmode1.
50	OUT	RESETOUT	USB reset out.
51	I/O	SIEDATA[8]	USB data 8.
52	I/O	SIEDATA[9]	USB data 9.
53	I/O	SIEDATA[10]	USB data 10.
54	I/O	SIEDATA[11]	USB data 11.
55	VDD	VDD	
56	N/C	N/C	
57	I/O	SIEDATA[12]	USB data 12.
58	I/O	SIEDATA[13]	USB data 13.
59	GND	GND	
60	GND	GND	
61	GND	GND	
62	I/O	SIEDATA[14]	USB data 14.
63	I/O	SIEDATA[15]	USB data 15.
64	I/O	VALIDH	USB Tx or Rx high byte valid.
65	OUT	X_UCLK	USB clock out.
66	VDD	VDD	
67	N/C	N/C	
68	OUT	TERMSEL	USB transceiver termination select.
69	IN	UART-RXD	UART receive data.
70	OUT	UART_TXD	UART transmit data.
71	IN	ETCLK	MII transmit data.
72	IN	ERXCLK	MII receive data.
73	IN	ECRS	MII carrier sense.

Pin # LQFP	I/O	Pin Name	Description
74	GND	GND	
75	GND	GND	
76	GND	GND	
77	VDD	VDD	
78	N/C	N/C	
79	IN	ERXD[0]	MII receive data 0.
80	IN	ERXD[1]	MII receive data 1.
81	IN	ERXD[2]	MII receive data 2.
82	IN	ERXD[3]	MII receive data 3.
83	IN	ECOL	MII collision detected.
84	OUT	ETXD[0]	MII transmit data 0.
85	OUT	ETXD[1]	MII transmit data 1.
86	OUT	ETXD[2]	MII transmit data 2.
87	OUT	ETXD[3]	MII transmit data 3.
88	VDD	VDD	
89	VDD	VDD	
90	IN	PLLEN1	PLL #1 enable.
91	XIN	CLK	12 MHz clock/crystal input.
92	XOUT	X2	12 MHz crystal output.
93	GND	GND	
94	IN	VCO_IN1	PLL #1 VCO IN.
95	OUT	CP_OUT1	PLL #1 VCO OUT.
96	VDD	VDD	
97	IN	PLLEN2	PLL #2 enable.
98	GND	GND	
99	IN	VCO_IN2	PLL #2 VCO IN.
100	OUT	CP_OUT2	PLL #2 VCO OUT.
101	VDD	VDD	
102	GND	GND	
103	GND	GND	
104	GND	GND	
105	VDD	VDD	
106	N/C	N/C	
107	OUT	ETXER	MII transmit error.
108	OUT	ETXEN	MII transmit enable to PHY.
109	IN	ERXER	MII receive error.
110	GND	GND	
111	GND	GND	
112	GND	GND	
113	VDD	VDD	
114	N/C	N/C	
115	IN	ERXDV	MII receive data valid.
116	IN	n_TST	Test pin.
117	IN	n_RESET	Reset.
118	OUT	X_PCLK	Processor clock.
119	I/O	IO[0]	GPIO 0
120	I/O	IO[1]	GPIO 1
121	VDD	VDD	
122	N/C	N/C	
123	GND	GND	

Pin # LQFP	I/O	Pin Name	Description
124	GND	GND	
125	GND	GND	
126	I/O	IO[2]	GPIO 2
127	I/O	IO[3]	GPIO 3
128	I/O	IO[4]	GPIO 4
129	I/O	IO[5]	GPIO 5
130	I/O	IO[6]	GPIO 6
131	I/O	IO[7]	GPIO 7
132	VDD	VDD	
133	VDD	VDD	
134	I/O	IO[8]	GPIO 8
135	OUT	n_XRAM_SEL	External RAM byte low enable.
136	OUT	n_XBHE	External RAM byte high enable.
137	OUT	XA[0]	External address 0.
138	OUT	XA[1]	External address 1.
139	OUT	XA[2]	External address 2.
140	OUT	XA[3]	External address 3.
141	OUT	XA[4]	External address 4.
142	OUT	XA[5]	External address 5.
143	VDD	VDD	
144	N/C	N/C	
145	OUT	XA[6]	External address 6.
146	OUT	XA[7]	External address 7.
147	GND	GND	
148	GND	GND	
149	GND	GND	
150	OUT	XA[8]	External address 8.
151	OUT	XA[9]	External address 9.
152	OUT	XA[10]	External address 10.
153	OUT	XA[11]	External address 11.
154	VDD	VDD	
155	N/C	N/C	
156	OUT	XA[12]	External address 12.
157	OUT	XA[13]	External address 13.
158	OUT	XA[14]	External address 14.
159	OUT	XA[15]	External address 15.
160	I/O	XD[0]	External data 0.
161	I/O	XD[1]	External data 1.
162	GND	GND	
163	GND	GND	
164	GND	GND	
165	VDD	VDD	
166	N/C	N/C	
167	I/O	XD[2]	External data 2.
168	I/O	XD[3]	External data 3.
169	I/O	XD[4]	External data 4.
170	I/O	XD[5]	External data 5.
171	I/O	XD[6]	External data 6.
172	I/O	XD[7]	External data 7.
173	I/O	XD[8]	External data 8.

Pin # LQFP	I/O	Pin Name	Description
174	I/O	XD[9]	External data 9.
175	I/O	XD[10]	External data 10.
176	VDD	VDD	

Function Description

16 Bit Processor

The integrated 16 bit processor serves as a micro controller for USB peripherals. The processor can execute approximately five million instructions per second. With this processing power it allows the design of intelligent peripherals that can process data prior to passing it on to the host PC, thus improving overall performance of the system. The masked ROM (4K X 16) in the KL5KUSB220 or external memory contains a specialized instruction set that has been designed for highly efficient coding of processing algorithms and USB transaction processing.

The 16-bit processor is designed for efficient data execution by having direct access to the RAM Buffer, external memory, I/O interfaces, and all the control and status registers. The divide/multiply feature expands the capability of USB peripherals.

The processor supports prioritized vectored hardware interrupts. In addition, as many as 240 software interrupt vectors are available.

The processor provides six addressing modes, supporting memory-to-memory, memory-to-register, register-to-register, immediate-to-register or immediate-to-memory operations. Register, direct, immediate, indirect, and indirect indexed addressing modes are supported. In addition, there is an auto-increment mode in which a register, used as an address pointer is automatically incremented after each use, making repetitive operations more efficient both from a programming and a performance standpoint.

The processor features a full set of program control, logical, and integer arithmetic instructions. All instructions are sixteen bits wide, although some instructions require operands, which may occupy another one or two words. Several special " short immediate" instructions are available, so that certain frequently used operations with small constant operand will fit into a 16-bit instruction.

RAM Buffer

The USB controller contains a 32K byte internal buffer memory. The memory is used to buffer data and USB packets and accessed by the 16 Bit processor and the SIE. USB transactions are automatically routed to the memory buffer. The 16-bit processor has the ability to set up pointers and block sizes in buffer memory for USB transactions. Data is read from the interface and is processed and packetized by the 16-bit I/O processor.

PLL Clock Generator

A 12 MHz external crystal may be used with the KL5KUSB220 controller. Two pins, X1 and CLK, are provided to connect a lower cost crystal circuit to the device. There are two PLL's in the KL5KUSB220, one PLL is configured as a x4 multiplier and the second is configured as a x5 multiplier. The first PLL is used to generate the processor clock. The processor has the ability to select the desired processor clock to 48 MHz (default) or lower. The second PLL is used to generate the clock for the USB 2.0 SIE. Circuitry is provided to generate the internal 48MHz clock requirements of the device. If a n exteran 12 MHz clock is available in the application, it may be used in lieu of the crystal circuit vy connecting directly to the CLK input pin.

Unified Scatter Gather DMA Controller

The unified scatter gather DMA controller enables the high speed data through required for USB 2.0 to 100Mb Ethernet. The processor creates the DMA Control Blocks (DCB's) and enables reception or transmission on a channel. The unified DMA controller then receives/transmits the data to/from the corresponding buffer specified in the DCB.

USB 2.0 Interface

The KL5KUSB220 Controller has USB 2.0 SIE (Serial Interface Engine) allowing both HS (High Speed) and FS (Full Speed) operation. The controller has an interface to an external UTMI Transceiver.

10Mb, 100Mb/sec Ethernet Interface

The KL5KUSB220 Controller has a built in the Ethernet MAC (Media Access Controller) which is fully compliant with the IEEE 802.3 Ethernet standard. The KL5KUSB220 connects externally to a MII interface 10 Base -T and/or 100 Base-T PHY. The KL5KUSB220 Controller 16-bit processor has direct access to the registers of the MAC.

UART Interface

Supports a transfer rate of 7200 to 115.2K baud.

General Purpose I/O

Up to 12 general purpose I/O signals are available. However, most GPIO may be configured for special purpose functions such as UART, Serial EEPROM interface, Digital Input, etc.

Serial EEPROM Support

The USB Controller serial interface is used to provide access to external EEPROM's. The interface can support a variety of Serial EEPROM formats.

SRAM Interface

An address port and 16-bit data port has been provided to interface to an external SRAM.

DC CHARACTERISTICS

U2E is implemented with Kawasaki's 0.5um CMOS CBA and Embedded Memory KZ300EM Technology. The followings are the description of chip electric characteristics.

1. Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage	Vdd	–0.3 ~ 4.0	V
Input Voltage	Vin	–0.3 ~ 7.3	V
DC Output Current	Iout	±15	mA
Storage Temperature	Tstg	–55 ~ 125	°C

2. Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating supply voltage	Vdd	3.0	–	3.6	V
Operating ambient temperature	Ta	0	–	70	°C