3 ½ - Digit LED Display, A/D Converters

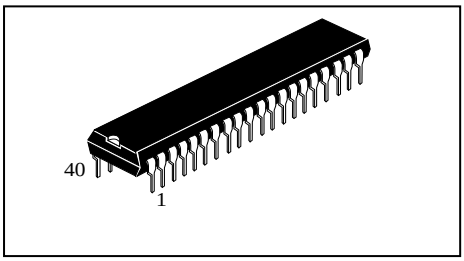
KL7107

DESCRIPTION

The KL7107 are high performance, low power, 3 ½ digit A/D converters. Included are seven segment decoders, display drivers, a reference, and a clock.

The KL7107 will directly drive an instrument size light emitting diode (LED) display.

The KL7107 bring together a combination of high accuracy,versatility, and true economy. It features autozero to less than 10 µV, zero drift of less than 1µV/°C, input bias current of 10pA (Max), and rollover error of less than one count. True differential inputs and reference are useful in all systems, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge type transducers.



DIP-40

ORDERING INFORMATION

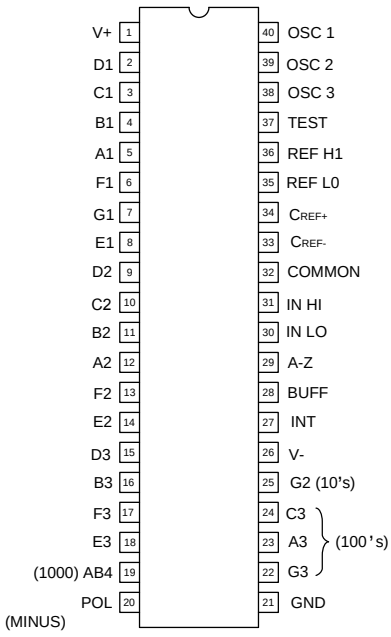
Device	Temperature Range	Package	Packing
KL7107N	T_A= 0°C …+70°C	DIP-40	Tube

FEATURES

- Guaranteed Zero Reading for 0V Input on All Scales
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference, Direct LED Display Drive
- Low Noise – Less Than 15µVp-p
- On Chip Clock and Reference
- Low Power Dissipation – Typically Less Than 10mW
- No Additional Active Circuits Required
- Enhanced Display Stability

PIN CONNECTIONS

TOP VIEW



Absolute Maximum Ratings

Supply Voltage : V+ to GND V- to GND	 6V -9V	Thermal Resistance (Typical, Note 2) PDIP Package	50
Analog Input Voltage (Either Input) (Note 1)	V+ to V-	Maximum Junction Temperature	150°C
Reference Input Voltage (Either Input)	V+ to V-	Maximum Storage Temperature Range	-65°C to 150°C
Clock Input	GND to V+	Maximum Lead Temperature (Soldering 10s)	300°C

Thermal Information

Operating Conditions

Temperature Range 0°C to 70°C

CAUTION: * Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.
Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
2. ΘJA is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications (Note 3)

Parameter	Test Conditions	Min	Typ	Max	Unit
SYSTEM PERFORMANCE					
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200mV	-000.0	±000.0	+000.0	Digital Reading
Stability (Last Digit)	Fixed Input Voltage (Note 5)	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF},V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error	-V_{IN}= +V_{IN} ≈ 200mV Difference in Reading for Equal Positive and Negative Inputs Near Full Scale	-	±0.2	±1	Counts
Linearity	Full Scale = 200mV or Full Scale = 2V Maximum Deviation from Best Straight Line Fit (Note 4)	-	±0.2	±1	Counts
Common Mode Rejection Ratio	V_{CM} = 1V, V_{IN}= 0V, Full Scale = 200mV (Note 4)	-	50	-	μV/V
Noise	V_{IN}= 0V, Full Scale = 200mV (Peak-To-Peak Value Not Exceeded 95% of Time)	-	15	-	μV
Leakage Current Input	V_{IN} = 0 (Note 4)	-	1	10	pA
Zero Reading Drift	V_{IN} = 0, 0°C to 70°C (Note 5)	-	0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199mV,0°C to 70°C, (Ext. Ref. 0ppm/x°C) (Note 4)	-	1	5	ppm/°C
End Power Supply Character V+ Supply Current	V_{IN} = 0 (Does Not Include LED Current)	-	1.0	1.8	mA
End Power Supply Character V- Supply Current	-	-	0.6	1.8	mA
COMMON Pin Analog Common Voltage	25kΩ Between Common and Positive Supply (With Respect to + Supply)	2.4	3.0	3.2	V
Temperature Coefficient of Analog Common	25kΩ Between Common and Positive Supply (With Respect to + Supply)	-	80	-	ppm/°C

Electrical Specifications (Note 3) **(Continued)**

Parameter	Test Conditions	Min	Typ	Max	Unit
DISPLAY DRIVER					
Segment Sinking Current Except Pins AB4 and POL	V+ = 5V, Segment Voltage = 3V	5	8	-	mA
Pin AB4 Only		10	16	-	mA
Pin POL Only		4	7	-	mA

NOTES:

3. Unless otherwise noted, specifications apply at $T_A = 25^oC$, f_{CLOCK} = 48kHz. MTr10 is tested in the circuit of Figure 1.
4. Not tested, guaranteed by design.
5. Sample Tested.

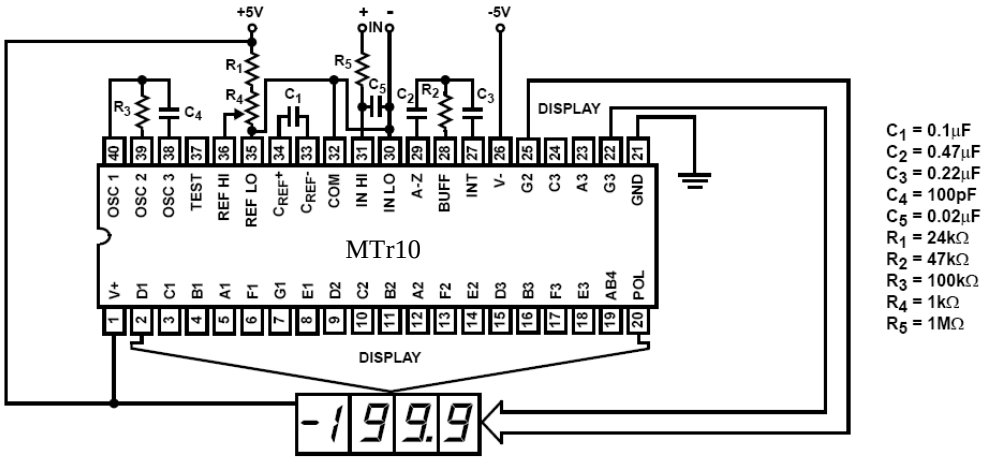


Figure 1. TEST CIRCUIT AND TYPICAL APPLICATION WITH LED DISPLAY COMPONENTS SELECTED FOR 200mV FULL SCALE

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**

  $f_{OSC} = 0.45/RC$
  $C_{OSC} > 50pF$; $R_{QSC} > 50k\Omega$
  f_{OSC} (Typ) = 48kHz

- **OSCILLATOR PERIOD**

  $t_{0SC} = RC/0.45$

- **INTEGRATION CLOCK FREQUENCY**

  $f_{CLOCK} = f_{0SC}/4$

- **INTEGRATION PERIOD**

  $t_{INT} = 1000 \times (4/f_{OSC})$

- **60/50HZ REJECTION CRITERION**

  t_{INT}/t_{60Hz} or t_{INT}/t_{60Hz} = Integer

- **OPTIMUM INTEGRATION CURRENT**

  $I_{INT} = 4\mu A$

- **FULL SCALE ANALOG INPUT VOLTAGE**

  V_{INFS}(Typ) = 200mV or 2V

- **INTEGRATE RESISTOR**

$$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$

- **INTEGRATE CAPACITOR**

$$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

- **INTEGRATOR OUTPUT VOLTAGE SWING**

$$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$

V_{INT} MAXIMUM SWING:

(V- + 0.5V) < V_{INT}< (V+ - 0.5V), V_{INT} (Typ) = 2V

- **DISPLAY COUNT**

$$COUNT = 1000x \frac{V_{IN}}{V_{REF}};$$

- **CONVERSION CYCLE**

  $t_{CYC} = t_{CLOCK}$ x 4000

  $t_{CYC} = t_{0SC}$ x 16,000

  when fosc = 48kHz; tcyc = 333ms

- **COMMON MODE INPUT VOLTAGE**

  (V-+ 1V) < V_{INT} < (V+ - 0.5V)

- **AUTO-ZERO CAPACITOR**

  $0.01\mu F < C_{AZ} < 1\mu F$

- **REFERENCE CAPACITOR**

  $0.1\mu F < C_{REF} < 1\mu F$

- **V_{COM}**

  Biased between Vi and V-.

- **V_{COM}=V+-2.8V**

  Regulation lost when V+ to V- < ≈ 6.8V
  If V_{COM} is externally pulled down to (V+ to V-)/2, the V_{COM} circuit will turn off.

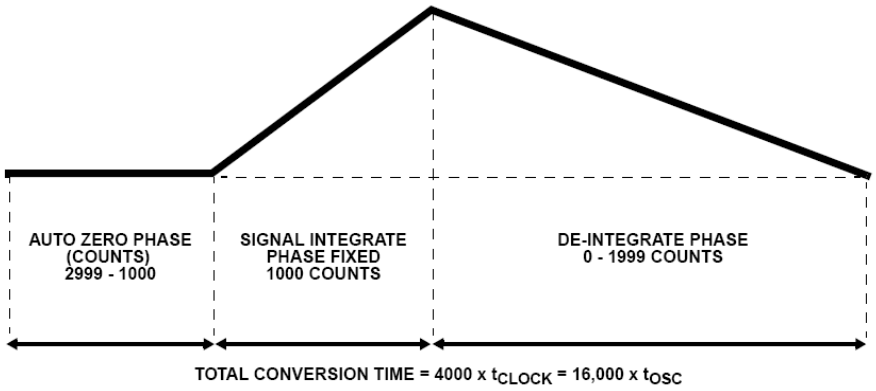
- **POWER SUPPLY: DUAL** ± 5.0V

  V+ = +5V to GND
  V- = -5V to GND
  Digital Logic and LED driver supply V+ to GND

- **DISPLAY: LED**

  Type: Non-Multiplexed Common Anode

Typical Integrator Amplifier Output Waveform (INT Pin)



Detailed Description

Analog Section

Figure 2 shows the Analog Section. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10µV.

Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to 1V from either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is:

$$\text{DISPLAY COUNT} = 1000\left(\frac{V_{IN}}{V_{REF}}\right)$$

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5V below the positive supply to 1V above the negative supply. In this range, the system has a CMRR of 86dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (See Component Value Selection.)

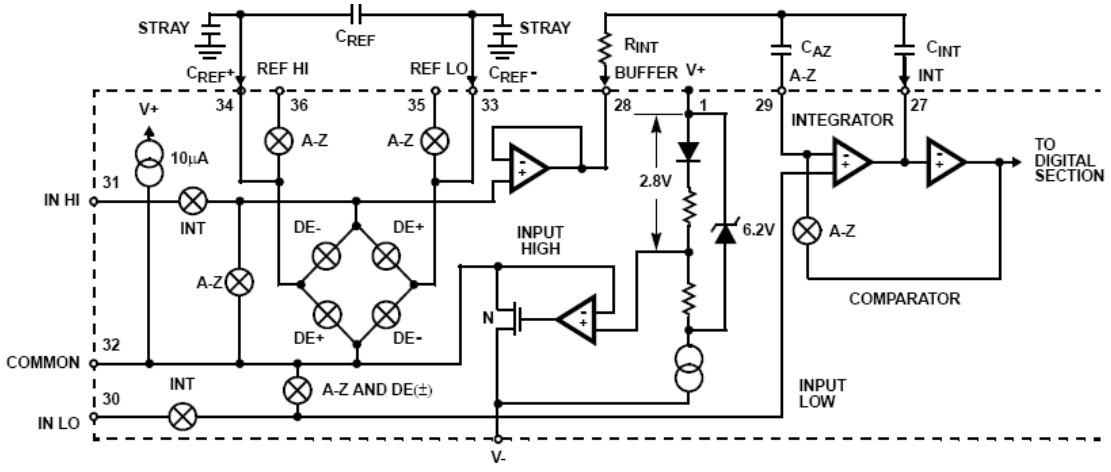


FIGURE 2. ANALOG SECTION

Digital Section

Figure 3 show the Digital Section for, respectively.

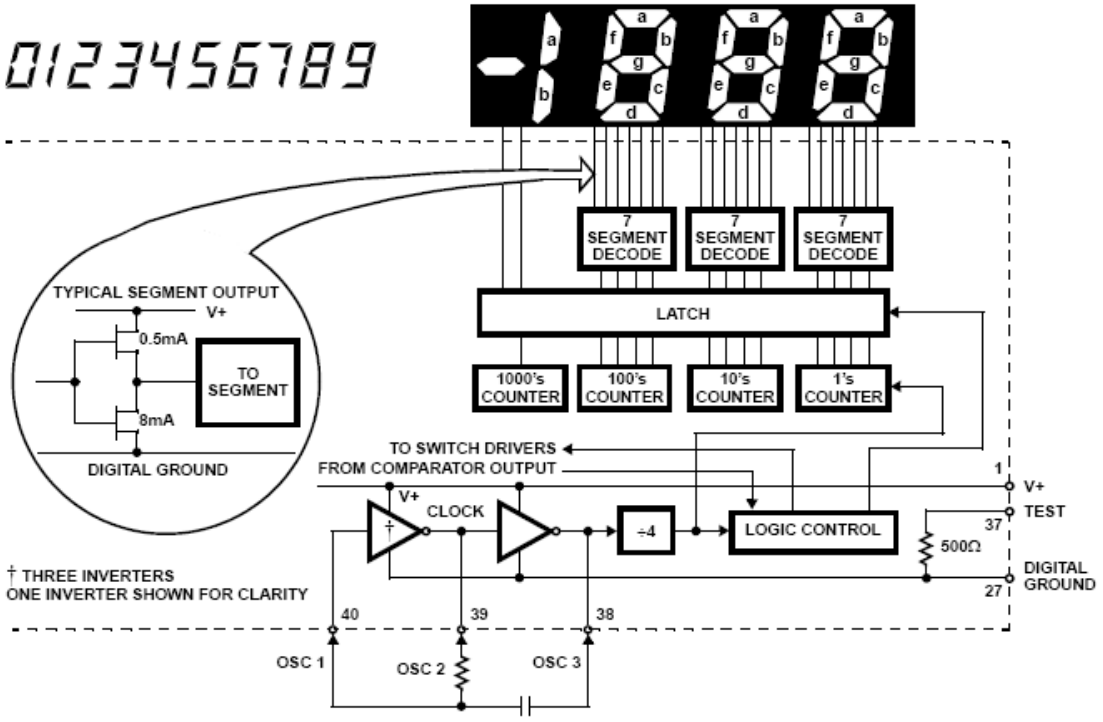


FIGURE 3. DIGITAL SECTION

System Timing

Figure 4 shows the clocking arrangement used in the. Two basic clocking arrangements can be used:

1. Figure 4A. An external oscillator connected to pin 40.
2. Figure 4B. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts) For signals less than full scale, auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, $33^{1}/_{3}$kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, $66^{2}/_{3}$kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz).

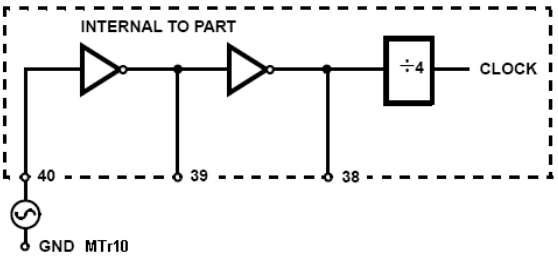


FIGURE 4A

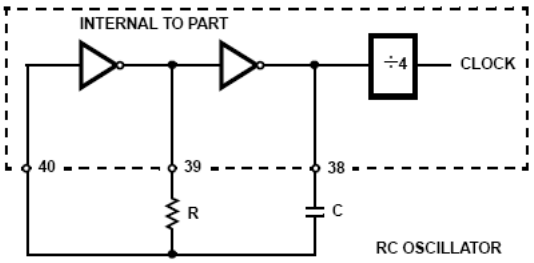


FIGURE 4B. CLOCK CIRCUITS

Component Value Selection

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100µA of quiescent current. They can supply 4µA of drive current with negligible nonlinearity The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance buildup will not saturate the integrator swing (approximately. 0.3V from either supply). In the NTr10, when the analog COMMON is used as a reference, a nominal +2V full-scale integrator swing is fine. For the MTr10 with +5V supplies and analog COMMON tied to supply ground, a ±3.5V to +4V swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22µF and 0.10µF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise For 200mV full scale where noise is very important, a 0.47µF capac recommended. On the 2V scale, a 0.047µF capacitor increases the recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1µF capacitor gives good results in most applications.

However, where a large common mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1µF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation:

$f = 0.45/RC$ For 48kHz Clock (3 Readings/sec),
$C = 100$ pF.

Reference Voltage

The analog input required to generate full scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200mV and 2V scale, V_{REF} should equal 100mV and 1V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.662V. Instead of dividing the input down to 200mV, the designer should use the input voltage directly and select $V_{REF} = 0.341$V Suitable values for integrating resistor and capacitor would be 120kΩ and 0.22µF This makes the system slightly quieter and also avoids a divider network on the input. The MTr10 with +5V supplies can accept input signals up to +4V. Another advantage of this system occurs when a digital reading of zero is desired for

$V_{IN} \neq 0$. Temperature and weighing systems with a variable fare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

Power Supplies

The Mtr10 is designed to work from +5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive 1C. Figure 5 shows this application.

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than +1.5V
3. An external reference is used.

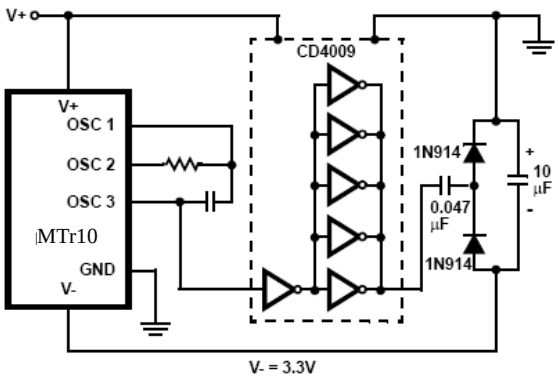
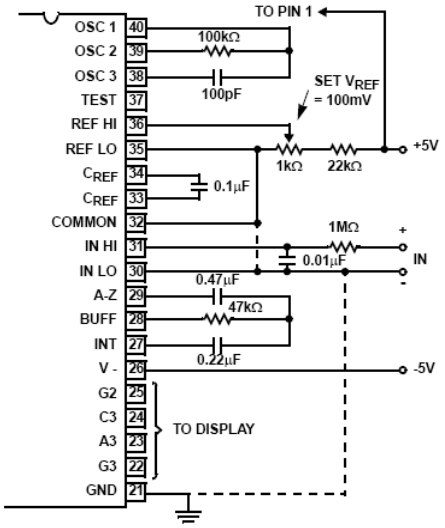


FIGURE 5. GENERATING NEGATIVE SUPPLY FROM +5V

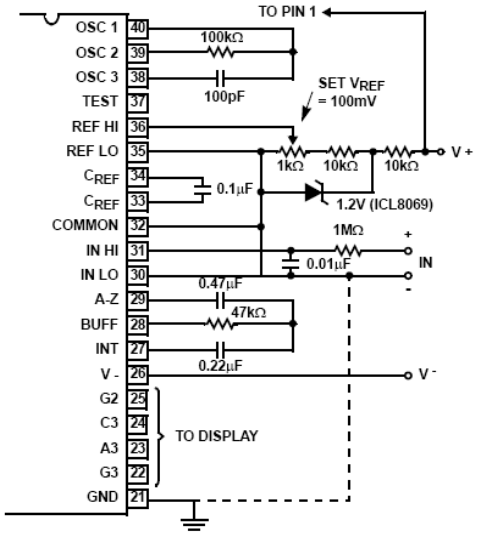
Typical Applications

The KL7107 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters. The following application notes contain very useful information on understanding and applying this part and are available from Intersil Corporation.



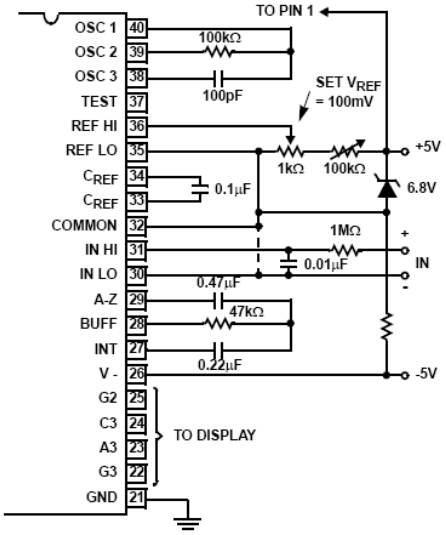
Values shown are for 200 mV full scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND fo single ended inputs. (See discussion under Analog COMMON).

FIGURE 6. USING THE INTERNAL REFERENCE



IN LO is tied to supply COMMON establishing the correct common mode voltage . If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ende (referred to supply GND) and the pre-regulator is overridden.

FIGURE 7. WITH AN EXTERNAL BAND-GAP REFERENCE (1.2V TYPE)



Since low TC zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 7, IN LO may be tied either COMMON or GND

FIGURE 8. WITH ZENER DIODE REFERENCE

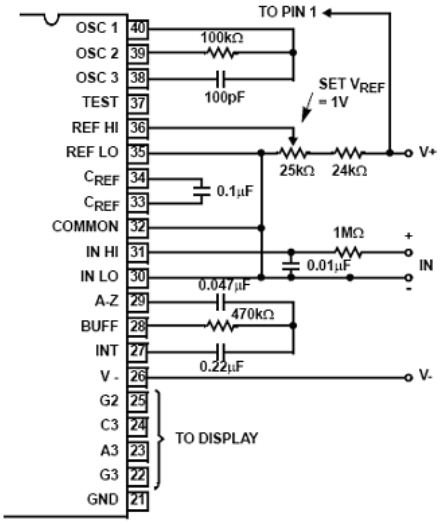
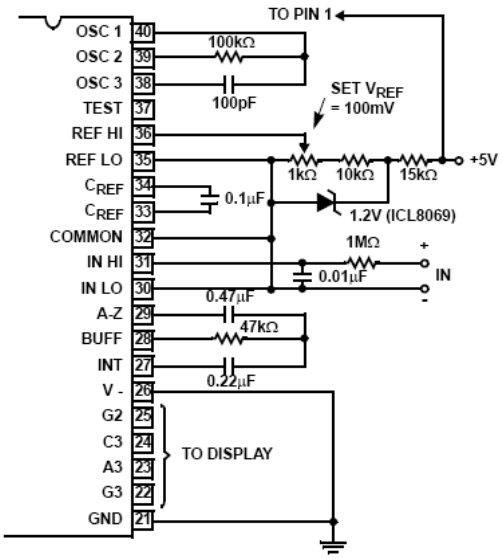


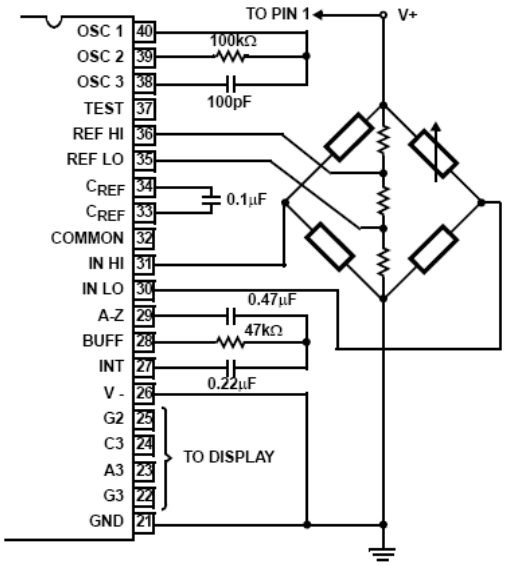
FIGURE 9. RECOMMENDED COMPONENT VALUES FOR 2V FULL SCALE

Typical Applications (Continued)



An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference.

FIGURE 10. OPERATED FROM SINGLE +5V



The resistor values within the bridge are determined by the desired sensitivity.

FIGURE 11. MEASURENG RATIOMETRIC VALUES OF QUAD LOAD CELL

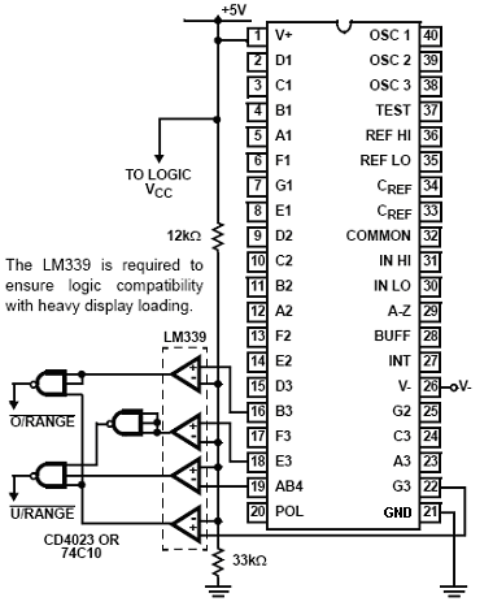


FIGURE 12. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNALS FROM OUTPUT

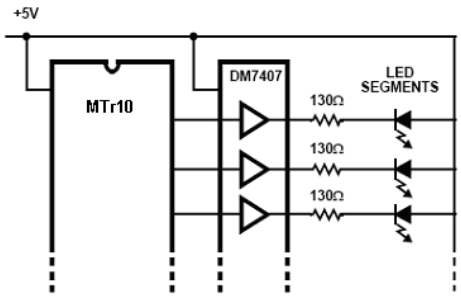


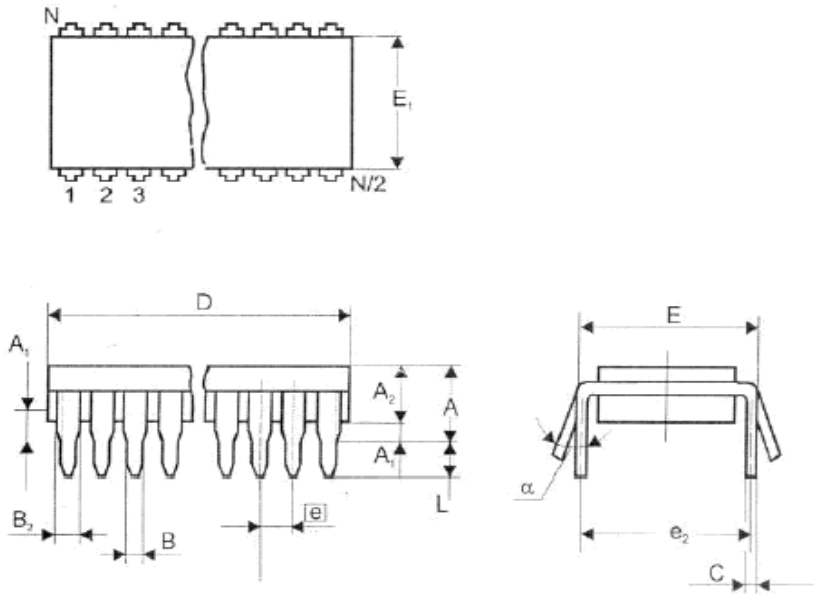
FIGURE 13. DISPLAY BUFFERING FOR INCREASED DRIVE CURRENT

Pin Description

Pin No	Description
01	Positive supply voltage
02	Activates the D segment
03	Activates the C segment
04	Activates the B segment
05	Activates the A segment
06	Activates the F segment
07	Activates the G segment
08	Activates the E segment
09	Activates the D segment
10	Activates the C segment
11	Activates the B segment
12	Activates the A segment
13	Activates the F segment
14	Activates the E segment
15	Activates the D segment
16	Activates the B segment
17	Activates the F segment
18	Activates the E segment
19	Activates the AB segment
-	No connection
20	Activates the negative polarity display
21	Ground
21	Ground
22	Activates the G segment
23	Activates the A segment
24	Activates the C segment
25	Activates the G segment
26	Negative supply voltage
27	Integrator output
28	Integration resistor connection
29	Pin auto-zero capacitor
30	The analog LOW input is connected to this pin
31	The analog HIGH input is connected to this pin
32	Common
33	Pin C^-
34	Pin C^+
35	Pin REF^-
36	Pin REF^+
-	No connection
37	Display test
38	Oscillator section 3
-	No connection
39	Oscillator section 2
40	Oscillator section 1

PAKAGE DIMENSION

40-Pin Plastic Dual-in-Line



Dimension, mm		
A	max	6.35
A1	min	0.38
A_2	min	3.18
	max	4.95
B	min	0.36
	max	0.56
B_2	min	0.77
	max	1.78
C	min	0.20
	max	0.38
D	min	50.30
	max	53.20
E	min	15.24
	max	15.87
E_1	min	12.32
	max	14.73
e	nom	2.54
e_2	nom	15.24
L	min	2.92
	max	5.08
α	min	0°
	max	10°