SAMSUNG moviNAND™

KLMxGxxEHx (FN3x based moviNAND)

Document Title

SAMSUNG moviNAND

Revision History

Revision No	History	Date	Remark
0.0	Initial issue	June. 01. 2009	Preliminary
0,1	1. Vddi cap is changed as min value in chapter 9.3.1 2. Smart Report filed is changed in chapter 4.2.2 3. typo was fixed in Chapter 3.1	Aug. 03. 2009	Preliminary

The attached data sheets are prepared and approved by SAMSUNG Electronics. And SAMSUNG Electronics has the right to change all the specifications in data sheets. SAMSUNG Electronics will evaluate and reply to any dear customer's requests and questions on the parameters of this moviNAND. If dear customer has any questions, please call or fax to Memory Product Planning Team, or contact the SAMSUNG branch office near your office

Table of Contents

NTRODUCTION

The SAMSUNG moviNAND is an embedded MMC solution designed in a BGA package form. moviNAND operation is identical to a MMC card and therefore is a simple read and write to memory using MMC protocol v4.3 which is a industry standard.

moviNAND consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF) whereas 1.8V or 3V dual supply voltage (VDD) is supported for the MMC controller. Maximum MMC interface frequency of 52MHz and maximum bus widths of 8 bit are supported.

There are several advantages of using moviNAND. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.

The embedded flash mangement software or FTL(Flash Transition Layer) of moviNAND manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash platform and achieves optimal performance. The current moviNAND performance is neither limited by the maximum interface frequency nor the maximum bus width but by the performance of NAND. Therefore the maximum performance of moviNAND will saturate at a certain MMC interface frequency and bus width depending on the type and the number of NAND used in moviNAND.

1.0 Product List

Capacities	moviNAND Part ID	NAND Flash Type	Power System	Package size	Pin Configuration
4GB	KLM4G1EEHM-B101	32Gb MLC x 1	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	14mm x 18mm x 1.2mm	169FBGA
8GB	KLM8G2EEHM-B101	32Gb MLC x 2			
16GB	KLMAG4EEHM-B101	32Gb MLC x 4			
32GB	KLMBG8EEHM-B101	32Gb MLC x 8		14mm x 18mm x 1.4mm	

2.0 Key Features

- MultiMediaCard System Specification Ver. 4.3 compatible (Boot operation is supported)
- Full backward compatibility with previous MultiMediaCard system (1bit data bus, multi-moviNAND systems)
- MMC I/F Clock frequency : 0~52MHz
  MMC I/F Boot frequency : 0~26MHz
- Data bus width : 1bit(default), 4bit and 8 bit
- Temperature : -25'C to 85'C (Operation) , -40'C to 85'C (Storage)
- NAND technology changes invisible to the host

3.0 Package Configurations

3.1 Pin Configuration

Pin NO	Name	Pin NO	Name
K6	VDD	AA5	VDD
T10	VDDF	W4	VDD
K2	VDDI	Y4	VDD
R10	Vss	AA3	VDD
W5	CMD	U9	VDDF
W6	CLK	M6	VDDF
H3	DAT0	N5	VDDF
H4	DAT1	U8	Vss
H5	DAT2	M7	Vss
J2	DAT3	AA6	Vss
J3	DAT4	P5	Vss
J4	DAT5	Y5	Vss
J5	DAT6	K4	Vss
J6	DAT7	Y2	Vss
		AA4	Vss

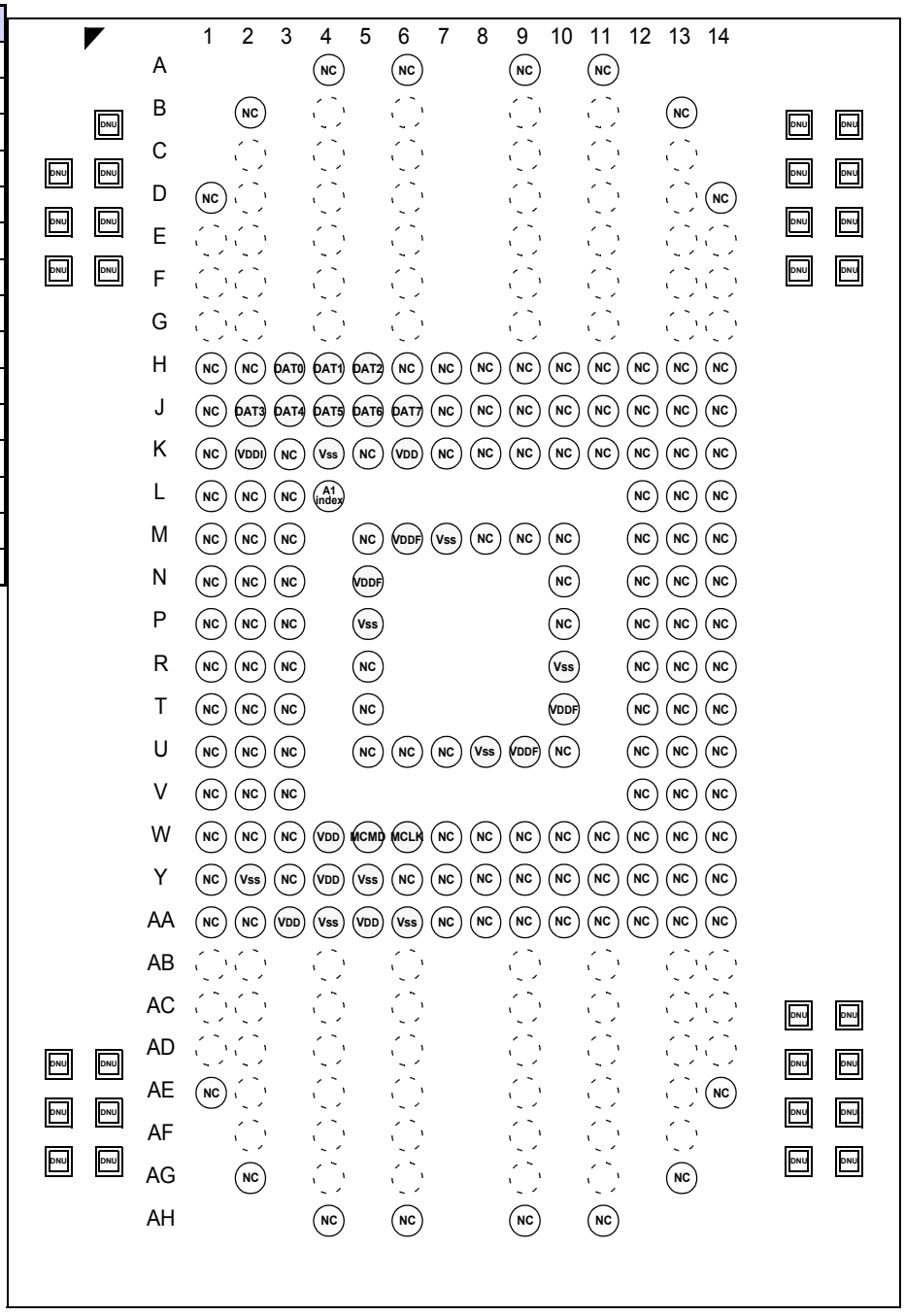


Figure 1. 169-FBGA

3.2 Package Dimensions

14mm x 18mm x 1.4mm(Max)

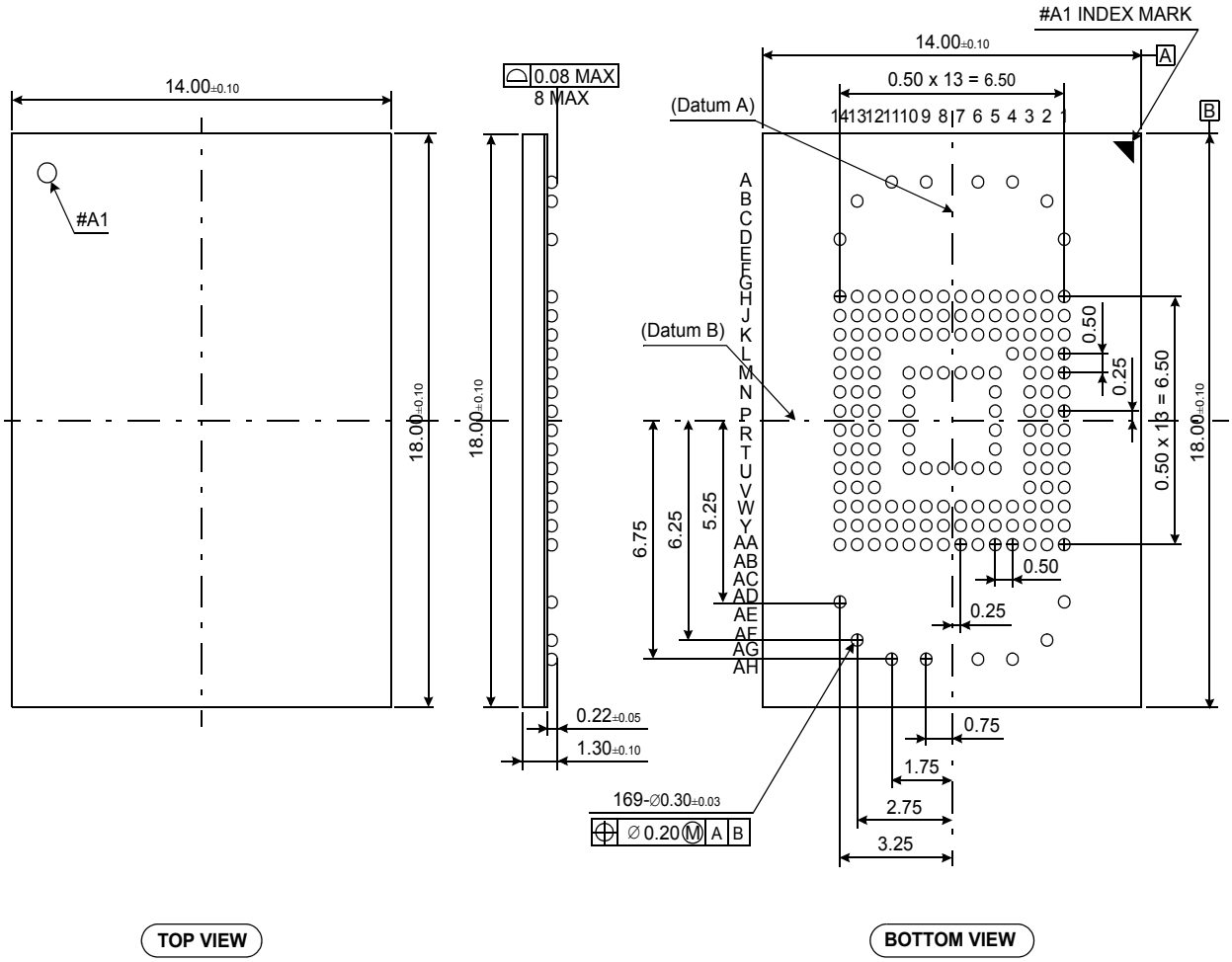


Figure 2. Package Dimension

14mm x 18mm x 1.2mm (Max)

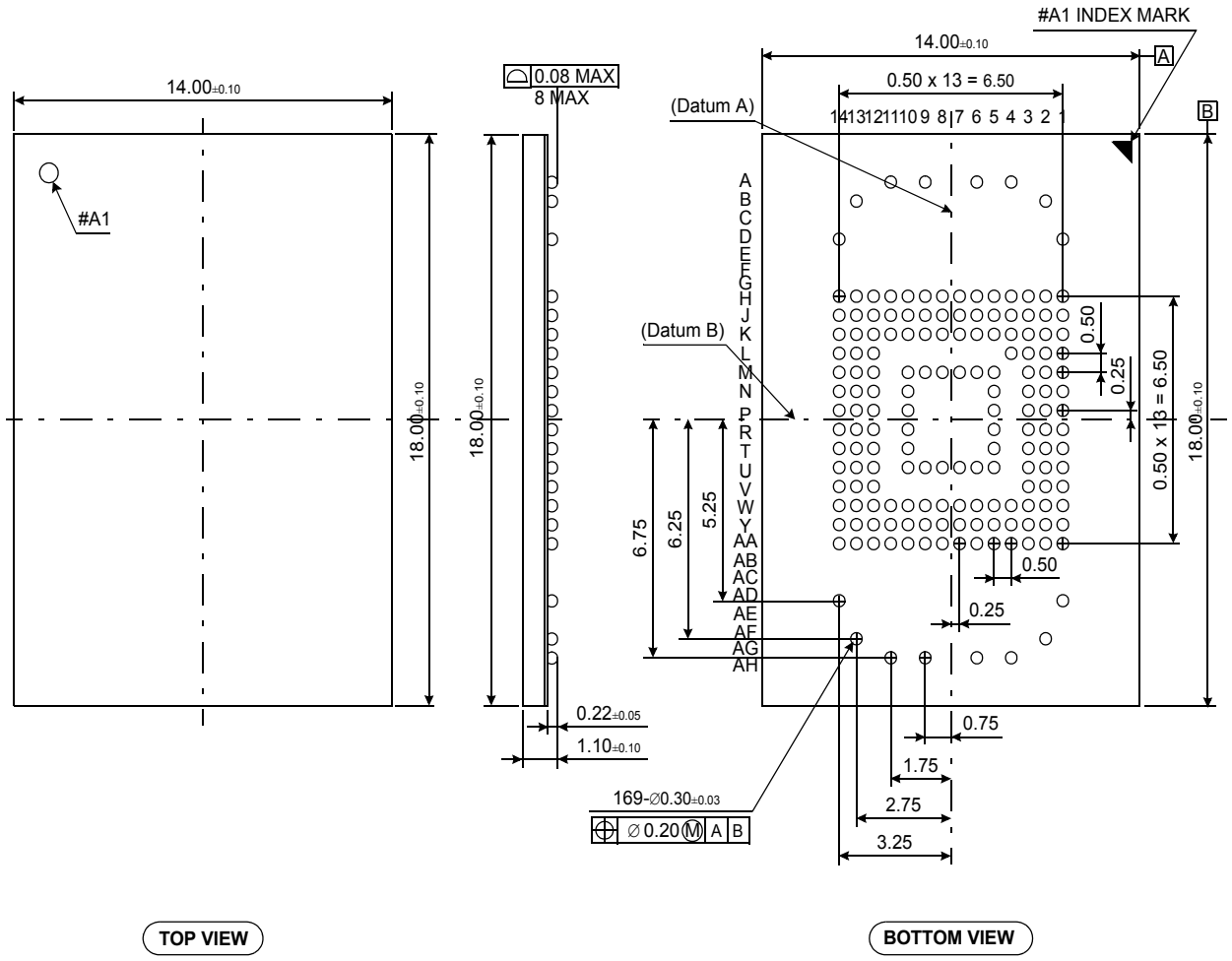


Figure 2. Package Dimension

3.3 Product Architecture

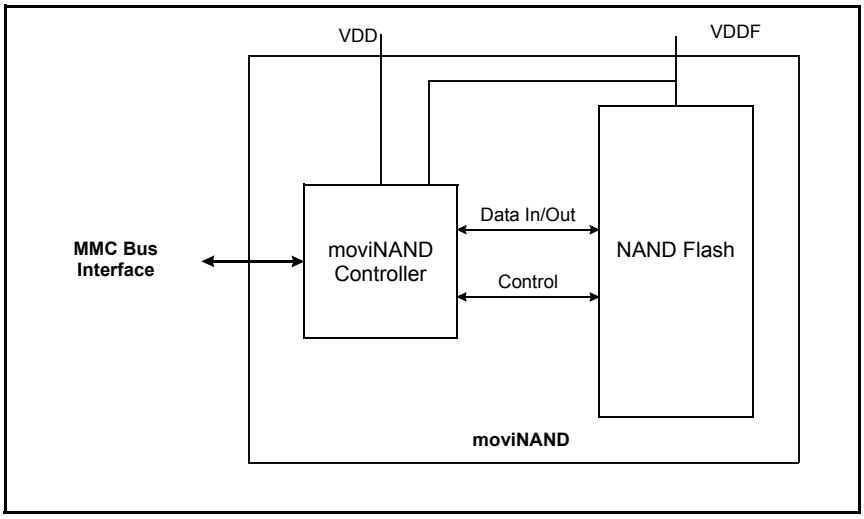


Figure 4. moviNAND Block Diagram

4.0 Features of moviNAND

This moviNAND follows MMC4.3 standards. KLMxGxxExM moviNAND series are housed in 169 ball BGA package and JEDEC standard package size.

4.1 Vendor specific command

CMD62 is a Vendor command which Samsung provides for customer to use moviNAND more usefully. One is for Boot partition setting and the other is Smart report.

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD62	ac	[31:0] Argument	R1b	VENDOR_CMD	Vendor command can provide two kinds of functions. One is Smart Report, Second is Boot partition setting.

4.1.1 Boot operation mode

In boot operation mode, the master (MultiMediaCard host) can read boot data from the slave (MMC device) by keeping CMD line low after power-on, or sending CMD0 with argument 0xFFFFFFFA (optional for slave), before issuing CMD1. The data can be read from either boot-area or user area depending on register setting. Detail description is refer to MMC 4.3 standard

4.1.2 Boot partition

Samsung moviNAND provide boot partition feature which users can set the boot partition size
There are two partition regions. The minimum size of each boot partition is 0KB. Boot partition size is calculated as follows: [227:226]
Maximum boot partition size = 128K byte x BOOT_SIZE_MULT
BOOT_SIZE_MULT: the value in Extended CSD register bytes [227:226]
The boot partitions are separated from the user area as shown in below figure.

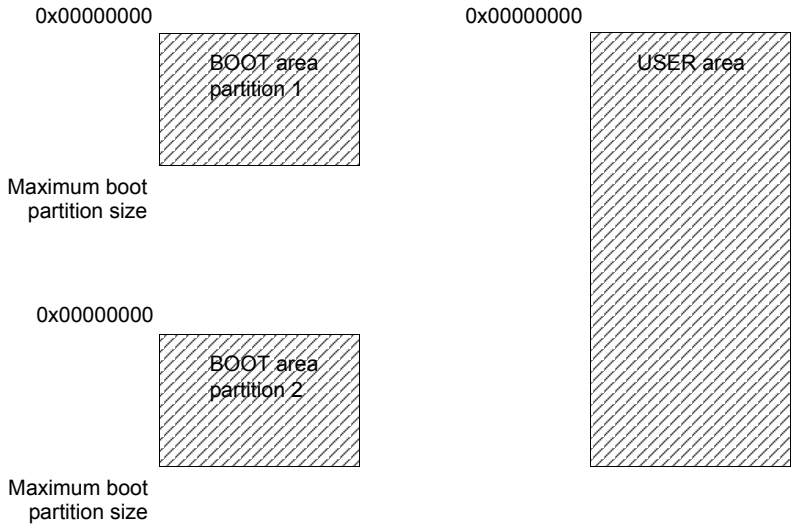


Figure 4. Memory Partition

Slave has boot configuration in Extended CSD register byte [179]. The master can choose the configuration by setting the register using CMD6 (switch). Slave also can be configured to boot from the user area by setting the BOOT_PARTITION_ ENABLE bits in the EXT_CSD register, byte [179] to 111b. If host boot from the user area, it will take longer time than boot partition area.

4.1.3 Change boot partition size

Initial boot partition size in moviNAND is set to zero. However, the boot partition size is allowed to be changed by user. Boot partition size changing sequence is following the sequence Figure 4-2 below. Argument of the third CMD62 can be set boot partition size. It can be calculated by this equation.

Argument (Boot Size) =(Number of Super Block for boot partition) / 2

For example, if user wants 10 super blocks for boot partition, argument of third CMD62 should be 0x5.

Detail values of moviNAND are referred to below Table.

After setting the boot partition size, all of data in the moviNAND is removed. And the value of EXT_CSD [227:226] and SEC_COUNT is automatically changing. So user should be careful changing boot partition size.

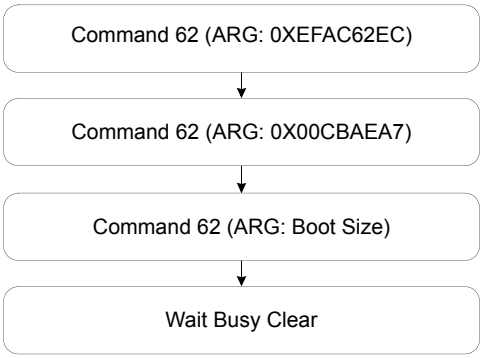


Figure 5. Boot Partition Size Changing Sequence

Density	Super Block Size	MAX Boot Partition Size	Max argument value
4GB	2MB	512MB	128
8GB	4MB	1024MB	128
16GB	4MB	1024MB	128
32GB	8MB	2GB	128

4.2 Smart Report

Samsung provide Report feature for the Host to notice the device state by Meta data. Samsung call this Smart Report. So Customer can acquire prime factor for understanding at the beginning analysis of error. Below table is the information about Smart Report.

Mode	Contents
Customer Report	1. Detect Error Mode 2. Detect Super Block Size 3. Detect Super Page Size 4. Detect Optimal Write Size 5. Detect Number Of Banks 6.The number of Initial Bad Block, Per Bank 7.the number of Run Time Bad Block, Per Bank 8.Number of remain block in Reserved Block 9.Max, Min, Avg Erase Count 10.Open count 11.Log message of the location that User Data ECC Error 12.Check result of Meta Data integrity

4.2.1 Smart Report Sequence

Functions	Command	Description
Entering Smart Report Mode	CMD62h(0xEFAC62EC) → CMD62h(0xCCEE)	After entering Smart Report Mode, the report-related Values are able to be checked on Read Command.
Confirming Smart Report	CMD17h(0x0)	It is possible to confirm Smart Report after reading Sector 1 at Address 0.
Removing Smart Report Mode	CMD62h(0xEFAC62EC) → CMD62h(0xDECCEE)	Smart Report Mode is removed by this command.

4.2.2 Smart Report Output Data (For Customer)

Data Slice	Field	Width	Remark
[3:0]	Error Mode	4 bytes	Normal : 0xD2D2D2D2, OpenFatalError : 0x37373737, RuntimeFatalError : 0x5C5C5C5C, MetaBrokenError : 0xE1E1E1E1 * In case of open error, other fields are not valid.
[7:4]	Super Block Size	4 bytes	Total Size(in byte) of simultaneously erasable physical blocks (e.g., Number of Channel * N-way Interleaving * physical block size)
[11:8]	Super Page Size	4 bytes	Total Size(in byte) of simultaneously programmable physical pages (e.g., Number of Channel * physical page size)
[15:12]	Optimal Write Size	4 bytes	Write size(in byte) at which the device performs best (e.g., Super Page Size * N-way Interleaving)
[19:16]	Number Of Banks	4 bytes	Number of banks connecting to each NAND flash. Bad blocks are managed by each banks.
[23:20]	Bank0 Init Bad Block	4 bytes	Number of initial defective physical blocks in Bank0
[27:24]	Bank0 Runtime Bad Block	4 bytes	Number of runtime defective physical blocks in Bank0
[31:28]	Bank0 remain reserved Block	4 bytes	Number of remain reserved physical blocks in Bank0
[35:32]	Bank1 Init Bad Block	4 bytes	Number of initial defective physical blocks in Bank1
[39:36]	Bank1 Runtime Bad Block	4 bytes	Number of runtime defective physical blocks in Bank1
[43:40]	Bank1 remain reserved Block	4 bytes	Number of remain reserved physical blocks in Bank1
[47:44]	Bank2 Init Bad Block	4 bytes	Number of initial defective physical blocks in Bank2
[51:48]	Bank2 Runtime Bad Block	4 bytes	Number of runtime defective physical blocks in Bank2
[55:52]	Bank2 remain reserved Block	4 bytes	Number of remain reserved physical blocks in Bank2
[59:56]	Bank3 Init Bad Block	4 bytes	Number of initial defective physical blocks in Bank3
[63:60]	Bank3 Runtime Bad Block	4 bytes	Number of runtime defective physical blocks in Bank3
[67:64]	Bank3 Reserved Block	4 bytes	Number of reserved physical blocks in Bank3
[71:68]	Max. Erase Count	4 bytes	Maximum erase count from among all physical blocks
[75:72]	Min. Erase Count	4 bytes	Minimum erase count from among all physical blocks
[79:76]	Avg. Erase Count	4 bytes	Average erase count of all physical blocks
[83:80]	Number of ECC Uncorrectable Error	4 bytes	Number of ECC Uncorrectable Error
[143:84]	ECC Uncorrectable Error Location	2 bytes * 30	Physical Block Address of ECC Uncorrectable Error
[203:144]	ECC Uncorrectable Error Location	2 bytes * 30	Physical Page Offset of ECC Uncorrectable Error
[219:204]	Reserved		
[223:220]	Read Reclaim Cnt	4 bytes	Number of Read Reclaim Count
[511:224]	Reserved		

Note: For 32GB
* Super Block Size : 8,388,608(8MB)
* Super Page Size : 16,384(16KB)
* Optimal Write Size : 65,536(64KB)
* Number Of Bank : 4

4.3 Reliable Write

MMC 4.3 supports reliable write sequence. Espicially Samsung moviNAND supports Max 255 sectors write by Reliable Write.
Detail description is in MMC4.3 Standard

CMD	Argument
CMD23	Bit[31] : reliable Write Request Bit[30:16] : set to 0 Bit[15:0] : number of blocks

5.0 Register Value

5.1 OCR Register

The 32-bit operation conditions register stores the V_{DD} voltage profile of the moviNAND. In addition, this register includes a status information bit. This status bit is set if the moviNAND power up procedure has been finished. The OCR register shall be implemented by all moviNANDs.

OCR bit	VDD voltage window[2]	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 - 1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode) -[*Higher than 2GB only]
[31]	moviNAND power up status bit (busy)[1]	

NOTE :
1) This bit is set to LOW if the moviNAND has not finished the power up routine
2) The voltage for internal flash memory(VDDF) should be 2.7-3.6v regardless of OCR Register value.

5.2 CID Register

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0x15
Reserved		6	[119:114]	---
Card/BGA	CBX	2	[113:112]	01
OEM/Application ID	OID	8	[111:104]	---[1]
Product name	PNM	48	[103:56]	See Product name table
Product revision	PRV	8	[55:48]	---[2]
Product serial number	PSN	32	[47:16]	---[3]
Manufacturing date	MDT	8	[15:8]	---[4]
CRC7 checksum	CRC	7	[7:1]	---[5]
not used, always '1'	-	1	[0:0]	---

NOTE :
1),4),5) description are same as MMC4.3 standard
2) PRV is composed of the revision count of VEX controller and the revision count of F/W patch
For example , the PRV of EVT1 Patch 02 are 0001 0010
3) A 32 bits unsigned binary integer. (Random Number)

5.2.1 Product name table (In CID Register)

Part Number	Density	Product Name in CID Register (PNM)
KLM4G1EEHM	4GB	0x4D344731474D
KLM8G2EEHM	8GB	0x4D384732474D
KLMAG4EEHM	16GB	0x4D414734474D
KLMBG8EEHM	32GB	0x4D424738474D

5.3 CSD Register

The Card-Specific Data register provides information on how to access the moviNAND contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27.

The type of the entries in the table below is coded as follows:

Name	Field	Width	Cell Type	CSD-slice	CSD Value			
					4GB	8GB	16GB	32GB
CSD structure	CSD_STRUCTURE	2	R	[127:126]	2 (CSD V1.2)			
System specification version	SPEC_VERS	4	R	[125:122]	4(V4.3)			
Reserved	-	2	R	[121:120]	-			
Data read access-time 1	TAAC	8	R	[119:112]	0x26			
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x01			
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32			
Card command classes	CCC	12	R	[95:84]	000011110101b Support :0,2,4,5,6,7 Not :1,3,8,9,10,11			
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x9			
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0 (Not Support)			
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0 (Not Support)			
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0 (Not Support)			
DSR implemented	DSR_IMP	1	R	[76:76]	0 (Not Support)			
Reserved	-	2	R	[75:74]	-			
Card size	C_SIZE	12	R	[73:62]	0xFFF			
Max. read current @ V_{DD} min	VDD_R_CURR_MIN	3	R	[61:59]	TBD	TBD	TBD	TBD
Max. read current @ V_{DD} max	VDD_R_CURR_MAX	3	R	[58:56]	TBD	TBD	TBD	TBD
Max. write current @ V_{DD} min	VDD_W_CURR_MIN	3	R	[55:53]	TBD	TBD	TBD	TBD
Max. write current @ V_{DD} max	VDD_W_CURR_MAX	3	R	[52:50]	TBD	TBD	TBD	TBD
Card size multiplier	C_SIZE_MULT	3	R	[49:47]	0x7			
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x7	0xF	0xF	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F			
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x1F			
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1 (enable)			
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0 (None)			
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x3	0x3	0x3	0x5
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x9 (512Byte)			
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0 (No)			
Reserved	-	4	R	[20:17]	-			
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0			
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0			

Copy flag (OTP)	COPY	1	R/W	[14:14]	1
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0 (No)
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0 (No)
File format	FILE_FORMAT	2	R/W	[11:10]	0
ECC code	ECC	2	R/W/E	[9:8]	None
CRC	CRC	7	R/W/E	[7:1]	-
Not used, always '1'	-	1	-	[0:0]	1

5.3.1 Write Protect Group Size

The unit of write protect in moviNAND is defined as multiples of Erase group size. For each density of moviNAND, detail information is described below.

Value	Register	Field				Calculation	Unit Size			
		4GB	8GB	16GB	32GB		4GB	8GB	16GB	32GB
Block Length	CSD	WRITE_BL_LEN				-	512B			
Erase Group		ERASE_GRP_SIZE (7) ERASE_GRP_MULT (31)	ERASE_GRP_SIZE (15) ERASE_GRP_MULT (31)	ERASE_GRP_SIZE (15) ERASE_GRP_MULT (31)	ERASE_GRP_SIZE (31) ERASE_GRP_MULT (31)	(ERASE_GRP_SIZE+1) x (ERASE_GRP_MULT+1) x BL_LEN (512B)	128KB	256KB	256KB	512KB
Write Protect Group		WP_GRP_SIZE (31)				Erase Group(Erasable Unit Size) X (WP_GRP_SIZE + 1)	4,096 KB	8,192 KB	8,192 KB	16,384 KB

5.4 Extended CSD Register

The Extended CSD register defines the moviNAND properties and selected modes. It is 512 bytes long.
The most significant 320 bytes are the Properties segment, which defines the moviNAND capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the moviNAND is working in. These modes can be changed by the host by means of the SWITCH command.

Name	Field	Size (Bytes)	Cell Type	CSD-slice	CSD Value			
					4GB	8GB	16GB	32GB
Properties Segment								
Reserved[1]		7		[511:505]	-			
Supported Command Sets	S_CMD_SET	1	R	[504]	0x01			
Reserved[1]		275	TBD	[503:229]	-			
Boot information	BOOT_INFO	1	R	[228]	0x1			
Boot partition size	BOOT_SIZE_MULTI[2]	1	R	[227]	0x00			
Boot partition size	BOOT_SIZE_MULTI[2]	1	R	[226]	0x00			
Access size	ACC_SIZE	1	R	[225]	0x06			
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x00			
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x00			
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0xFF			
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x00			
Sleep current (VDDF)	S_C_VCC	1	R	[220]	TBD	TBD	TBD	TBD
Sleep current (VDD)	S_C_VCCQ	1	R	[219]	TBD	TBD	TBD	TBD
Reserved[1]		1	TBD	[218]	-			
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	TBD	TBD	TBD	TBD
Reserved[1]		1	TBD	[216]	-			
Sector Count	SEC_COUNT	4	R	[215:212]	see density specification table			
Reserved[1]		1		[211]	-			
Minimum Write Performance for 8bit @52MHz	MIN_PERF_W_8_52	1	R	[210]	TBD	TBD	TBD	TBD
Minimum Read Performance for 8bit @52MHz	MIN_PERF_R_8_52	1	R	[209]	TBD	TBD	TBD	TBD
Minimum Write Performance for 8bit @26MHz /4bit @52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	TBD	TBD	TBD	TBD
Minimum Read Performance for 8bit @26MHz /4bit @52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	TBD	TBD	TBD	TBD
Minimum Write Performance for 4bit @26MHz	MIN_PERF_W_4_26	1	R	[206]	TBD	TBD	TBD	TBD
Minimum Read Performance for 4bit @26MHz	MIN_PERF_R_4_26	1	R	[205]	TBD	TBD	TBD	TBD
Reserved[1]		1		[204]	-			
Power Class for 26MHz @ 3.6V	PWR_CL_26_360	1	R	[203]	TBD	TBD	TBD	TBD
Power Class for 52MHz @ 3.6V	PWR_CL_52_360	1	R	[202]	TBD	TBD	TBD	TBD
Power Class for 26MHz @ 1.95V	PWR_CL_26_195	1	R	[201]	TBD	TBD	TBD	TBD

Power Class for 52MHz @ 1.95V	PWR_CL_52_195	1	R	[200]	TBD	TBD	TBD	TBD
Reserved[1)]		3		[199:197]	-			
Card Type	CARD_TYPE	1	R	[196]	0x03			
Reserved[1)]		1		[195]	-			
CSD Structure Version	CSD_STRUCTURE	1	R	[194]	0x02			
Reserved[1)]		1		[193]	-			
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	0x03			
Modes Segment								
Command Set	CMD_SET	1	R/W	[191]	0x00			
Reserved[1)]		1		[190]	-			
Command Set Revision	CMD_SET_REV	1	RO	[189]	0x0			
Reserved[1)]		1		[188]	-			
Power Class	POWER_CLASS	1	R/W	[187]	0x00			
Reserved[1)]		1		[186]	-			
High Speed Interface Timing	HS_TIMING	1	R/W	[185]	0x00			
Reserved[1)]		1		[184]	-			
Bus Width Mode	BUS_WIDTH	1	WO	[183]	0x00			
Reserved[1)]		1		[182]	-			
Erased Memory Content	ERASED_MEM_CONT	1	RO	[181]	0x00			
Reserved[1)]		1		[180]	-			
Boot configuration	BOOT_CONFIG	1	R/W	[179]	0x00			
Reserved[1)]		1		[178]	-			
Boot bus width1	BOOT_BUS_WIDTH	1	R/W	[177]	0x00			
Reserved[1)]		1		[176]	-			
High-density erase group definition	ERASE_GROUP_DEF	1	R/W	[175]	0x00			
Reserved[1)]		175		[174:0]	-			

NOTE :
1) Reserved bits should be read as "0."
2) BOOT_SIZE_MULTI is extended one more byte for Boot partition size.

5.4.1 Density Specification

Parameter	4GB	8GB	16GB	32GB
User area density	more than 4,000,000,000Byte	more than 8,000,000,000Byte	more than 16,000,000,000Byte	more than 30,000,000,000Byte
SEC_COUNT_ in Extended CSD	0x767000	0xEFA000	0x1E0E000	0x3BF8000

6.0 Power Up

An moviNAND bus power-up is handled locally in each device and in the bus master. Figure 6 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence.

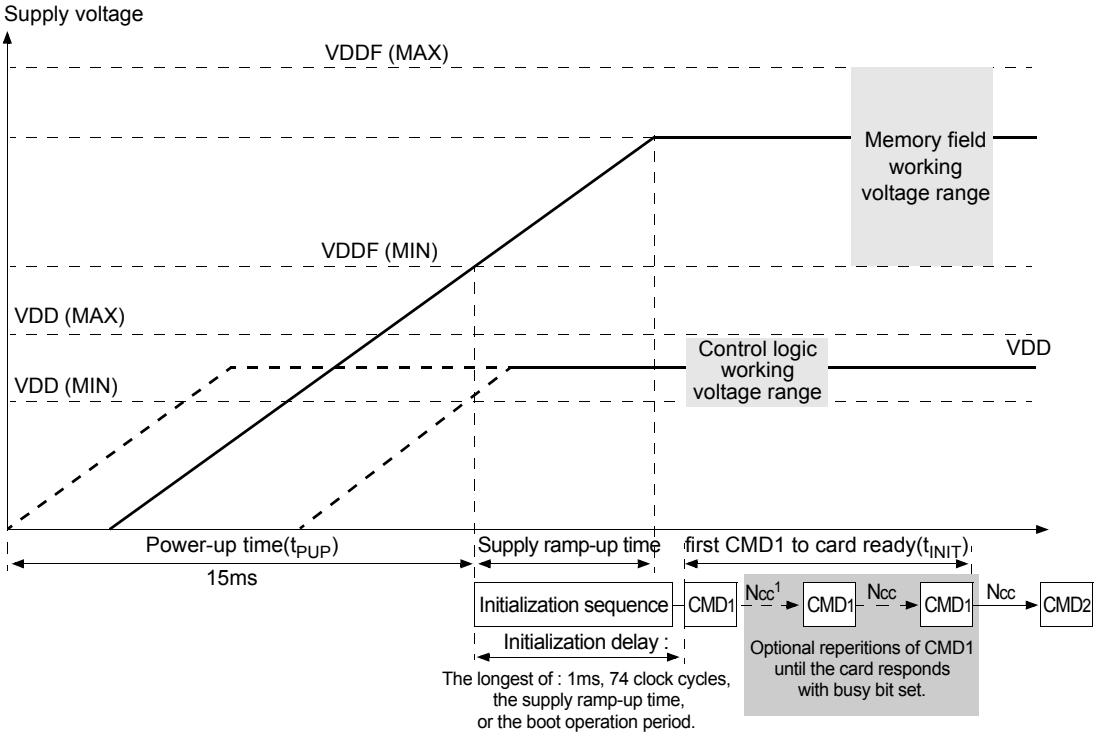


Figure 6. moviNAND Power up Sequence

7.0 Power Down

Before power off, BUSY bit should be cleared. When a CPU reset is requested during a data write, VDDF is recommended to remain stable for 500ms to minimize the data corruption. Figure 7 shows the power-down sequence.

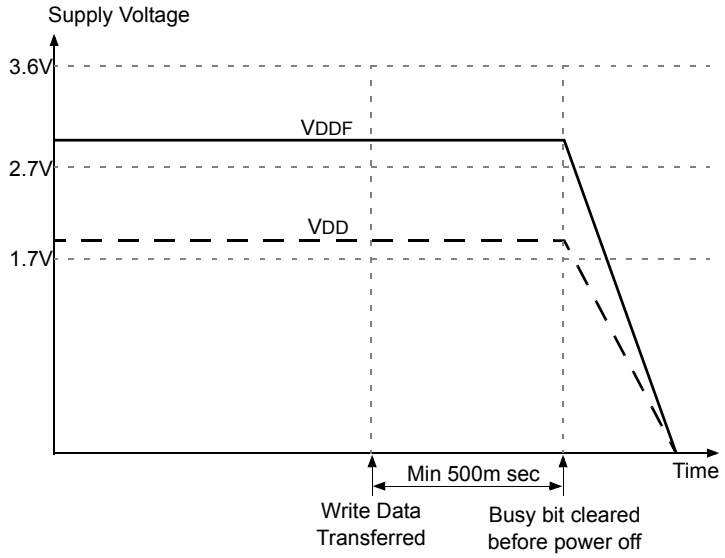


Figure 7. Power Down sequence

8.0 AC Parameter

8.1 ime out Parameter

Parameter	Symbol	Max	Unit
Initialization Time Out [1]	t_{INIT}	1	s
Power-up time [2]	t_{PUP}	15	ms
Write Time Out	-	600	ms
Erase Time Out [3]	-	1	s
Read Time Out	-	100	ms

8.2 Bus Timing Parameter

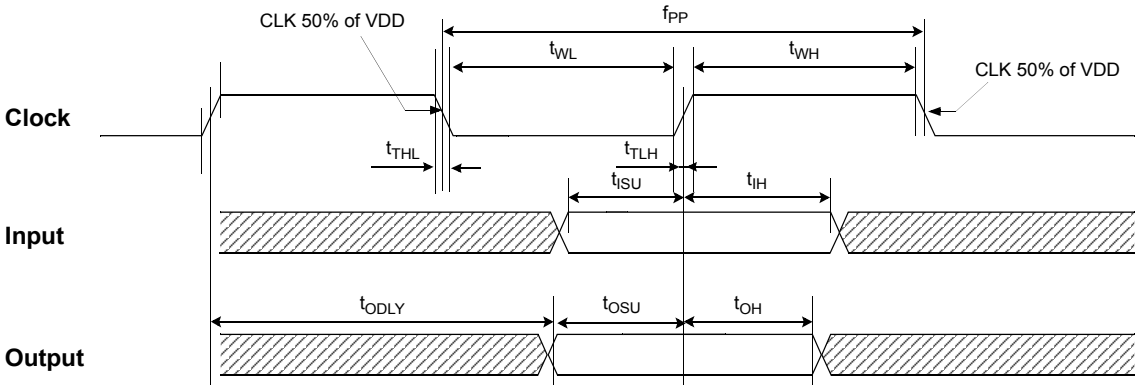


Figure 9. Timing Diagram - Data Input/Output Referenced to Clock

Default (under 26MHz)

Parameter	Symbol	Min	Max	Unit	Remark[1]
Clock CLK(All values are referred to min(V_{IH}) and max(V_{IL})[2]					
Clock frequency Data Transfer Mode3	fPP	0[4]	26	MHz	CL <= 30 pF Tolerance: +100KHz
Clock frequency Identification Mode	f_{OD}	0[4]	400	kHz	Tolerance: +20KHz
Clock low time	t_{WL}	10		ns	C_L <= 30 pF
Clock high time	t_{WH}	10			
Clock rise time[5]	t_{TLH}		10	ns	C_L <= 30 pF
Clock fall time	t_{THL}		10	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output hold time	t_{OH}	8.3		ns	CL <= 30 pF
Output set-up time	t_{OSU}	11.7		ns	CL <= 30 pF

NOTE :
1)The card must always start with the backward-compatible interface timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
2) CLK timing is measured at 50% of VDD.
3) For compatibility with cards that suport the v4.2 standard or earlier, host should not use>20MHz before switching to high-speed interface timing.
4) Frequency is periodically sampled and not 100% tested.
5) CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL}).

High-Speed Mode

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK(All values are referred to min(V_{IH}) and max(V_{IL})[1]					
Clock frequency Data Transfer Mode[2]	f_{PP}	0[3]	52[4]	MHz	C_L <= 30 pF
Clock frequency Identification Mode	f_{OD}	0[3]	400	kHz	CL <= 30 pF
Clock low time	t_{WL}	6.5		ns	C_L <= 30 pF
Clock High time	t_{WH}	6.5		ns	C_L <= 30 pF
Clock rise time[5]	t_{TLH}		3	ns	C_L <= 30 pF
Clock fall time	t_{THL}		3	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	CL <= 30 pF
Output hold time	t_{OH}	2.5			C_L <= 30 pF
Signal rise time[6]	t_{RISE}		3	ns	C_L <= 30 pF
Signal fall time	t_{FALL}		3	ns	C_L <= 30 pF

NOTE :
1) CLK timing is measured at 50% of V_{DD}.
2) A MultiMediaCard shall support the full frequency range from 10-26MHz, or 10-52MHz
3) Frequency is periodically sampled and not 100% tested.
4) Card can operate as high-speed card interface timing at 26MHz clock frequency.
5) CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL}).6) Inputs CMD, DAT rise and fall times are measured by min(V_{IH}) and max(V_{IL}), and outputs CMD, DAT rise and fall times are measured by min(V_{OH}) and max(V_{OL}).

9.0 DC Parameter

9.1 Current

Parameter	Value	Unit
Max RMS Current	150	mA
Max stand-by Current	450	μA

Note:
The measurement for max RMS current is the average RMS current consumption over a period of 100ms.
Max peak current is defined as the absolute max value. Max Current should always be within this value

9.2 Bus Operating Conditions

Parameter	Min	Max	Unit
Peak voltage on all lines	-0.5	3.6	V
Input Leakage Current	-10	10	μA
Output Leakage Current	-10	10	μA

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	1.70(or 2.7)	1.95(or 3.6)	V
	V_{DDF}	2.7	3.6	V
	V_{SS}	-0.5	0.5	V

9.3 Bus Signal Line Load

The total capacitance C_L of each line of the moviNAND bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{movi} of the moviNAND connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{movi}$$

The sum of the host and bus capacitances should be under 20pF.

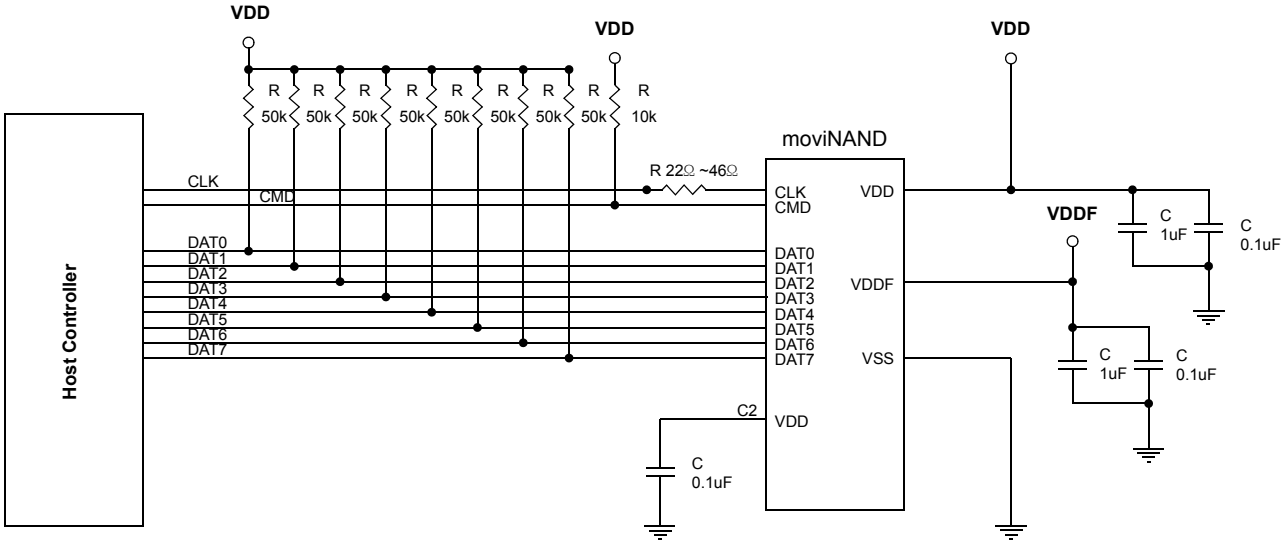
Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	50	100	KOhm	to prevent bus floating
Internal pull up resistance DAT0-DAT7	R_{int}	50	150	KOhm	to prevent unconnected lines floating
Bus signal line capacitance	C_L		30	pF	Single moviNAND
Single moviNAND capacitance	C_{movi}		13	pF	
Maximum signal line inductance			16	nH	f_{PP} <= 52 MHz

9.3.1 moviNAND Connection Guide

This Connection guide is an example for customers to adopt moviNAND more easily

9.3.1.1 x8 support Host connection Guide

- This appendix is Just guideline for moviNAND connection. This value and schematic can be changed depens on the system environment.
- Coupling capacitor (1 μF + 0.1μF (TBD)) have to be connected with VDD and VSS as close as possible.
- VDDI Capacitor is min 0.1uF



9.3.1.2 x4 support Host connection Guide