Samsung e·MMC Product family

e.MMC 4.5 Specification compatibility

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	1. Initial issue	Sep. 29, 2011	Target	S.M.Lee
0.5	1. Engineering Sample 2. 64GB is deleted 3. Discard Time is added in Table 10 4. Init time is changed to 3sec which is the value after partition setting in Table 44 5. Extended CSD Register values are changed in Chapter 7.4 - HPI_FEATURES is changed from 0x03 to 0x01 - DATA_TAG_SUPPORT is changed from 0x00 to 0x01 - INI_TIMEOUT_AP is changed from 0x0A to 0x1E - TRIM_MULT is changed from 0x01 to 0x02 - SEC_ERASE_MULT is changed from 0x0A to 0x1B - SEC_TRIM_MULT is changed from 0x0A to 0x11 - ACC_SIZE is changed from 0x05 to 0x07 - OUT_OF_INTERRUPT_TIME is changed from 0x01 to 0x02 6. Time Parameters are changed in Table 60 - Initialization time is divided into 'Normal' and 'After partition setting' - Write timeout is changed from 300ms to 350ms - Erase timeout is changed from 10ms to 15ms - Secure Erase timeout is changed from 3sec to 8sec - Secure Trim step1 timeout is changed from 300ms to 5sec - Trim timeout is changed from 300ms to 600ms - Packed command timeout is changed from 300ms to 350ms - Discard timeout is deleted	Dec. 16, 2011	Preliminary	S.M.Lee
1.0	1. Customer Sample 2. 16GB is deleted 3. Maximum enhanced partition size is changed in Table 47 4. Performance is updated with measured value in Table 54 5. Extended CSD Register values are changed in Chapter 7.4 - HC_WP_GRP_SIZE is changed from 0x40 to 0x50 - MAX_ENH_SIZE_MULT is changed from 0x1D1 to 0x174	Jan. 16, 2012	Final	S.M.Lee
1.1	1. Read Timeout Typo is corrected in Table 60	Feb. 09 ,2012	Final	S.M.Lee
1.2	1. Typo of default Boot Area Partition size is corrected in Chapter 6.1.1.1 [512KB -> 2,048KB]	Mar. 12, 2012	Final	S.M.Lee
1.3	1. 16GB and 64GB products are added 2. 'Dual Data Rate mode is supported' is added in Chapter 2.0 3. List of interruptible command is changed in Table 28 4. Information of Wear Leveling is deleted in Chapter 6.1.4 5. Information of 'End of Life Management' is deleted in Chapter 6.1.7 6. Information of Smart Report is deleted in Chapter 6.2	May. 11, 2012	Final	S.M.Lee
1.4	1. Maximum Enhanced Partition Size of 16GB is changed in Table 46 2. User Density Size of 16GB is changed in Table 47 3. Extended CSD Register values are changed in Chapter 7.4 - SEC_COUNT of 16GB is changed from 0x1D5A000 to 0x1D1F000 - MAX_ENH_SIZE_MULT of 16GB is changed from 0xBB to 0xBA	Jul.20, 2012	Final	S.M.Lee

Revision History Appendix(0.5)

Before(ver.0.0)

[Table 1] Product List

Capacities	e·MMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
16GB	KLMAG4FE4B-B001	32Gb MLC x 4	91.0%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 1.0mm	153FBGA
32GB	KLMBG8FE4B-B001	32Gb MLC x 8			11.5mm x 13mm x 1.2mm	
64GB	KLMCGAFE4B-B001	32Gb MLC x 16			11.5mm x 13mm x 1.4mm	

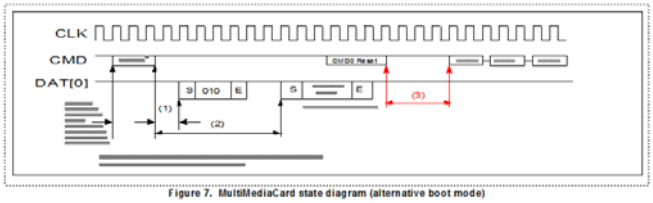


Figure 7. MultiMediaCard state diagram (alternative boot mode)

[Table 43] Boot ACK and Boot Data timing value and Initialization time

Timing Factor	Value
(1) Boot ACK Time	< 50 ms
(2) Boot Data Time	< 60 ms
(3) Initialization Time*	< 200 ms

* Definition of Initialization Time : CMD0 ~ CMD1 busy bit clearing time. For Initialization time after partition setting, Please refer to INI_TIMEOUT_AP in 7.4 Extended CSD Register.

Minimum function for reading boot data is initialized during boot time and after that full function is initialized during initialization time.

[Table 58] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD-slice	CSD Value 16GB	32GB	64GB
HPI features	HPI_FEATURES	1	R	[503]		0x03	
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]		0x00	
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]		0x0A	
TRIM Multiplier	TRIM_MULT	1	R	[232]		0x01	
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]		0x0A	
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]		0x0A	
Access size	ACC_SIZE	1	R	[225]		0x05	
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[196]		0x01	

[Table 59] Time Parameter

Timing Paramter	Max. Value	Unit
Initialization Time (tINIT)	1	s
Read Timeout	100	ms
Write Timeout	300	ms
Erase Timeout	10	ms
Force Erase Timeout	3	min
Secure Erase Timeout	3	s
Secure Trim step1 Timeout	300	ms
Secure Trim step2 Timeout	3	s
Trim Timeout	300	ms
Partition Switching Timeout (after Init)	100	us
Packed Command Timeout	300	ms
Discard Timeout	10	ms
Power Off Notification (Short) Timeout	100	ms
Power Off Notification (Long) Timeout	600	ms

After(ver.0.5)

[Table 1] Product List

Capacities	e·MMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
16GB	KLMAG4FE4B-B001	32Gb MLC x 4	91.0%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 1.0mm	153FBGA
32GB	KLMBG8FE4B-B001	32Gb MLC x 8			11.5mm x 13mm x 1.2mm	

[Table 10] Discard Time

Timing Factor	Value
Discard 1)	< 15ms

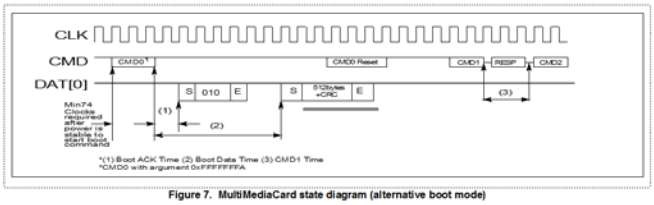


Figure 7. MultiMediaCard state diagram (alternative boot mode)

[Table 44] Boot ack, boot data and initialization Time

Timing Factor	Value
(1) Boot ACK Time	< 50 ms
(2) Boot Data Time	< 60 ms
(3) Initialization Time*1)	< 3 secs

NOTE:
1) This initialization time includes partition setting. Please refer to INI_TIMEOUT_AP in 7.4 Extended CSD Register.
Normal initialization time (without partition setting) is completed within 1sec.

[Table 59] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD-slice	CSD Value 16GB	32GB
HPI features	HPI_FEATURES	1	R	[503]		0x01
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]		0x01
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]		0x1E
TRIM Multiplier	TRIM_MULT	1	R	[232]		0x02
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]		0x1B
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]		0x11
Access size	ACC_SIZE	1	R	[225]		0x07
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]		0x02

[Table 60] Time Parameter

Timing Paramter		Max. Value	Unit
Initialization Time (tINIT)	Normal 1)	1	s
	After partition setting 2)	3	s
Read Timeout		100	ms
Write Timeout		350	ms
Erase Timeout		15	ms
Force Erase Timeout		3	min
Secure Erase Timeout		8	s
Secure Trim step1 Timeout		5	s
Secure Trim step2 Timeout		3	s
Trim Timeout 3)		600	ms
Partition Switching Timeout (after Init)		100	us
Packed Command Timeout		350	ms
Power Off Notification (Short) Timeout		100	ms
Power Off Notification (Long) Timeout		600	ms

NOTE:
1) Normal Initialization Time without partition setting
2) Initialization Time after partition setting, refer to INI_TIMEOUT_AP in 7.4 EXT_CSD register
3) If 8KB Size and Address are aligned, Max. Timeout value is 300ms

Revision History Appendix(1.0)

Before(ver.0.5)

[Table 1] Product List

Capacities	e-MMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
16GB	KLMAG4FE4B-B001	32Gb MLC x 4	91.0%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 1.0mm	153FBGA
32GB	KLMBG8FE4B-B001	32Gb MLC x 8			11.5mm x 13mm x 1.2mm	

[Table 54] Performance

Density	Sequential Read (MB/s)	Sequential Write (MB/s)
32 GB	85	40

* Test/ Estimation Condition : Bus width x8, 52MHz DDR, 4MB data transfer, w/o file system overhead

[Table 59] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD-slice	CSD Value 32GB
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x40
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x1D1

After(ver.1.0)

[Table 1] Product List

Capacities	e-MMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
32GB	KLMBG8FE4B-B001	32Gb MLC x 8	91.0%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 1.2mm	153FBGA

[Table 54] Performance

Density	Sequential Read (MB/s)	Sequential Write (MB/s)
32 GB	75	43

* Test Condition : Bus width x8, 50MHz DDR, 4MB data transfer, w/o file system overhead, measured on Samsung's internal board

[Table 59] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD-slice	CSD Value 32GB
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x50
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x174

Revision History Appendix(1.1)

Before(ver.1.0)

[Table 60] Time Parameter

Timing Paramter		Max. Value	Unit
Initialization Time (tINIT)	Normal [1]	1	s
Read Timeout	After partition setting [2]	3	s

After(ver.1.1)

[Table 60] Time Parameter

Timing Paramter		Max. Value	Unit
Initialization Time (tINIT)	Normal [1]	1	s
	After partition setting [2]	3	s
Read Timeout		100	ms

Revision History Appendix(1.2)

Before(ver.1.1)

6.1.1.1 Boot Area Partition and RPMB Area Partition

Default size of each Boot Area Partition is 512KB and can be changed by Vendor Command as multiple of 512KB.
Default size of RPMB Area Partition is 128 KB and can be changed by Vendor Command as multiple of 128KB.

After(ver.1.2)

6.1.1.1 Boot Area Partition and RPMB Area Partition

Default size of each Boot Area Partition is 2,048KB and can be changed by Vendor Command as multiple of 512KB.
Default size of RPMB Area Partition is 128 KB and can be changed by Vendor Command as multiple of 128KB.

Revision History Appendix(1.3)

Before(ver.1.2)

[Table 1] Product List

Capacities	e-MMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
32GB	KLMBG8FE4B-B001	32Gb MLC x 8	91.0%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 1.2mm	153FBGA

[Table 28] List of Interruptible Command

Commands	Names	Notes
CMD24	WRITE SINGLE BLOCK	-
CMD25	WRITE MULTIPLE BLOCKS	-
CMD25	RELIABLE WRITE	Stopping a reliable write command with 'High Priority Interrupt' flag set turns that command into a reliable write command
CMD38	ERASE	-
	TRIM	-
	SECURE ERASE	-
	SECURE TRIM	-
CMD6	SWITCH	BACKGROUND OPERATION ONLY

After(ver.1.3)

[Table 1] Product List

Capacities	e-MMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
16GB	KLMAG4FE4B-B001	32Gb MLC x 4	91.0%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 1.0mm	153FBGA
32GB	KLMBG8FE4B-B001	32Gb MLC x 8			11.5mm x 13mm x 1.2mm	
64GB	KLMCGAFE4B-B001	32Gb MLC x 16			11.5mm x 13mm x 1.4mm	

[Table 28] List of Interruptible Command

Command Index	Name	Is interruptible?
CMD24	WRITE_BLOCK	Yes
CMD25	WRITE_MULTIPLE_BLOCK	Yes
CMD38	ERASE	Yes
CMD6	SWITCH, byte BKOPS_START, any value	Yes
	SWITCH, byte SANITIZE_START, any value	Yes
	SWITCH, byte POWER_OFF_NOTIFICATION, value POWER_OFF_LONG	Yes
	SWITCH, byte POWER_OFF_NOTIFICATION, other values	No
	CACHE_CTRL when used for turning the cache OFF	Yes
	FLUSH_CACHE	Yes
	SWITCH, other bytes, any value	No
All others		No

Revision History Appendix(1.4)

Before(ver.1.3)

[Table 46] Maximum Enhanced Partition Size

Device	Max. Enhanced Partition Size
16 GB	7,843,348,480 Bytes
32 GB	15,602,810,880 Bytes
64 GB	31,247,564,800 Bytes

[Table 47] User Density Size

Device	User Density Size
16 GB	15,758,000,128 Bytes
32 GB	31,268,536,320 Bytes
64 GB	62,537,072,640 Bytes

[Table 55] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD slice	CSD Value		
					16GB	32GB	64GB
Sector Count	SEC_COUNT	4	R	[215:212]	0x1D5A000	0x3A3E000	0x747C000
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0xBB	0x174	0x2E9

After(ver.1.4)

[Table 46] Maximum Enhanced Partition Size

Device	Max. Enhanced Partition Size
16 GB	7,801,405,440 Bytes
32 GB	15,602,810,880 Bytes
64 GB	31,247,564,800 Bytes

[Table 47] User Density Size

Device	User Density Size
16 GB	15,634,268,160 Bytes
32 GB	31,268,536,320 Bytes
64 GB	62,537,072,640 Bytes

[Table 55] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD slice	CSD Value		
					16GB	32GB	64GB
Sector Count	SEC_COUNT	4	R	[215:212]	0x1D1F000	0x3A3E000	0x747C000
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0xBA	0x174	0x2E9

Table Of Contents

INTRODUCTION

The SAMSUNG e·MMC is an embedded MMC solution designed in a BGA package form. e·MMC operation is identical to a MMC card and therefore is a simple read and write to memory using MMC protocol v4.5 which is a industry standard.

e·MMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF) whereas 1.8V or 3V dual supply voltage (VDD) is supported for the MMC controller. Maximum MMC interface frequency of 52MHz and maximum bus widths of 8 bit are supported.

There are several advantages of using e·MMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.

The embedded flash mangement software or FTL(Flash Transition Layer) of e·MMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

1.0 PRODUCT LIST

[Table 1] Product List

Capacities	e·MMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
16GB	KLMAG4FE4B-B001	32Gb MLC x 4	91.0%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 1.0mm	153FBGA
32GB	KLMBG8FE4B-B001	32Gb MLC x 8			11.5mm x 13mm x 1.2mm	
64GB	KLMCGAFE4B-B001	32Gb MLC x 16			11.5mm x 13mm x 1.4mm	

2.0 KEY FEATURES

- MultiMediaCard System Specification Ver. 4.5 compatible. Detail description is referenced by JEDEC Standard
- SAMSUNG e·MMC supports below special features of eMMC4.5 which are being discussed in JEDEC

  - Supported Features : Packed command, Cache, Discard, Sanitize, Power Off Notification

  - Non-supported Features : Partition types, Context ID, Data Tag, Real Time Clock, Dynamic Device Capacity, Thermal Spec, Large Sector Size (4KB)

- Full backward compatibility with previous MultiMediaCard system (1bit data bus, multi-e·MMC systems)
- Data bus width : 1bit (Default) , 4bit and 8bit
- MMC I/F Clock Frequency : 0 ~ 52MHz
  MMC I/F Boot Frequency : 0 ~ 52MHz
- Dual Data Rate mode is supported
- Temperature : Operation(-25°C ~ 85°C), Storage without operation (-40°C ~ 85°C)
- Power : Interface power → VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) , Memory power → VDDF(2.7V ~ 3.6V)

3.0 PACKAGE CONFIGURATIONS

3.1 153 Ball Pin Configuration

[Table 2] 153 Ball Information

Pin NO	Name
A3	DAT0
A4	DAT1
A5	DAT2
B2	DAT3
B3	DAT4
B4	DAT5
B5	DAT6
B6	DAT7
K5	RSTN
C6	VDD
M4	VDD
N4	VDD
P3	VDD
P5	VDD
E6	VDDF
F5	VDDF
J10	VDDF
K9	VDDF
C2	VDDI
M5	CMD
M6	CLK
C4	VSS
E7	VSS
G5	VSS
H10	VSS
K8	VSS
N2	VSS
N5	VSS
P4	VSS
P6	VSS

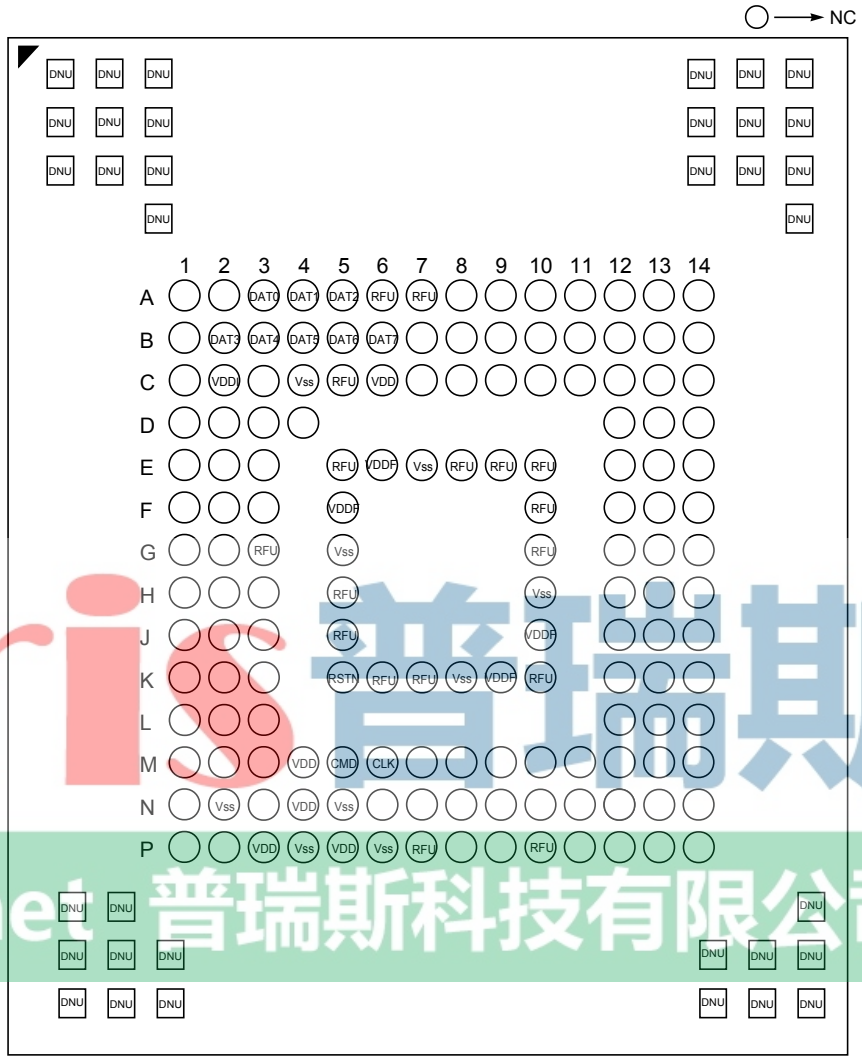


Figure 1. 153-FBGA

3.1.1 11.5mm x 13mm x 1.0mm Package Dimension

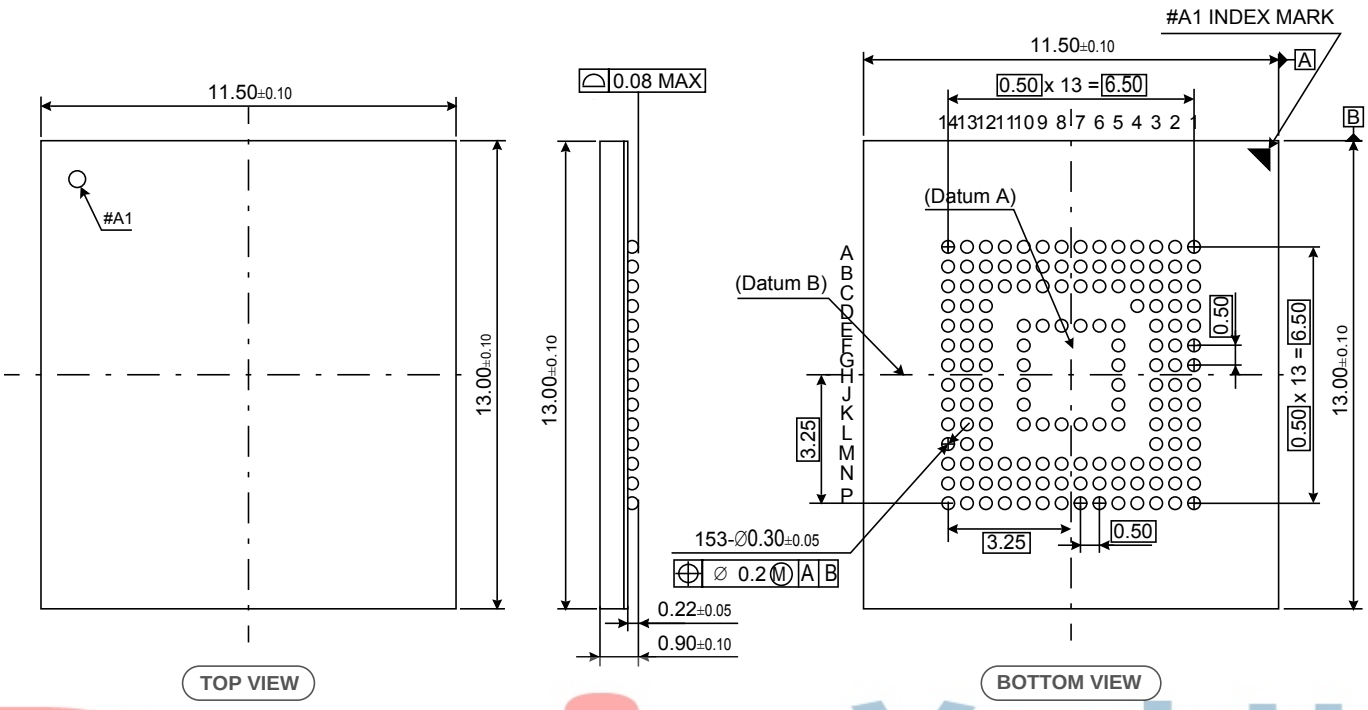


Figure 2. 11.5mm x 13mm x 1.0mm Package Dimension

3.1.2 11.5mm x 13mm x 1.2mm Package Dimension

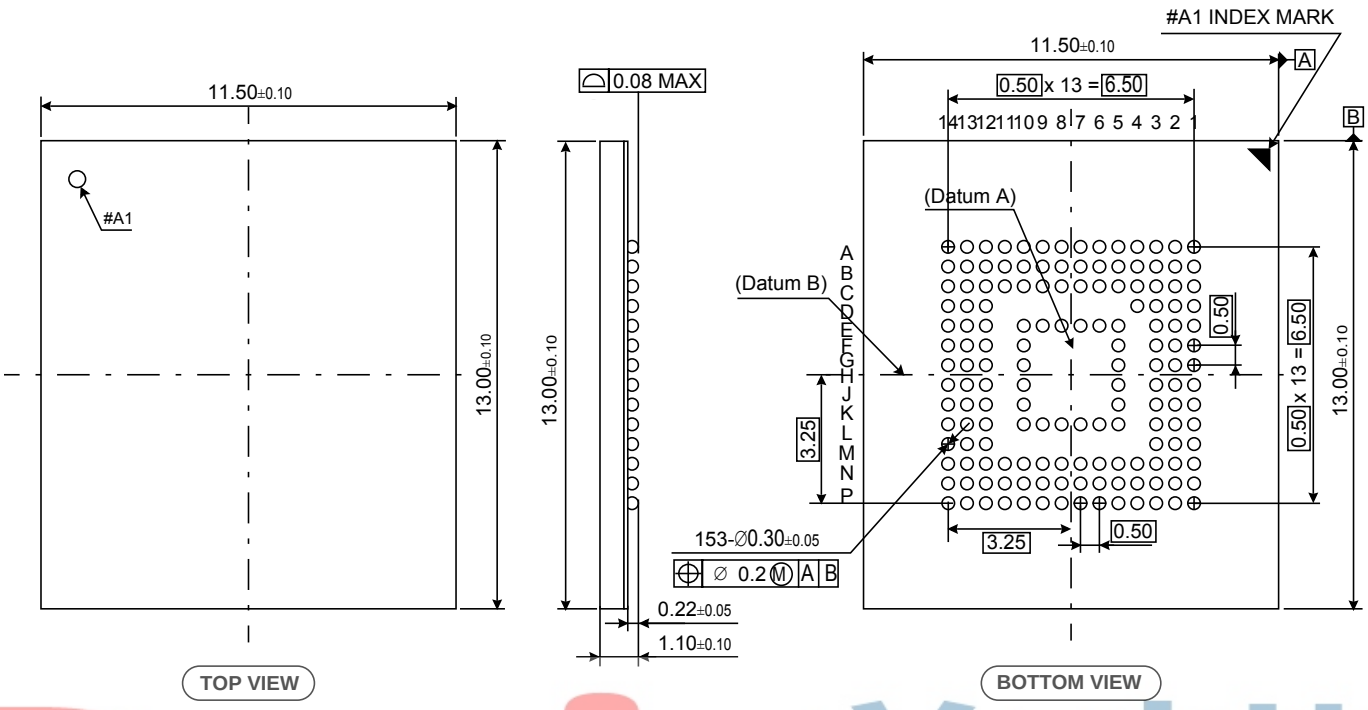


Figure 3. 11.5mm x 13mm x 1.2mm Package Dimension

3.1.3 11.5mm x 13mm x 1.4mm Package Dimension

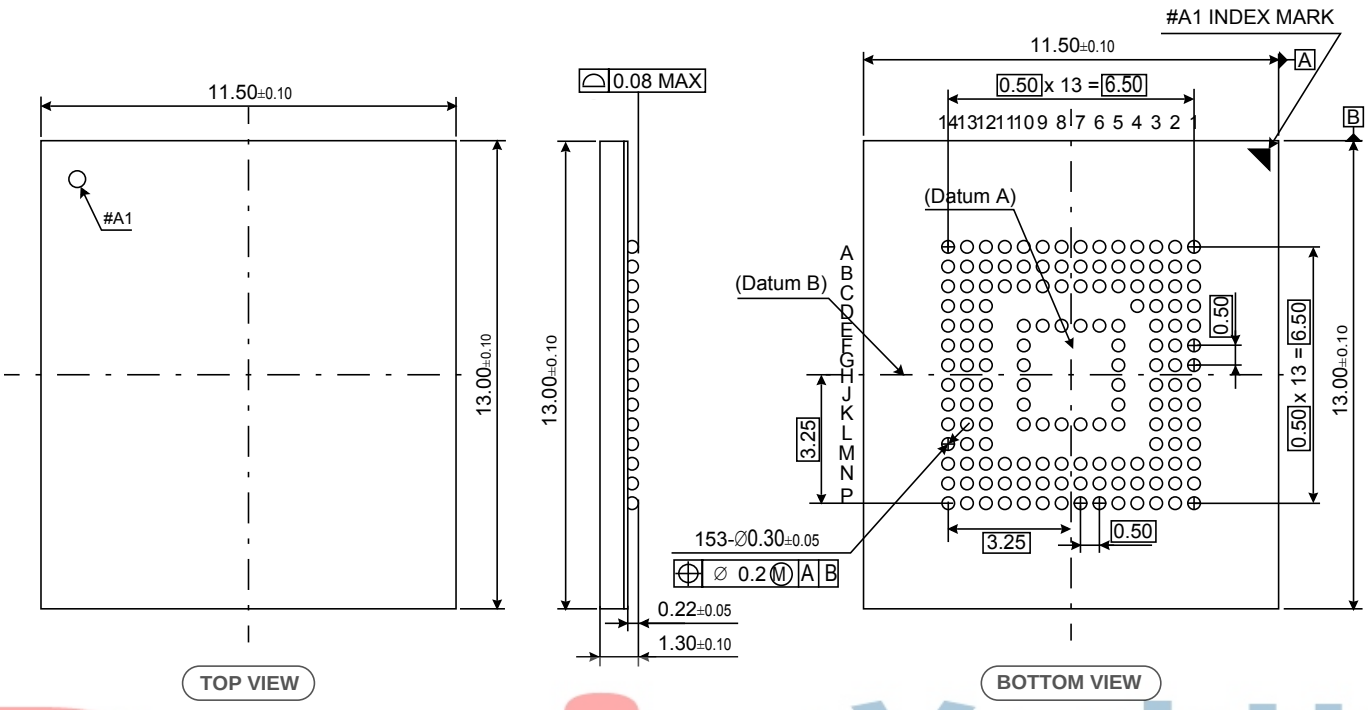


Figure 4. 11.5mm x 13mm x 1.4mm Package Dimension

3.2 Product Architecture

- e·MMC consists of NAND Flash and Controller. VDD is for Controller power and VDDF is for flash power

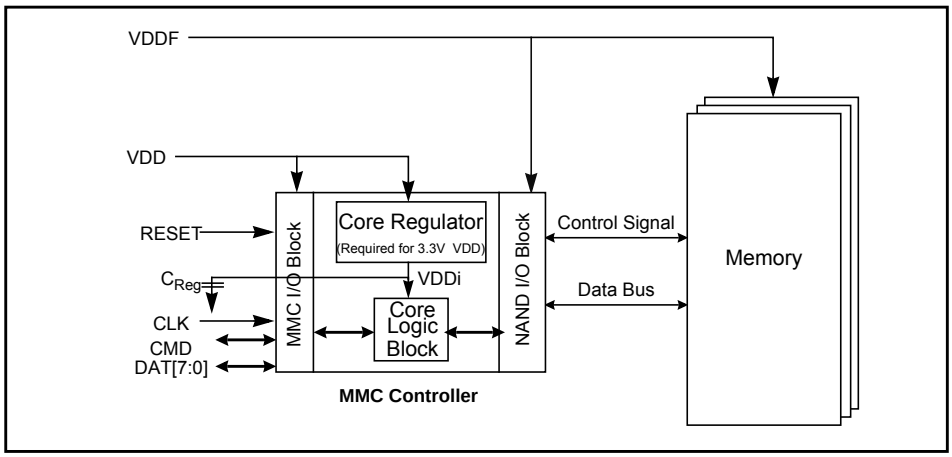


Figure 5. e·MMC Block Diagram

4.0 e.MMC 4.5 features

4.1 Packed Command

Packed command is a host and device communication technique to improve performance of eMMC. In order to reduce command overhead, read and write commands can be packed in groups of commands (either all read or all write) that transfer data for all commands in the group on the bus in one transfer. Packed Write operation should be transacted in order.

[Packed Write and Read Sequence]

• Packed Write : Packed Write Command can group several write multiple block commands by using SET_BLOCK_COUNT (CMD23) with the Packed flag set → WRITE_MULTIPLE_BLOCK (CMD25) with 1st block containing the packed command header → Write the data in order of appearance in the header

• Packed Read : Packed Read Command can group several read multiple block commands by using SET_BLOCK_COUNT (CMD23) with the Packed flag set and block count of one → WRITE_MULTIPLE_BLOCK (CMD25) with the header → CMD23 with the Packed flag set and total block count which is sum of all block count of all data reads (This CMD23 is optional, Open-ended read is also available) → READ_MULTIPLE_BLOCK (CMD18) → Read the data

[Table 3] Command description related to Packed Read and Write

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD18	adtc	[31:0] data address	R1	READ_MULTIPLE_BLOCK	Continuously transfers data blocks from Device to host until interrupted by a stop command, or the requested number of data blocks is transmitted. If sent as part of a packed read command, the argument shall contain the 1st read data address in the pack (address of 1st individual read command inside the pack.
CMD23 (packed)	Ac	[31] set to 0 [30] '1' packed [29:16] set to 0 [15:0] number of blocks	R1	SET_BLOCK_COUNT	Packed command version Defines the number of blocks (read/write) for the following packed write command or for the header of the following packed read command. For packed write commands, the number of blocks should include the total number of blocks all packed commands plus one for the header block. For packed read commands, the number of blocks should equal one as only header is sent inside the following CMD25. After that, a separate normal read command is sent to get the packed data.
CMD25	adtc	[31:0] data address1	R1	WRITE_MULTIPLE_BLOCK	Continuously writes blocks of data until a STOP_TRANSMISSION follows or the requested number of block received. If sent as a packed command (either packed write, or the header of packed read) the argument shall contain the 1st read/write data address in the pack. (address of 1st individual command inside the pack)

[Table 4] EXT_CSD value for Packed Command

Name	Field	Size (Bytes)	Cell Type	CSD-Slice	Value
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x00
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00

[Table 5] Definition of EXT_CSD value for Packed Command

Field	Definition
MAX_PACKED_READS	Max. number of commands that can be packed in the packed read command. Min. value is '5'
MAX_PACKED_WRITES	Max. number of commands that can be packed in the packed write command. Min. value is '3'
EXCEPTION_EVENTS_CTRL	Bit [15:4], Bit [0] : Reserved Bit [3] : PACKED_EVENT_EN Bit [2] : SYSPOOL_EVENT_EN Bit [1] : DYNCAP_EVENT_EN
EXCEPTION_EVENTS_STATUS	Bit [15:4] : Reserved Bit [3] : PACKED_FAILURE (If this bit is set, the last packed command has failed. Host should check EXT_CSD field PACKED_COMMAND_STATUS for the detailed cause.) Bit [2] : SYSPOOL_EXHAUSTED Bit [1] : DYNCAP_NEEDED Bit [0] : URGENT_BKOPS
PACKED_COMMAND_STATUS	Status of the last packed command. Bit [7:2] : Reserved Bit [1] : Indexed Error, Bit [0] : Error If any error occurs during packed command operation, the 'Error bit' (Bit 0) is set. If the error is a result of one of the individual commands inside the packed command, its index is reported in PACKED_FAILURE_INDEX [35] and 'Indexed Error' bit (bit 1) is set as well.
PACKED_FAILURE_INDEX	If the 'Indexed Error' bit (bit 1) in PACKED_COMMAND_STATUS is set, this field specifies the index in the header of the failed command.

[Table 6] Packed command structure

Entry Index	Offset (Bytes)	Name	Length (Bytes)
-	+0	VERSION	1
	+1	R/W	1
	+2	NUM_ENTRIES(=N)	1
	+3	padding to 8B	5
1	+8	CMD23_ARG_1	4
	+12	CMDxx_ARG_1	4
2	+16	CMD23_ARG_2	4
	+20	CMDxx_ARG_2	4
3	+24	CMD23_ARG_3	4
	+28	CMDxx_ARG_3	4

N	+8N	CMD23_ARG_	4
	+8N+4	CMDxx_ARG_1	4
-	+8N+8	Radding	till block ends

4.2 Cache

Cache is a temporary storage in an eMMC device. The cache reduces read and write access time compared to directly access to Non-volatile storage so that performance of the device is improved. The cache is not directly accessible by host. Moreover, there is no maximum timeout for flushing the cached data to the main Non-volatile storage. In order to stop the flush operation, the host should issue High Priority Interrupt(HPI) function. In this case, the cache will not be considered as completely flushed. So, the host should re-initiate to finish the flush operation.

[Description of Cache]

• Caching of data is only valid under the commands as follows :

1) Single block read/write (CMD17/CMD24)
2) Pre-defined multiple block read/write (CMD23 + CMD18/CMD25)
3) Open-ended multiple block read/write (CMD18/CMD25 + CMD12)

• Data in the cache may be lost when sudden power off occurs. If there was the flush operation which was ongoing when power was lost, the data may be lost as well.

• Cached data also may be lost in SLEEP state, host should finish the flush operation before the device enters to the sleep state.

• The device shall clear the data in case of RST_n or CMD0 is received.

• Cache write mode can be operated out of order compared to Packed command which is only operated in order.

[Table 7] Command description related to Cache

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD6	ac	[31:26] Set to 0 [25:24] Access [23:16] Index [15:8] Value [7:3] Set to 0 [2:0] CMD set	R1b	SWITCH	Switches the mode of operation of the selected Device or modifies the EXT_CSD registers.

[Table 8] EXT_CSD value for Cache

Name	Field	Size (Bytes)	Cell Type	CSD-Slice	Value
Cache Size	CACHE_SIZE	4	R	[252:249]	0x10000
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x00
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00

[Table 9] Definition of EXT_CSD value for Cache

Field	Definition
CACHE_SIZE	Size of Cache in the eMMC device. 0x00 : No cache existence in the device Higher than 0x00 : There is cache existing and size of it. Size of the Cache : CACHE_SIZE x 1Kb
CACHE_CTRL	Cache can be turned ON/OFF by writing the CACHE_EN bit. Bit [7:1] : Reserved, Bit [0] : CACHE_EN (0x0 : Cache is OFF, 0x1 : Cache is ON)
FLUSH_CACHE	Data in cache shall be flushed to Non-Volatile storage by setting the FLUSH bit. Bit [7:1] : Reserved, Bit [0] : FLUSH (0x0 : Reset value, 0x1 : Triggers the flush)

4.3 Discard

Discard allows the device to know data which is no longer required. So, the device can erase the data during background operation when it's necessary. Discard is similar operation to TRIM. For the TRIM function that is not aligned to optimal trim size, redundant programs are needed. Difference between TRIM and Discard is that the contents of write block where the discard command is issued shall be 'don't care.' After discard operation, the original data may be remained partially or fully depending on device. The device will decide the data of discarded address range for performance.

[Discard command sequence]

• In case of a discard operation, both CMD35 and CMD36 is used to identify the addresses of write blocks rather than erase groups.
1) Define the start address of the range using the ERASE_GROUP_START (CMD35)
2) Define the last address of the range using the ERASE_GROUP_END (CMD36)
3) Start the erase process by issuing ERASE (CMD38) command with argument bit0 and bit1 set to '1' and the remainder of the arguments set to '0'.

[Table 10] Discard Time

Timing Factor	Value
Discard[1)]	< 15ms

NOTE :
1) TRIM_MULT which is related to Discard timeout is 0x02 in Extended CSD register, but, actual Discard operation can be completed within 15ms

[Table 11] Command description related to Discard

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Descrlptlon
CMD35	ac	[31:0] data address1,2	R1	ERASE_GROUP_START	Sets the address of the 1st erase group within a range to be selected for erase
CMD36	ac	[31:0] data address1,2	R1	ERASE_GROUP_END	Sets the address of the last Erase group within a continuous range to be selected for erase
CMD38	ac	[31] obsolete set to 0 [30:16] set to 0 [15] obsolete set to 0 [14:2] set to 0 [1] Trimmed data definition [0] Identify Write block for Erase	R1b	ERASE	Erase all previously selected write blocks according to argument bits. To maintain backward compatibility, the device must not report an error if bits 31 and 15 are set. The device behavior when these are set is undefined .

[Table 12] Erase Command valid arguments

Arguments	Command Description	SEC_GB_CL_EN (EXT_CSD[231] bit 4)	SEC_ER_EN (EXT_CSD[231] bit 0)
0x00000003	Discard : the write blocks identified by CMD35 & 36. The controller can perform partial or full the actual erase at a convenient time.	n/a	n/a

[Table 13] EXT_CSD value for Discard

Name	Field	Size (Bytes)	Cell Type	CSD-Sllce	Value
TRIM Multiplier	TRIM_MULT	1	R	[232]	0x02

[Table 14] Definition of EXT_CSD value for Discard

Field	Definition
TRIM_MULT	This register is used to calculate the Discard function timeout. Discard Timeout = 300ms x TRIM_MULT

4.4 Sanitize

Sanitize is a feature which is used to remove data from the device. Once Sanitize operation is executed, the device physically removes the data from the unmapped user address space. There is no timeout related to the sanitize operation. While the device is performing the sanitize operation, the busy line is asserted. Until one of the following events occurs, the device will continue the sanitize operation with busy line asserted.
After the sanitize operation is completed, no data should exist in the unmapped address range of the device.

1) Sanitize operation is finished
2) HPI (High Priority Interrupt) is used to abort Sanitize
3) Power failure
4) H/W reset

If the sanitize operation is interrupted by HPI, Power failure and H/W reset, the state of the unmapped address range can not be guaranteed. In order to restart the sanitize operation, host must re-initiate by writing to the SANITIZE_START [165].

[Sanitize command sequence]

• Sanitize operation is initiated by writing a value to the EXT_CSD register SANITIZE_START [165] by using switch command (CMD6)

[Table 15] Command description related to Sanitize

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD6	ac	[31:26] Set to 0 [25:24] Access [23:16] Index [15:8] Value [7:3] Set to 0 [2:0] CMD set	R1b	SWITCH	Switches the mode of operation of the selected Device or modifies the EXT_CSD registers.

[Table 16] EXT_CSD value for Sanitize

Name	Field	Size (Bytes)	Cell Type	CSD-Slice	Value
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00

[Table 17] Definition of EXT_CSD value for Sanitize

Field	Definition
SANITIZE_START	Writing any value to this field shall manually start a Sanitize operation. Device shall busy till no more background operations are needed.

4.5 Power Off Notification

Device has no idea when host powers off. Power Off Notification allows the host to notify the device before the host powers off. This enables the device to better prepare itself for being powered off. This feature can be used by the host to write meta data in advance that can reduce initialization time in the next power up sequence.

[Power Off Notification sequence]

- If the power off notification is supported by host, the host shall first set POWER_OFF_NOTIFICATION byte in EXT_CSD [34] to POWERED_ON (0x01)
- Before powering the device down, the host will change the value to either POWER_OFF_SHORT (0x02) or POWER_OFF_LONG (0x03)

[Power Off Notification Mode]

- The difference between two types of Power Off modes is that how quickly host wants to turn power off.
  1) Power Off Long (0x03) : The device should respond to POWER_OFF_LONG_TIME timeout if more time for power off is acceptable.
  2) Power Off Short (0x02) : The device should respond to POWER_OFF_SHORT under the Generic CMD6 timeout.

[Table 18] Command description related to Power Off Notification

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD6	ac	[25:24] Access [23:16] Index [15:8] Value [7:3] Set to 0 [2:0] CMD set	R1b	SWITCH	Switches the mode of operation of the selected Device or modifies the EXT_CSD registers.

[Table 19] EXT_CSD value for Power Off Notification

Name	Field	Size (Bytes)	Cell Type	CSD-Slice	Value
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x0A
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x3C
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00

[Table 20] Definition of EXT_CSD value for Power Off Notification

Field	Definition
GENERIC_CMD6_TIME (Power off short)	The default max. timeout for a SWITCH command (CMD6) Generic CMD6 timeout = 10ms x GENERIC_CMD6_TIME
POWER_OFF_LONG_TIME	Max. timeout for the SWITCH command (CMD6) when notifying the device that the power is about to be turned off. Power off long timeout = 10ms x POWER_OFF_LONG_TIME
POWER_OFF_NOTIFICATION	This field allows host to notify the device when the host powers off. Any other values which don't exist in the [Table 3] are invalid. If the host sets invalid values, the device will result in SWITCH_ERROR.

[Table 21] Valid POWER_OFF_NOTIFICATION values

Value	Name	Description
0x00	NO_POWER_NOTIFICATION	Power off notification is not supported by host, device shall not assume any notification.
0x01	POWERED_ON	Host shall notify before powering off the device, and keep power supplies alive and active until then.
0x02	POWER_OFF_SHORT	Host is going to power off the device. The device shall respond within GENERIC_CMD6_TIME.
0x03	POWER_OFF_LONG.	Host is going to power off the device. The device shall respond within POWER_OFF_LONG_TIME

5.0 e.MMC 4.41 features

5.1 Data Write

Host can configure reliability mode to protect existing data per each partition.

This reliability mode has to be set before partitioning is completed.

This reliability setting only impacts the reliability of the main user area and the general purpose partitions.

[Table 22] EXT_CSD value for reliability setting in write operation

Name	Field	Size (Bytes)	Cell Type	EXT_CSD-slice	Value
Data Reliability Configuration	WR_REL_SET	1	R/W	[167]	0x1F
Data Reliability Supports	WR_REL_PARAM	1	R	[166]	0x05

Explanation of each field in the upper table is mentioned below

[Table 23] Definition of EXT_CSD value for reliability setting

Fields	Definitions
HS_CTRL_REL	0x0: All the WR_DATA_REL parameters in the WR_REL_SET registers are read only bits. 0x1: All the WR_DATA_REL parameters in the WR_REL_SET registers are R/W.
EN_REL_WR	0x0: The device supports the previous definition of reliable write. 0x1: The device supports the enhanced definition of reliable write

The below table shows each field for WE_REL_SET

[Table 24] Description of each field for WE_REL_SET

Name	Field	Bit	Size	Type
Write Data Reliability (user Area)	WR_DATA_REL_USR	0	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 1	WR_DATA_REL_1	1	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 2	WR_DATA_REL_2	2	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 3	WR_DATA_REL_3	3	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 4	WR_DATA_REL_4	4	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Reserved	-	7:5	-	-

5.2 Reliable Write

[Table 25] EXT_CSD value for reliable write

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Data Reliability Supports	WR_REL_PARAM	1	R	[166]	0x05

Reliable write with EN_REL_WR is 0x1 supports atomicity of sector unit.

The block size defined by SET_BLOCKLEN (CMD16) is ignored and reliable write is executed as only 512 byte length. There is no limit on the size of the reliable write.

[Table 26] EXT_CSD value for reliable write

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Reliable Write Sector Count	REL_WR_SEC_C	1	R	[222]	0x01

5.3 Secure Trim

Even though Secure Trim is obsolete function for eMMC4.5, it is implemented to maintain backward compatibility on customer's request.

Secure Trim operation consists of Secure Trim Step1 and Secure Trim Step2.
In Secure Trim Step 1 the host defines the range of write blocks that it would like to mark for the secure purge.

Area marked by Secure Trim Step1 is shown as EXT_CSD[181](ERASED_MEM_CONT) before Secure Trim Step2 is completed.

When Secure Trim Step2 is issued, if there is no data marked by Secure Trim Step1, Secure Trim Step2 does not work.

5.4 High Priority Interrupt

High Priority Interrupt is to stop ongoing operation and perform read operation with high priority

Command set for High Priority Interrupt operation is the below

[Table 27] Command List for High Priority Interrupt

CMD Index	Type	Argument	Resp	Abbreviation	Command Description
CMD13	ac	[31:16] – RCA [15:1] – stuff bits [0] – High Priority Interrupt	R1	SEND_STATUS	If High Priority Interrupt flag is set the device shall interrupt its internal operations in a well defined timing

Interruptible commands by read while write operation are the below.

[Table 28] List of Interruptible Command

Command Index	Name	Is interruptible?
CMD24	WRITE_BLOCK	Yes
CMD25	WRITE_MULTIPLE_BLOCK	Yes
CMD38	ERASE	Yes
CMD6	SWITCH, byte BKOPS_START, any value	Yes
	SWITCH, byte SANITIZE_START, any value	Yes
	SWITCH, byte POWER_OFF_NOTIFICATION, value POWER_OFF_LONG	Yes
	SWITCH, byte POWER_OFF_NOTIFICATION, other values	No
	CACHE_CTRL when used for turning the cache OFF	Yes
	FLUSH_CACHE	Yes
	SWITCH, other bytes, any value	No
All others		No

[Table 29] EXT_CSD value for HPI

Name	Field	Size(Bytes)	Cell Type	CSD-Slice	Value
HPI features	HPI_FEATURES	1	R	[503]	0x01
Number of correctiy programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x01
Out of interrupt busytiming	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x02
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00

[Table 30] Definition of EXT_CSD value for HPI

Fields	Definitions
HPI_FEATURES	Bit 0 means HPI_SUPPORT Bit 0 = 0x0 : High Priority Interrupt mechanism not supported Bit 0 = 0x1 : High Priority Interrupt mechanism supported Bit 1 means HPI_IMPLEMENTATION 0x0 : HPI mechanism implementation based on CMD13 0x1 : HPI mechanism implementation based on CMD12
CORRECTLY_PRG_SECTOR_NUM	This field indicates how many 512B sectors were successfully programmed by the last WRITE_MULTIPLE_BLOCK command (CMD25). CORRECTLY_PRG_SECTORS_NUM=EXT_CSD[242]*2^0+EXT_CSD[243]*2^8 +EXT_CSD[244]*2^16 + EXT_CSD[245]*2^24
PARTITION_SWITCH_TIME	This field indicates the maximum timeout for the SWITCH command (CMD6) when switching partitions by changing PARTITION_ACCESS bits in PARTITION_CONFIG field (EXT_CSD byte [179]). Time is expressed in units of 10 milliseconds
OUT_OF_INTERRUPT_TIME	This field indicates the maximum timeout to close a command interrupted by HPI - time between the end bit of CMD12 / CMD 13 to the DAT0 release by the device.
HPI_MGMT	Bit 0 means HPI_EN 0x0 : HPI mechanism not activated by the host 0x1 : HPI mechanism activated by the host

5.5 Background Operation

When the host is not being serviced, e·MMC can do internal operation by using “Background Operation” command. In this operation which takes long time to complete can be handled later when host ensure enough idle time (In Back ground operation)

Background Operation Sequence is the following

[Table 31] Background Operation Sequence

Function	Command	Description
Background Operation Check	CMD8 Or Card Status Register	If BKOPS_STATUS is not 0 or 6th bit of card status register is set, there are something to be performed by background operation
Background Operation Start	CMD6	Background operation starts by BKOPS_START is set to any value. When background operation is completed BKOPS_STATUS is set to 0 and BKOPS_START is set to 0.
Background Operation Stop	HPI	If the background operation is stopped BKOPS_START is set to 0

[Table 32] EXT_CSD value for Background Operation

Name	Field	Size(Bytes)	Cell Type	CSD-Slice	Value
Background operations Support	BKOPS_SUPPORT	1	R	[502]	0x01
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations hand shake	BKOP_EN	1	R/W	[163]	0x00

[Table 33] Definition of EXT_CSD value for Bakgrourd Operation

Fields	Definitions
BKOPS_SUPPORT	‘0’ means Background operation is not supported ‘1’ means Background operation is supported
BKOPS_ STATUS	‘0’ means No background work pending ‘1’ means pending background work existing. ‘2’ means pending background work existing & performance being impacted. ‘3’ means pending background work existing & critical
BKOPS_START	Background operation start while BKOPS_START is set to any value. ‘0’ means Background operation is enabled.
BKOPS_EN	‘0’ means host does not support background operation ‘1’ means host use background operation manually

[Table 34] Card Status Register for Background Operation

Bits	Identifier	Type	Det Mode	Value	Description	Clear Cond
6	EXCEPTION_EVENT	S	R	“0” = no event “1” = an exception event has occurred	If set, one of the exception bits in field EXCEPTION_EVENTS_STATUS was set to indicate some exception has occurred. Host should check that field to discover which exception has occurred to understand what further actions are needed in order to clear this bit	A

6.0 Technical Notes

6.1 S/W Agorithm

6.1.1 Partition Management

The device initially consists of two Boot Partitions and RPMB Partition and User Data Area.

The User Data Area can be divided into four General Purpose Area Partitions and User Data Area partition. Each of the General Purpose Area partitions and a section of User Data Area partition can be configured as enhanced partition.

6.1.1.1 Boot Area Partition and RPMB Area Partition

Default size of each Boot Area Partition is 2,048KB and can be changed by Vendor Command as multiple of 512KB.
Default size of RPMB Area Partition is 128 KB and can be changed by Vendor Command as multiple of 128KB.

Boot Partition size & RPMB Partition Size are set by the following command sequence :

[Table 35] Setting sequence of Boot Area Partition size and RPMB Area Partition size

Function	Command	Description
Partition Size Change Mode	CMD62(0xEFAC62EC)	Enter the Partition Size Change Mode
Partition Size Set Mode	CMD62(0x00CBAEA7)	Partition Size setting mode
Set Boot Partition Size	CMD62(BOOT_SIZE_MULTI)	Boot Partition Size value
Set RPMB Partition Size	CMD62(RPMB_SIZE_MULTI)	RPMB Partition Size value F/W Re-Partition is executed in this step.
Power Cycle		

Boot partition size is calculated as (128KB * BOOT_SIZE_MULTI)
The size of Boot Area Partition 1 and 2 can not be set independently. It is set as same value.

RPMB partition size is calculated as (128KB * RPMB_SIZE_MULTI).
In RPMB partition, CMD 0, 6, 8, 12, 13, 15, 18, 23, 25 are admitted.

Access Size of RPMB partition is defined as the below:

[Table 36] REL_WR_SEC_C value for write operation on RPMB partition

REL_WR_SEC_C	Description
REL_WR_SEC_C = 1	Access sizes 256B and 512B supported to RPMB partition
REL_WR_SEC_C > 1	Access sizes up to REL_WR_SEC_C * 512B supported to RPMB partition with 256B granularity

Any undefined set of parameters or sequence of commands results in failure access.

If the failure is in data programming case, the data is not programmed. And if the failure occurs in data read case, the read data is ‘0x00’.

6.1.1.2 Enhanced Partition (Area)

SAMSUNG e·MMC adopts Enhanced User Data Area as SLC Mode. Therefore when master adopts some portion as enhanced user data area in User Data Area, that area occupies double size of original set up size. (ex> if master set 1MB for enhanced mode, total 2MB user data area is needed to generate 1MB enhanced area)

Max Enhanced User Data Area size is defined as (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512kBytes)

6.1.2 Write protect management

In order to allow the host to protect data against erase or write, the device shall support write protect commands.

[Table 37] Write Protection Hierarchy (when disable bits are clear)

Current Protection mode	CSD[12]	Action	Resulting Protection mode
Permanent	N/A	Power failure of hardware reset	Permanent
Permanent	N/A	SET_WRITE_PROT (US_PERM_WP_EN = 0)	Permanent
Power-ON	1	Power failure or hardware reset	Temporary
Power-ON	0	Power failure or hardware reset	None
Power-ON	N/A	SET_WRITE_PROT (US_PERM_WP_EN = 1)	Permanent
Power-ON	N/A	SET_WRITE_PROT (US_PERM_WP_EN =0 and US_PWR_WP_EN = 0)	Power-ON
Temporary	1	Power failure or hardware reset	Temporary
Temporary	1	SET_WRITE_PROT (US_PERM_WP_EN = 1)	Permanent
Temporary	1	SET_WRITE_PROT (US_PERM_WP_EN = 0 and US_PWR_WP_EN = 1)	Power-ON

6.1.2.1 User Area Write Protection

TMP_WRITE_PROTECT (CSD[12]) and PERM_WRITE_PROTECT(CSD[13]) registers allow the host to apply write protection to whole device including Boot Partition, RPMB Partition and User Area.

[Table 38] Whole device write protect priority

Class	Setting
Permanent write protect	SET : One time programmable
	CLR : Not available
Temporary write protect	SET : Multiple programmable
	CLR : Multiple programmable

USER_WP (EXT_CSD[171]) register allows the host to apply write protection to all the partitions in the user area.

[Table 39] User area write protect priority

Class	Setting
Permanent write protect	SET : One time programmable
	CLR : Not available
Power-on write protect	SET : One time programmable on power-on
	CLR : After power reset
Temporary write protect	SET : Multiple programmable
	CLR : Multiple programmable

[Table 40] Write Protection Types (when disable bits are clear)

US_PERM_WP_EN	US_PWR_WP_EN	Type of protection set by SET_WRITE_PROT command
0	0	Temporary
0	1	Power-ON
1	0	Permanent
1	1	Permanent

Issuing CMD28 when both US_PERM_WP_EN and US_PWR_WP_EN, will result in the write protection group being permanently protected.

[Table 41] User area write protection

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PERM_PSWD_DIS	CD_PERM_WP_DIS	Reserved	US_PERM_WP_DIS	US_PWR_WP_DIS	US_PERM_WP_EN	Reserved	US_PWR_WP_EN
R//W	R/W		R/W	R/W/C_P	R/W/E_P		R/W/E_P

* For more detailed information, please refer to Page159 of JEDEC Standard No. 84-B45

6.1.2.2 Boot Partition Write Protection

BOOT_WP (EXT_CSD [173]) register allows the host to apply write protection to Boot Area Partitions.

[Table 42] Boot area write protect priority

Class	Setting
Permanent write protect	SET : One time programmable
	CLR : Not available
Power-on write protect	SET : One time programmable on power-on
	CLR : After power reset

An attempt to set both the disable and enable bit for a given protection mode (permanent or power-on) in a single switch command will have no impact. If both permanent (B_PERM_WP_EN) and power on (B_PWR_WP_EN) protection are applied to the same sector(s), permanent protection will take precedence and the sector(s) will be permanently protected.

[Table 43] BOOT area write protection

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B_SEC_WP_SEL	B_PWR_WP_DIS	Reserved	B_PERM_WP_DIS	B_PERM_WP_SEC_SEL	B_PERM_WP_EN	B_PWR_WP_SEC_SEL	B_PWR_WP_EN
R/W/C_P	R/W/C_P		R/W	R/W/C_P	R/W	R/W/C_P	R/W/E_P

* For more detailed information, please refer to Page158 of JEDEC Standard No. 84-B45

6.1.3 Boot operation

Device supports not only boot mode but also alternative boot mode. Device supports high speed timing and dual data rate during boot.

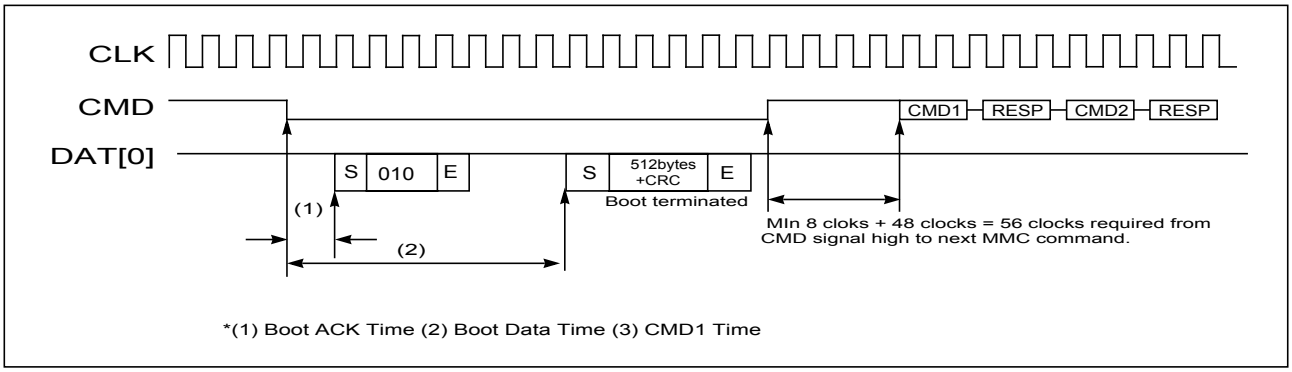


Figure 6. MultiMediaCard state diagram (boot mode)

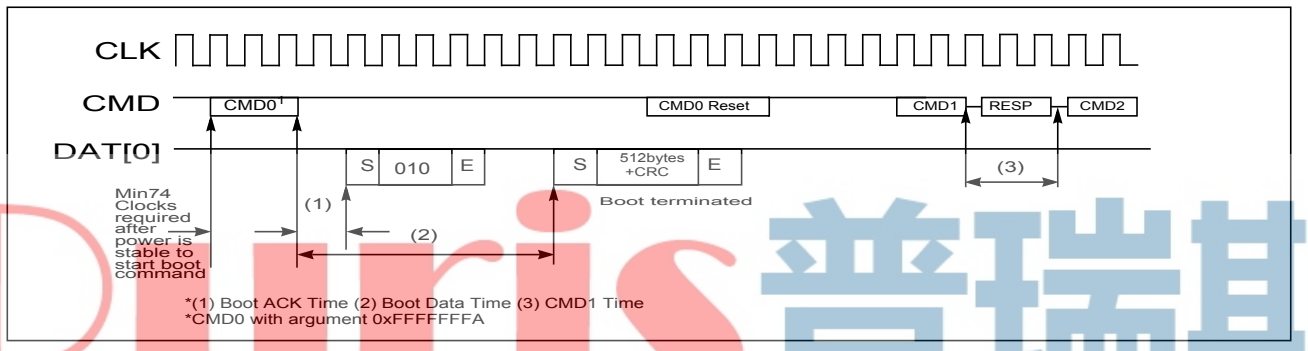


Figure 7. MultiMediaCard state diagram (alternative boot mode)

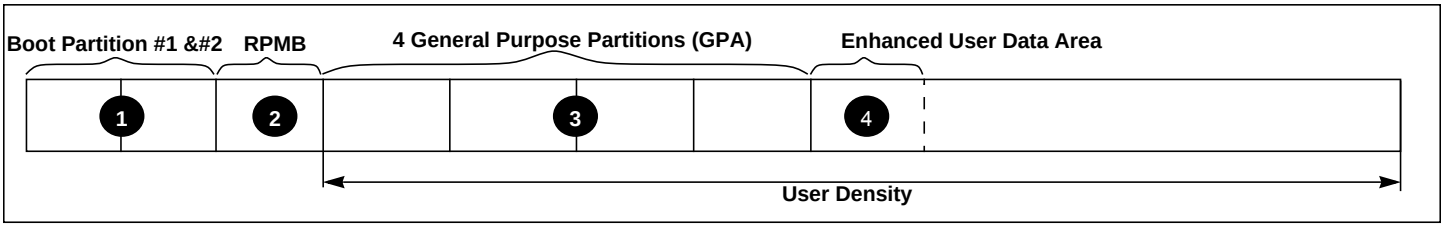
[Table 44] Boot ack, boot data and initialization Time

Timing Factor	Value
(1) Boot ACK Time	< 50 ms
(2) Boot Data Time	< 60 ms
(3) Initialization Time[1)]	< 3 secs

NOTE:
1) This initialization time includes partition setting, Please refer to INI_TIMEOUT_AP in 7.4 Extended CSD Register.
Normal initialization time (without partition setting) is completed within 1sec

6.1.4 User Density

Total User Density depends on device type.
For example, 32MB in the SLC Mode requires 64MB in MLC.
This results in decreasing of user density



[Table 45] Capacity according to partition

	Boot partition 1	Boot partition 2	RPMB
Min.	2,048KB	2,048KB	128KB
Max.	16,384KB	16,384KB	4,096KB

[Table 46] Maximum Enhanced Partition Size

Device	Max. Enhanced Partition Size
16 GB	7,801,405,440 Bytes
32 GB	15,602,810,880 Bytes
64 GB	31,247,564,800 Bytes

[Table 47] User Density Size

Device	User Density Size
16 GB	15,634,268,160 Bytes
32 GB	31,268,536,320 Bytes
64 GB	62,537,072,640 Bytes

6.1.5 Auto Power Saving Mode

If host does not issue any command during a certain duration (1ms), after previously issued command is completed, the device enters "Power Saving mode" to reduce power consumption.

At this time, commands arriving at the device while it is in power saving mode will be serviced in normal fashion

[Table 48] Auto Power Saving Mode enter and exit

Mode	Enter Condition	Escape Condition
Auto Power Saving Mode	When previous operation which came from Host is completed and no command is issued during a certain time.	If Host issues any command

[Table 49] Auto Power Saving Mode and Sleep Mode

	Auto Power Saving Mode	Sleep Mode
NAND Power	ON	OFF
GotoSleep Time	< 1ms	< 1ms

6.1.6 Performance

[Table 50] Performance

Density	Sequential Read (MB/s)	Sequential Write (MB/s)
16 GB	75	43
32 GB		
64 GB		

* Test Condition : Bus width x8, 50MHz DDR, 4MB data transfer, w/o file system overhead, measured on Samsung's internal board

7.0 REGISTER VALUE

7.1 OCR Register

The 32-bit operation conditions register stores the VDD voltage profile of the e·MMC. In addition, this register includes a status information bit. This status bit is set if the e·MMC power up procedure has been finished. The OCR register shall be implemented by all e·MMCs.

[Table 51] OCR Register

OCR bit	VDD voltage window[2]	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 - 1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode) -[*Higher than 2GB only]
[31]	e·MMC power up status bit (busy)[1]	

NOTE :
1) This bit is set to LOW if the e·MMC has not finished the power up routine
2) The voltage for internal flash memory(VDDF) should be 2.7-3.6v regardless of OCR Register value.

7.2 CID Register

[Table 52] CID Register

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0x15
Reserved		6	[119:114]	---
Card/BGA	CBX	2	[113:112]	01
OEM/Application ID	OID	8	[111:104]	___1
Product name	PNM	48	[103:56]	See Product name table
Product revision	PRV	8	[55:48]	___2
Product serial number	PSN	32	[47:16]	___3
Manufacturing date	MDT	8	[15:8]	___4
CRC7 checksum	CRC	7	[7:1]	___5
not used, always '1'	-	1	[0:0]	---

NOTE :
1),4),5) description are same as e.MMC JEDEC standard
2) PRV is composed of the revision count of controller and the revision count of F/W patch
3) A 32 bits unsigned binary integer. (Random Number)

7.2.1 Product name table (In CID Register)

[Table 53] Product name table

Part Number	Density	Product Name in CID Register (PNM)
KLMAG4FE4B-B001	16 GB	0 x 4D4147344642
KLMBG8FE4B-B001	32 GB	0 x 4D4247384642
KLMCGAFE4B-B001	64 GB	0 x 4D4347414642

7.3 CSD Register

The Card-Specific Data register provides information on how to access the e·MMC contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows:
R : Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E : Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple wtitable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

[Table 54] CSD Register

Name	Field	Width	Cell Type	CSD-slice	CSD Value		
					16GB	32GB	64GB
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x03		
System specification version	SPEC_VERS	4	R	[125:122]	0x04		
Reserved	-	2	R	[121:120]	-		
Data read access-time 1	TAAC	8	R	[119:112]	0x27		
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x01		
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32		
Device command classes	CCC	12	R	[95:84]	0xF5		
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x09		
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00		
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00		
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00		
DSR implemented	DSR_IMP	1	R	[76:76]	0x00		
Reserved	-	2	R	[75:74]	-		
Device size	C_SIZE	12	R	[73:62]	0xFFF		
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x06		
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x06		
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x06		
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x06		
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07		
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F		
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F		
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x1F		
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01		
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0x00		
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x03		
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09		
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00		
Reserved	-	4	R	[20:17]	-		
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x00		
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x00		
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x01		
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00		
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00		
File format	FILE_FORMAT	2	R/W	[11:10]	0x00		
ECC code	ECC	2	R/W/E	[9:8]	0x00		
CRC	CRC	7	R/W/E	[7:1]	0x01		
Not used, always'1'	-	1	—	[0:0]	-		

7.4 Extended CSD Register

The Extended CSD register defines the e·MMC properties and selected modes. It is 512 bytes long.
The most significant 320 bytes are the Properties segment, which defines the e·MMC capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the e·MMC is working in. These modes can be changed by the host by means of the SWITCH command.

R : Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E : Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple wtitable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable

[Table 55] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD-slice	CSD Value		
					16GB	32GB	64GB
Properties Segment							
Reserved[1]		7	-	[511:505]	-		
Supported Command Sets	S_CMD_SET	1	R	[504]	0x01		
HPI features	HPI_FEATURES	1	R	[503]	0x01		
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01		
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F		
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F		
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	0x01		
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0x04		
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0x00		
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x05		
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x07		
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x03		
Reserved[1]		255	-	[493:253]	-		
Cache size	CACHE_SIZE	4	R	[252:249]	0x10000		
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x0A		
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x3C		
Background operations status	BKOPS_STATUS	1	R	[246]	0x00		
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00		
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E		
Reserved[1]		1	-	[240]	-		
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00		
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x00		
Power class for 200MHz at 3.6V	PWR_CL_200_360	1	R	[237]	0x00		
Power class for 200MHz, at 1.95V	PWR_CL_200_195	1	R	[236]	0x00		
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00		
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00		
Reserved[1]		1	-	[233]	-		
TRIM Multiplier	TRIM_MULT	1	R	[232]	0x02		
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55		
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x1B		

Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x11		
Boot information	BOOT_INFO	1	R	[228]	0x07		
Reserved[1]		1	-	[227]	-		
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	0x10		
Access size	ACC_SIZE	1	R	[225]	0x07		
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x01		
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x01		
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01		
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x50		
Sleep current (VCC)	S_C_VCC	1	R	[220]	0x07		
Sleep current (VCCQ)	S_C_VCCQ	1	R	[219]	0x07		
Reserved[1]		1	-	[218]	-		
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x11		
Reserved[1]		1	-	[216]	-		
Sector Count	SEC_COUNT	4	R	[215:212]	0x1D1F000	0x3A3E000	0x747C000
Reserved[1]		1	-	[211]	-		
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0x00		
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0x00		
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00		
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00		
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0x00		
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0x00		
Reserved[1]		1	-	[204]	-		
Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x00		
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x00		
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x00		
Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x00		
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x01		
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x02		
I/O Driver Strength CSD structure version	DRIVER_STRENGTH	1	R	[197]	0x00		
Device type	DEVICE_TYPE	1	R	[196]	0x07		
Reserved[1]		1	-	[195]	-		
CSD structure version	CSD_STRUCTURE	1	R	[194]	0x02		
Reserved[1]		1	-	[193]	-		
Extended CSD revision	EXT_CSD_REV	1	R	[192]	0x05	0x06	
Modes Segment							
Command set	CMD_SET	1	R/W/E_P	[191]	0x00		
Reserved[1]		1	-	[190]	-		
Command set revision	CMD_SET_REV	1	R	[189]	0x00		
Reserved[1]		1	-	[188]	-		
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x00		
Reserved[1]		1	-	[186]	-		
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x00		

Reserved[1]		1	-	[184]	-		
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x00		
Reserved[1]		1	-	[182]	-		
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x00		
Reserved[1]		1	-	[180]	-		
Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	[179]	0x00		
Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	[178]	0x00		
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x00		
Reserved[1]		1	-	[176]	-		
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00		
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x00		
Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0x00		
Reserved[1]		1	-	[172]	-		
User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	[171]	0x00		
Reserved[1]		1	-	[170]	-		
FW configuration	FW_CONFIG	1	R/W	[169]	0x00		
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x01		
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F		
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x05		
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00		
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00		
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0x00		
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00		
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00		
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	0x07		
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0xBA	0x174	0x2E9
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00		
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	0x00		
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x00		
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00		
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x00		
Reserved[1]		1	-	[135]	-		
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00		
Reserved[1]		1	-	[133]	-		
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00		
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00		
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0x01		
Reserved[1]		2	-	[129:128]	-		
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	<vendor specific>	[127:64]			
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x00		
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00		
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00		

1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0x00
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x00
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x00
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x00
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00
Reserved[1]		32	-	[31:0]	-

NOTE :
1) Reserved bits should read as “0.”

8.0 AC PARAMETER

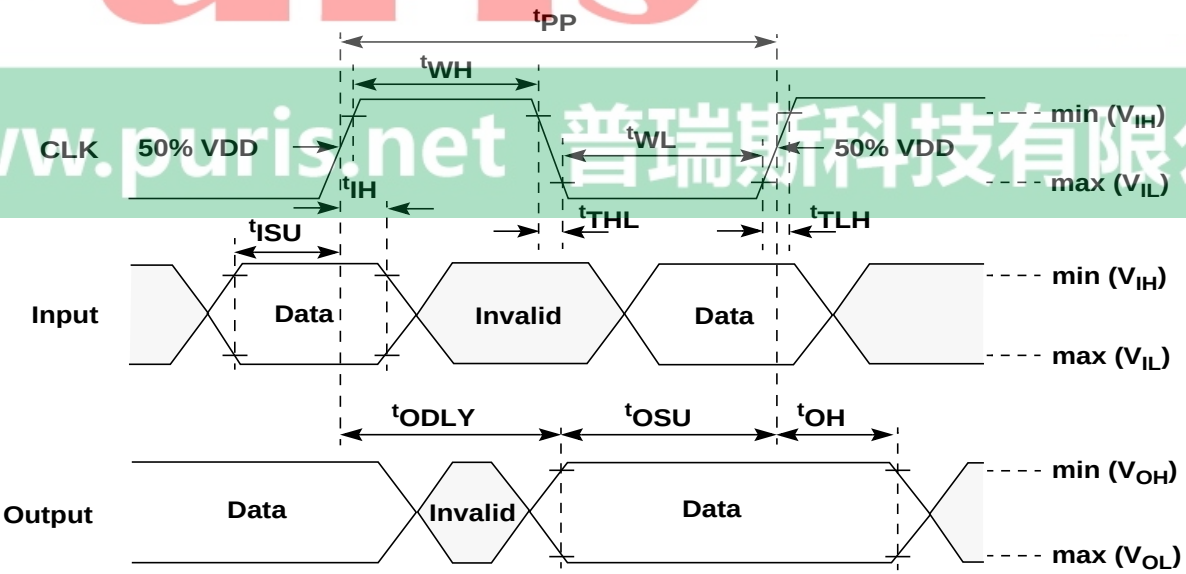
8.1 Time Parameter

[Table 56] Time Parameter

Timing Paramter		Max. Value	Unit
Initialization Time (tINIT)	Normal 1)	1	s
	After partition setting 2)	3	s
Read Timeout		100	ms
Write Timeout		350	ms
Erase Timeout		15	ms
Force Erase Timeout		3	min
Secure Erase Timeout		8	s
Secure Trim step1 Timeout		5	s
Secure Trim step2 Timeout		3	s
Trim Timeout 3)		600	ms
Partition Switching Timeout (after Init)		100	us
Packed Command Timeout		350	ms
Power Off Notification (Short) Timeout		100	ms
Power Off Notification (Long) Timeout		600	ms

NOTE:
1) Normal Initialization Time without partition setting
2) Initialization Time after partition setting, refer to INI_TIMEOUT_AP in 7.4 EXT_CSD register
3) If 8KB Size and Address are aligned, Max. Timeout value is 300ms

8.2 Bus Timing Parameter



Data must always be sampled on the rising edge of the clock.

Figure 8. Bus signal levels

[Table 57] Default (under 26MHz)

Parameter	Symbol	Min	Max	Unit	Remark[1]
Clock CLK(All values are referred to min(V_{IH}) and max(V_{IL})[2]					
Clock frequency Data Transfer Mode3	fPP	0[4]	26	MHz	CL <= 30 pF Tolerance: +100KHz
Clock frequency Identification Mode	f_{OD}	0[4]	400	kHz	Tolerance: +20KHz
Clock low time	t_{WL}	10		ns	C_L <= 30 pF
Clock high time	t_{WH}	10			
Clock rise time[5]	t_{TLH}		10	ns	C_L <= 30 pF
Clock fall time	t_{THL}		10	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output hold time	t_{OH}	8.3		ns	CL <= 30 pF
Output set-up time	t_{OSU}	11.7		ns	CL <= 30 pF

NOTE :
1)The card must always start with the backward-compatible interface timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
2) CLK timing is measured at 50% of VDD.
3) For compatibility with cards that suport the v4.2 standard or earlier verison, host should not use>20MHz before switching to high-speed interface timing.
4) Frequency is periodically sampled and is not 100% tested.
5) CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL}).

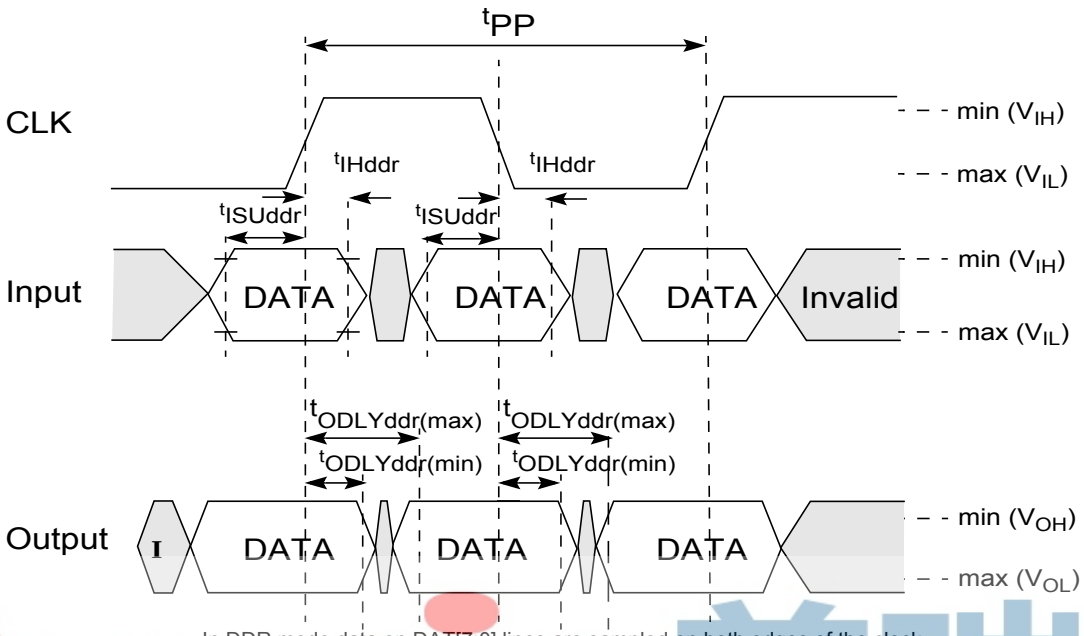
[Table 58] High-Speed Mode

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK(All values are referred to min(V_{IH}) and max(V_{IL})[1]					
Clock frequency Data Transfer Mode[2]	f_{PP}	0[3]	52[4)]	MHz	C_L <= 30 pF
Clock frequency Identification Mode	f_{OD}	0[3]	400	kHz	CL <= 30 pF
Clock low time	t_{WL}	6.5		ns	C_L <= 30 pF
Clock High time	t_{WH}	6.5		ns	C_L <= 30 pF
Clock rise time[5]	t_{TLH}		3	ns	C_L <= 30 pF
Clock fall time	t_{THL}		3	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	CL <= 30 pF
Output hold time	t_{OH}	2.5			C_L <= 30 pF
Signal rise time	t_{RISE}		3	ns	C_L <= 30 pF
Signal fall time	t_{FALL}		3	ns	C_L <= 30 pF

NOTE :
1) CLK timing is measured at 50% of VDD.
2) A MultiMediaCard shall support the full frequency range from 0-26MHz, or 0-52MHz
3) Frequency is periodically sampled and is not 100% tested.
4) Card can operate as high-speed card interface timing at 26MHz clock frequency.
5) CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL}).6) Inputs CMD, DAT rise and fall times are measured by min(V_{IH}) and max(V_{IL}), and outputs CMD, DAT rise and fall times are measured by min(V_{OH}) and max(V_{OL}).

8.3 Bus timing for DAT signals during 2x data rate operation

These timings applies to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operates synchronously of both the rising and the falling edges of CLK.The CMD signal still operates synchronously of the rising edge of CLK and there fore it complies with the bus timing specified in chapter 7.2, Therefore there is no timing change for the CMD signal



In DDR mode data on DAT[7:0] lines are sampled on both edges of the clock (not applicable for CMD line)

Figure 9. Timing diagram: data input/output in dual data rate mode

8.3.1 Dual data rate interface timings

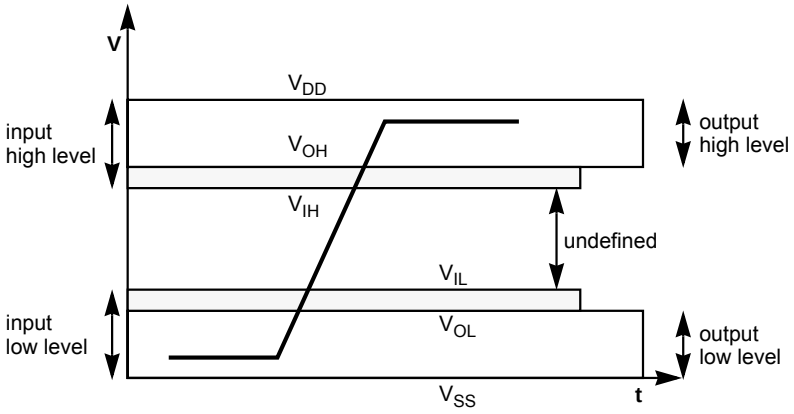
[Table 59] High-speed dual rate interface timing

Parameter	Symbol	Min	Max.	Unit	Remark[1]
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL ≤ 20 pF
Input hold time	tIHddr	2.5		ns	CL ≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL ≤ 20 pF
Signal rise time (all signals)[2]	tRISE		2	ns	CL ≤ 20 pF
Signal fall time (all signals)	tFALL		2	ns	CL ≤ 20 pF

NOTE :
1) CLK timing is measuted at 50% of VDD
2) Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max(V_{IL}), and outputs CMD,DATrise and fall times measured by min(V_{OH}) and max(V_{OL})

8.4 Bus signal levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



8.4.1 Open-drain mode bus signal level

[Table 60] Open-drain bus signal level

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{DD} - 0.2		V	I_{OH} = -100 uA
Output LOW voltage	V_{OL}		0.3	V	I_{OL} = 2 mA

The input levels are identical with the push-pull mode bus signal levels.

8.4.2 Push-pull mode bus signal level.high-voltage MultiMediaCard

To meet the requirements of the JEDEC standard JESD8C.01, the card input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range:

[Table 61] Push-pull signal level.high-voltage MultiMediaCard

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75*V_{DD}		V	I_{OH} = -100 uA@V_{DD} min
Output LOW voltage	V_{OL}		0.125*V_{DD}	V	I_{OL} = 100 uA@V_{DD} min
Input HIGH voltage	V_{IH}	0.625*V_{DD}	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25*V_{DD}	V	

8.4.3 Push-pull mode bus signal level.dual-voltage MultiMediaCard

The definition of the I/O signal levels for the Dual voltage MultiMediaCard changes as a function of V_{DD}.

- 2.7V - 3.6V: Identical to the High Voltage MultiMediaCard (refer to Chapter 8.4.2 on page38 above).
- 1.95V - 2.7V: Undefined. The card is not operating at this voltage range.
- 1.70V - 1.95V: Compatible with EIA/JEDEC Standard “EIA/JESD8-7 Normal Range” as defined in the following table.

[Table 62] Push-pull signal level—dual-voltage MultiMediaCard

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{DD} - 0.45V		V	I_{OH} = -2mA
Output LOW voltage	V_{OL}		0.45V	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65*V_{DD} 1)	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35*V_{DD} 2)	V	

NOTE:
1) 0.7*V_{DD} for MMC4.3 and older revisions.
2) 0.3*V_{DD} for MMC4.3 and older revisions.

8.4.4 Push-pull mode bus signal level.e·MMC

The definition of the I/O signal levels for the e·MMC devices changes as a function of VCCQ.

- 2.7V-3.6: Identical to the High Voltage MultiMediaCard (refer to Chapter 8.4.2 on page38).
- 1.95- 2.7V: Undefined. The e·MMCdevice is not operating at this voltage range.
- 1.65V-1.95V: Identical to the 1.8V range for the Dual Voltage MultiMediaCard (refer to Chapter 8.4.3 on page38).
- 1.3V - 1.65V: Undefined. The e·MMC device is not operating at this voltage range.
- 1.1V-1.3V: Compatible with EIA/JEDEC Standard “JESD8-12A.01 normal range: as defined in the following table.

[Table 63] Push-pull signal level.1.1V-1.3V VCCQ range e·MMC

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	$0.75V_{CCQ}$		V	I_{OH} = -2mA
Output LOW voltage	V_{OL}		$0.25V_{CCQ}$	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	$0.65*V_{CCQ}$	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	$0.35*V_{CCQ}$	V	

9.0 DC PARAMETER

9.1 Active Power Consumption during operation

[Table 64] Active Power Consumption during operation

Density	NAND Type	CTRL	NAND	Unit
16GB	32Gb MLC x 4	100	200	mA
32GB	32Gb MLC x 8			
64GB	32Gb MLC x 16			

* Power Measurement conditions: Bus configuration =x8 @52MHz
* The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

9.2 Standby Power Consumption in auto power saving mode and standby state.

[Table 65] Standby Power Consumption in auto power saving mode and standby state

Density	NAND Type	CTRL		NAND		Unit
		25°C(Typ)	85°C	25°C(Typ)	85°C	
16GB	32Gb MLC x 4	100	250	60	200	uA
32GB	32Gb MLC x 8			120	400	
64GB	32Gb MLC x 16			240	800	

NOTE:
Power Measurement conditions: Bus configuration =x8 , No CLK
*Typical value is measured at Vcc=3.3V, TA=25°C. Not 100% tested.

9.3 Sleep Power Consumption in Sleep State

[Table 66] Sleep Power Consumption in Sleep State

Density	NAND Type	CTRL		NAND	Unit
		25°C(Typ)	85°C		
16GB	32Gb MLC x 4	100	250	0[1)]	uA
32GB	32Gb MLC x 8				
64GB	32Gb MLC x 16				

NOTE:
Power Measurement conditions: Bus configuration =x8 , No CLK
1) In auto power saving mode , NAND power can not be turned off .However in sleep mode NAND power can be turned off. If NAND power is alive , NAND power is same with that of the Standby state.

9.4 Supply Voltage

[Table 67] Supply voltage

Item	Min	Max	Unit
VDD	1.70 (2.7)	1.95 (3.6)	V
VDDF	2.7	3.6	V
Vss	-0.5	0.5	V

9.5 Bus Operating Conditions

[Table 68] Bus Operating Conditions

Parameter	Min	Max	Unit
Peak voltage on all lines	-0.5	3.6	V
Input Leakage Current	-2	2	μA
Output Leakage Current	-2	2	μA

9.6 Bus Signal Line Load

The total capacitance C_L of each line of the e·MMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{movi} of the e·MMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{movi}$$

The sum of the host and bus capacitances should be under 20pF.

[Table 69] Bus SIgnal Line Load

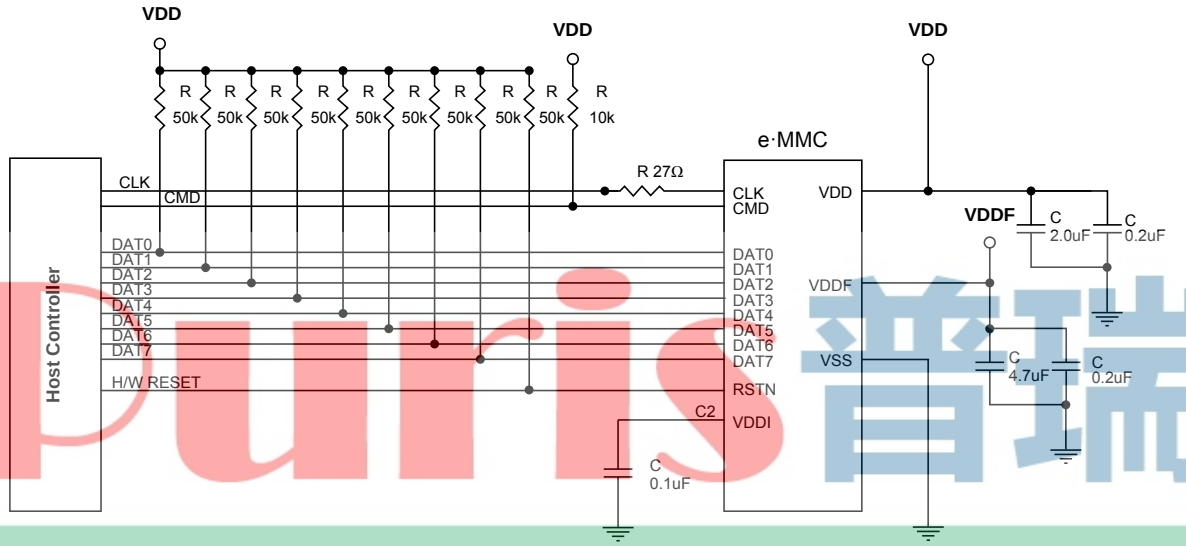
Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single e·MMC capacitance	C_{movi}		7	12	pF	
Maximum signal line inductance				16	nH	f_{PP} <= 52 MHz

A. e·MMC Connection Guide

This Connection guide is an example for customers to adopt e·MMC more easily

- This appendix is just guideline for e·MMC connection. This value and schematic can be changed depending on the system environment.
- Coupling capacitor should be connected with VDD and VSS as closely as possible.
- VDDI Capacitor is min 0.1uF
- Impedance on CLK match is needed.
- SAMSUNG recommends 27Ω for resistance on CLK line. However 0Ω ~47Ω is also available.
- If host does not have a plan to use H/W reset, it is not needed to put 50KΩ pull-up resistance on H/W rest line.
- SMASUNG Recommends to separate VDD and VDDF power.

A.1 x8 support Host connection Guide



A.2 x4 support Host connection Guide