16K x 8 Bit Mask ROM

FEATURES

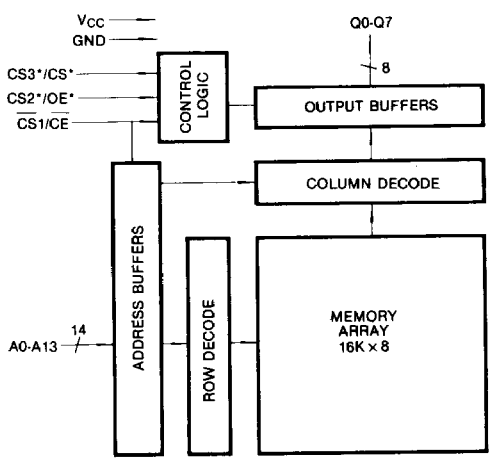
- **23128: Non-power down**
- **23128S: Automatic power down**
- **Fully static operation**
- **Silicon gate NMOS technology**
- **Maximum access time**
  23128/23128S-15: 150 ns
  23128/23128S-20: 200 ns
  23128/23128S-25: 250 ns
- **Fully TTL compatible**
- **5 volt only operation**
- **Byte-wide industry standard JEDEC pin-out**
- **Available in three temperature ranges**
  23128 (Commercial): 0°C to 70°C
  23128I (Industrial): −40°C to 85°C
  23128HR (Military): −55°C to 125°C

GENERAL DESCRIPTION

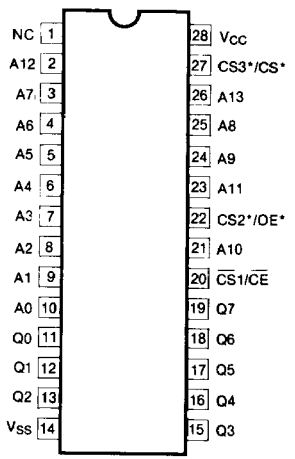
The KM23128 is a mask programmable read-only-memories with a 16K word by 8 bit organizations. Designed for ease of use, this device requires only a 5 volt supply, is TTL compatible, and because of its totally static (asynchronous) operation, requires no clock. This memory device is available in two versions. The KM23128 is non-power down version where the active level of chip selects CS2 and CS3 is programmable and is defined by the user to facilitate system memory expansion. The KM23128S offers an automatic power down feature (standby) controlled by the chip enable CE input. When CE goes high, the device automatically powers down and remains in a low power standby mode as long as CE remains high. Also, on the 23128S, the active level of chip select CS and output enable OE is programmable, thereby providing easier system implementation. The KM23128 is packaged in a 28 pin DIP with an industry standard bytewide JEDEC pin-out. Optionally, this device is available in a space saving 28 pin surface mounted plastic leaded chip carrier.

5

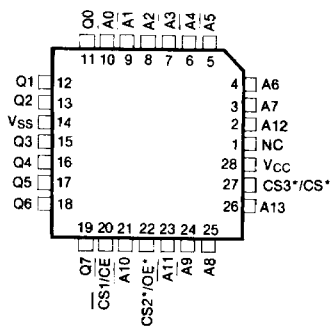
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



*Programmable Active High or Low



Pin Name	Pin Function
A_0-A_{13}	Address Inputs
Q_0-Q_7	Data Outputs
$\overline{CS}1$, CS2 CS3, CS	Chip Selects
NC	No Connection
$\overline{CE}$	Chip Enable
OE	Output Enable
V_{CC}	5V ± 10% Power Supply
V_{SS}	Ground

Note: 23128 Only: Chip Selects $\overline{CS}1$, CS2 and CS3 are normally AND'd, ie, ($\overline{CS}1 \cdot CS2 \cdot CS3$). At the option of the user, $\overline{CS}1$ and CS2 may be internally OR'd and then AND'd with CS3 ie, [($\overline{CS}1 + CS2) \cdot CS3$]

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Voltage on Any Pin with Respect to Ground	V_{CC}	−0.5 to +7V	V
Storage Temperature	T_{stg}	−65 to +150	°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	KM23128			KM23128I			KM23128HR			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage*	V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	Volts
Input High Level Voltage	V_{IH}	2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	Volts
Input Low Level Voltage	V_{IL}	−0.5		0.8	−0.5		0.8	−0.5		0.8	Volts
Operating Ambient Temperature	T_A	0		70	−40		85	−55		125	°C

*V_{CC} must be applied at least 100μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{CC} max			10	μA
Output Leakage Current	I_O	V_O = 0.2 to V_{CC} max Chip Deselected			± 10	μA
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			Volts
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA			0.4	Volts
Supply Current-Active	I_{CC}	Outputs Open			75	mA
Supply Current-Standby	I_{SB}*	Chip Deselected			10	μA

*Applies to KM23128S Power Down Versions only.

5

CAPACITANCE (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	All pins except pin under test are tied to ground			7.0	pF
Output Capacitance	C_O				12.5	pF

Notes: Characteristics are the same for all Operating Temperature Ranges.

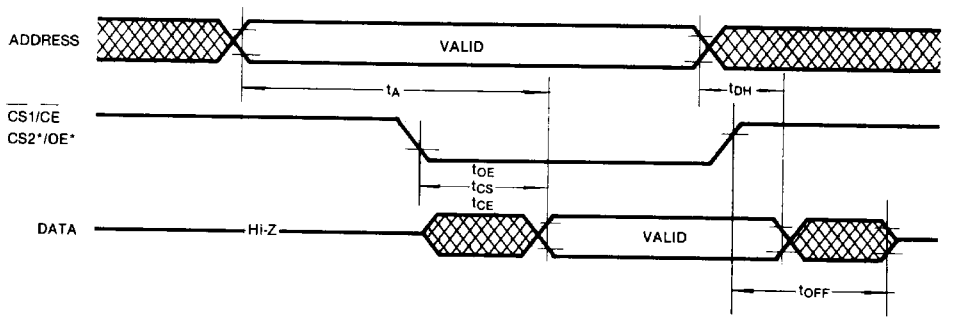
AC CHARACTERISTICS

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	23128-15 23128I-15		23128-20 23128I-20		23128-25, 23128I-25, 23128HR-25		Units
		Min	Max	Min	Max	Min	Max	
Address Access Time	t_A		150		200		250	ns
Chip Enable Access Time	t_{CE}		150		200		250	ns
Chip Select Access Time	t_{CS}		75		100		120	ns
Output Enable Access Time	t_{OE}		75		100		120	ns
Data Hold Time	t_{DH}	0		0		0		ns
CS Active to Data High Impedance	t_{OFF}		75		100		120	ns

TIMING DIAGRAMS

AC WAVEFORMS

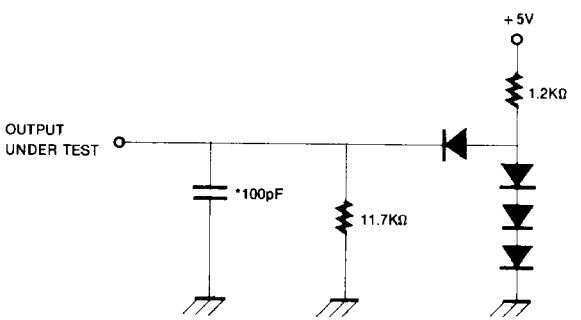


* Programmable chip selects CS, CS2 and CS3 and output Enable OE are assumed to be active low for this example

AC CONDITIONS OF TEST

Input Pulse Levels ..... 0.8 volts to 2.0 volts
Input Rise & Fall Times ..... 10 ns
Output Timing Levels ..... 0.8 volts to 2.0 volts

AC TEST LOAD CIRCUIT

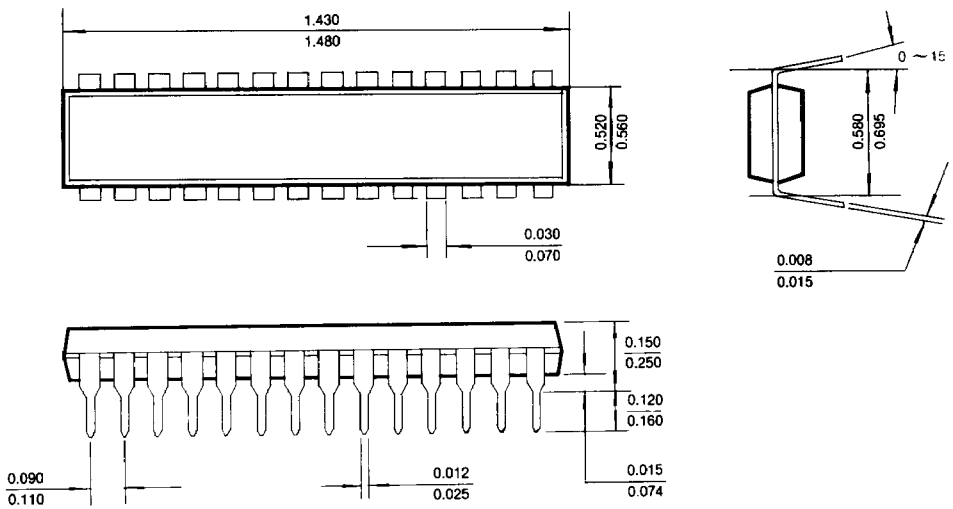


* includes jig capacitance.
All diodes 1N3064 or equivalent.

PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit: Inches



28 LEAD CERAMIC DUAL IN LINE PACKAGE

Unit: Inches