32M-Bit (2M X 16) CMOS MASK ROM

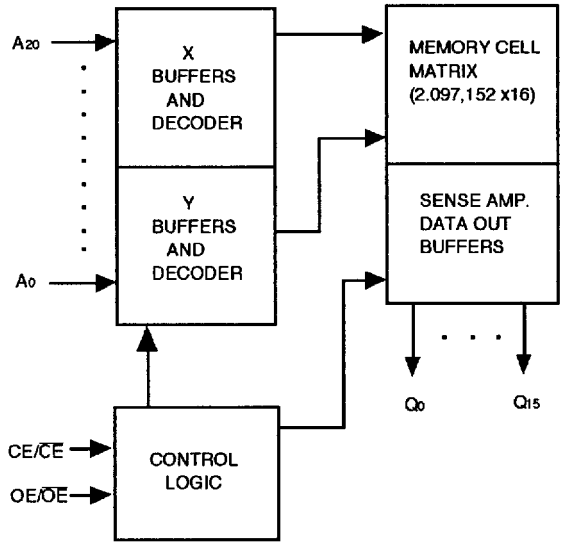
FEATURES

- 2,097,152 x 16bit Organization
- Fast access time : 120ns (max.)
- Supply voltage : single +5V
- Current consumption
  Operating : 60 mA(max.)
  Standby : 50 μA (max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Polarity programmable chip enable and output enable pin
- Package
  - KM23C32000A : 42-DIP-600

GENERAL DESCRIPTION

The KM23C32000A is a fully static mask programmable ROM organized 2,097,152x16bit.It is fabricated using silicon-gate CMOS process technology.
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.
It is suitable for use in program memory of micro-processor, and data memory, character generator.
The KM23C32000A is packaged in a 42-DIP and provides polarity programmable CE and OE buffer as user option mode.

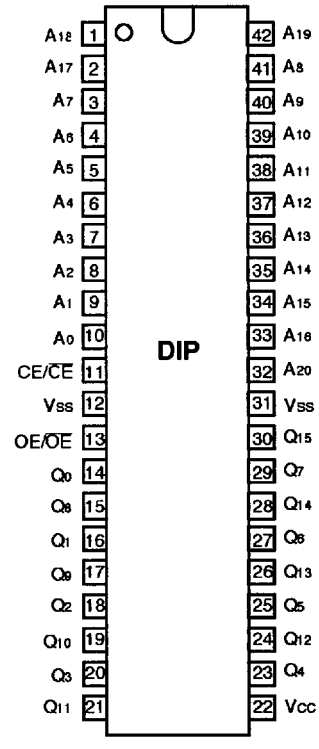
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A0-A20	Address Inputs
Q0-Q15	Data Outputs
CE/CE*	Chip Enable
OE/OE*	Output Enable
Vcc	Power (+5V)
Vss	Ground

* User Selectable Polarity

PIN CONFIGURATION



KM23C32000A

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}	-0.3 to +7.0	V
Temperature Under Bias	Tbias	-10 to +85	°C
Storage Temperature	Tstg	-55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}$=$\overline{OE}$=V_{IL}, f=6.7MHz all outputs open	-	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}$=V_{IH}, all outputs open	-	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}$=V_{CC}, all outputs open	-	50	μA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	-	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC}	-	10	μA
Input High Voltage, All Inputs	V_{IH}		2.2	V_{CC}+0.3	V
Input Low Voltage, All Inputs	V_{IL}		-0.3	0.8	V
Output High Voltage Level	V_{OH}	I_{OH}= - 400 μA	2.4	-	V
Output Low Voltage Level	V_{OL}	I_{OL}= 2.1 mA	-	0.4	V

CAPACITANCE (T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT} = 0V	-	12	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	12	pF

Note : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	Dout	Active

AC CHARACTERISTICS (T_A= 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise noted.)

TEST CONDITIONS

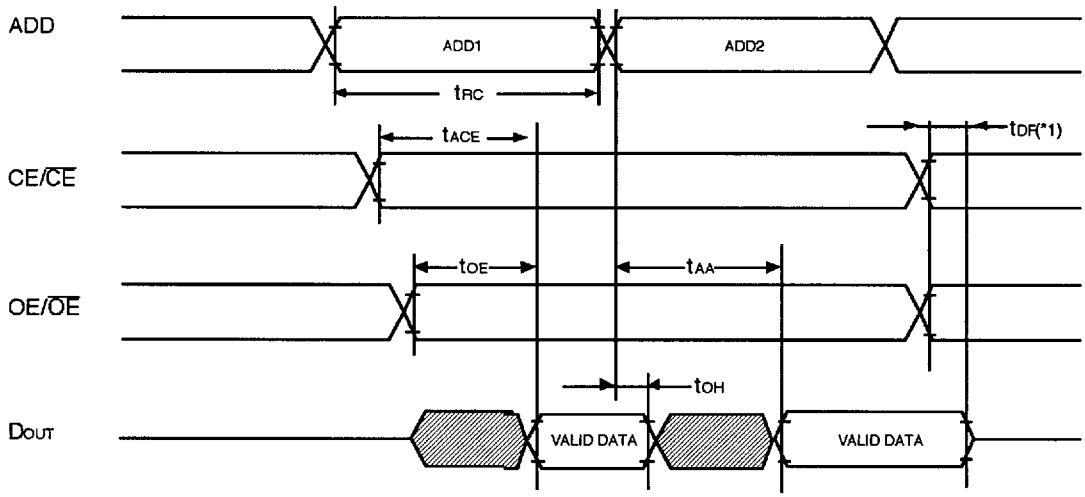
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and C_L=100pF

READ CYCLE

Parameter	Symbol	KM23C32000A-12		KM23C32000A-15		KM23C32000A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	120		150		200		ns
Chip Enable Access Time	tACE		120		150		200	ns
Address Access Time	tAA		120		150		200	ns
Output Enable Access Time	tOE		60		70		90	ns
Output or Chip Disable to Output High-Z	tDF		20		30		40	ns
Output Hold from Address Change	tOH	0		0		0		ns

TIMING DIAGRAM

READ



(*1) tDF is defined as the time at which the outputs achieve the open circuit condition and is not referenced to V_{OH} or V_{OL} level.

PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit : mm/Inch