KM2864A/KM2864AH

8K × 8 Bit EEPROM with Latches and Auto-Write

FEATURES

- Simple Byte Write
  - Single TTL Level Write Signal
  - Latched Address and Data
  - Automatic Internal Erase-before-Write
  - Automatic Write Timing
  - $\overline{DATA}$ Polling and Verification
- Enhanced Write Protection
- Single 5 volt Supply
- Byte Write: 10ms (max)—KM2864A
  - 2ms (max)—KM2864AH
- Fast Access Time: 200ns
- Power: 50mA—Standby (max)
  - 120mA—Operating (max)
- Two Line Control-Eliminates Bus Contention
- 10,000 Cycle Endurance
- JEDEC Byte-wide Memory Pinout

GENERAL DESCRIPTION

The KM2864A/AH is a 65,536 bit Electrically Erasable and Programmable Read-Only-Memory organized as 8,192 words by 8-bits. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

Writing data into the KM2864A/AH is very simple. The internally self-timed write cycle latches both address and data to provide a free system bus during the write period which is 10ms (max) for the KM2864A or 2ms (max) for the KM2864AH.

The KM2864A/AH features $\overline{DATA}$ Polling, a software scheme to detect the early completion of a write cycle without requiring the use of any additional external hardware. The KM2864A/AH is fabricated with the well-defined floating gate NMOS technology using Fowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM
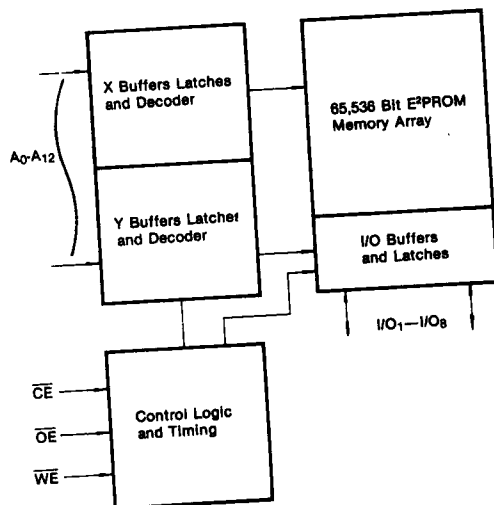
PIN CONFIGURATION
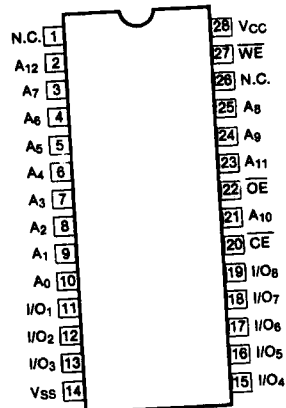
Pin Name	Pin Function
A_0-A_{12}	Address Inputs
I/O_1—I/O_8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
N.C.	No Connection
V_{cc}	Power (+5V)
V_{ss}	Ground

SAMSUNG SEMICONDUCTOR

2.3 Static RAM

Capacity	Part Number	Organization	Speed (ns)	Technology	Active, mA Typ (max)	Standby, µA Typ (max)	Packages	Remark
16K bit	KM6816A-12	2K×8	120	CMOS	20 (40)	10 (50)	24-Pin DIP	Now
	KM6816A-15	2K×8	150	CMOS	20 (40)	10 (50)	24-Pin DIP	Now
	KM6816AL-12	2K×8	120	CMOS	20 (40)	1 (10)	24-Pin DIP	Now
	KM6816AL-15	2K×8	150	CMOS	20 (40)	1 (10)	24-Pin DIP	Now
64K bit	KM6264-12	8K×8	120	CMOS	35 (45)	(1mA)	28-Pin DIP	Now
	KM6264-15	8K×8	150	CMOS	35 (45)	(1mA)	28-Pin DIP	Now
	KM6264L-12	8K×8	120	CMOS	35 (45)	2 (0.1mA)	28-Pin DIP	Now
	KM6264L-15	8K×8	150	CMOS	35 (45)	2 (0.1mA)	28-Pin DIP	Now
256K bit	††KM62256P-10	32K×8	100	CMOS	30 (45)	(1mA)	28-Pin DIP	TBA
	††KM62256P-12	32K×8	120	CMOS	30 (45)	(1mA)	28-Pin DIP	TBA
	††KM62256P-15	32K×8	150	CMOS	30 (45)	(1mA)	28-Pin DIP	TBA
	††KM62256LP-10	32K×8	100	CMOS	30 (45)	(4 µA)	28-Pin DIP	TBA
	††KM62256LP-12	32K×8	120	CMOS	30 (45)	(4 µA)	28-Pin DIP	TBA
	††KM62256LP-15	32K×8	150	CMOS	30 (45)	(4 µA)	28-Pin DIP	TBA

2.4 EEPROM

Capacity	Part Number	Organization	Speed (ns)	Technology	Write Cycle Time (max) (ms)	Features	Packages	Remark
16K bit	KM2816A-25	2K×8	250	NMOS	10	—	24-Pin DIP	Now
	KM2816A-30	2K×8	300	NMOS	10	—	24-Pin DIP	Now
	KM2816A-35	2K×8	350	NMOS	10	—	24-Pin DIP	Now
	KM2817A-25	2K×8	250	NMOS	10	Ready/Busy	28-Pin DIP	Now
	KM2817A-30	2K×8	300	NMOS	10	Ready/Busy	28-Pin DIP	Now
	KM2817A-35	2K×8	350	NMOS	10	Ready/Busy	28-Pin DIP	Now
64K bit	KM2864A-20	8K×8	200	NMOS	10	Data Polling	28-Pin DIP	Now
	KM2864A-25	8K×8	250	NMOS	10	Data Polling	28-Pin DIP	Now
	KM2864A-30	8K×8	300	NMOS	10	Data Polling	28-Pin DIP	Now
	KM2865A-20	8K×8	200	NMOS	10	Data Polling, Ready/Busy	28-Pin DIP	Now
	KM2865A-25	8K×8	250	NMOS	10	Data Polling, Ready/Busy	28-Pin DIP	Now
	KM2865A-30	8K×8	300	NMOS	10	Data Polling, Ready/Busy	28-Pin DIP	Now
	†KM2864AH-20	8K×8	200	NMOS	2	Data Polling	28-Pin DIP	Now
	†KM2864AH-25	8K×8	250	NMOS	2	Data Polling	28-Pin DIP	Now
	†KM2864AH-30	8K×8	300	NMOS	2	Data Polling	28-Pin DIP	Now
	†KM2865AH-20	8K×8	200	NMOS	2	Data Polling, Ready/Busy	28-Pin DIP	Now
	†KM2865AH-25	8K×8	250	NMOS	2	Data Polling, Ready/Busy	28-Pin DIP	Now
	†KM2865AH-30	8K×8	300	NMOS	2	Data Polling, Ready/Busy	28-Pin DIP	Now
	††KM28C64-15	8K×8	150	CMOS	10	Data Polling, Page Mode	28-Pin DIP	TBA
	††KM28C64-20	8K×8	200	CMOS	10	Data Polling, Page Mode	28-Pin DIP	TBA
	††KM28C64-25	8K×8	250	CMOS	10	Data Polling, Page Mode	28-Pin DIP	TBA

† New Product
†† Under Development
TBA: To Be Announced

8K × 8 Bit EEPROM with Latches and Auto-Write

FEATURES

- **Simple Byte Write**
  - — Single TTL Level Write Signal
  - — Latched Address and Data
  - — Automatic Internal Erase-before-Write
  - — Automatic Write Timing
  - — $\overline{DATA}$ Polling and Verification
  - — Ready/$\overline{Busy}$ Output Pin (KM2865A)
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Byte Write: 10ms (max)**
- **Fast Access Time: 200ns**
- **Power: 50mA—Standby (max)**
  120mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **NMOS Floating Gate Technology**
- **10,000 Cycle Endurance**
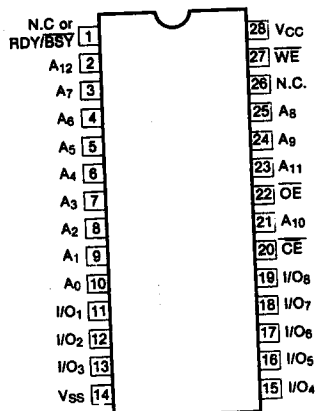- **JEDEC Byte-wide Memory Pinout**
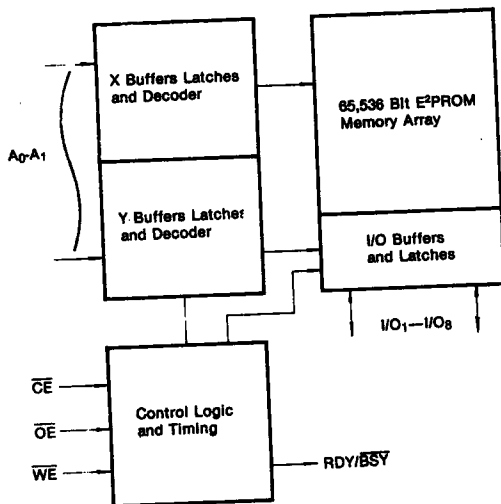
GENERAL DESCRIPTION

The KM2864A/65A is a 65,536 bit Electrically Erasable and Programmable Read-Only-Memory organized as 8,192 words by 8-bits. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

Writing data into the KM2864A/65A is very simple. The internally self-timed write cycle latches both address and data to provide a free system bus during the 10ms (max) write period.

The KM2864A features $\overline{DATA}$ Polling, which enables the E²PROM to signal the processor that a write operation is complete without requiring the use of any external hardware. The KM2865A is identical to the KM2864A and in addition has a Ready/$\overline{Busy}$ output on pin 1 which signals when the write operation is complete.

FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION

Pin Name	Pin Function
A_0-A_{12}	Address Inputs
I/O_1—I/O_8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{Busy}$ Output
N.C.	No Connect
V_{CC}	Power (+5V)
V_{SS}	Ground

SAMSUNG SEMICONDUCTOR

8K × 8 Bit High Performance EEPROM with Latches and Auto-Write

FEATURES

- **Simple Byte Write**
  - **Fast Byte Write Time**
  - **Single TTL Level Write Signal**
  - **Latched Address and Data**
  - **Automatic Internal Erase-before-Write**
  - **Automatic Write Timing**
  - **DATA Polling and Verification**
  - **Ready/Busy Output Pin (KM2865AH)**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Byte Write: 2ms (max)**
- **Fast Access Time: 200ns**
- **Power: 50mA—Standby (max)**
  120mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **NMOS Floating Gate Technology**
- **10,000 Cycle Endurance**
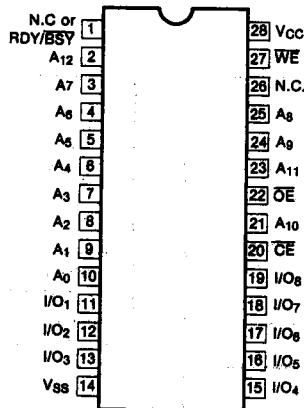- **JEDEC Byte-wide Memory Pinout**
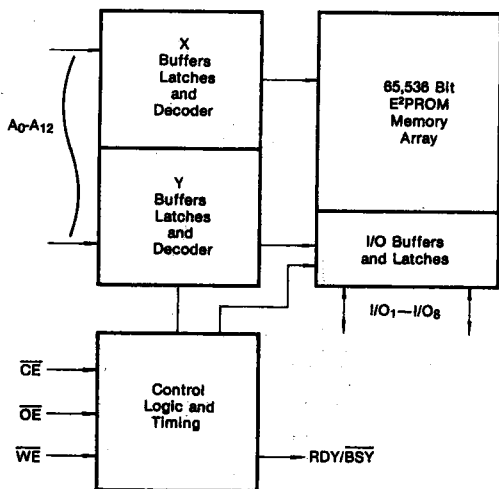
GENERAL DESCRIPTION

The KM2864AH/65AH is a 65,536 bit Electrically Erasable and Programmable Read-Only-Memory organized as 8,192 words by 8-bits. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

Writing data into the KM2864AH/65AH is very simple. The internally self-timed write cycle latches both address and data to provide a free system bus during the 2ms (max) write period.

The KM2864AH features $\overline{DATA}$ Polling, which enables the E²PROM to signal the processor that a write operation is complete without requiring the use of any external hardware. The KM2865AH is identical to the KM2864AH and in addition has a Ready/Busy output on pin 1 which signals when the write operation is complete. For systems requiring faster byte write time the KM2864AH/65AH is specified at 2ms.
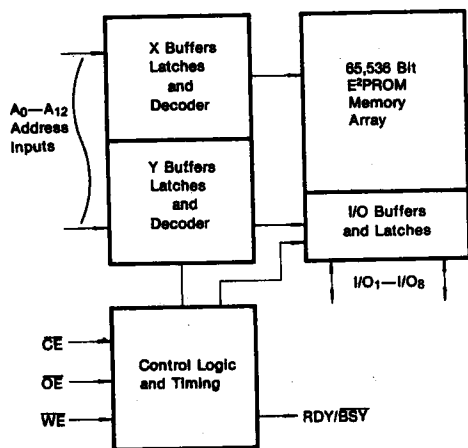
FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION

Pin Name	Pin Function
A_0-A_{12}	Address Inputs
I/O_1—I/O_8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/Busy Output
N.C.	No Connect
V_{CC}	Power (+ 5V)
V_{SS}	Ground

KM28C64/KM28C65

8K × 8 CMOS Electrically Eraseble PROM

FEATURES

- Simple Byte Write
  - Single TTL Level Write Signal
  - Latched Address and Data
  - Automatic Internal Erase-before-Write
  - Automatic Write Timing
  - DATA Polling and Verification
  - Ready/Busy Output Pin (KM28C65)
- 32-byte page write: 5mS max
  - Effective 150μS/byte write
- Enhanced Write Protection
- Single 5 volt Supply
- Fast Access Time: 150nS
- Power: 100 μA — Standby (max)
         30 mA — Operating (max)
- Two Line Control-Eliminates Bus Contention
- 10,000 Cycle Endurance
- JEDEC Byte-wide Memory Pinout

GENERAL DESCRIPTION

The KM28C64/C65 is a 8,192 × 8 bit electrically erasable and programable Read Only Memory. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

Writing data into the KM28C64/C65 is very simple. The internally self-timed write cycle latches both address bus during the 5mS (max) write period.

A 32-byte page write enables an entire chip written in 1.3 second.

The KM28C64/C65 features DATA-polling, which enables the EEPROM to signal the processor that a write operation is complete without requiring the use of any external hardware. Ready/Busy is a hardware scheme in which Pin 1 is used to signal the status of the write operation and is especially useful in interrupt driven systems.

The KM28C64/C65 is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION

Pin Name	Pin Function
A$_0$—A$_{12}$	Address Inputs
I/O$_1$—I/O$_8$	Data Inputs/Outputs
CE	Chip Enable
OE	Output Enable
WE	Write Enable
RDY/BSY	Ready/Busy Output
N.C.	No Connect
V$_{CC}$	+5V
V$_{SS}$	Ground

KM28C64/KM28C65

8K × 8 CMOS Electrically Erasable PROM

FEATURES

- Simple Byte Write
  - Single TTL Level Write Signal
  - Latched Address and Data
  - Automatic Internal Erase-before-Write
  - Automatic Write Timing
  - DATA Polling and Verification
  - Ready/Busy Output Pin (KM28C65)
- 32-byte page write: 5ms max
  - Effective 150μS/byte write
- Enhanced Write Protection
- Single 5 volt Supply
- Fast Access Time: 150ns
- Power: 100 μA — Standby (max)
         30 mA — Operating (max)
- Two Line Control-Eliminates Bus Contention
- 10,000 Cycle Endurance
- JEDEC Byte-wide Memory Pinout

GENERAL DESCRIPTION

The KM28C64/C65 is a 8,192 × 8 bit electrically erasable and programmable Read Only Memory. Its data can be modified using simple TTL level signals and a single 5 volt power supply.
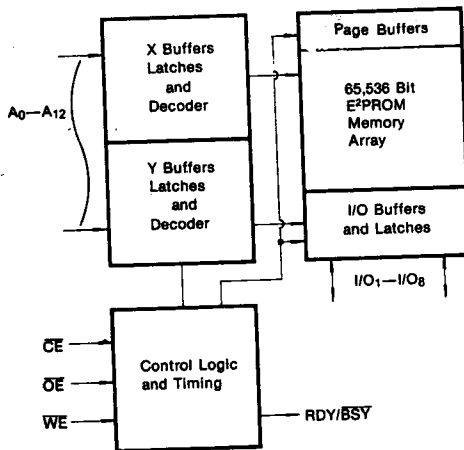
Writing data into the KM28C64/C65 is very simple. The internally self-timed write cycle latches both address bus during the 5mS (max) write period.

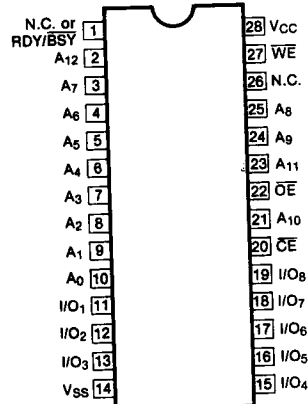A 32-byte page write enables an entire chip written in 1.3 second.

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8K × 8 Bit EEPROM with Latches and Auto-Write

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  - $\overline{\text{DATA}}$ Polling and Verification
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- **10,000 Cycle Endurance**
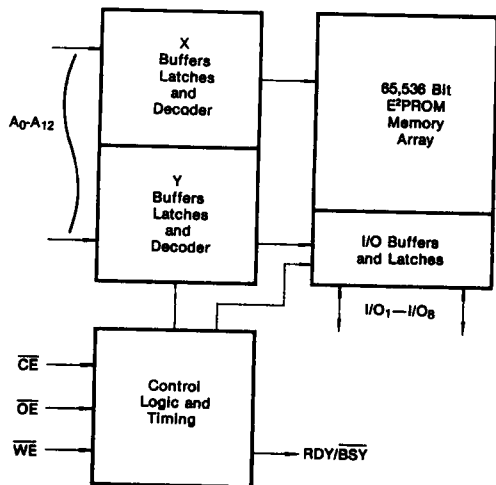- **JEDEC Byte-wide Memory Pinout**

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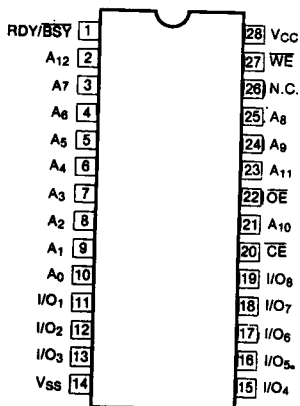
The KM2865A/AH features two end of write detection schemes to provide maximum design flexibility while enhancing the system performance. $\overline{\text{DATA}}$ Polling is a software scheme to detect the early completion of a write cycle without using any additional hardware. Ready/$\overline{\text{Busy}}$ is a hardware scheme in which Pin 1 is used to signal the status of the write operation and is especially useful in interrupt driven systems.

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SAMSUNG SEMICONDUCTOR