Document Title

4M x 8 bit NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Data Sheet, 1997	April 10th 1997	

1.0	Data Sheet, 1998
	1. Changed t_{BERS} parameter : 5ms(Typ.) $\rightarrow$ 2ms(Typ.)
	2. Removed reverse type package.
	3. The 1st block(00h block address) is guaranteed to be a good block.
	4. Changed AC parameters.
	    t_{WH} : 10ns(Min.) $\rightarrow$ 15ns(Min).
	    t_{REH} : 10ns(Min) $\rightarrow$ 15ns(Min).
		April 10th 1998	

1.1	Data Sheet, 1998	July 14th 1998	Final

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4M x 8 Bit NAND Flash Memory

FEATURES

- Single 3.3 volt Supply
- Organization
  - Memory Cell Array : (4M + 128K)bit x 8bit
  - Data Register   : (512 + 16)bit x8bit
- Automatic Program and Erase
  - Page Program : (512 + 16)Byte
  - Block Erase   : (8K + 256)Byte
  - Status Register
- 528-Byte Page Read Operation
  - Random Access   : 10 μs(Max.)
  - Serial Page Access : 50ns(Min.)
- Fast Write Cycle Time
  - Program time   : 250 μs(typ.)
  - Block Erase time : 2ms(typ.)
- Command/Address/Data Multiplexed I/O port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 1M Program/Erase Cycles
  - Data Retention : 10 years
- Command Register Operation
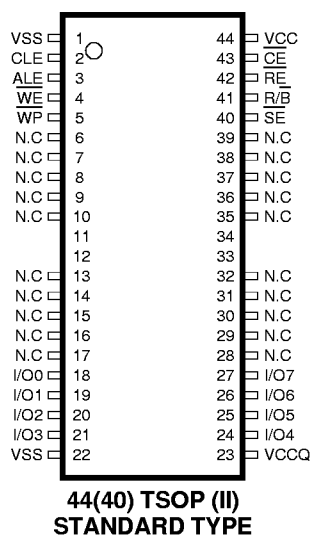- 44(40) - Lead TSOP Type II (400mil / 0.8 mm pitch)
  - Forward Type

GENERAL DESCRIPTION

The KM29V32000 is a 4M(4,194,304)x8bit NAND Flash Memory with a spare 128K(131,072)x8bit. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation programs the 528-byte page in typically 250 μs and an erase operation can be performed in typically 2ms on an 8K-byte block.

Data in the page can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command inputs. The on-chip write controller automates all program and erase system functions, including pulse repetition, where required, and internal verify and margining of data. Even the write-intensive systems can take advantage of the KM29V32000 extended reliability of one million program/erase cycles by providing either ECC(Error Correction Code) or real time mapping-out algorithm. These algorithms have been implemented in many mass storage applications and also the spare 16 bytes of a page combined with the other 512 bytes can be utilized by system-level ECC.

The KM29V32000 is an optimum solution for large nonvolatile storage application such as solid state storage, digital voice recorder, digital still camera and other portable applications requiring nonvolatility.

PIN CONFIGURATION

```
          ┌─────────────┐
   VSS ☐  1 ○        44 ☐ VCC
   CLE ☐  2          43 ☐ CE
   ALE ☐  3          42 ☐ RE
   WE  ☐  4          41 ☐ R/B
   WP  ☐  5          40 ☐ SE
   N.C ☐  6          39 ☐ N.C
   N.C ☐  7          38 ☐ N.C
   N.C ☐  8          37 ☐ N.C
   N.C ☐  9          36 ☐ N.C
   N.C ☐ 10          35 ☐ N.C
        11          34
        12          33
   N.C ☐ 13          32 ☐ N.C
   N.C ☐ 14          31 ☐ N.C
   N.C ☐ 15          30 ☐ N.C
   N.C ☐ 16          29 ☐ N.C
   N.C ☐ 17          28 ☐ N.C
  I/O0 ☐ 18          27 ☐ I/O7
  I/O1 ☐ 19          26 ☐ I/O6
  I/O2 ☐ 20          25 ☐ I/O5
  I/O3 ☐ 21          24 ☐ I/O4
   VSS ☐ 22          23 ☐ VCCQ
          └─────────────┘
```

44(40) TSOP (II)
STANDARD TYPE

PIN DESCRIPTION

Pin Name	Pin Function
I/O0 ~ I/O7	Data Inputs/Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
CE	Chip Enable
RE	Read Enable
WE	Write Enable
WP	Write Protect
SE	Spare area Enable
R/B	Ready/Busy output
Vcc	Power(+3.3V)
Vccq	Output Buffer Power(+3.3V or 5.0V)
Vss	Ground
N.C	No Connection

NOTE : Connect all Vcc, Vccq and Vss pins of each device to power supply outputs.
       Do not leave Vcc or Vss disconnected.

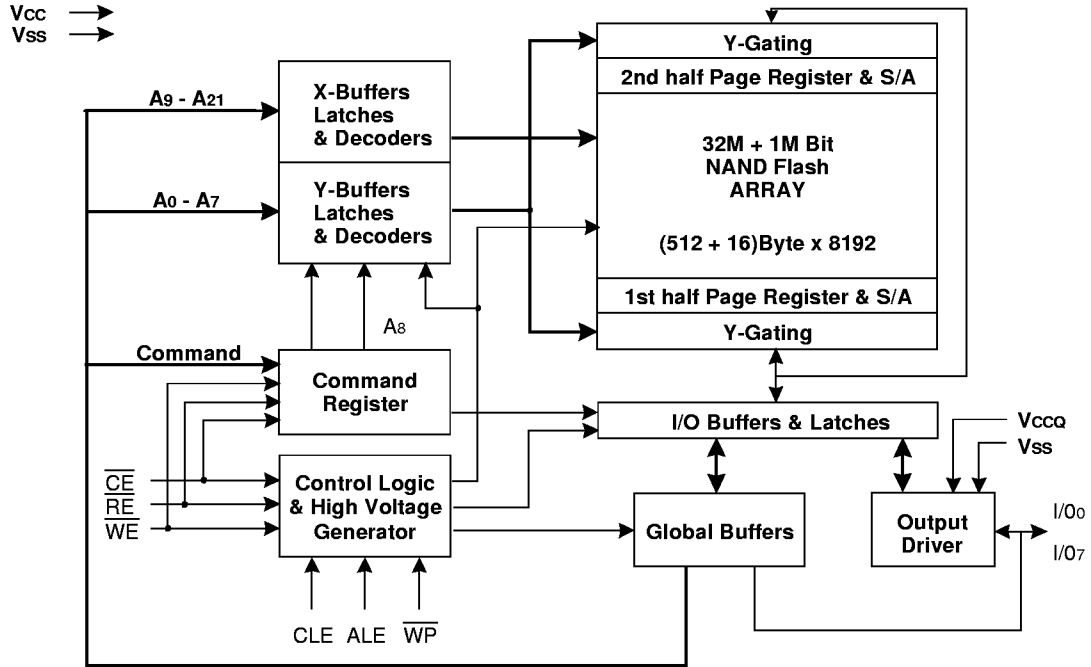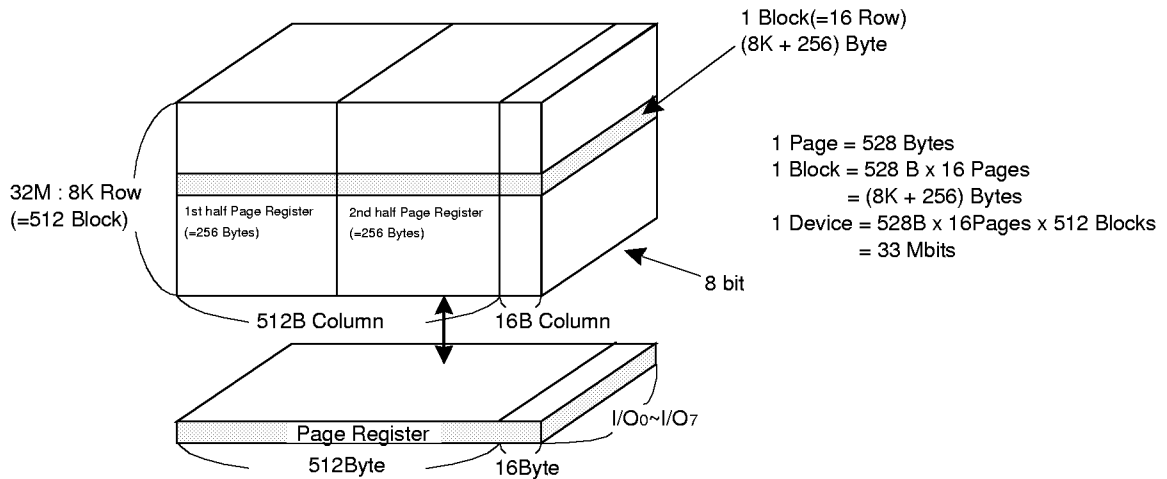## Figure 1. FUNCTIONAL BLOCK DIAGRAM

Figure 2. ARRAY ORGANIZATION

1 Block(=16 Row)
(8K + 256) Byte

1 Page = 528 Bytes
1 Block = 528 B x 16 Pages
= (8K + 256) Bytes
1 Device = 528B x 16Pages x 512 Blocks
= 33 Mbits

32M : 8K Row
(=512 Block)

1st half Page Register
(=256 Bytes)

2nd half Page Register
(=256 Bytes)

8 bit

512B Column   16B Column

I/O0~I/O7

Page Register

512Byte   16Byte

	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	**Column Address**
2nd Cycle	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	**Row Address**
3rd Cycle	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	*X	*X	*X	**(Page Address)**

NOTE : Column Address : Starting Address of the Register.

00H Command(Read) : Defines the starting Address of the 1st half of the Register.

01H Command(Read) : Defines the sarting Address of the 2nd half of the Register.

* A_8 is initially set to "Low" or "High" by the 00H or 01H Command.

* X can be High or Low.

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PRODUCT INTRODUCTION

The KM29V32000 is a 33Mbit(34,603,008 bit) memory organized as 8192 rows by 528 columns. Spare sixteen columns are located from column address of 512 to 527. A 528-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of the 16 pa ges formed by one NAND structures, totaling 528 NAND structures of 16 cells. The array organization is shown in Figure 2. The progra m and read operations are executed on a page basis, while the erase operation is executed on block basis. The memory array consist s of 512 separately or grouped erasable 8K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the KM29V32000.

The KM29V32000 has addresses multiplexed into 8 I/O s. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written throug h I/O s by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except for Block Erase command which requires two cycles : a cycle for erase-setup and another for erase-execution after block address loading. The 4M byte physical space requires 22 addresses, thereby requiring three cycles for byte-level addressing: col umn address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following the required command input. In Block Erase operation, however, only the two row address cycles are used.

Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the KM29V32000.

Table 1. COMMAND SETS

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Sequential Data Input	80h	-	
Read 1	00h/01h[1]	-	
Read 2	50h[2]	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	10h	-	
Block Erase	60h	D0h	
Erase Suspend	B0h	-	O
Erase Resume	D0h	-	
Read Status	70h	-	O

NOTE : 1. The 00H command defines starting address of the 1st half of registers.
         The 01H command defines starting address of the 2nd half of registers.
         After data access on the 2nd half of register by the 01H command, the status pointer is
         automatically moved to the 1st half register(00H) on the next cycle.
      2. The 50H command is valid only when the $\overline{SE}$(pin 40) is low level.

PIN DESCRIPTION

Command Latch Enable(CLE)

The CLE input controls the path activation for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.

Address Latch Enable(ALE)

The ALE input controls the path activation for address and input data to the internal address/data register.
Addresses are latched on the rising edge of $\overline{WE}$ with ALE high, and input data is latched when ALE is low.

Chip Enable($\overline{CE}$)

The $\overline{CE}$ input is the device selection control. When $\overline{CE}$ goes high during a read operation the device is returned to standby mode. However, when the device is in the busy state during program or erase, $\overline{CE}$ high is ignored, and does not return the device to standby mode.

Write Enable($\overline{WE}$)

The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.

Read Enable($\overline{RE}$)

The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t REA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.

Spare Area Enable($\overline{SE}$)

The $\overline{SE}$ input controls the spare area selection when $\overline{SE}$ is high, the device is deselected the spare area during Read1, Sequential data input and page Program.

I/O Port : I/O$_0$~I/O$_7$

The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high- z when the chip is deselected or when the outputs are disabled.

Write Protect($\overline{WP}$)

The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.

Ready/$\overline{Busy}$(R/$\overline{B}$)

The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.

Power Line(V$_{CC}$ & V$_{CCQ}$)

The V$_{CCQ}$ is the power supply for I/O interface logic. It is electrically isolated from main power line(V$_{CC}$=3.3V) for supporting 5V toler-ant I/O with 5V power supply at V$_{CCQ}$.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V ss		V_{IN}	-0.6 to +6.0	V
Temperature Under Bias	KM29V32000T	T_{BIAS}	-10 to +125	°C
	KM29V32000IT		-40 to +125	
Storage Temperature		T_{STG}	-65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA

NOTE :
1. Minimum DC voltage is -0.3V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is VccQ+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.

2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions
   as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, KM29V32000T:T_A=0 to 70°C, KM29V32000IT:T_A=-40 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Supply Voltage	$V_{CCQ}{}^{1)}$	3.0	-	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

NOTE :

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Current	Sequential Read	I_{CC1}	tcycle=50ns	$\overline{CE}=V_{IL}$, I_{OUT}=0mA	-	10	20	mA
	Command, Address Input	I_{CC3}	tcycle=50ns		-	10	20	mA
	Data Input	I_{CC4}	-		-	10	20	mA
	Program	I_{CC6}	-		-	10	20	mA
	Erase	I_{CC7}	-		-	10	20	mA
Stand-by Current(TTL)		I_{SB1}	$\overline{CE}=V_{IH}$, $\overline{WP}=\overline{SE}$=0V/Vcc		-	-	1	mA
Stand-by Current(CMOS)		I_{SB2}	$\overline{CE}=V_{CC}$-0.2, $\overline{WP}=\overline{SE}$=0V/Vcc		-	10	50	μA
Input Leakage Current		I_{LI}	V_{IN} =0 to 3.6V		-	-	±10	μA
Output Leakage Current		I_{LO}	V_{OUT}=0 to 3.6V		-	-	±10	μA
Input High Voltage		V_{IH}	I/O pins		2.0	-	Vccq+0.3	V
			Except I/O pins		2.0	-	Vcc+0.3	
Input Low Voltage, All inputs		V_{IL}	-		-0.3	-	0.8	V
Output High Voltage Level		V_{OH}	I_{OH}=-400μA		2.4	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=2.1mA		-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V		8	10	-	mA

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	502	508	511	Blocks

NOTE :
1. The KM29V32000 may or may not include bad blocks. Bad blocks are defined as blocks that contain one or more bad bits. Do not try to access these bad blocks for program and erase. The Minimum valid blocks are guaranteed for 10 years data retention or 1M program erase cyclin g. (Refer to the attached technical notes)
2. The 1st block, which is placed on 00h block address, is guaranteed to be a good block

AC TEST CONDITION
(KM29V32000T:T_A=0 to 70°C, KM29V32000IT:T_A=-40 to 85°C, V_{CC}=3.3V±10%   unless otherwise noted)

Parameter	Value
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL GATE and CL=100pF

CAPACITANCE (T_A=25°C, V_{CC}=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	CE	WE	RE	SE	WP	Mode	
H	L	L	⌐_⌐	H	X	X	Read Mode	Command Input
L	H	L	⌐_⌐	H	X	X		Address Input(3clock)
H	L	L	⌐_⌐	H	X	H	Write Mode	Command Input
L	H	L	⌐_⌐	H	X	H		Address Input(3clock)
L	L	L	⌐_⌐	H	L/H(3)	H	Data Input	
L	L	L	H	⌐_⌐	L/H(3)	X	Sequential Read & Data Output	
L	L	L	H	H	L/H(3)	X	During Read(Busy)	
X	X	X	X	X	L/H(3)	H	During Program(Busy)	
X	X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc(2)	0V/Vcc(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}
        2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.
        3. When $\overline{SE}$ is high, spare area is deselected.

Program/Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	0.25	1.5	ms
Number of Partial Program Cycles in the Same Page	Nop	-	-	10	cycles
Block Erase Time	t_{BERS}	-	2	10	ms

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	tCLS	0	-	ns
CLE Hold Time	tCLH	10	-	ns
CE Setup Time	tCS	0	-	ns
CE Hold Time	tCH	10	-	ns
WE Pulse Width	tWP	25	-	ns
ALE Setup Time	tALS	0	-	ns
ALE Hold Time	tALH	10	-	ns
Data Setup Time	tDS	20	-	ns
Data Hold Time	tDH	10	-	ns
Write Cycle Time	tWC	50	-	ns
WE High Hold Time	tWH	15	-	ns

AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	tR	-	10	μs
ALE to RE Delay(read ID)	tAR1	150	-	ns
ALE to RE Delay(Read cycle)	tAR2	50	-	ns
CE to RE Delay(ID read)	tCR	100	-	ns
Ready to RE Low	tRR	20	-	ns
RE Pulse Width	tRP	30	-	ns
WE High to Busy	tWB	-	100	ns
Read Cycle Time	tRC	50	-	ns
RE Access Time	tREA	-	35	ns
RE High to Output Hi-Z	tRHZ	15	30	ns
CE High to Output Hi-Z	tCHZ	-	20	ns
RE High Hold Time	tREH	15	-	ns
Output Hi-Z to RE Low	tIR	0	-	ns
Last RE High to Busy(at sequential read)	tRB	-	100	ns
CE High to Ready(in case of interception by CE at read)[1]	tCRY	-	50 +tr(R/B)[2]	ns
CE High Hold Time(at the last serial read) [3]	tCEH	100	-	ns
RE Low to Status Output	tRSTO	-	35	ns
CE Low to Status Output	tCSTO	-	45	ns
RE High to WE Low	tRHW	0	-	ns
WE High to RE Low	tWHR	60	-	ns
Erase Suspend Input to Ready	tSR	-	500	μs
RE access time(Read ID)	tREADID	-	35	ns
Device Resetting Time (Read/Program/Erase/after erase suspend)	tRST	-	5/10/500/5	μs

NOTE : 1. If CE goes high within 30ns after the rising edge of the last RE, R/B will not return to VOL.
    2. The time to Ready depends on the value of the pull-up resistor tied R/B pin.
    3. To break the sequential read cycle, CE must be held high for longer time than tCEH.

KM29V32000 Technical Notes

INVALID BLOCKS

The KM29V32000 Flash device may or may not contain up to 10 invalid blocks. Invalid blocks are defined as blocks that contain on e or more invalid bits. Typically, an invalid block will contain a single bad bit. Devices with invalid block(s) have the same qu ality levels as devices with all valid blocks and havet the same AC and DC characteristics. An invalid block(s) does not affect the performan ce of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design mus t be able to mask out the invalid block(s) via address mapping. The 1st block of the KM29V32000, however, is fully guaranteed to be a good block.

Identifying Invalid Block(s) in the KM29V32000

All device locations are erased(FFh) prior to shipping. Device with invalid Block(s) will be randomly written with 00h data with in the first or second page in the invalid Block(s). This page may or may not contain the invalid cell(s). The 00h data just marks the block(s) that contains the invalid cell(s). A system that can utilize these devices must be able to recognize invalid block(s) via the fo llowing suggested flow chart
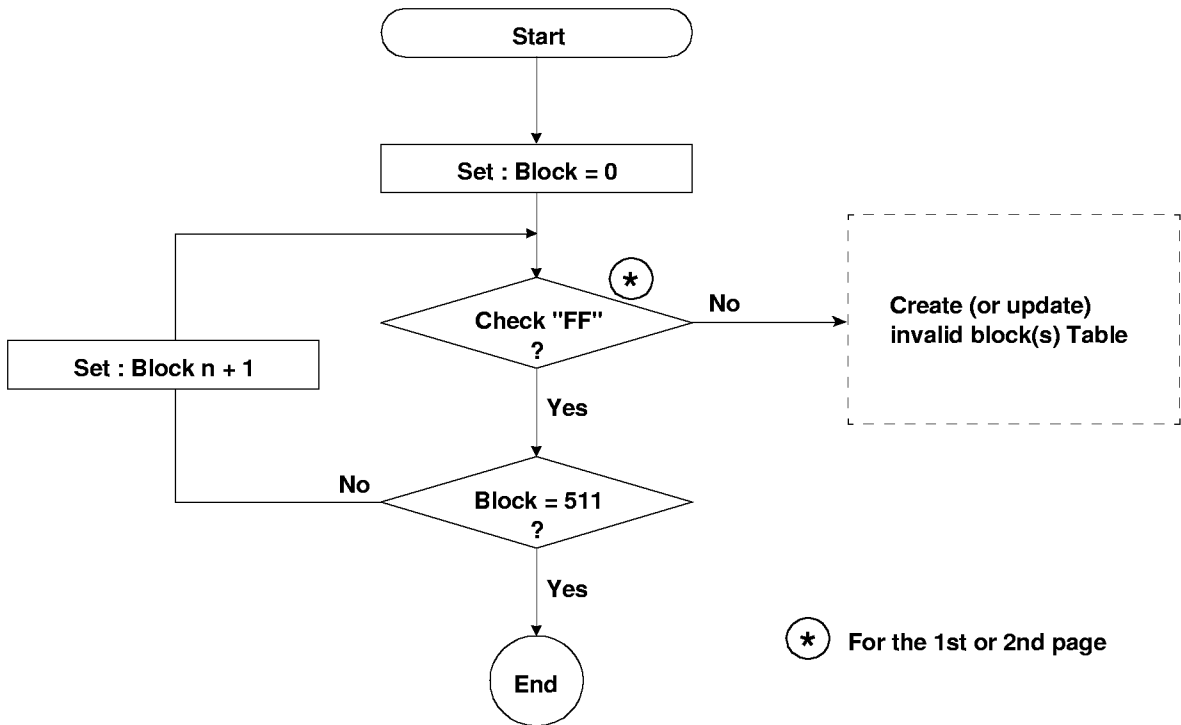(Figure 1).

Figure 1. Flow chart to create invalid block table.

KM29V32000 Technical Notes (Continued)

Error in program or erase operation

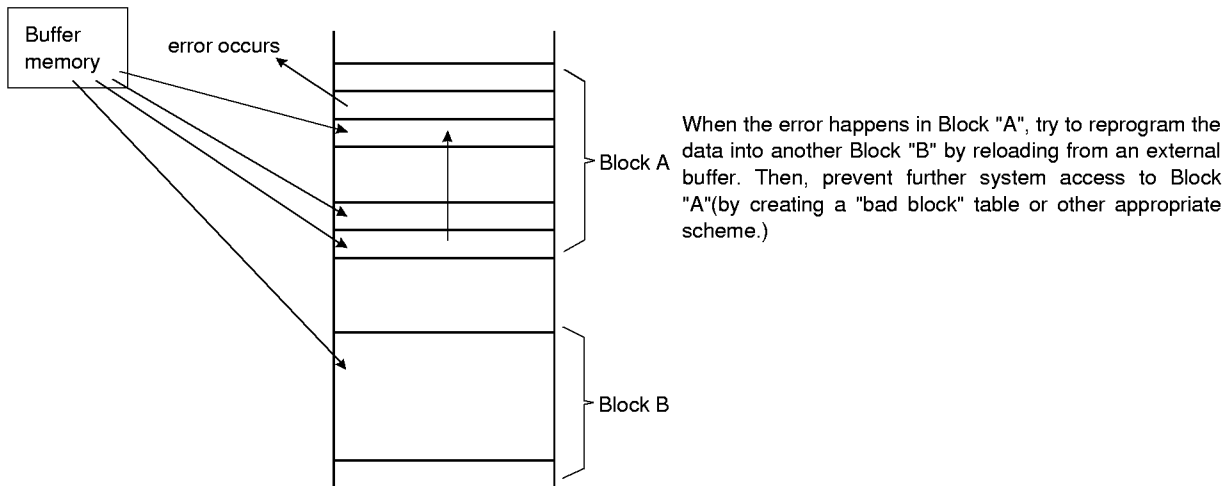The device may fail during a program or erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

Failure Mode		Detection and Countermeasure sequence
Block	Erase Failure	Status Read after Erase --> Block Replacement
Page	Program Failure	Status Read after Program --> Block Replacement
Single Bit	Program Failure ("1" --> "0")	Block Verify after Program --> Retry or ECC

ECC   : Error Correcting Code --> Hamming Code etc.
                         Example) 1bit correction & 2bit detection

Block Replacement

During Program operation ;

When the error happens in Block "A", try to reprogram the data into another Block "B" by reloading from an external buffer. Then, prevent further system access to Block "A"(by creating a "bad block" table or other appropriate scheme.)

During Erase operation ;

When the error occurs after an erase operation, prevent future accesses to this bad block
(again by creating a table within the system or other appropriate scheme.)

Pointer Operation of KM29V32000

The KM29V32000 has three read modes to set the destination of the pointer. The pointer is set to "A" area by the "00h" command,   to "B" area by the "01" command, and to "C" area by the "50h" command. Table 1 shows the destination of the pointer, and figure 2 shows the block diagram of its operations.
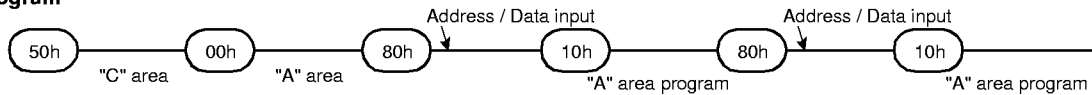
Table 1. Destination of the pointer

Command	Pointer position	Area
00H	0 ~ 255 byte	1st half array(A)
01H	256 ~ 511 byte	2nd half array(B)
50H	512 ~ 527 byte	spare array(C)
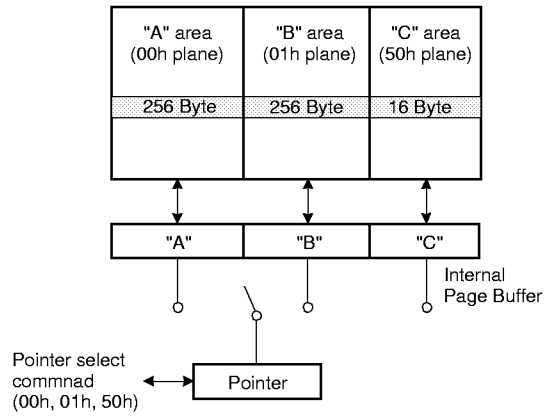
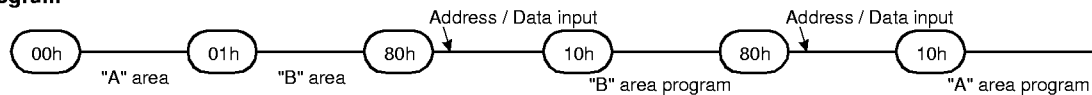Figure 2. Block diagram of pointer Operation
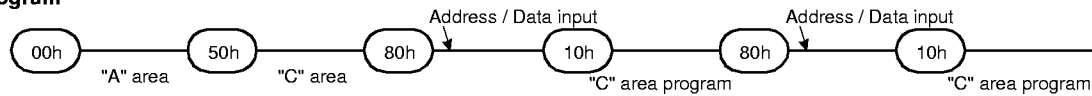
Example of Pointer Operation programming

(1) "A" area program

(2) "B" area program

(3) "C" area program


Table 2. Pointer Status after each operation

Operation	Pointer status after operation
Program/Erase	With previous 00H, Device is set to 00H Plane With previous 01H, Device is set to 00H Plane* With previous 50H, Device is set to 50H Plane
Reset	"00h" Plane("A" area)
Power up	"00h" Plane("A" area)

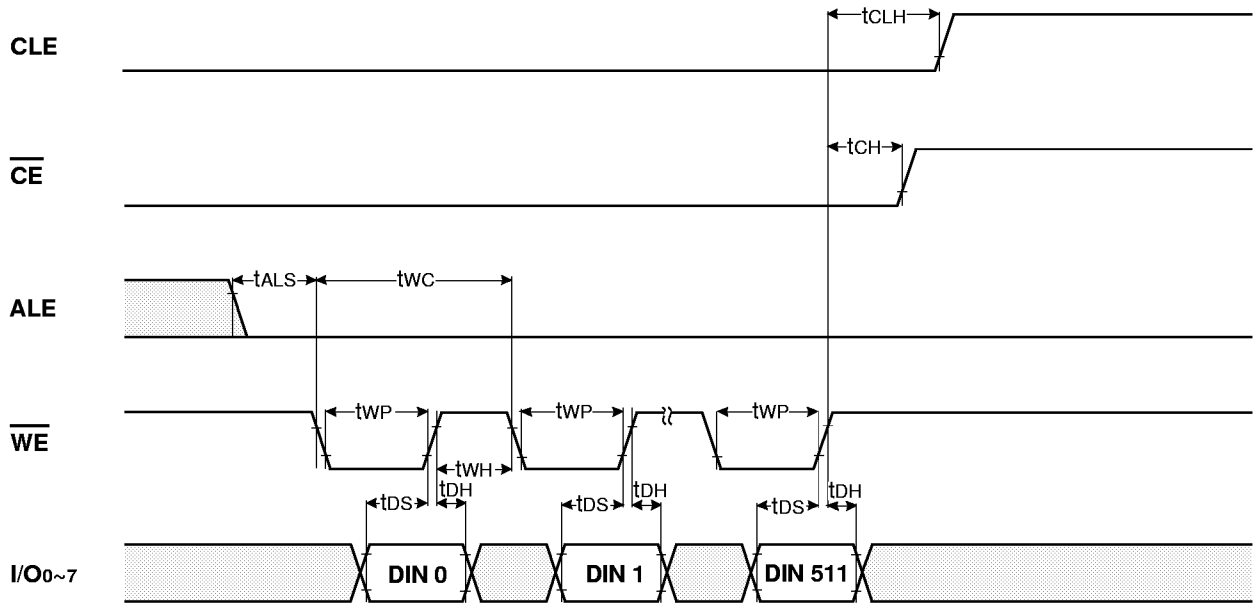* 01H command is valid just one time when it is used as a pointer for program/erase.
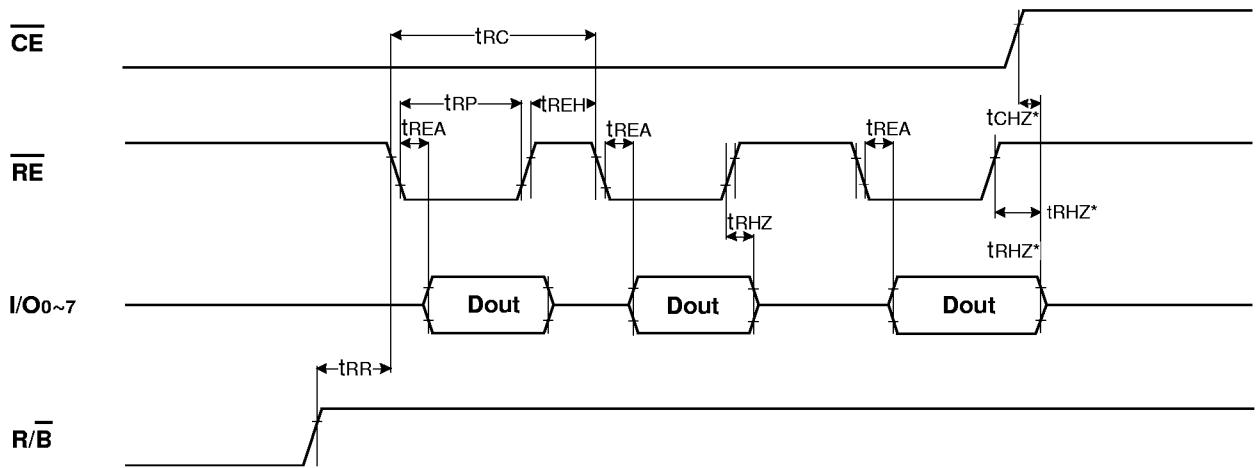
* Command Latch Cycle
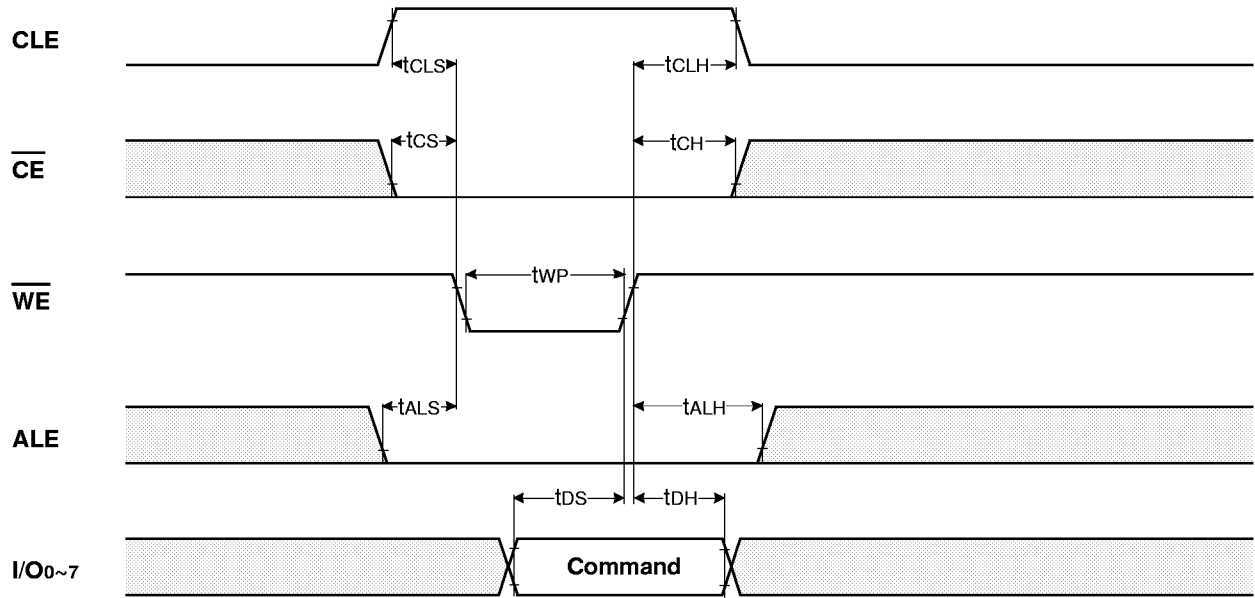
* Address Latch Cycle
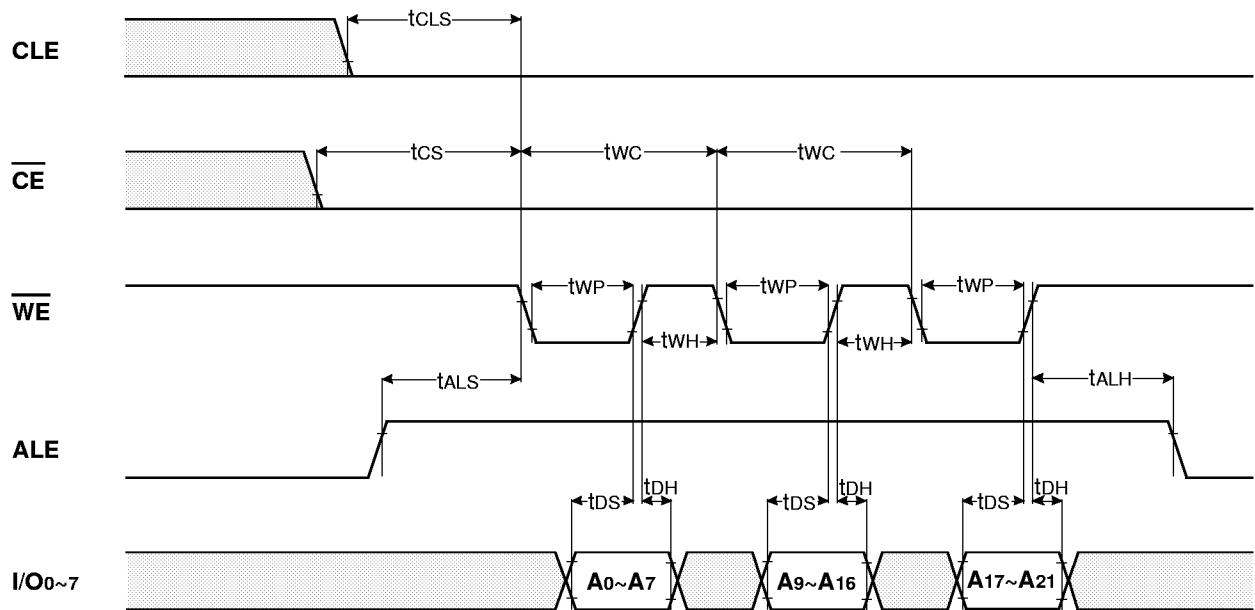
* Input Data Latch Cycle

* Sequential Out Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)

* Status Read Cycle

CLE

CE

WE

RE

I/O0~7

tCLS
tCLH
tCLS
tCS
tCH
tWP
tCSTO
tCHZ*
tWHR
tDS
tDH
tIR
tRSTO
tRHZ*
70H
Status Output
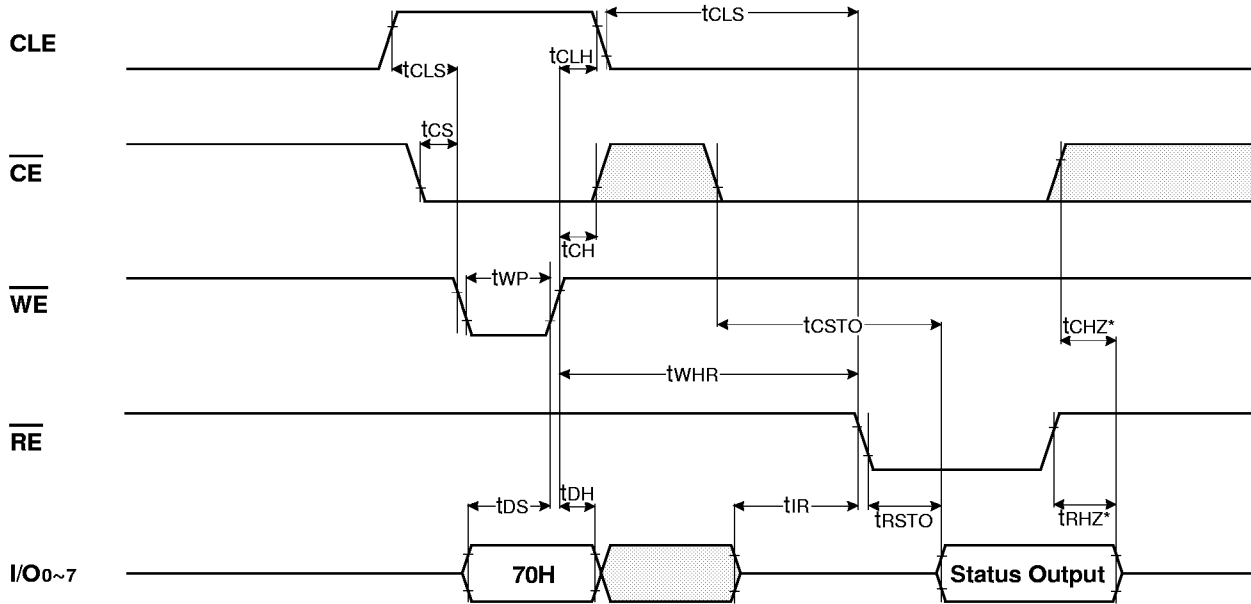
NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

READ1 OPERATION (READ ONE PAGE)

CLE

CE

WE

ALE

RE

I/O0~7

R/B

tCEH
tCHZ
tWC
tWB
tAR2
tCRY
tR
tRC
tRHZ
tRR
00h or 01h   A0 ~ A7   A9 ~ A16   A17 ~ A21   Dout N   Dout N+1   Dout N+2   Dout N+3   Dout 527
Column Address   Page(Row) Address
Busy
tRB
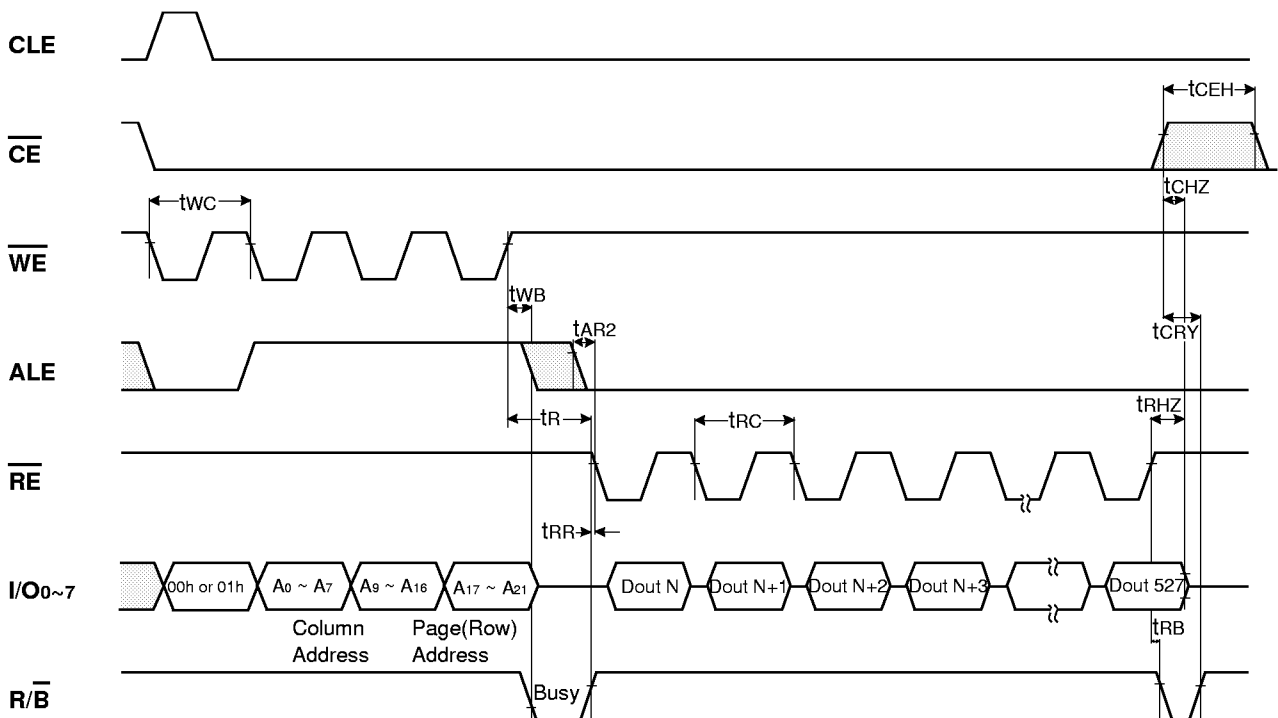
READ1 OPERATION (INTERCEPTED BY $\overline{CE}$)
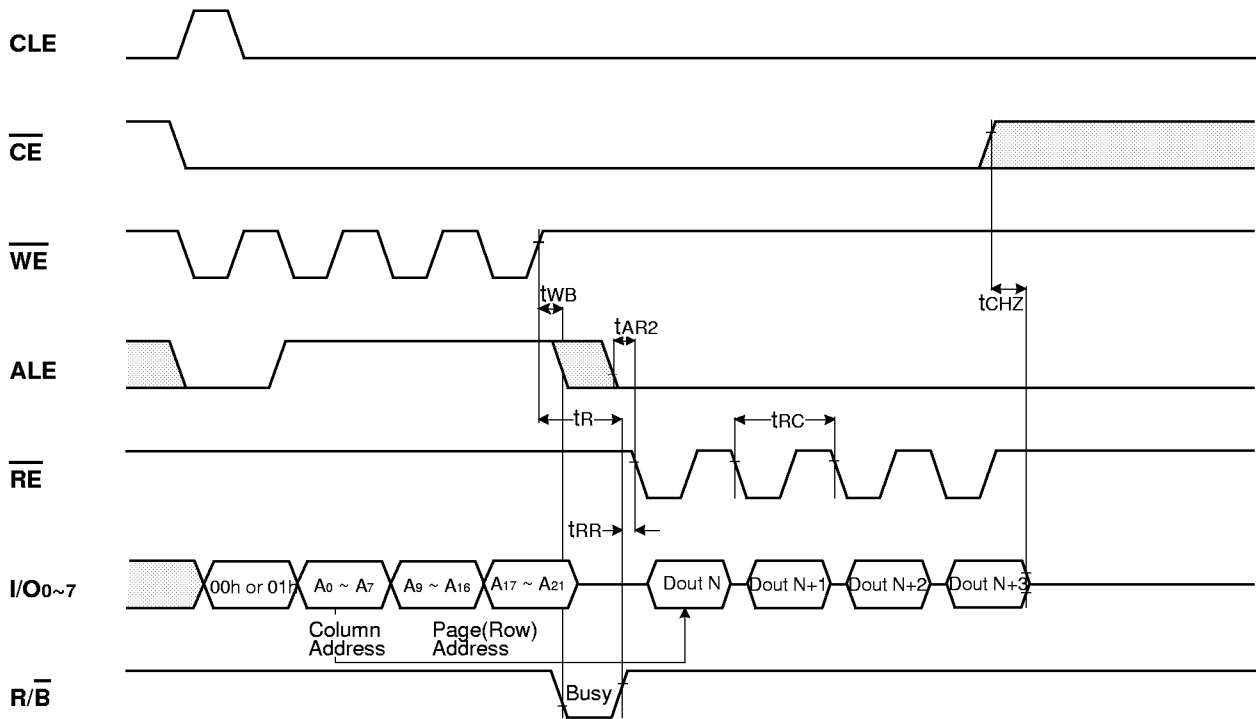
READ2 OPERATION (READ ONE PAGE)
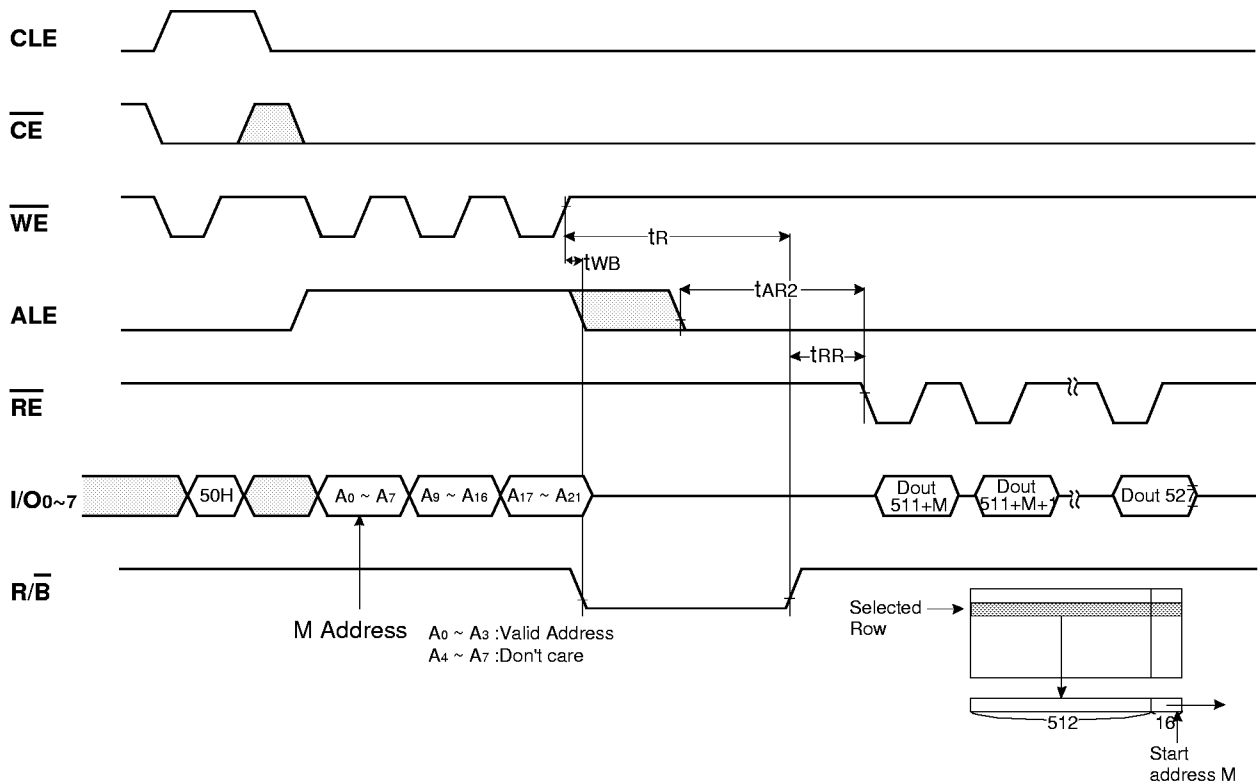
SEQUENTIAL ROW READ OPERATION

CLE

CE

WE

ALE

RE

I/O0~7   00H   A0 ~ A7   A9 ~ A16   A17 ~ A2?   Dout N   Dout N+1   Dout N+2   Dout 527   Dout 0   Dout 1   Dout 2   Dout 527

R/B   Busy   Busy

M

M+1

N   Output   Output

PAGE PROGRAM OPERATION

CLE

CE

tWC   tWC   tWC

WE

tWB   tPROG

ALE

RE

I/O0~7   80H   A0 ~ A7   A9 ~ A16   A17 ~ A2?   Din N   Din N+1   Din 527   10H   70H   I/O0

Sequential Data   Column   Page(Row)   1 up to 528 Byte Data   Program   Read Status
Input Command   Address   Address   Sequential Input   Command   Command

R/B

I/O0=0 Successful Program
I/O0=1 Error in Program

BLOCK ERASE OPERATION (ERASE ONE BLOCK)

CLE					
CE					
WE					
ALE					
RE					
I/O$_{0\sim7}$	60H	A$_9$ ~ A$_{16}$ A$_{17}$ ~ A$_{21}$	D0H	70H	I/O$_0$
R/B					

Block Address

Busy

Auto Block Erase Setup Command   Erase Command   Read Status Command   I/O0=0 Successful Erase
                                                                                            I/O0=1 Error in Erase
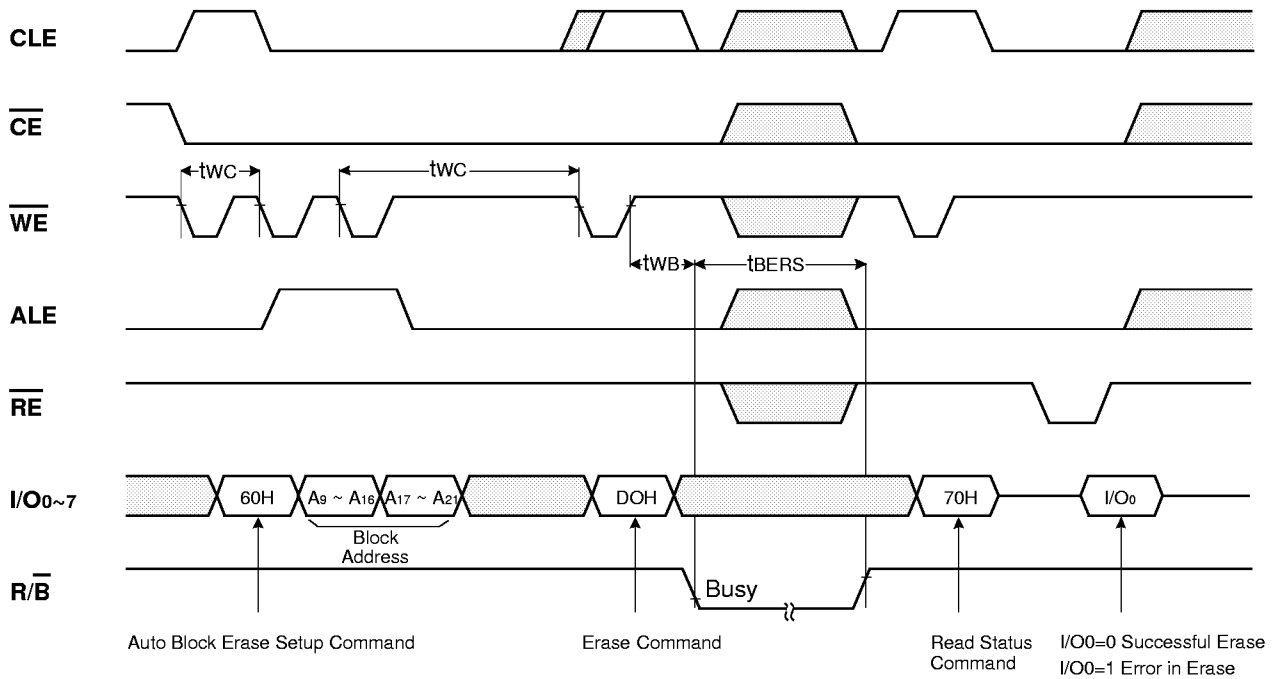
SUSPEND & RESUME OPERATION DURING BLOCK ERASE

CLE							
CE							
WE							
ALE							
RE							
I/O$_{0\sim7}$	60H		D0H	B0H	D0H	70H	I/O$_0$
R/B							

Block Address

A$_9$ ~ A$_{16}$ A$_{17}$ ~ A$_{21}$

Busy

Auto Block Erase Setup Command   Suspend   Program/Read Function are Acceptable   Resume   I/O0=0 Successful Erase
                                                                                                                        I/O0=1 Error in Erase
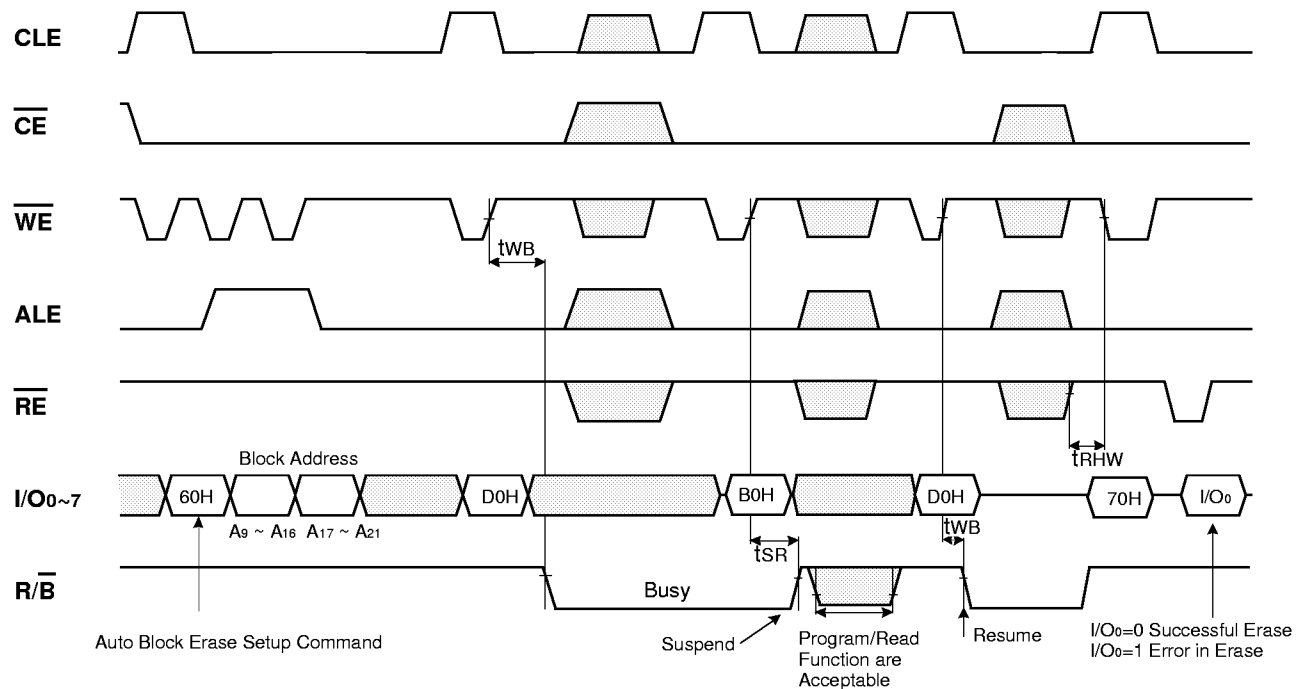
MANUFACTURE & DEVICE ID READ OPERATION

CLE

$\overline{CE}$

$\overline{WE}$

ALE

$\overline{RE}$

t_{REAID}

I/O$_{0\sim7}$ 90H   00H   ECH   Note*

Read ID Command   Maker Code   Device Code

Note* KM29V32000 : E3H
       KM29N32000 : E5H
   KM29W32000 : E3H
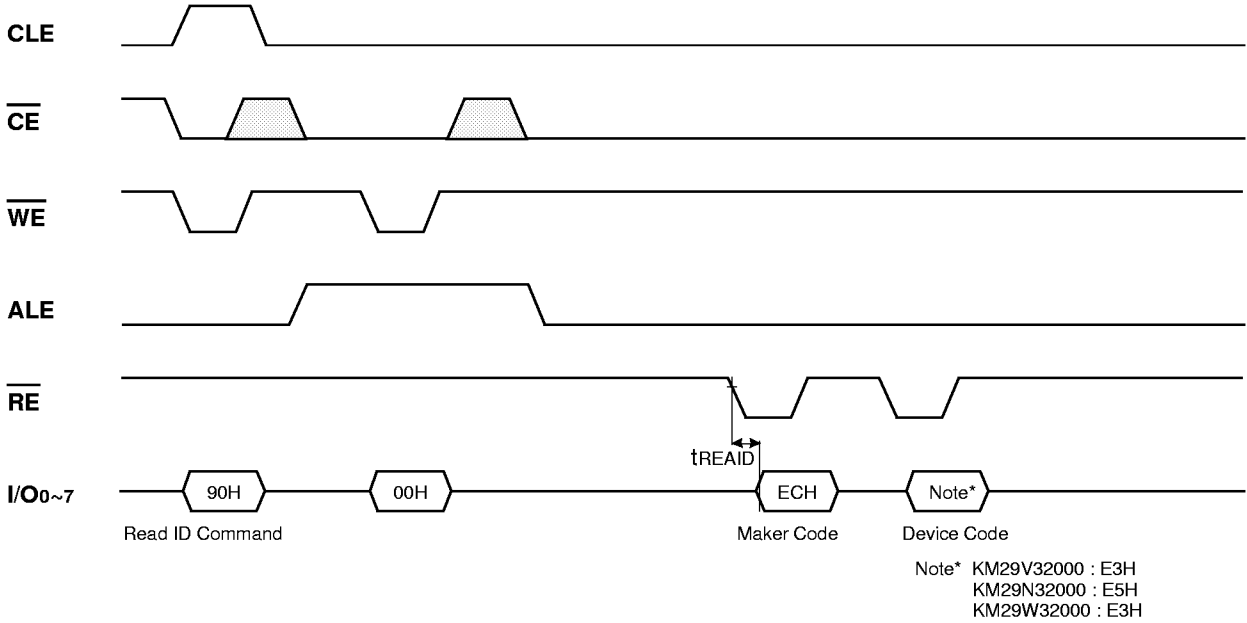
DEVICE OPERATION

PAGE READ

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00H to the command   register along with three address cycles. Once the command is latched, it does not need to be written for the following page read o peration. Three types of operations are available : random read, serial page read and sequential read.

The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 10 μs(t_R). The CPU can detect the completion of this data transfer(t_R) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing $\overline{RE}$ with $\overline{CE}$ staying low. High to low transitions of the $\overline{RE}$ clock output the data starting from the selected column address up to the last column address(column 511 or 527 depending on state of $\overline{SE}$ pin).

After the data of last column address is clocked out, the next page is automatically selected for sequential read.
Waiting 10μs again allows for reading of the selected page. The sequential read operation is terminated by bringing $\overline{CE}$ high. The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read2 command with $\overline{SE}$ pin low. Addresses A_0 to A_3 set the starting address of the spare area while addresses A_4 to A_7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command(00H/01H) is needed to move the pointer back to the main area. Figures 3 thru 6 show typical sequence and timings for each read operation.

Figure 3. Read1 Operation
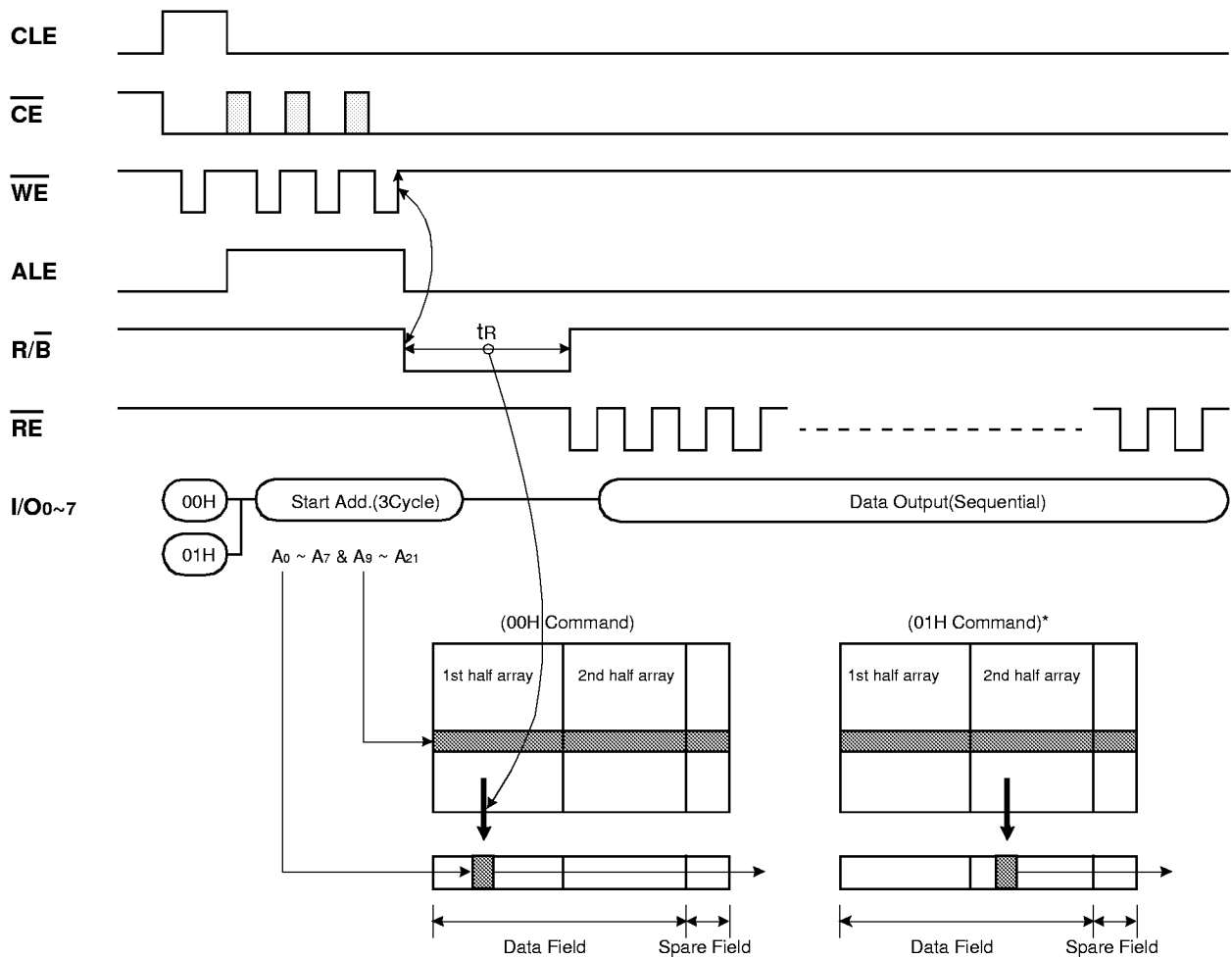
* After data access on 2nd half array by 01H command, the start pointer is automatically moved to 1st half array (00H) at next   cycle.
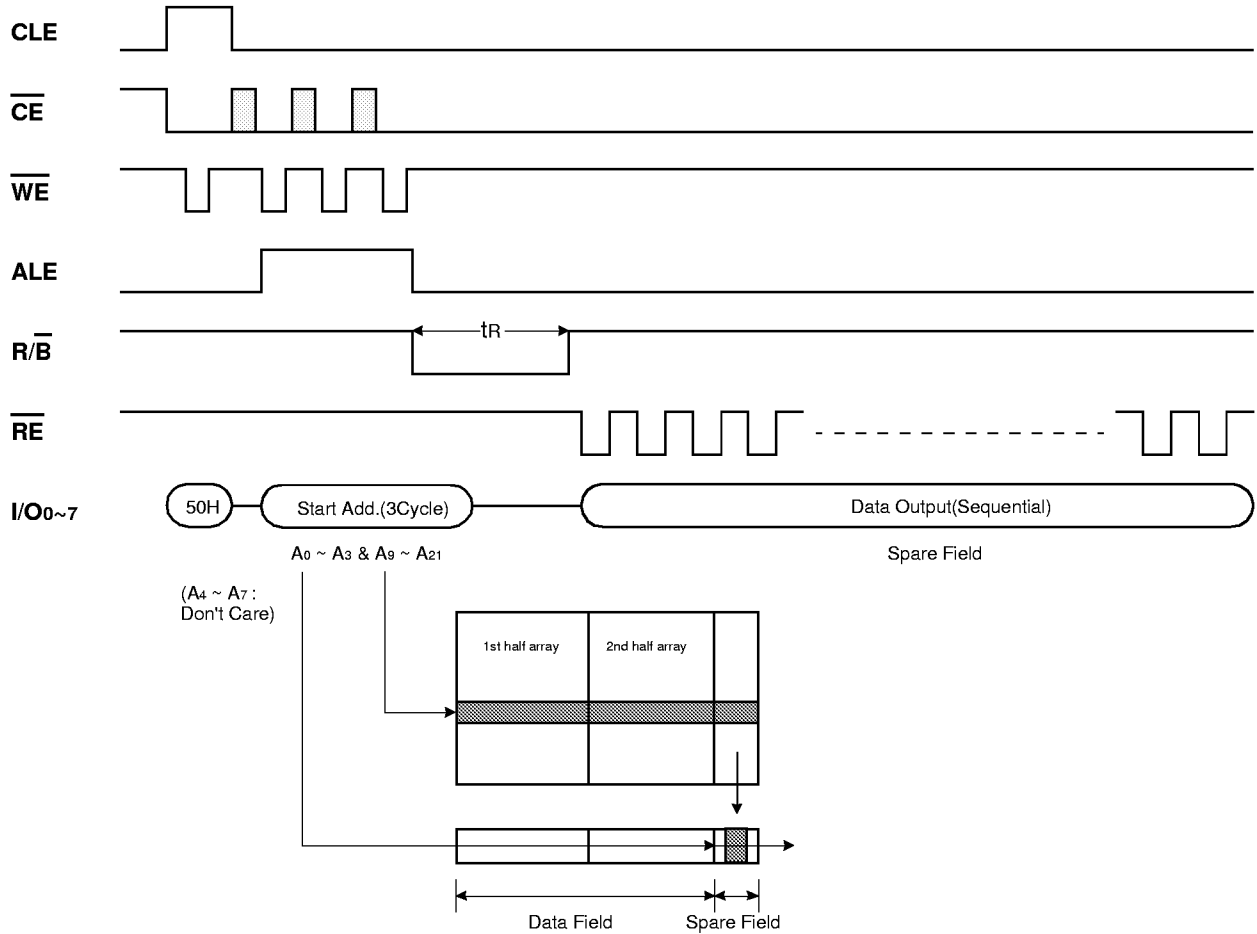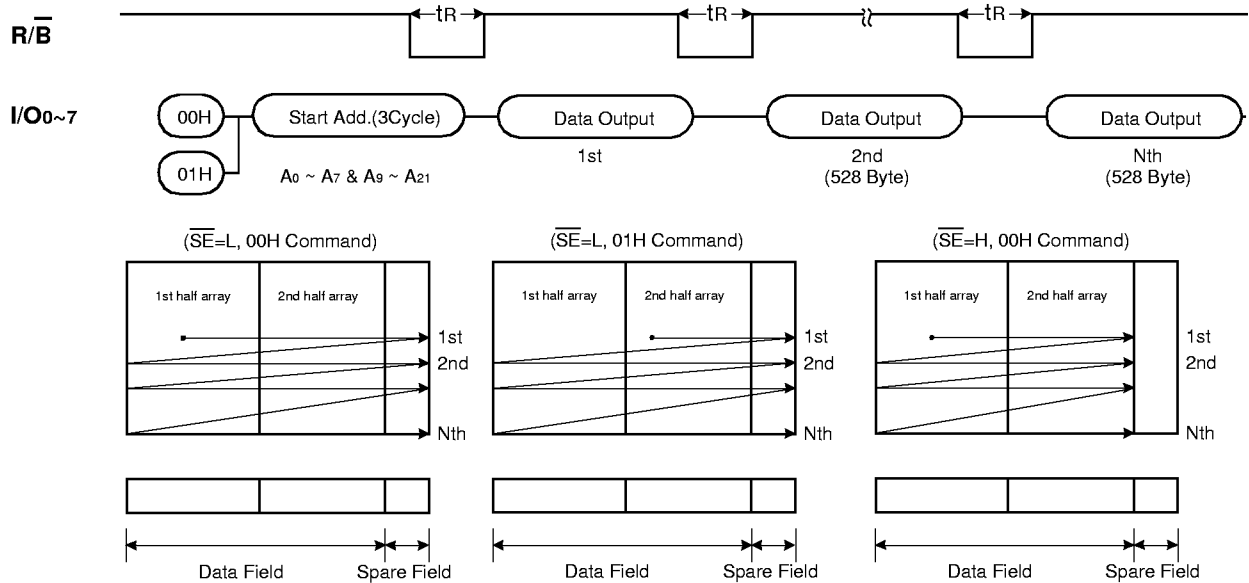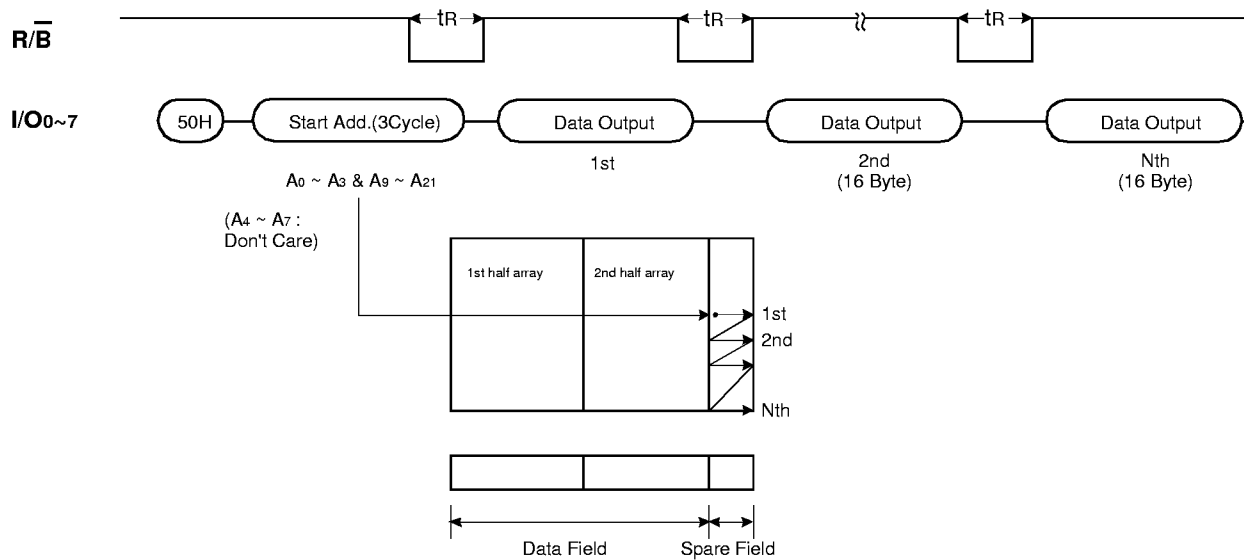
Figure 4. Read2 Operation

CLE

CE

WE

ALE

R/B̄ ◄─ tR ─►

RE

I/O0~7 (50H)─(Start Add.(3Cycle))──────(Data Output(Sequential))

A0 ~ A3 & A9 ~ A21   Spare Field

(A4 ~ A7 :
Don't Care)

1st half array   2nd half array

Data Field   Spare Field

Figure 5. Sequential Row Read1 Operation

R/B̄ ◄─tR─►   ◄─tR─►   ◄─tR─►

I/O0~7 (00H)─(Start Add.(3Cycle))─(Data Output)───(Data Output)───(Data Output)
        (01H)   A0 ~ A7 & A9 ~ A21   1st   2nd   Nth
                                                          (528 Byte)   (528 Byte)

(SĒ=L, 00H Command)   (SĒ=L, 01H Command)   (SĒ=H, 00H Command)

1st half array 2nd half array   1st half array 2nd half array   1st half array 2nd half array
                            1st   1st   1st
                            2nd   2nd   2nd
                            Nth   Nth   Nth

Data Field   Spare Field   Data Field   Spare Field   Data Field   Spare Field

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Figure 6. Sequential Read2 Operation ($\overline{SE}$=fixed low)

R/$\overline{B}$

I/O$_0$~7

PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed ten. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page registe r, followed by a nonvolatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array. About the pointer operation, please refer to the attached technical notes.The serial data loadin g period begins by inputting the Serial Data Input command(80H), followed by the three cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded.

The Page Program confirm command(10H) initiates the programming process. Writing 10H alone without perviously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and t imings necessary for program and verify, thereby freeing the CPU for other tasks. Once the program process starts, the Read Status Regi s-ter command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The CPU can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O $_6$) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O $_0$) may be checked(Figure 7). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The comm and register remains in Read Status command mode until another valid command is written to the command register.

Figure 7. Program & Read Status Operation

R/$\overline{B}$

I/O$_0$~7

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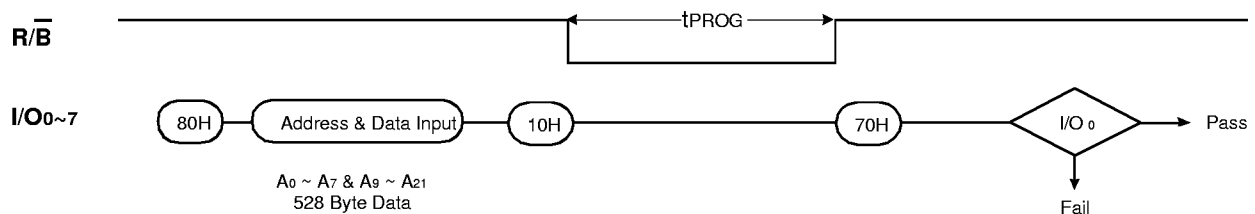
BLOCK ERASE

The Erase operation can erase on a block(8K Byte) basis. Block address loading is accomplished in two cycles initiated by an Era se Setup command(60H). Only address A$_{13}$ to A$_{21}$ is valid while A$_9$ to A$_{12}$ is ignored. The addresses of the block to be erased to FFH. The Erase Confirm command(D0H) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution ensures that memory contents are not accidentally erased due to external noise condition s. At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase, erase-verify and pulse repetition where required. If an erase operation error is detected, the internal verify is halted and erase operation is termina ted. When the erase operation is completed, the Write Status Bit(I/O $_0$) may be checked.
Figure 8 details the sequence.

Figure 8. Block Erase Operation
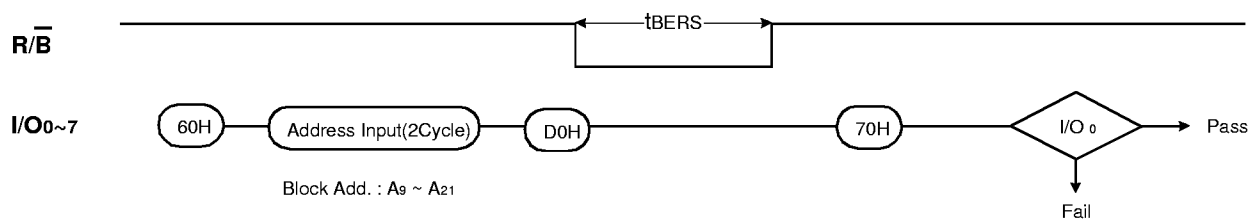
ERASE SUSPEND/ERASE RESUME

The Erase Suspend allows interruption during any erase operation in order to read or program data to or from another block of memory. Once an erase process begins, writing the Erase Suspend command (B0H) to the command register suspends the internal erase process, and the R/$\overline{B}$ signal return to "1". Erase Suspend Status bit will be also set to "1" when the Status Register is read. At this time, blocks other than the suspended block can be read or programmed. The Status Register and R/ $\overline{B}$ operation will function as usual. After the Erase Resume command is written to it, the erase process is restarted from the beginning of the erasing period. The Erase Suspend Status bit and R/ $\overline{B}$ will return to "0". Refer to Figure 9 for operation sequence.

Figure 9. Erase Suspend & Erase Resume Operation

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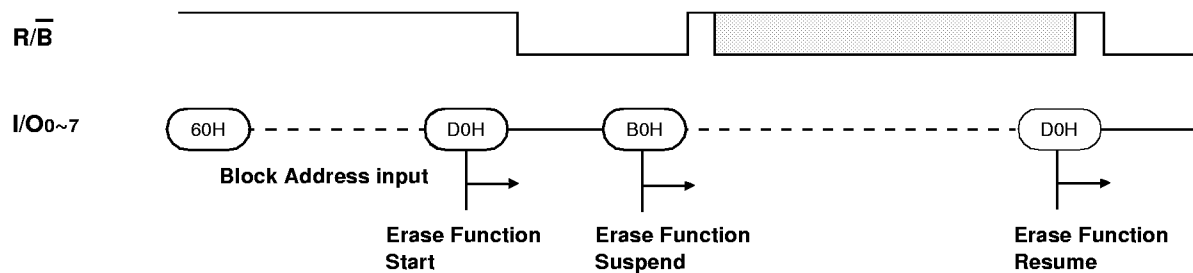
READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is complete, and whether the program or erase operation completed successfully. After writing 70H command to the command register, a read cycle outputs the contents of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/ $\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random r ead cycle, a read command(00H or 50H) should be given before sequential page read cycle.

### Table2. Status Register Definition

SR	Status	Definition
I/O$_0$	Program / Erase	"0" : Successful Program / Erase
		"1" : Error in Program / Erase
I/O$_1$	Reserved for Future Use	"0"
I/O$_2$		"0"
I/O$_3$		"0"
I/O$_4$		"0"
I/O$_5$	Erase Suspend	"0" : Erase in Progress / Completed
		"1" : Suspended
I/O$_6$	Device Operation	"0" : Busy "1" : Ready
I/O$_7$	Write Protect	"0" : Protected "1" : Not Protected

READ ID

The device contains a product identification mode, initiated by writing 90H to the command register, followed by an address inpu t of 00H. Two read cycles sequentially output the manufacture code(ECH), and the device code (Note*) respectively. The command reg- ister remains in Read ID mode until further commands are issued to it. Figure 9 shows the operation sequence.

Note* KM29V32000 : E3H
         KM29N32000 : E5H
         KM29W32000 : E3H

Figure 9. Read ID Operation

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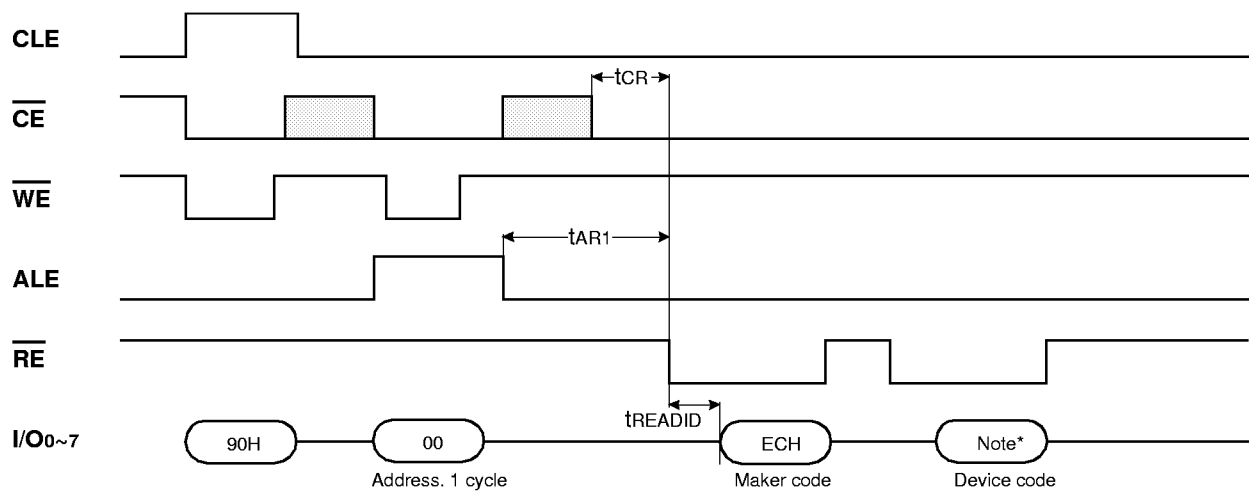
RESET

The device offers a reset feature, executed by writing FFH to the command register. When the device is in Busy state during rand om read, program or erase modes, the reset operation will abort these operation. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. Internal address registers are cleared to "0"s and data regist ers to "1"s. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0H when $\overline{WP}$ is high. Refer to table 3 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted to by the command register. The R/$\overline{B}$ pin transitions to low for t RST after the Reset command is written. Reset command is not necessary for normal operation. Refer to Figure 10 below.
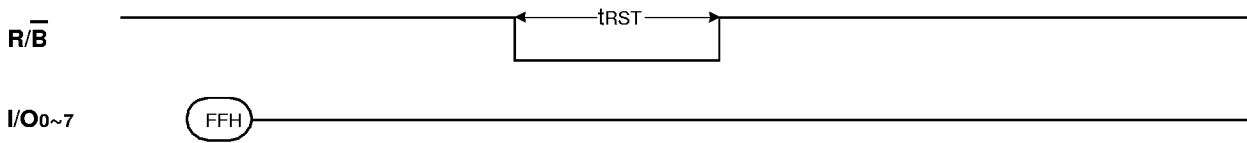
Figure 10. RESET Operation

$R/\overline{B}$

I/O0~7   FFH

Table3. Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

DATA PROTECTION

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage dete ctor disables all functions whenever Vcc is below about 2V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V IL during power-up and power-down as shown in Figure 8. The two step command sequence for program/erase provides additional software protection.

**Figure 8. AC Waveforms for Power Transition**

Vcc

High

$\overline{WP}$
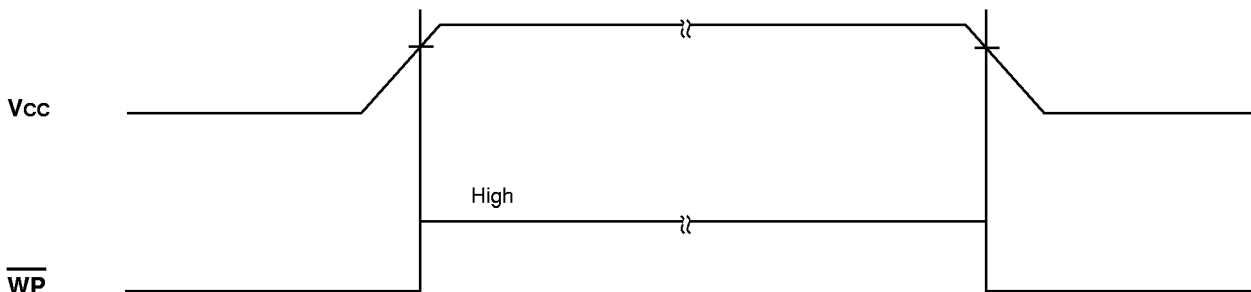
READY/BUSY

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is begin after address loading. It returns to high when the internal controller has finished the operation.   The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. An appropriate pull-up resister is required for proper operation and the value may be calculated by following equation.

Vcc

R/$\overline{B}$
open drain output

GND
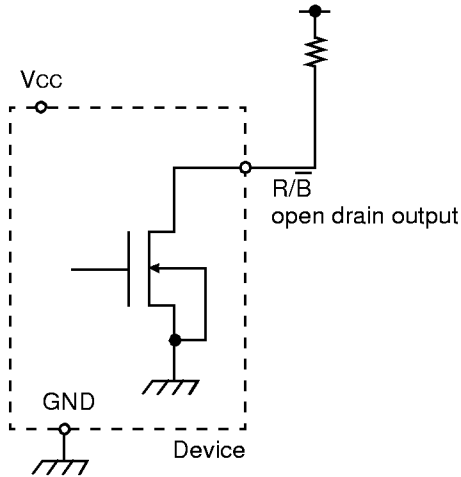
Device

$$Rp = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \sum I_L} = \frac{Note^*}{8mA + \sum I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Note* KM29V32000 : 3.2V
       KM29N32000 : 5.1V
       KM29W32000 : 5.1V When Vcc=3.6~5.5V
                    3.2V When Vcc=2.7~3.6V

PACKAGE DIMENSIONS

44(40) LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II)

44(40) - TSOP2 - 400F   Unit :mm/Inch

#44(40)   #23(21)

#1   #22(20)

11.76 ± 0.20 / 0.463 ± 0.008

$0\sim8°$

$\dfrac{0.25}{0.010}$ TYP

$\dfrac{0.45\sim0.75}{0.018\sim0.030}$

$\dfrac{10.16}{0.400}$

$\dfrac{0.50}{0.020}$

$\dfrac{0.15^{+0.10}_{-0.05}}{0.006^{+0.004}_{-0.002}}$

$\dfrac{18.81}{0.741}$ Max.

$\dfrac{18.41\pm0.10}{0.725\pm0.004}$

$\dfrac{1.00\pm0.10}{0.039\pm0.004}$

$\dfrac{1.20}{0.047}$ Max.

$\left(\dfrac{0.805}{0.032}\right)$

$\dfrac{0.35\pm0.10}{0.014\pm0.004}$

$\dfrac{0.80}{0.0315}$

$\dfrac{0.05}{0.002}$ Min.

$\dfrac{0.10}{0.004}$ MAX