

32 BIT COMPARATOR LSI FOR MOTION CONTROL APPLICATIONS

FEATURES

- Interfaces directly with an 8 bit microprocessor
- Has a wide application range
- Reduces the number of counter IC's
- 40 pin plastic dual in-line package
- +5V single power supply
- 32 bit Command Counter
- 24 bit Error Counter
- Adjustable output rate to the D/A
- 20 MHz clock

APPLICATIONS

- Motion control systems
- Robotics
- Drawing machines
- Electrical discharge machines
- Special machinery

SPECIFICATIONS

Clock rate:	20MHz (max.)
Output pattern:	16 bits (max.)
Output update period:	Adjustable (5 ~ 300 clock periods)
Input voltage:	+5V ± 5%
Power dissipation:	750mW
Operating temperature:	-20°C to +75°C/-4°F to +167°F
Storage temperature:	-55°C to +125°C/-67°F to +257°F

DESCRIPTION

The KM3702BD is a position control CMOS LSI which monitors the difference between the COMMAND (\pm COM) and FEEDBACK (\pm FB) pulses, under the conditions by the CPU, and uses this position error to output a bit pattern to the D/A Converter.

The KM3702BD uses a single +5V power supply and

has TTL-compatible input and output. Its system clock (CP) frequently is 20MHz maximum.

COMMAND and FEEDBACK pulses can be input either synchronously or asynchronously. If synchronous input is selected, the pulse count increases for every clock pulse while the input pulse line is held low. For asynchronous input, the pulse count increases only on a falling edge of the input pulse. Quadrature rotary encoder pulses can be input directly to the KM3702BD's \pm FB inputs and the multiplier for the quadrature encoder can be set to x1, x2 and x4.

To keep track of the input pulses, there are two binary up/down counters:

COMMAND COUNTER-----32 bits, cumulative value of +COM, -COM input pulses.

ERROR COUNTER-----24 bits, difference between +COM and -COM input and +FB and -FB input pulses.

Data can be preset into these counters, and the counter values can be read out by the host CPU.

Commands from the CPU can be used to create a ZERO CLAMP condition or floating state condition on the outputs to the D/A Converter. ZERO CLAMP means that for the purposes of the D/A Converter, the output pattern will be zero even though the ERROR COUNTER continues for function normally.

To produce the output pattern for the D/A Converter, the output lines ($\overline{O0} \sim \overline{O15}$) are updated with the value in the ERROR COUNTER at an update rate specified by the host CPU. The number of bits output to the D/A Converter can be selected in the range of 8 to 16 bits. The D/A update rate can be set to from 5 to 300 clock cycles. The default D/A update rate is set to 20 clock cycles.

The actual value of the ERROR COUNTER can be read by the host CPU. In addition, the status of the COMMAND COUNTER and the ERROR COUNTER can be read by the host CPU, according to the following definitions:

KM3702BD

SATURATION ZONE----- Selection of number of bits for D/A Converter output pattern (8 ~ 16 Bits).
* +SAT, -SAT flags.

COMMAND COUNTER---- Zero and over flow detection.
*CR ZERO flag.
*CR OVER flag.

POSITION ZONE----- Detection of nearly ZERO.
*POS flag.

These status flags (except for NEG flags) can be set up to interrupt the host CPU, using INT output line.

ALARM ZONE----- ERROR COUNTER Over range (Alarm Detection).
*ALM flag.

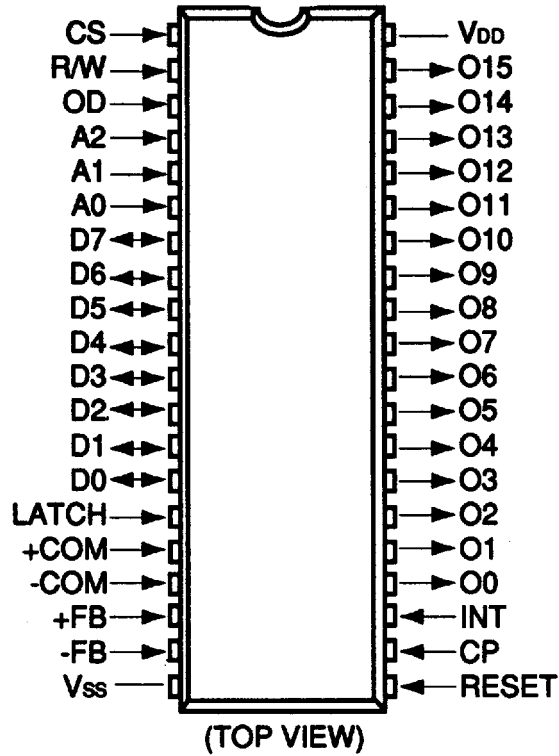
The KM3702BD comes in a 40 pin, DIP (Dual In-Line Package), plastic package.

ERROR COUNTER----- Negative and zero detection.
*NEG flag,
*ER ZERO flag.

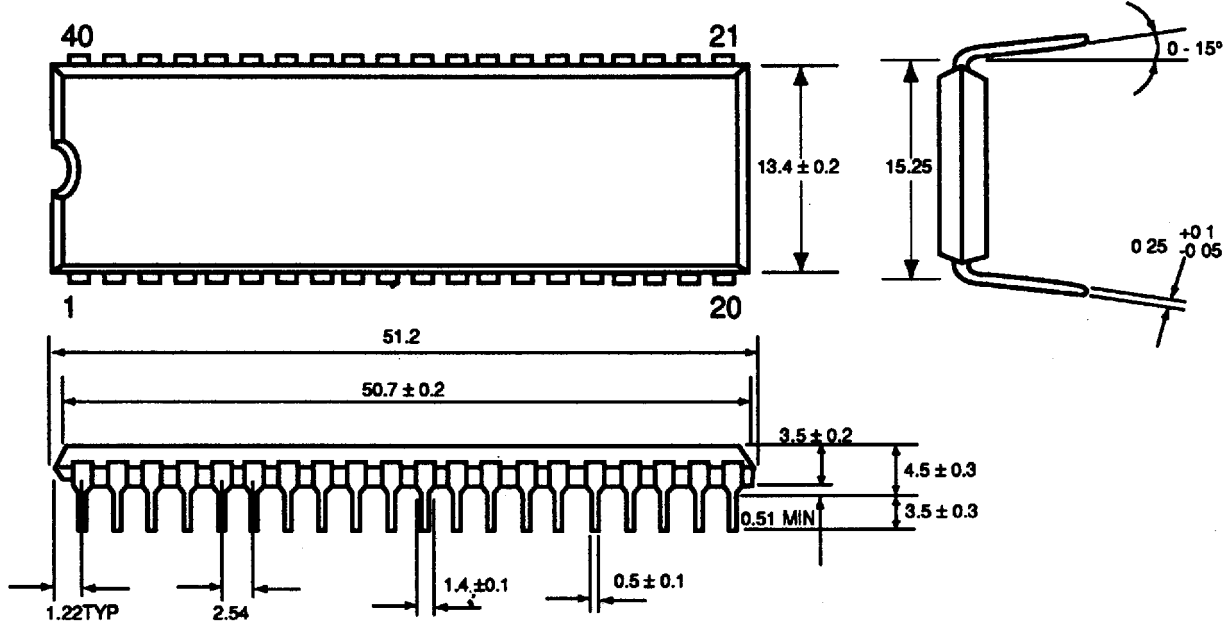
PIN FUNCTION

Signal Name	Symbol	Pin No.	I/O	Remarks
Power Supply	VDD	40	≡	+5V 5%
Power Supply	VSS	20	≡	GROUND
CHIP SELECT	CS	1	I	Device Select Signal.
WRITE	RW	2	I	WRITE Command Signal.
OUTPUT DISABLE	OD	3	I	READ Command Signal.
ADDRESS	A0 ~ A2	4 ~ 6	I	ADDRESS Select Signal.
DATA	D0 ~ D7	7 ~ 14	I/O	READ/WRITE Data. Tri-state I/O.
ERROR COUNTER LATCH	LATCH	15	I	If active for more than 3 clock pulses, the value of the ERROR COUNTER is transferred to the DATA REGISTER.
+COMMAND	+COM	16	I	+COMMAND Pulse.
-COMMAND	-COM	17	I	-COMMAND Pulse.
+FEEDBACK	+FB	18	I	+FEEDBACK Pulse.
-FEEDBACK	-FB	19	I	-FEEDBACK Pulse.
RESET	RESET	21	I	RESET Signal.
CLOCK PULSE	CP	22	I	Basic Clock.
INTERRUPT	INT	23	O	CPU Interrupr signal; COMMAND COUNTER and ERROR COUNTER values are within the range set by the CPU.
OUTPUT for D/A Converter	O0 ~ O15	24 ~ 39	O	Output Pattern for D/A Converter.

PIN ASSIGNMENT



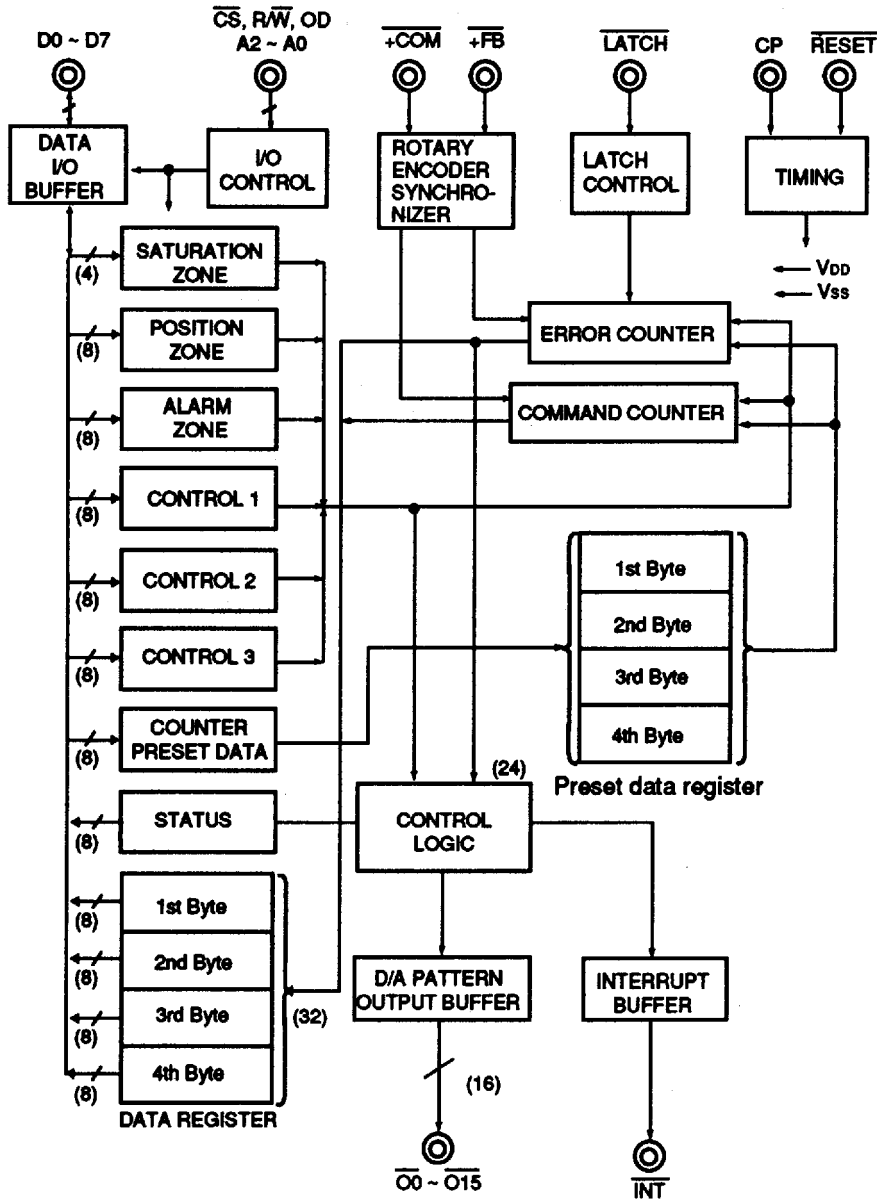
DIMENSIONS (40-Pin Plastic Dual In-Line Package)



Unit: mm

KM3702BD

BLOCK DIAGRAM



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Toko America, Inc.
 1250 Feehanville Drive, Mt. Prospect, IL 60056
 Tel: (708) 297-0070 Fax: (708) 699-7864

TOKO SALES LOCATIONS

TOKO America, Inc.
 1250 Feehanville Drive
 Mount Prospect, IL 60056
 Tel: (708) 297-0070
 Fax: (708) 699-7864

TOKO America, Inc.
 2480 North First Street
 Suite 260
 San Jose, CA 95131
 Tel: (408) 432-8281
 Fax: (408) 943-9790

TOKO America, Inc.
 107 Mill Plain Road
 Danbury, CT 06811
 Tel: (203) 748-6871
 Fax: (203) 797-1223

TOKO America, Inc.
 201 Finney Drive
 Huntsville, AL 35824
 Tel: (205) 772-8904
 Fax: (205) 772-8955