2M x 16Bit x 2 Bank Synchronous DRAM

FEATURES

- JEDEC standard 3.3V Power Supply.
- LVTTL/SSTL_3 (Class II) compatible with multiplexed address.
- Dual banks operation.
- MRS cycle with address key programs.
  - -. CAS Latency
    - . LVTTL : 1, 2 & 3
    - . SSTL : 3 & 4
  - -. Burst Length (1, 2, 4, 8 & Full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst Read Single-bit Write Operation.
- DQM for masking
- Auto & Self Refresh.
- 64ms Refresh Period. (4K cycle)

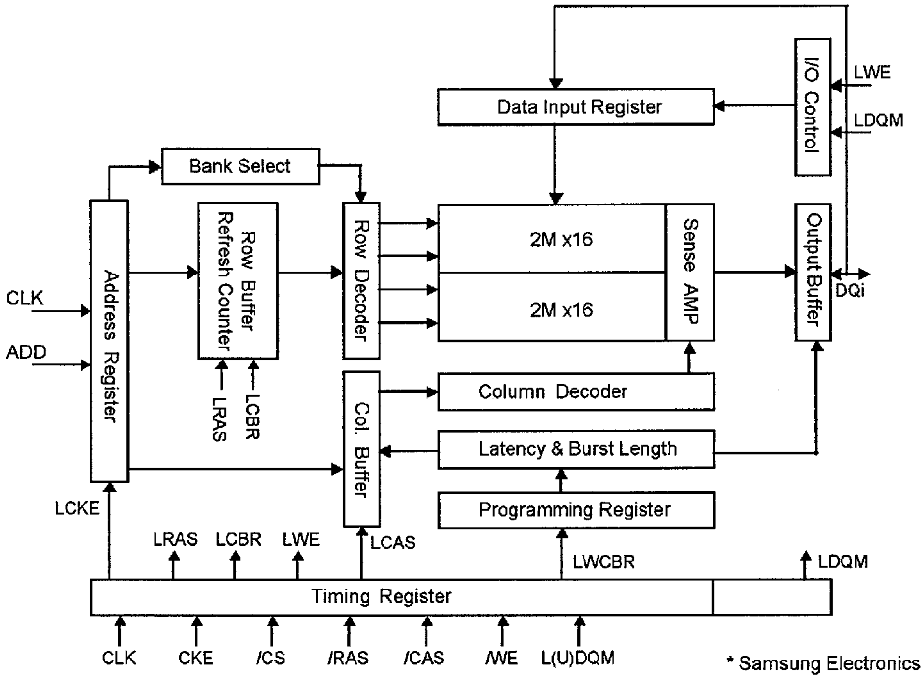
GENERAL DESCRIPTION

The KM416S4020A/KM416S4021A are 67,108,864 bits synchronous high data rate Dynamic RAM organized as 2 x 2,097,152 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length, and programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part NO.	Max Freq.	Interface	Package
KM416S40321AT-G/F7	143MHz	SSTL_3 (Class II)	54 TSOP (II)
KM416S4021AT-G/F8	125MHz		
KM416S4021AT-G/F9	111MHz		
KM416S4020AT-G/F9	111MHz	LVTTL	
KM416S4020AT-G/F10	100MHz		
KM416S4020AT-G/F12	83MHz		

FUNCTIONAL BLOCK DIAGRAM



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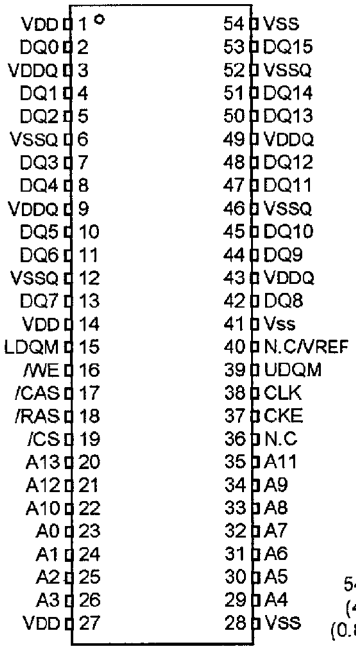
PIN CONFIGURATION (TOP VIEW)



54 PIN TSOP (II)
(400mil x 875mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
/CS	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE, and DQM
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A12	*Address*	Row / Column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA7
A13	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
/RAS	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with /RAS low. Enables row access & precharge.
/CAS	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with /CAS low. Enables column access.
/WE	*Write Enable*	Enables write operation and row precharge. Latches data in starting from /CAS, /WE active.
L(U)DQM	*Data Input/Output Mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ 15	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
VDD /VSS	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
VDDQ /VSSQ	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
VREF	*Reference Voltage*	Reference voltage for inputs, used at SSTL interface only.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	Ios	50	mA

Note : Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS (LVTTL)

Recommended operating conditions (Voltages referenced to Vss = 0V, T_A =0 to 70 °C)

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Supply voltage	V_{DD},V_{DDQ}	3.0	3.3	3.6	V	
Intput logic high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	Note 1
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} =-2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	Note 2
Output leakage current	I_{OL}	-5	-	5	uA	Note 3

Note : 1. V_{IL}(min.) = -1.5V AC (pulse width$\leq$ 5 ns)
2. Any input 0V$\leq$ V_{IN} $\leq$$V_{DD}$ + 0.3V, all other pins are not under test = 0V.
3. Dout is disabled, 0$\leq$$V_{OUT}$$\leq$ V_{DD}.

DC OPERATING CONDITIONS (SSTL)

Recommended operating conditions (Voltages referenced to Vss = 0V, T_A = 0 to 70 °C)

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Device Supply voltage	V_{DD}	V_{DDQ}	-	3.6	V	1
Output Supply voltage	V_{DDQ}	3.0	3.3	3.6	V	1
Input reference voltage	V_{REF}	1.3	1.5	1.7	V	2, 3
Termination voltage	Vtt	V_{REF}-0.05	V_{REF}	V_{REF}+0.05	V	4
Intput logic high voltage	V_{IH}	V_{REF}+0.2	-	V_{DDQ}+0.3	V	
Input logic low voltage	V_{IL}	-0.3	-	V_{REF}-0.2	V	
Output logic high voltage	V_{OH}	Vtt+0.8	-	-	V	I_{OH} =-16mA
Output logic low voltage	V_{OL}	-	-	Vtt-0.8	V	I_{OL} = 16mA
Input leakage current	I_{IL}	-5	-	5	uA	
Output leakage current	I_{OL}	-5	-	5	uA	

Note : 1. Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
2. Typically the value of V_{REF} is expected to be about 0.45* V_{DDQ} of the transmitting device.
V_{REF} is expected to track variations in V_{DDQ}.
3. Peak to peak AC noise on V_{REF} may not exceed 2% V_{REF}(DC).
4. Vtt of transmitting device must track V_{REF} of receiving device.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{13})	C_{IN1}	-	4	pF
Input capacitance (CLK, CKE, /CS, /RAS, /CAS, /WE & L(U)DQM)	C_{IN2}	-	4	pF
Data input/output capacitance (DQ_0 ~ DQ_{15})	C_{OUT}	-	5	pF

DC CHARACTERISTICS

(Recommended Operating Conditions Unless Otherwise Noted, T_A = 0 to 70 °C)

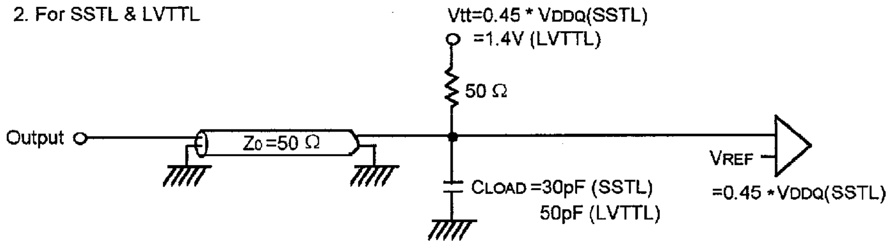
Parameter	Symbol	Test Condition	CAS Latency	Version						Unit	Note
				SSTL			LVTTL				
				-7	-8	-9	-9	-10	-12		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \ge t_{RC}$(min) I_{OL} = 0 mA	4	100	90	85	-	-	-	mA	1
			3	90	80	75	90	80	75		
			1, 2	-	-	-	90	80	75		
Precharge Standby Current in Power-down mode	I_{CC2}P	CKE ≤ V_{IL}(max), t_{CC} =15ns		3						mA	
	I_{CC2}PS	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		2							
Precharge Standby Current in Non power-down mode	I_{CC2}N	CKE ≥ V_{IH}(min), /CS ≥ V_{IH}(min), t_{CC} =15ns Input signals are changed one time during 30ns		25						mA	
	I_{CC2}NS	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		8							
Active Standby Current in power-down mode	I_{CC3}P	CKE ≤ V_{IL}(max), t_{CC} =15ns	4	20			-			mA	
			3	3			3				
			1, 2	-			3				
	I_{CC3}PS	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		2							
Active Standby Current in Non power-down mode (One Bank Active)	I_{CC3}N	CKE ≥ V_{IH}(min), /CS ≥ V_{IH}(min), t_{CC} =15ns Input signals are changed one time during 30ns	4	45			-			mA	
			3	30			30				
			1, 2	-			30				
	I_{CC3}NS	CKE ≥ V_{IH}(min), CLK ≥ V_{IL}(max), t_{CC} = ∞ Input signals are stable		15							
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst All Banks activated t_{CCD}=t_{CCD}(min)	4	180	170	160	-	-	-	mA	1, 2
			3	130	120	110	130	120	110		
			2	-	-	-	95	85	80		
			1	-	-	-	70	60	55		
Refresh Current	I_{CC5}	$t_{RC} \ge t_{RC}$(min)		120	115	110	120	115	110	mA	3
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		2						mA	4
				250						uA	5

Note : 1. Measured with outputs open.
2. Assumes minimum column address update cycle t_{CCD}(min)
3. Refresh period is 64ms.
4. KM416S4020AT-G**
KM416S4021AT-G**
5. KM416S4020AT-F**
KM416S4021AT-F**

AC OPERATING TEST CONDITIONS (VDD = 3.3V± 0.3V, TA = 0 to 70 °C)

Parameter	Value	Unit	Note
Input reference voltage	0.45 * VDDQ	V	1
Input signal maximum peak swing	2.0	V	1
Input signal minimum slew rate	1.0	V / ns	1
Input levels (Vih/Vil)	VREF+0.4/VREF-0.4(SSTL), 2.4/0.4(LVTTL)	V	2
Input timing measurement reference level	VREF(SSTL), 1.4(LVTTL)	V	2
Output timing measurement reference level	Vtt(SSTL), 1.4(LVTTL)	V	2
Output load condition	See Fig. 1		2

Note : 1. For SSTL only
2. For SSTL & LVTTL



(Fig. 1) Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version						Unit	Note
		SSTL			LVTTL				
		-7	-8	-9	-9	-10	-12		
Row active to Row active delay	tRRD(min)	18	20	24	18	20	24	ns	1
/RAS to /CAS delay	tRCD(min)	24	26	30	24	26	30	ns	1
Row precharge time	tRP(min)	24	26	30	24	26	30	ns	1
Row active time	tRAS(min)	54	60	65	54	60	65	ns	1
	tRAS(max)	100						us	
Row cycle time	tRC(min)	90	96	100	90	96	100	ns	1
Last data in to new col. address delay	tCDL(min)	1						CLK	2
Last data in to Row precharge	tRDL(min)	1						CLK	2
Last data in to burst stop	tBDL(min)	1						CLK	2
Col. address to col. address delay	tCCD(min)	1						CLK	3
Number of valid output data	CAS Latency= 4	3			-			ea	4
	CAS Latency= 3	2			2				
	CAS Latency= 2	-			1				
	CAS Latency= 1	-			0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of Row precharge interrupt, Auto precharge and Read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	SSTL						LVTTL						Unit	Note
			-7		-8		-9		-9		-10		-12			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=4	tCC	7	11	8	11	9	11	-	-	-	-	-	-	ns	1
	CAS latency=3		9	1000	10	1000	12	1000	9	1000	10	1000	12	1000		
	CAS latency=2		-		-		-		13		14		15			
	CAS latency=1		-		-		-		26		28		30			
CLK to valid output delay	CAS latency=4	tSAC		5		5.5		6		-		-		-	ns	1, 2
	CAS latency=3			7		7.5		8.5		7		7.5		8.5		
	CAS latency=2			-		-		-		8		8.5		9		
	CAS latency=1			-		-		-		21		23		25		
Output data hold time	CAS latency=4	tOH	2		2		2		-		-		-		ns	2
	CAS latency=3		2.5		2.5		2.5		2.5		2.5		2.5			
	CAS latency=2		-		-		-		3		3		3			
	CAS latency=1		-		-		-		5		5		5			
CLK high pulse width		tCH	2.5		3		3		3		3.5		4		ns	3
CLK low pulse width		tCL	2.5		3		3		3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		2		2.5		3		ns	3
Input hold time		tSH	0.5		1		1		0.5		1		1		ns	3
CLK to output in low-Z		tSLZ	1		1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=4	tSHZ		6		7		8		-		-		-	ns	
	CAS latency=3			7		8		9		7		8		8		
	CAS latency=2			-		-		-		10		11		11		
	CAS latency=1			-		-		-		16		18		18		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.

Frequency vs. AC Parameter relationship Table

(Below tables refer to the LVTTL interface only.)

KM416S4020AT-9 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	54ns	24ns	18ns	24ns	9ns	9ns	9ns
111MHz (9.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	9	6	3	2	3	1	1	1
83MHz (12.0ns)	3	8	5	2	2	2	1	1	1
75MHz (13.3ns)	2	7	5	2	2	2	1	1	1
66MHz (15.2ns)	2	6	4	2	2	2	1	1	1

KM416S4020AT-10 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		96ns	60ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	10	6	3	2	3	1	1	1
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	2	2	2	1	1	1
66MHz (15.2ns)	2	7	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1

KM416S4020AT-12 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		100ns	65ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	9	6	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	3	2	3	1	1	1
66MHz (15.2ns)	2	7	5	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	4	2	2	2	1	1	1

Frequency vs. AC Parameter relationship Table

(Below tables refer to the SSTL interface only.)

KM416S4021AT-7 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	54ns	24ns	18ns	24ns	7ns	7ns	7ns
143MHz (7.0ns)	4	13	8	4	3	4	1	1	1
133MHz (7.5ns)	4	12	8	4	3	4	1	1	1
100MHz (10.0ns)	3	9	6	3	2	3	1	1	1
83MHz (12.0ns)	3	8	5	2	2	2	1	1	1
75MHz (13.3ns)	3	7	5	2	2	2	1	1	1

KM416S4021AT-8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		96ns	60ns	26ns	20ns	26ns	8ns	8ns	8ns
125MHz (8.0ns)	4	12	8	4	3	4	1	1	1
100MHz (10.0ns)	3	10	6	3	2	3	1	1	1
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	2	2	2	1	1	1
66MHz (15.2ns)	3	7	4	2	2	2	1	1	1

KM416S4021AT-9 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		100ns	65ns	30ns	24ns	30ns	9ns	9ns	9ns
111MHz (9.0ns)	4	12	8	4	3	4	1	1	1
100MHz (10.0ns)	4	10	7	3	3	3	1	1	1
83MHz (12.0ns)	3	9	6	3	2	3	1	1	1
75MHz (13.3ns)	3	8	5	3	2	3	1	1	1
66MHz (15.2ns)	3	7	5	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	A13	A10	A12 - A11 A9 - A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Address			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address $(A_0 \sim A_7)$	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address $(A_0 \sim A_7)$	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note :

1. OP Code : Operand Code
   $A_0 \sim A_{13}$: Program keys.(@MRS)
2. MRS can be issued only at both banks precharge state.
   A new command can be issued after 2 clock cycles of MRS
3. Auto refresh functions as same as CBR refresh of DRAM..
   The automatical precharge without Row precharge command is meant by "Auto".
   Auto/Self refresh can be issued only at both banks precharge state.
4. A_{13} : Bank select address.
   If "Low" at read, write, Row active and precharge, bank A is selected.
   If "High" at read, write, Row active and precharge, bank B is selected.
   If A_{10} is "High" at Row precharge, A_{11} is ignored and both banks are selected.
5. During burst read or write with auto precharge,
   new read/write command cannot be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK
   masks the data-in at the very CLK (Write DQM latency is 0)
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	A_{11} ~A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Function	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		
	(Note 2)	(Note 1)									

Test Mode		
A_8	A_7	Type
0	0	Mode Register Set
0	1	Reserved
1	0	Reserved
1	1	Reserved

Write Burst Length	
A_9	Length
0	Burst
1	Single Bit

CAS Latency			
A_6	A_5	A_4	Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Type	
A_3	Type
0	Sequential
1	Interleave

Burst Length				
A_2	A_1	A_0	BT = 0	BT = 1
0	0	0	1	Reserved
0	0	1	2	Reserved
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	256(Full)	Reserved

POWER UP SEQUENCE

1. Apply power and start clock, Attempt to maintain CKE="H", DQM="H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us
3. Issue precharge commands for all banks of the devices.
4. Issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

cf.) Power up sequence 4 & 5 are regardless of the order.

The device is now ready for normal operation.

NOTE : 1. If A_9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. RFU (Reserved for future use) should stay "0" during MRS cycle.

BURST SEQUENCE (BURST LENGTH = 4)

Initial address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operation are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high, all inputs are assumed to be in valid state (low or high) for the duration of set-up and hold time around positive edge of the clock for proper functionality and I_{CC} specifications.

CLOCK ENABLE (CKE)

The clock enable(CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. when both banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "t_{PDE}" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

BANK SELECT (A_{11})

This SDRAM is organized as two independent banks of 524,288 words x 16 bits memory arrays. The A_{11} input is latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. When A_{11} is asserted low, bank A is selected. When A_{11} is asserted high, bank B is selected. The bank select A_{11} is latched at bank activate, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A_0~A_{10})

The 19 address bits required to decode the 524,288 word locations are multiplexed into 11 address input pins (A_0~A_{10}). The 11 bit row address is latched along with $\overline{RAS}$ and A_{11} during bank activate command. The 8 bit column address is latched along with $\overline{CAS}$, $\overline{WE}$ and A_{11} during read or write command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, the SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

POWER-UP

The following sequence is recommended for POWER UP

1. Power must be applied to either CKE and DQM inputs to pull them high and the other pins are NOP codition at the inputs before or along with V_{DD}(and V_{DDQ}) supply. The clock signal must also be asserted at the same time
2. After V_{DD} reaches the desired voltage, a minimum pause of 200 microseconds is required with inputs in NOP condition.
3. Both banks must be precharged now.
4. Perform a minimum of 8 Auto refresh cycles to stabilize the internal circuitry.
5. Perform a MODE REGISTER SET cycle to program the CAS latency, burst length and burst type as the default value of mode register is undefined.
   At the end of two clock cycles from the mode register set cycle, the device is ready for operation.
   when the above sequence is used for Power-up, all the outputs will be in high impedance state. The high impedance of outputs is not guaranteed in any other power-up sequence.
   cf) Sequence 4 & 5 can be changed.

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, addressing mode, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A_0~A_{10} and A_{11} in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as both banks are in the idle state.

The mode register is divided into various fields depending on functionality. The burst length field uses A_0~A_2, addressing mode uses A_3, CAS latency (read latency from column address) uses A_4~A_6, A_7, A_8, A_{10} and A_{11} are used for vendor specific options or test mode. And the write burst length is programmed using A_9. A_7,A_8,A_{10} and A_{11} must be set to low for normal SDRAM operation.

Refer to table for specific codes for various burst length, addressing modes and CAS latencies.

DEVICE OPERATIONS (Continued)

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address a row access is initiated. The read or write operation can occur after a time delay of t_{RCD}(min) from the time of bank activation.
t_{RCD}(min) is an internal timing parameter of SDRAM therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD}(min) with cycle time of the clock and then rounding off the result to the next higher integer. The SDRAM has two internal banks on the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of both banks immediately. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before the other bank can be sensed reliably. t_{RRD}(min) specifies the minimum time required between activating different banks. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS}(min). Every SDRAM bank activate command must satisfy t_{RAS}(min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS}(max). The number of cycles for both t_{RAS}(min) and t_{RAS}(max) can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{CAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least t_{RCD}(min) before the burst read command is issued. The first output appears CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command, and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing may not have been completed yet. The writing can to complete to burst length. The burst write can be terminated by issuing a burst read and DQM for blocking data inputs or burst write in the same or the other active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and precharging the bank "t_{RDL}" after the last data input to be written into the active row. See DQM OPERATION also.

DQM OPERATION

The DQM is used to mask input and output operations. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in the read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock, therefore the masking occurs for a complete cycle. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required. DQM is also used for device selection, byte selection and bus control in a memory system. LDQM controls DQ0 to DQ7, UDQM controls DQ8 to DQ15. Please refer to DQM timing diagrams also.

PRECHARGE

The precharge operation is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A_{10} with valid A_{11} of the bank to be precharged. The precharge command can be asserted anytime after t_{RAS}(min) is satisfied from the bank activate command in the desired bank. "t_{RP}" is defined as the minimum time required to precharge a bank. The minimum number of clock cycles required to complete row precharge is calculated by dividing "t_{RP}" with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS}(max). Therefore, each bank has to be precharged within t_{RAS}(max) from the bank activate command. At the end of precharge, the bank enters the Idle state and is ready to be activated again.

DEVICE OPERATIONS (Continued)

Entry to Power Down, Auto refresh, Self refresh and Mode register Set etc. is possible only when both banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy t_{RAS}(min) and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A_{10}. If burst read or burst write command is issued with low on A_{10}, the bank is left active until a new command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

BOTH BANK PRECHARGE

Both banks can be precharged at the same time by using precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A_{10} after both banks have satisfied t_{RAS}(min) requirement, performs precharge on both banks. At the end of t_{RP} after performing precharge all, both banks are in idle state.

AUTO REFRESH

The storage cells of SDRAM need to be refreshed every 32ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by "t_{RC}(min)". The minimum number of clock cycles required can be calculated by dividing "t_{RC}" with clock cycle time and then rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. Both banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6 μs or a burst of 2048 auto refresh cycles once in 32ms.

SELF REFRESH

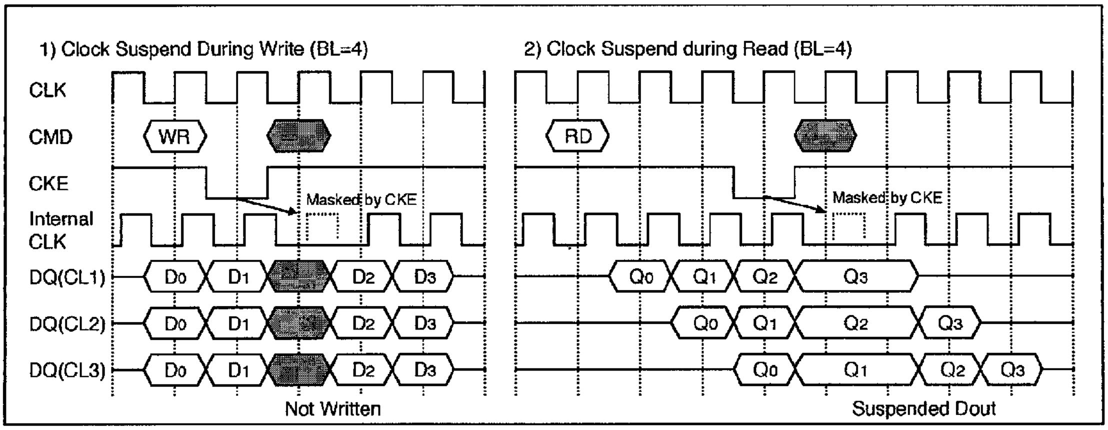
The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption.

The self refresh mode is entered from both bank idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the self refresh.

The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of "t_{RC}" before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 2048 auto refresh cycles immediately after exiting self refresh.

BASIC FEATURE AND FUNCTION DESCRIPTIONS

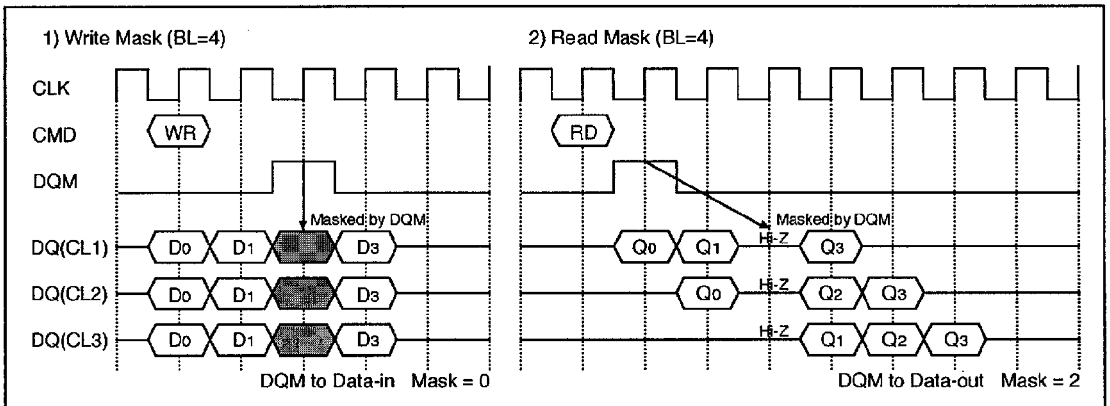
1. CLOCK Suspend



1) Clock Suspend During Write (BL=4)

2) Clock Suspend during Read (BL=4)

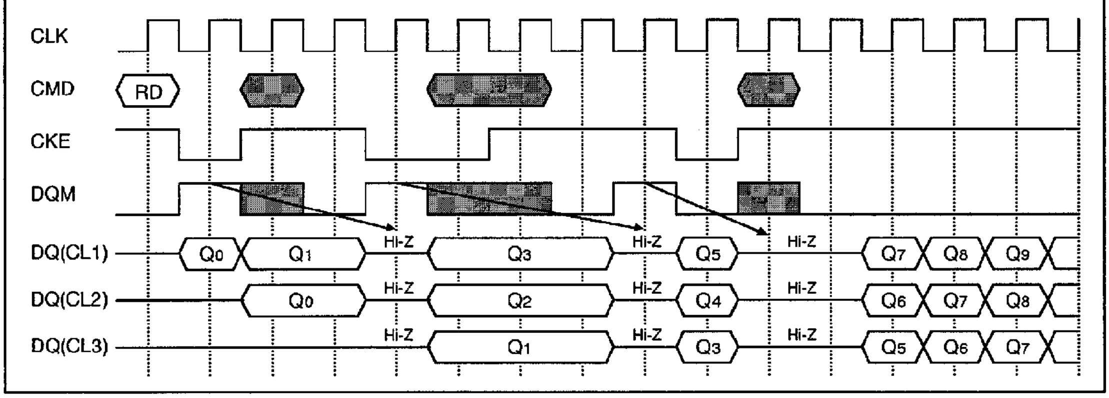
2. DQM Operation



1) Write Mask (BL=4)

2) Read Mask (BL=4)

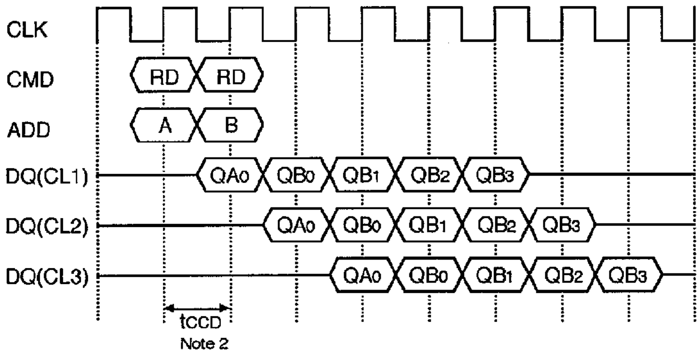
3) DQM with Clock Suspend (Full Page Read)Note 2



Note : 1. CKE to CLK disable/enable = 1 clock.
2 . DQM makes data out Hi-Z after 2 clocks which should masked by CKE "L".
3. DQM mask both data-in and data-out.

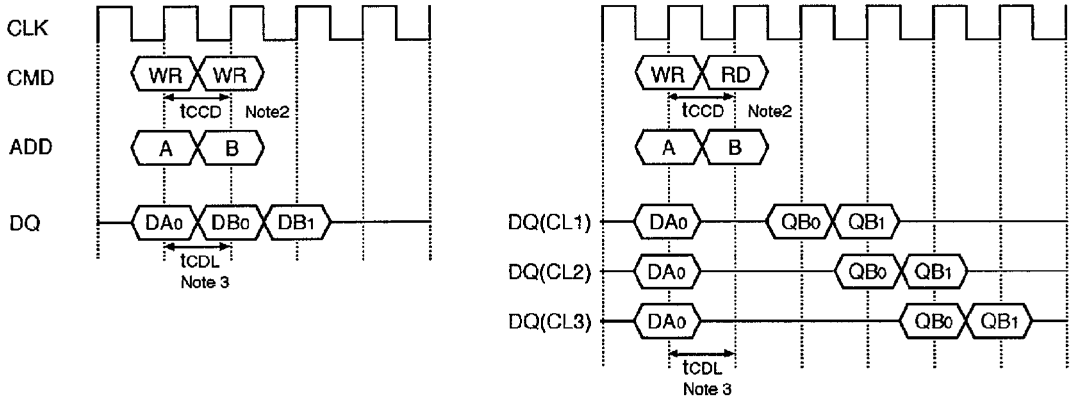
3. $\overline{\text{CAS}}$ Interrupt (I)

1) Read interrupted by Read (BL=4) Note 1



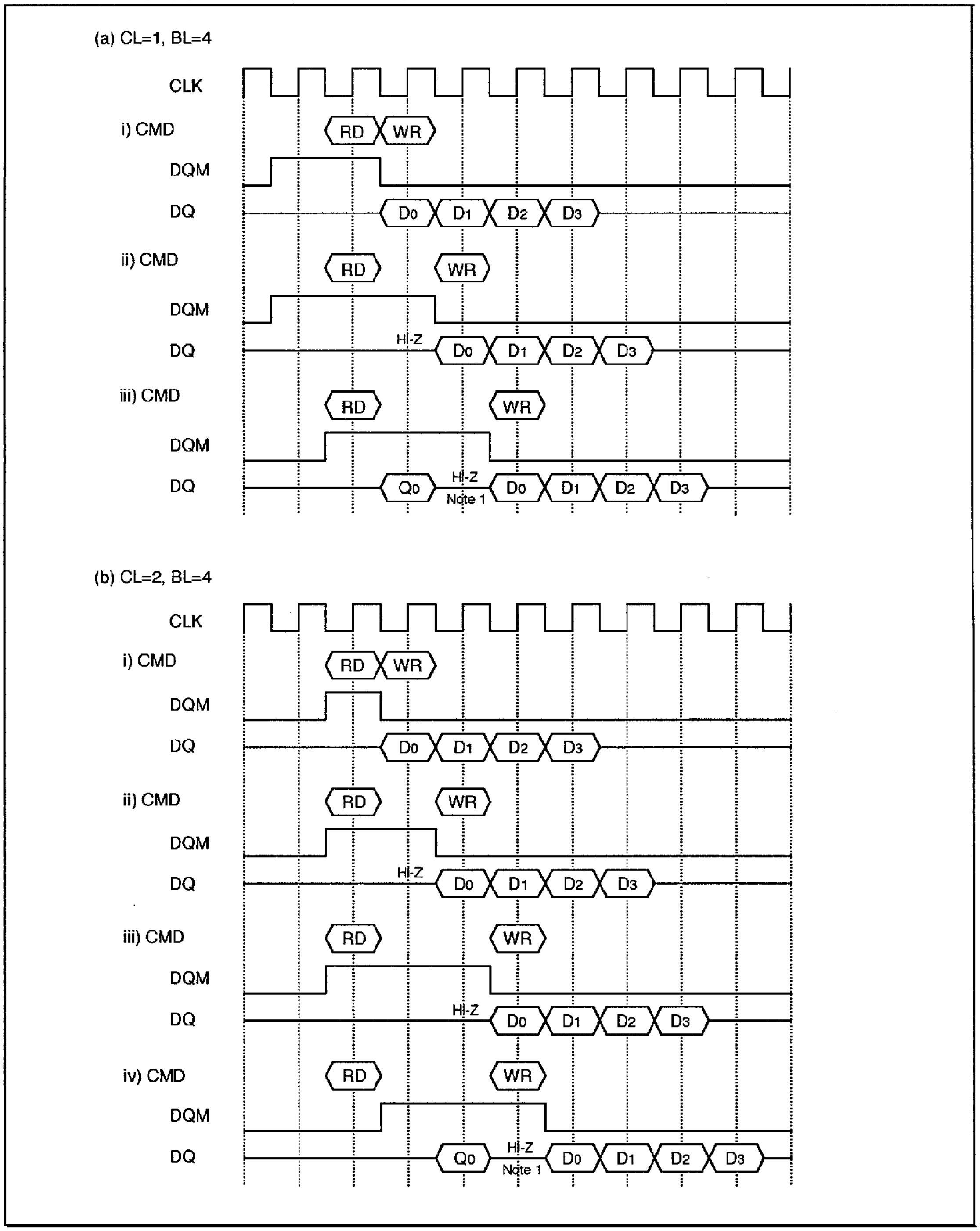
2) Write interrupted by Write (BL=2)

3) Write interrupted by Read (BL=2)



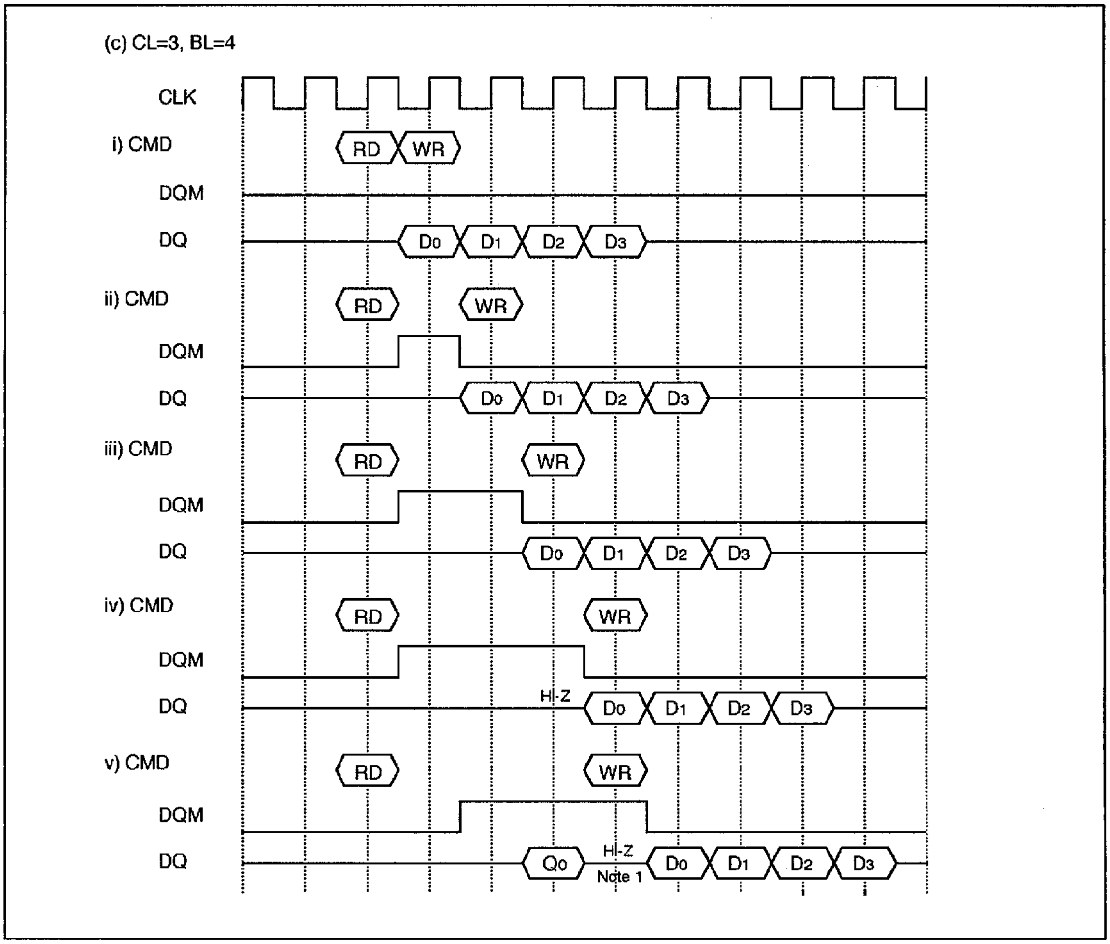
Note :
1. By "Interrupt", It is meant to stop burst read/write by external command before the end of burst.
   By "$\overline{\text{CAS}}$ Interrupt", to stop burst read/write by $\overline{\text{CAS}}$ access ; read and write.
2. t_{CCD} : $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ delay. (=1CLK)
3. t_{CDL} : Last data in to new column address delay. (=1CLK)

4. $\overline{CAS}$ Interrupt (II) : Read Interrupted by Write & DQM

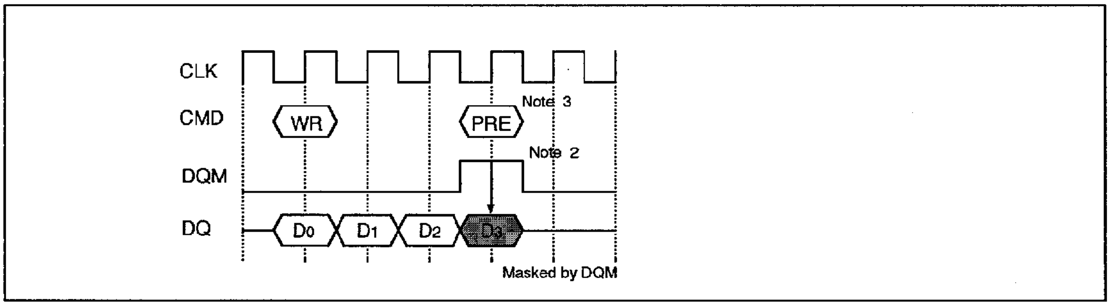


Note : 1. To prevent bus contension, there should be at least one gap between data in and data out.

(Continued)



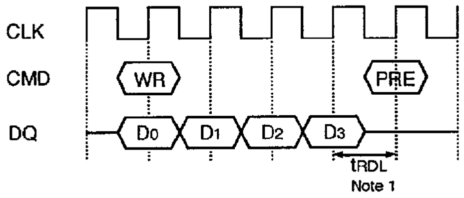
5. Write Interrupted by Precharge & DQM



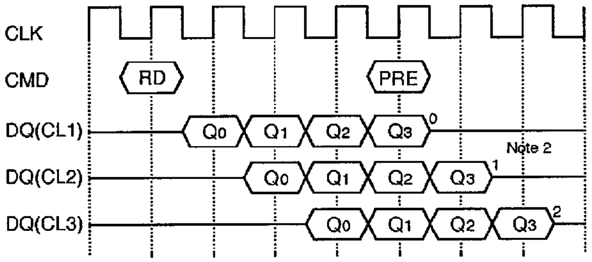
Note :
1. To prevent bus contension, DQM should be issued which makes at least one gap between data in and data out.
2. To inhibit invalid write, DQM should be issued.
3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of dual bank operation.

6. Precharge

1) Normal Write (BL=4)

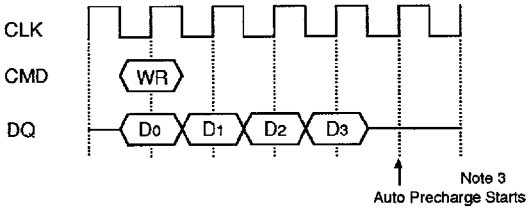


2) Normal Read (BL=4)

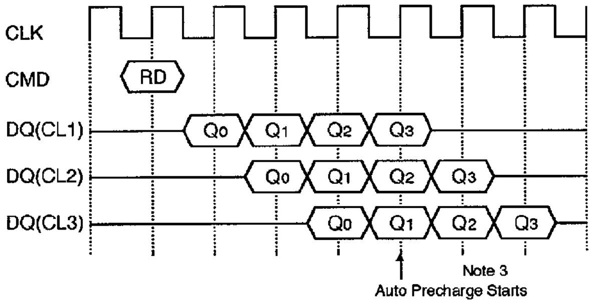


7. Auto Precharge

1) Normal Write (BL=4)



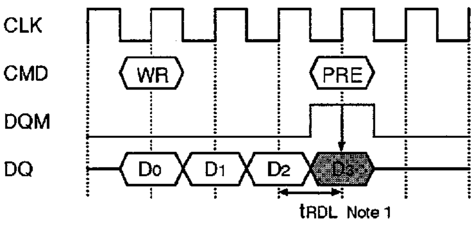
2) Normal Read (BL=4)



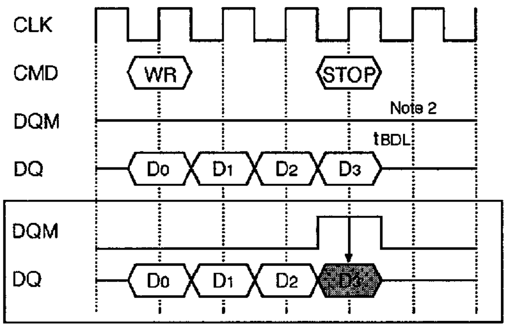
Note :
1. tRDL : Last Data in to Row Precharge Delay
2. Number of valid output data after Row Precharge : 0,1,2, for CAS Latency=1,2,3, respectively.
3. The row active command of the precharge bank can be issued after tRP from this point.
   The new read/write command of another activated bank can be issued from this point.
   At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.

8. Burst Stop & Interrupted by Precharge

1) Normal Write (BL=4)

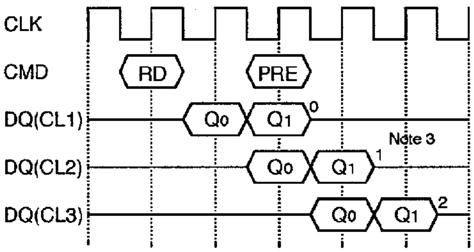


2) Write Burst Stop (BL=8)

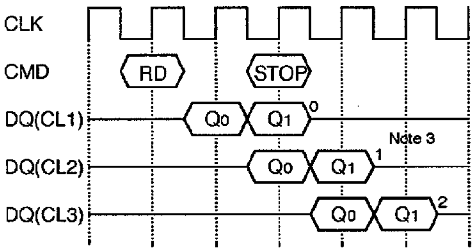


If t_{BDL}=1 is required, DQM should be issued with Burst Stop.

3) Read Interrupted by Precharge (BL=4)

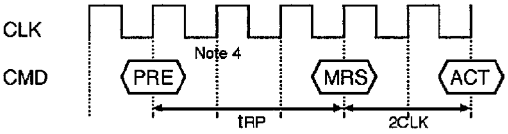


4) Read Burst Stop (BL=4)



9. MRS

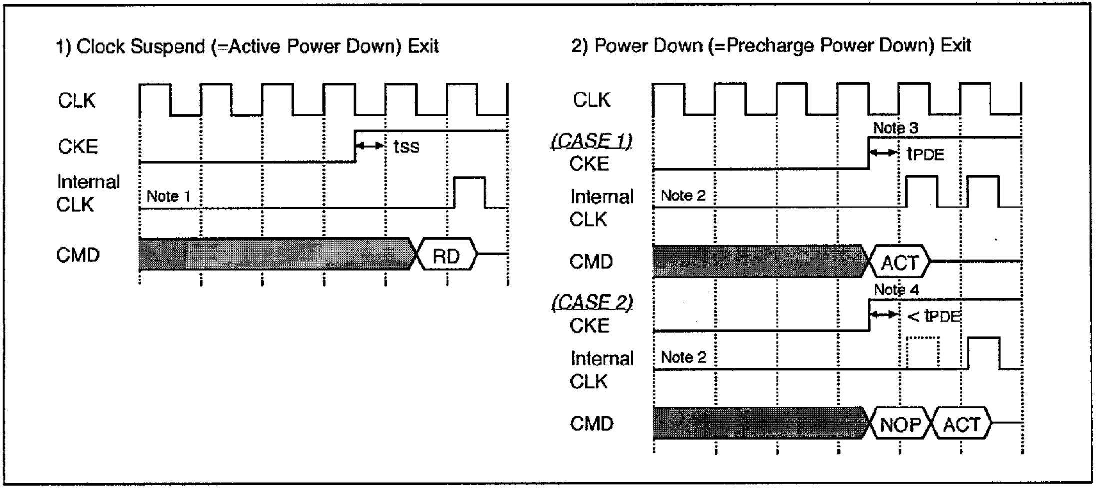
1) Mode Register Set



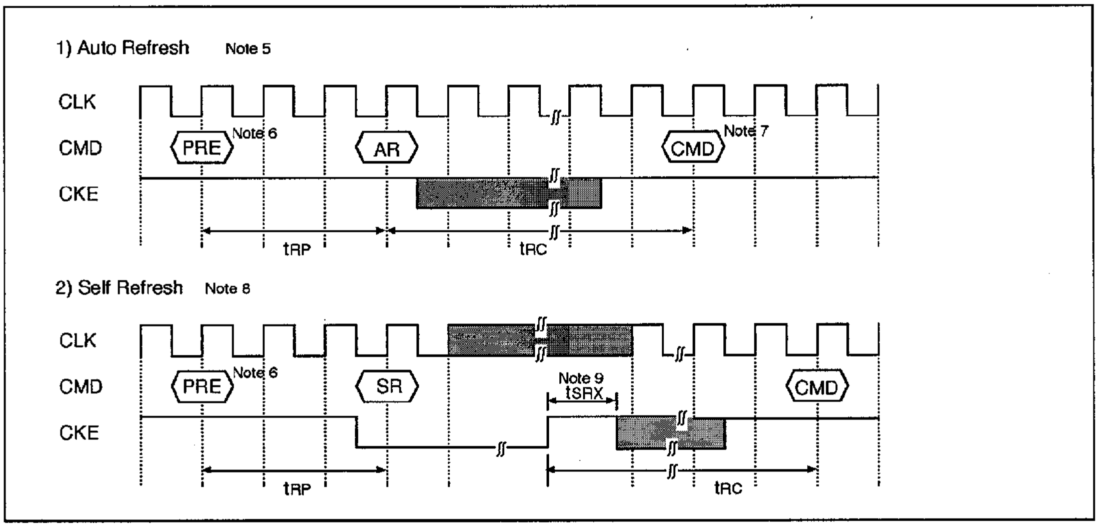
Note : 1. t_{RDL} : 1 CLK

2. t_{BDL} = 0 CLK ; Last Data in to Burst Stop Delay.
To inhibit write at the cycle of burst stop, DQM should be issued.
Read or write burst stop command is valid at every burst length.
3. Number of valid output data after Row precharge or burst stop : 0,1,2, for CAS Latency=1,2,3, Respectively.
4. PRE : Both Bank Precharge if necessary.
MRS can be issued only at both bank precharge state.

10. CLOCK Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh



Note :
1. Active power down : one or both bank active state.
2. Precharge power down : both bank precharge state.
3. t_{PDE} : Asynchronous AC parameter. Time for Power Down Exit Setup Time.
   Only valid at precharge power down exit.
4. $t_{SS} < t_{PDE}$, NOP should be issued. And new command can be issued after 1 Clock.
5. The auto refresh is the same as CBR refresh of conventional DRAM.
   No precharge commands are required after auto refresh command.
   During t_{RC} from auto refresh command, any other command cannot be accepted.
6. Before executing auto/self refresh command, both banks must be idle state.
7. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
8. During self refresh mode, refresh interval and refresh operation are performed internally.
   After self refresh entry, self refresh mode is kept while CKE is LOW.
   During self refresh mode, all inputs execept CKE will be don't care all outputs will be in a Hi-Z state.
   During tRC from self refresh exit command any other command cannot be accepted.
   Before/After self refresh mode, burst auto refresh cycle (2K cycle) is recommended.
9. t_{SRX} : minimum CKE "High" for Self Refresh Exit.

12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS, A_3 = "0". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=1,2,4,8 and full page.
	Interleave Counting	At MRS, A_3 = "1". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=4,8, At BL=1,2 Interleave Counting = Sequential Counting
Pseudo- MODE	*Pseudo-* Decrement Sequential Counting	At MRS, A_3 = "1". (Set to Interleave Counting Mode) Starting Address LSB 3 bits $A_{0\text{-}2}$ should be "000" or "111". @BL=8. -- if LSB = "000" : Increment Counting. -- if LSB = "111" : Decrement Counting. For Example, (Assume Addresses except LSB 3 bits are all 0, BL=8) -- @ write, LSB = "000", Accessed Column in order 0-1-2-3-4-5-6-7 -- @ read, LSB = "111", Accessed Column in order 7-6-5-4-3-2-1-0 At BL=4, same applications are possible. As above example, at Interleave Counting mode, by confining starting address to some values, *Pseudo-* Decrement Counting Mode can be realized. See the BURST SEQUENCE TABLE carefully.
Random MODE	Random column Access t_{CCD} = 1CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Dout Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS, $A_{2,1,0}$ = "000" At auto precharge, t_{RAS} should not be violated.
	2	At MRS, $A_{2,1,0}$ = "001" At auto precharge, t_{RAS} should not be violated.
	4	At MRS, $A_{2,1,0}$ = "010"
	8	At MRS, $A_{2,1,0}$ = "011"
	Full Page	At MRS, $A_{2,1,0}$ = "111" At the end of the burst length, burst will be stop automatically.
Special MODE	BRSW	At MRS, A_9 = "1" Read Burst = 1,2,4,8, full page/Write Burst = 1 At auto precharge of write, t_{RAS} should not be violated.
Random MODE	Burst Stop	t_{BDL}=0, Valid DQ after burst stop is 0,1,2 for CL 1,2,3 respectively Using burst stop command, any burst length control is possible.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t_{RDL}=1 with DQM, Vaild DQ after burst stop is 0,1,2 for CL 1,2,3 respectively During read/write burst with auto precharge, $\overline{RAS}$ interrupt cannot be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with auto precharge, $\overline{CAS}$ interrupt cannot be issued.

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	NOTE
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA,A10	ILLEGAL	2
	L	L	H	H	BA	RA	Row (& Bank) Active ; Latch RA	
	L	L	H	L	BA	A10	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP code	OP code	Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A10	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A10	Begin Write ; latch CA ; determine AP	2
	L	L	H	H	BA	RA	ILLEGAL	
	L	L	H	L	BA	A10	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	3
	L	H	L	H	BA	CA, A10	Term burst , New read, Determine AP	3
	L	H	L	L	BA	CA, A10	Term burst , New write, Determine AP	2
	L	L	H	H	BA	RA	ILLEGAL	
	L	L	H	L	BA	A10	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A10	Term burst, New read, Determine AP	3
	L	H	L	L	BA	CA, A10	Term burst, New write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	Term burst, Precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA,A10	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Pre-charging	H	X	X	X	X	X	NOP --> Idle after tRP	
	L	H	H	H	X	X	NOP --> Idle after tRP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	NOP --> Idle after tRP	4

FUNCTION TRUTH TABLE (TABLE 1, Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	NOTE
Row Activating	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	H	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP --> Idle after t_{RC}	
	L	H	H	X	X	X	NOP --> Idle after t_{RC}	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP --> Idle after 2 clocks	
	L	H	H	H	X	X	NOP --> Idle after 2 clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

ABBREVIATIONS :

RA = Row Address
BA = Bank Address
NOP = No Operation Command
CA = Column Address
AP = Auto Precharge

Notes :
1. All entries assume that CKE was active (High) during the preceding clock cycle and the current clock cycle.
2. Illegal to bank in specified state ; Function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and A_{10}).
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE for CKE (TABLE 2)

Current State (n)	CKE (n-1)	CKE n	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDR	ACTION	NOTE
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh --> Idle after t_{RC} (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh --> Idle after t_{RC} (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
Both Bank Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down --> ABI	7
	L	H	L	H	H	H	X	Exit Power Down --> ABI	7
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	Enter Power Down	8
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	X	X	ILLEGAL	
	H	L	L	L	L	H	X	Enter Self Refresh	8
	H	L	L	L	L	L	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP	
Any State other than Listed Above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain clock Suspend	

Abbreviations : ABI = All Banks Idle

Notes : 6. CKE low to high transition is asynchronous.
A minimum pulse width time t_{SRX} must be satisfied.
7. CKE low to high transition is asynchronous as if restarts internal clock.
A minimum setup time t_{PDE} must be satisfied before any command other than exit.
8. Power-down and self refresh can be entered only from the all banks idle state.
9. Must be a legal command.