2M x 16Bit x 2 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- SSTL_3 (Class II) compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - -. CAS Latency (2 & 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

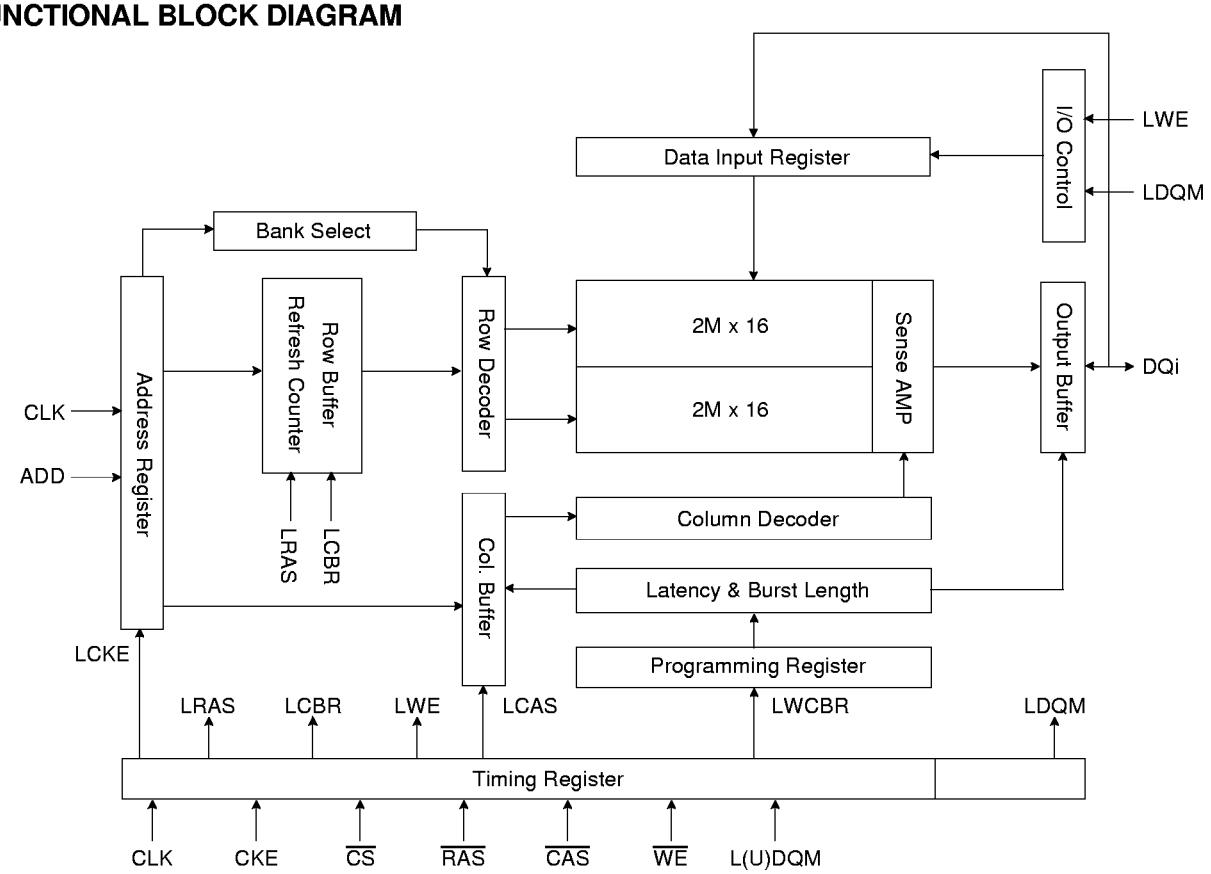
GENERAL DESCRIPTION

The KM416S4021B is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 2 x 2,097,152 words by 16 bits, fabricated with SAMSUNG s high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clcok cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

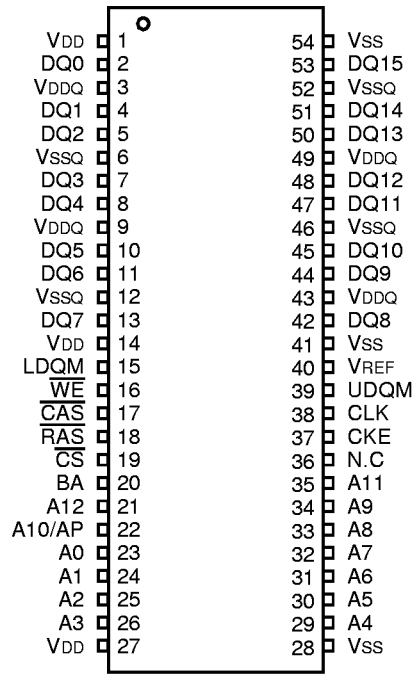
Part NO.	MAX Freq.	Interface	Package
KM416S4021BT-G7	143MHz	SSTL_3 (Class II)	54 TSOP(II)
KM416S4021BT-G8	125MHz		

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (TOP VIEW)



54PIN TSOP (II)
(400mil x 875mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{12}	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{12}, column address : CA_0 ~ CA_7
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
$DQ_{0 \sim 15}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
V_{REF}	*Reference Voltage*	Reference voltage for inputs.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device supply voltage	V_{DD}	3.0	-	3.6	V	1
Output supply voltage	V_{DDQ}	3.0	3.3	3.6	V	1
Input reference voltage	V_{REF}	1.3	1.5	1.7	V	2, 3
Termination voltage	Vtt	V_{REF}-0.05	V_{REF}	V_{REF}+0.05	V	
Input logic high votlage	V_{IH}	V_{REF}+0.2	-	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	V_{REF}-0.2	V	2
Output logic high voltage	V_{OH}	Vtt+0.8	-	-	V	5
Output logic low voltage	V_{OL}	-	-	Vtt-0.8	V	5
Input leakage current	I_{IL}	-5	-	5	uA	6
Output leakage current	I_{OL}	-5	-	5	uA	7

Note : 1.Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
2. Typically, the value of V_{REF} is expected to be about 0.45 *V_{DDQ} of the transmitting device. V_{REF} is expected to track variations in V_{DDQ}.
3. Peak to peak AC noise on V_{REF} may not exceed 2% V_{REF} (DC)
4. Vtt of transmitting device must track V_{REF} of receiving device.
5. Voltage level measured at device pin with I_{OH}/I_{OL} = -16mA/16mA.
6. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
7. Dout buffer is disabled, 0V ≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & L(U)DQM	C_{IN}	2	4	pF
Address	C_{ADD}	2	4	pF
DQ_0 ~ DQ_{15}	C_{OUT}	2	5	pF

DC CHARACTERISTICS

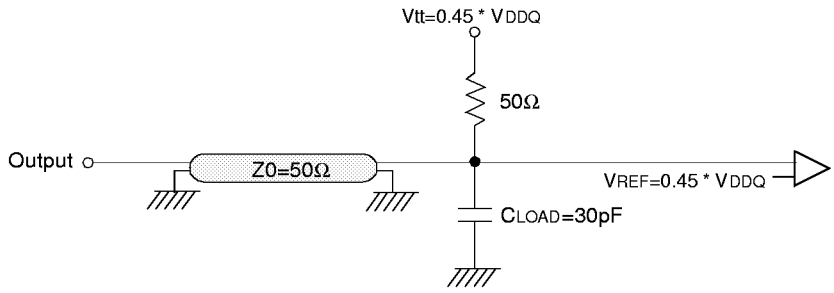
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -7	Version -8	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		120	110	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE≤V_{IL}(max), t_{CC} = 15ns		2		mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), t_{CC} = ∞		2			
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		20		mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC} = ∞ Input signals are stable		10			
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), t_{CC} = 15ns		3		mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), t_{CC} = ∞		2			
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		30		mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC} = ∞ Input signals are stable		25		mA	
Operating Current (Burst Mode)	I_{CC4}	I_O = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	170	150	mA	1
			2	120	110		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		160	150	mA	2
Self Refresh Current	I_{CC6}	CKE≤V_{IL}(max)		2		mA	3

Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
Input reference voltage	0.45 *V_{DDQ}	V
Input signal maximum peak swing	2.0	V
Inout signal minimum slew rate	1.0	V / ns
AC Input levels (Vih/Vil)	V_{REF}+0.4 / V_{REF}-0.4	V
Input timing measurement reference level	V_{REF}	V
Output timing measurement reference level	Vtt	V
Output load condition	See Fig. 1	



(Fig. 1) Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Veraion		Unit	Note
			-7	-8		
Row active to row active delay		$t_{RRD(min)}$	14	16	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	21	24	ns	1
Row precharge time		$t_{RP(min)}$	21	24	ns	1
Row active time		$t_{RAS(min)}$	48	50	ns	1
		$t_{RAS(max)}$	100		us	
Row cycle time		$t_{RC(min)}$	70	80	ns	1
Last data in to new col. address delay		$t_{CDL(min)}$	1		CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1		CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1		CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-7		-8		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7	1000	8	1000	ns	1
	CAS latency=2		12		13			
CLK to valid output delay	CAS latency=3	tSAC		5.5		6	ns	1, 2
	CAS latency=2			7		8		
Output data hold time		tOH	2.5		2.5		ns	2
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2.5		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.5		6	ns	
	CAS latency=2			7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM416S4021BT-G7 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	21ns	14ns	21ns	7ns	7ns	7ns
143MHz (7.0ns)	3	10	7	3	2	3	1	1	1
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	3	2	3	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	1	2	1	1	1

KM416S4021BT-G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	7	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	7	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	1	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don t Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA is ignored and both banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Wirte DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)