256K x 4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM44C256C/CL/CSL-6	60ns	15ns	110ns
KM44C256C/CL/CSL-7	70ns	20ns	130ns
KM44C256C/CL/CSL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or Output Enable Controlled Write**
- **Single 5V±10% power supply**
- **Refresh Cycle**
  - **— 512 cycle/8ms refresh (Normal)**
  - **— 512 cycle/64ms refresh (L-version)**
  - **— 512 cycle/128ms refresh (SL-version)**
- **Power Dissipation**
  - **—Standby : 5.5mW (Normal)**
    1.1mW (L-version)
    0.55mW (SL-version)
  - **— Active(60/70/80ms) : 385/360/330mW**
- **JEDEC standard pinout**
- **Available in plastic DIP, SOJ, ZIP, TSOP(I), and TSOP(II) Packages**

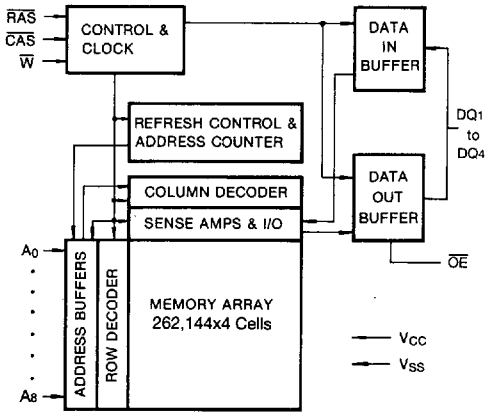
GENERAL DESCRIPTION

The Samsung KM44C256C/CL/CSL is a CMOS high speed 262,144 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance microprocessor computers.

The KM44C256C/CL/CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C256C/CL/CSL is fabricated using Samsung's advanced CMOS process.

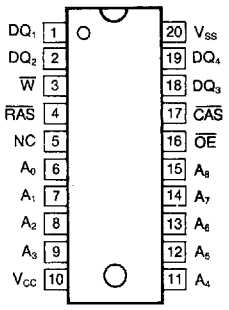
FUNCTIONAL BLOCK DIAGRAM



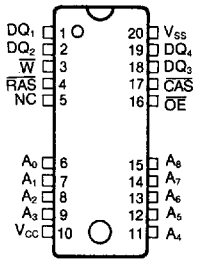
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

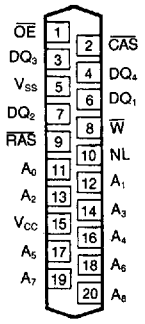
• KM44C256CP/CLP/CSLP



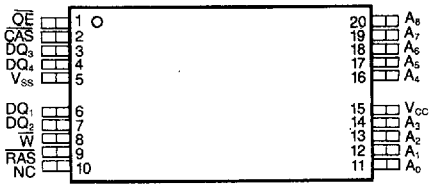
• KM44C256CJ/CLJ/CSLJ



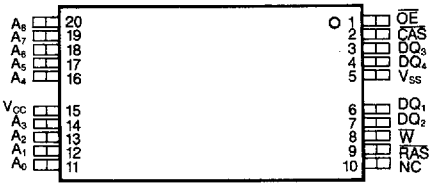
• KM44C256CZ/CLZ/CSLZ



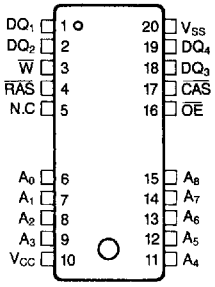
• KM44C256CV/CLV/CSLV



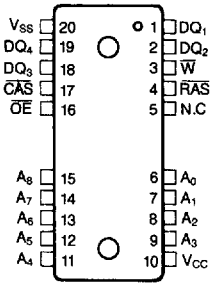
• KM44C256CVR/CLVR/CSLVR



• KM44C256CT/CLT/CSLT



• KM44C256CTR/CLTR/CSLTR



Pin Names	Pin Function
A_0-A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1-DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
NL	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V_{DD}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	Vcc +1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM44C256C/CL/CSL-6	I_{CC1}	-	70	mA
	KM44C256C/CL/CSL-7		-	65	mA
	KM44C256C/CL/CSL-8		-	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM44C256C/CL/CSL-6	I_{CC3}	-	70	mA
	KM44C256C/CL/CSL-7		-	65	mA
	KM44C256C/CL/CSL-8		-	60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM44C256C/CL/CSL-6	I_{CC4}	-	55	mA
	KM44C256C/CL/CSL-7		-	50	mA
	KM44C256C/CL/CSL-8		-	45	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)	KM44C256C	I_{CC5}	-	1	mA
	KM44C256CL		-	200	μA
	KM44C256CSL		-	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM44C256C/CL/CSL-6	I_{CC6}	-	70	mA
	KM44C256C/CL/CSL-7		-	65	mA
	KM44C256C/CL/CSL-8		-	60	mA
Battery Back Up Current Average Power Supply Current, Battery back up Mode ($\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V, $\overline{W}$=Vcc-0.2V or o.2V, A_0~A_9= Vcc-0.2V or o.2V, D_{IN}=Vcc-0.2V, o.2V or OPEN : t_{RC}=250μS, t_{RAS}=t_{RAS} min.~1μS)	KM44C256CL	I_{CC7}	-	200	μA
	KM44C256CSL		-	100	μA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤Vcc)		$I_{O(L)}$	-10	10	μA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}, I_{CC4}, Address can be changed maximum once during a Fast Page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		175		195		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	55		55		60		ns	6
Write command pulse width	tWP	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	50		55		60		ns	6
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (Low power)	tREF		64		64		64	ms	
Refresh period (Super Low power)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		45		45		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		35		40	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		85		90		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	tCP	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	20		20	ns	
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

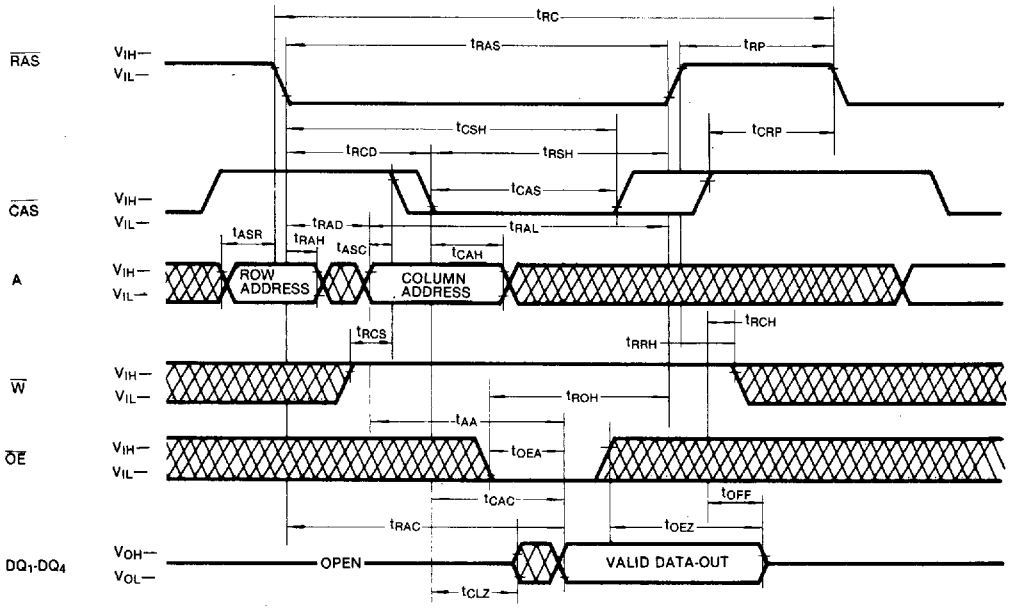
NOTES (Continued)

5. Assumes that $t_{RCD} \geq t_{RCD}(max)$.
6. t_{WCR}, t_{DHR} are referenced to $t_{RAD}(max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}(min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(min)$, $t_{RWD} \geq t_{RWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAC}(max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled by t_{AA}.

2

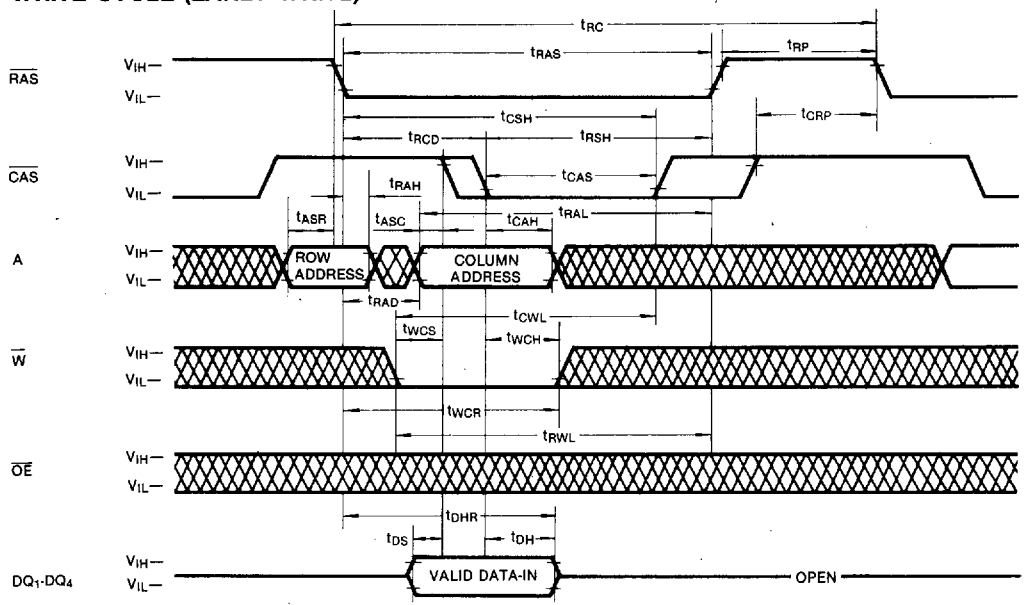
TIMING DIAGRAMS

READ CYCLE

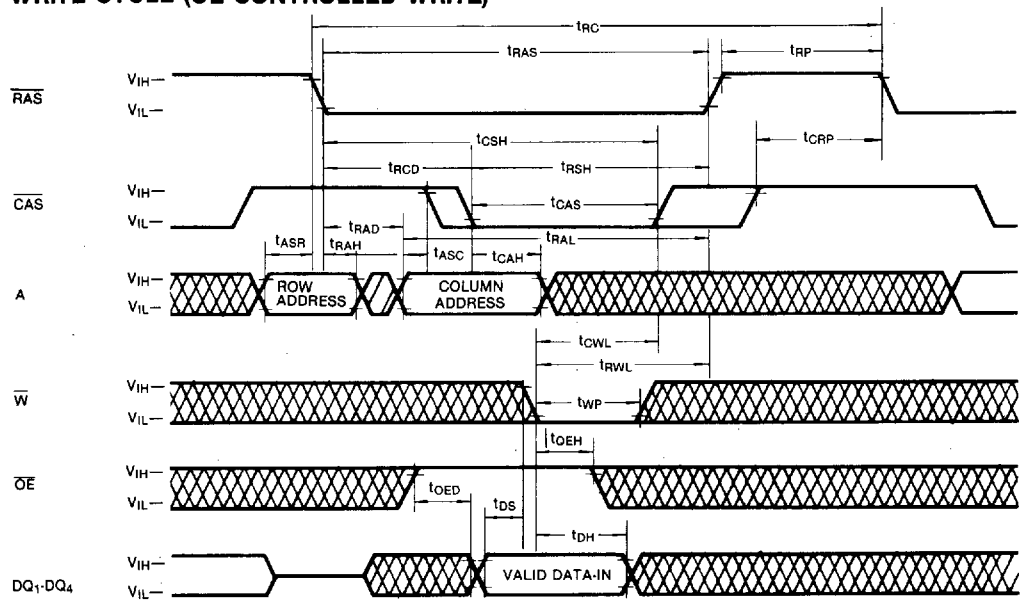


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

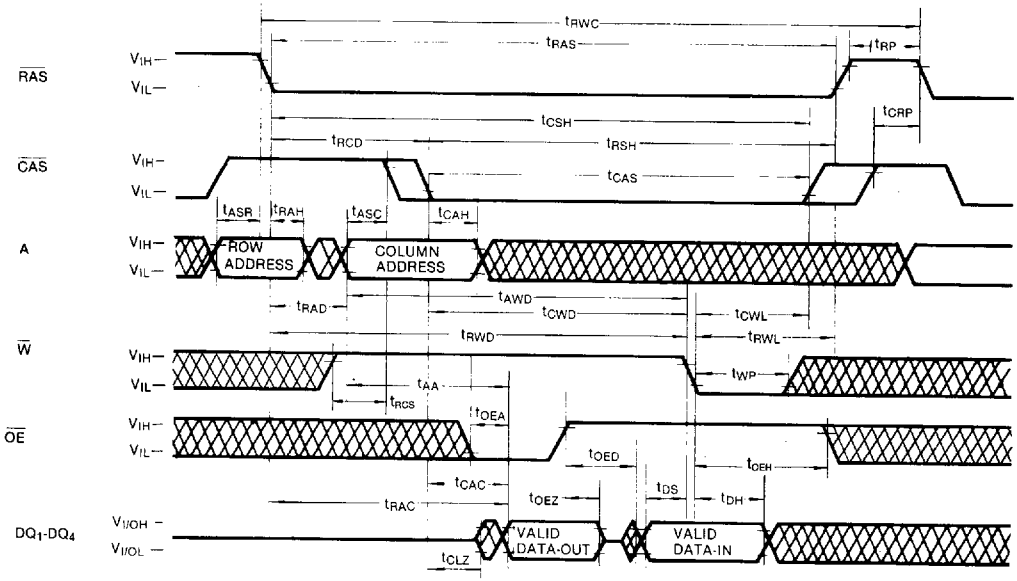


WRITE CYCLE (OE CONTROLLED WRITE)

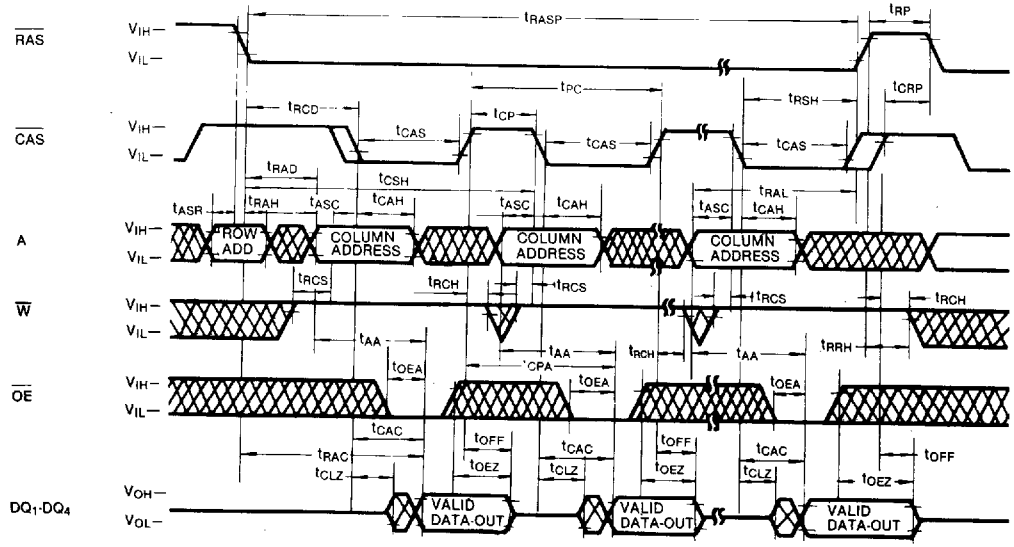


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

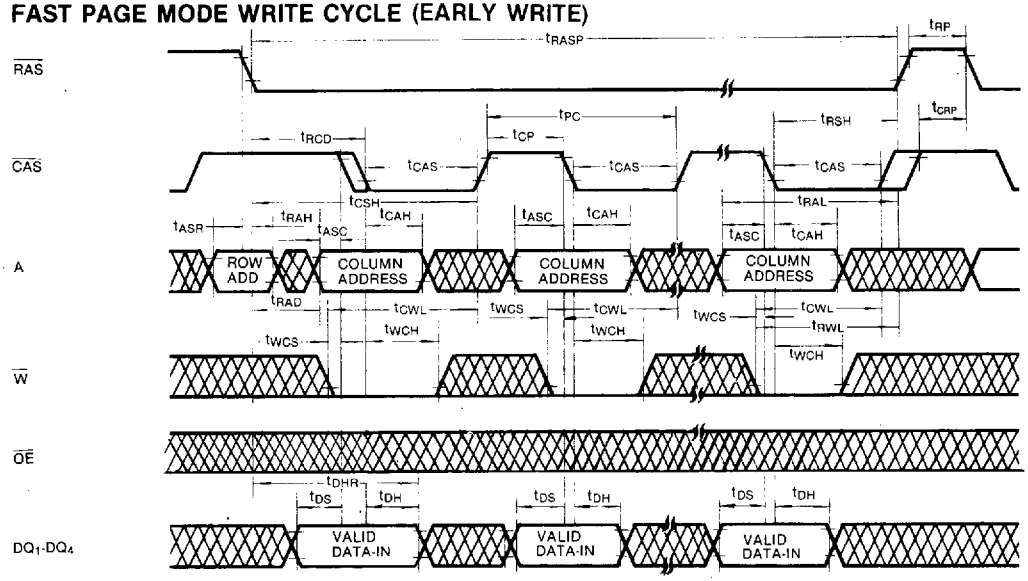


DON'T CARE

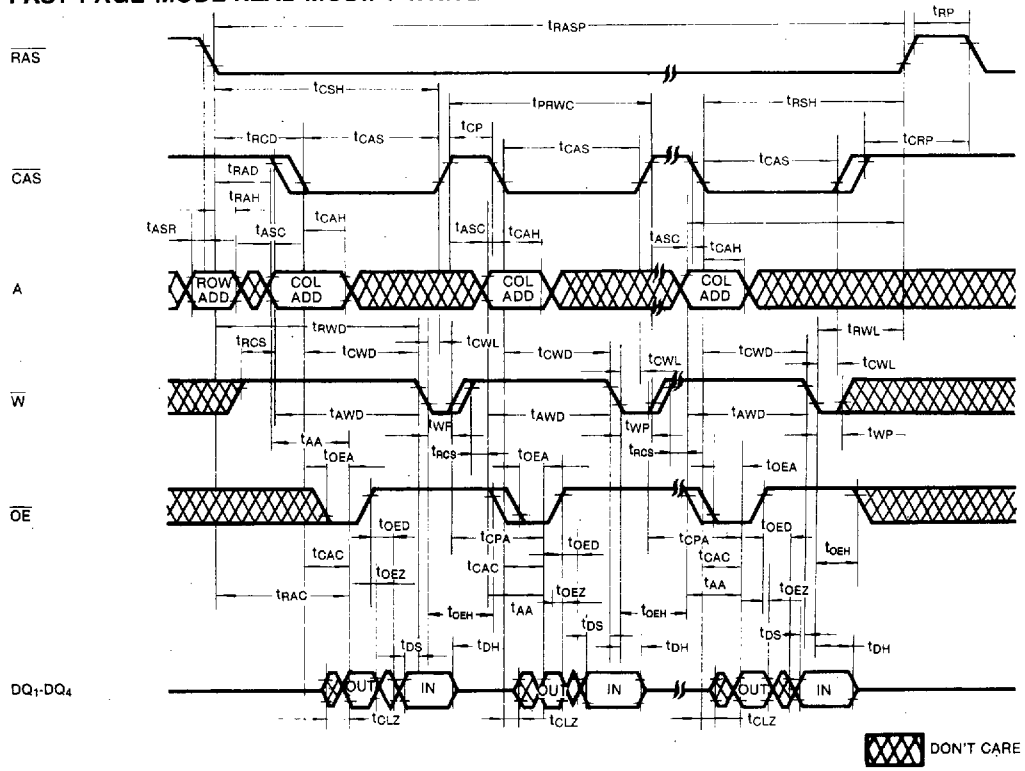
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE

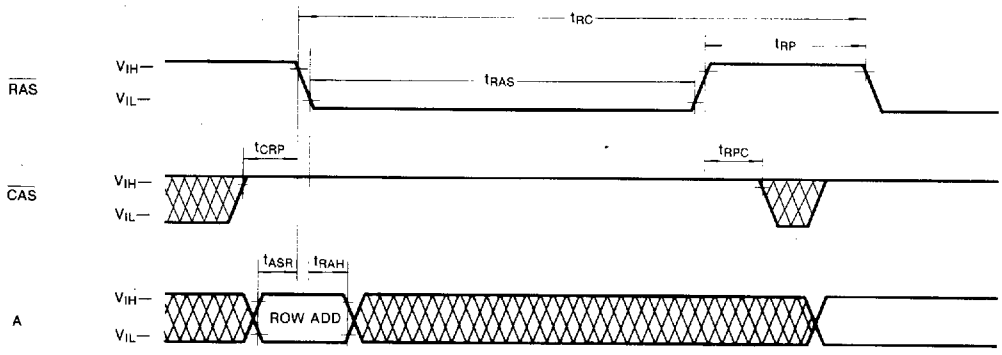


SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

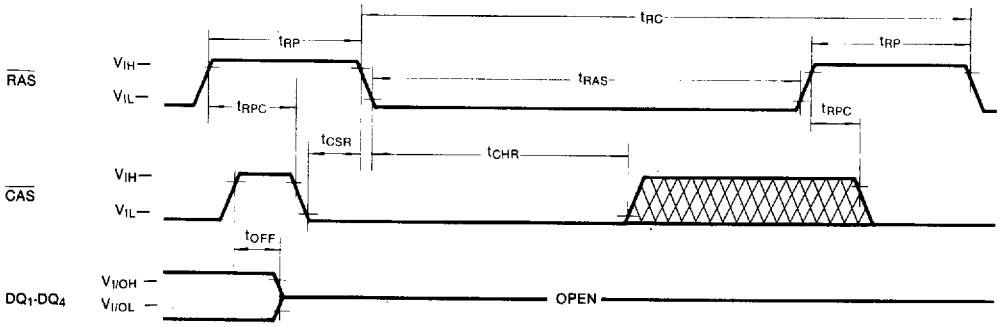
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

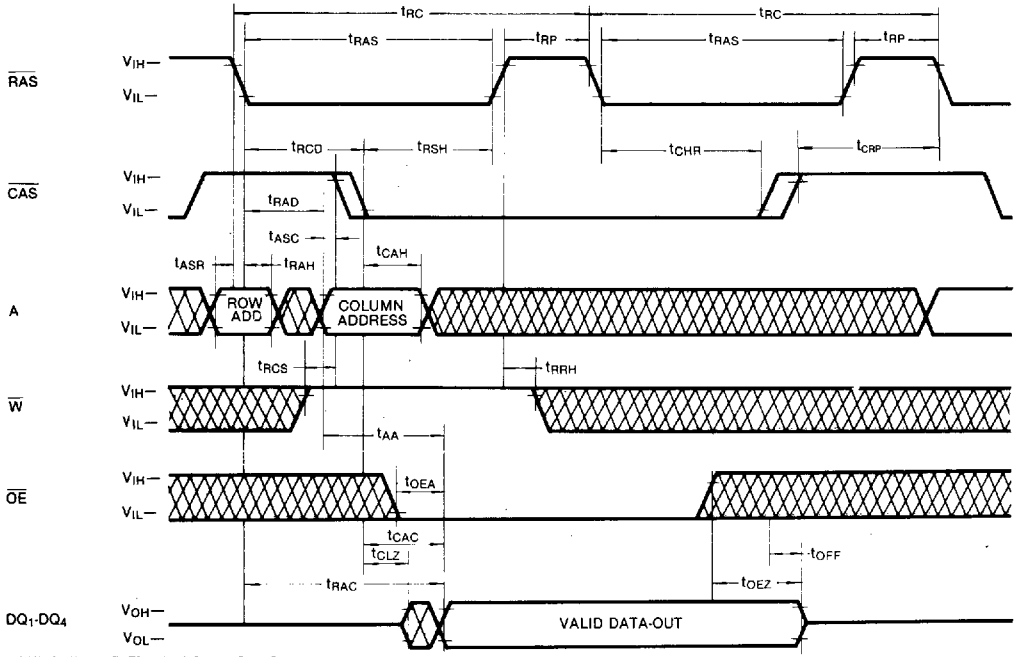
Note: $\overline{W}$, $\overline{OE}$, A = Don't care



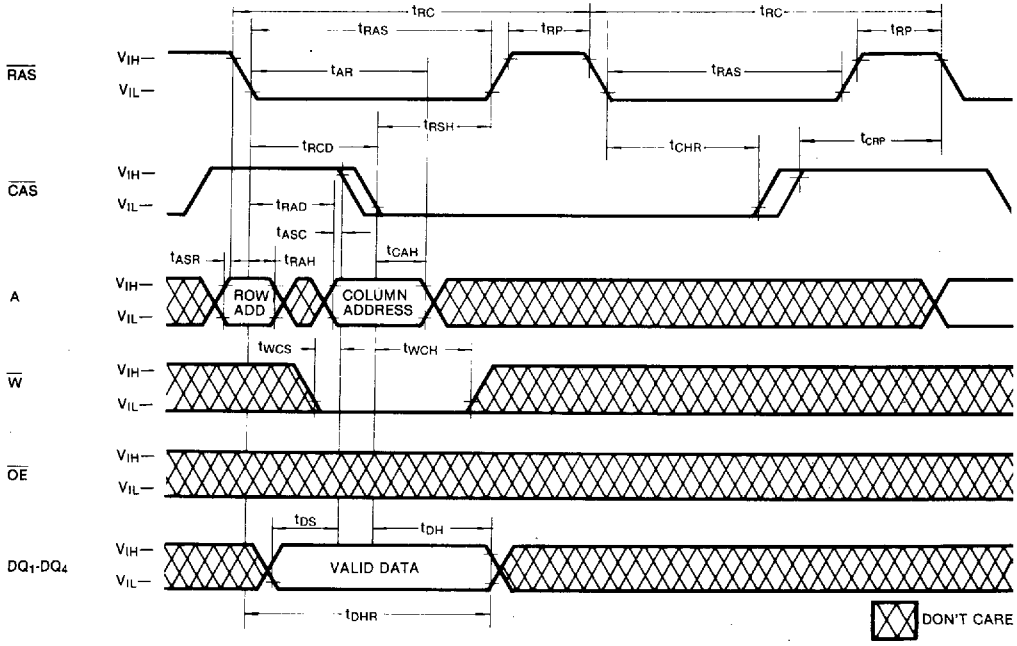
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

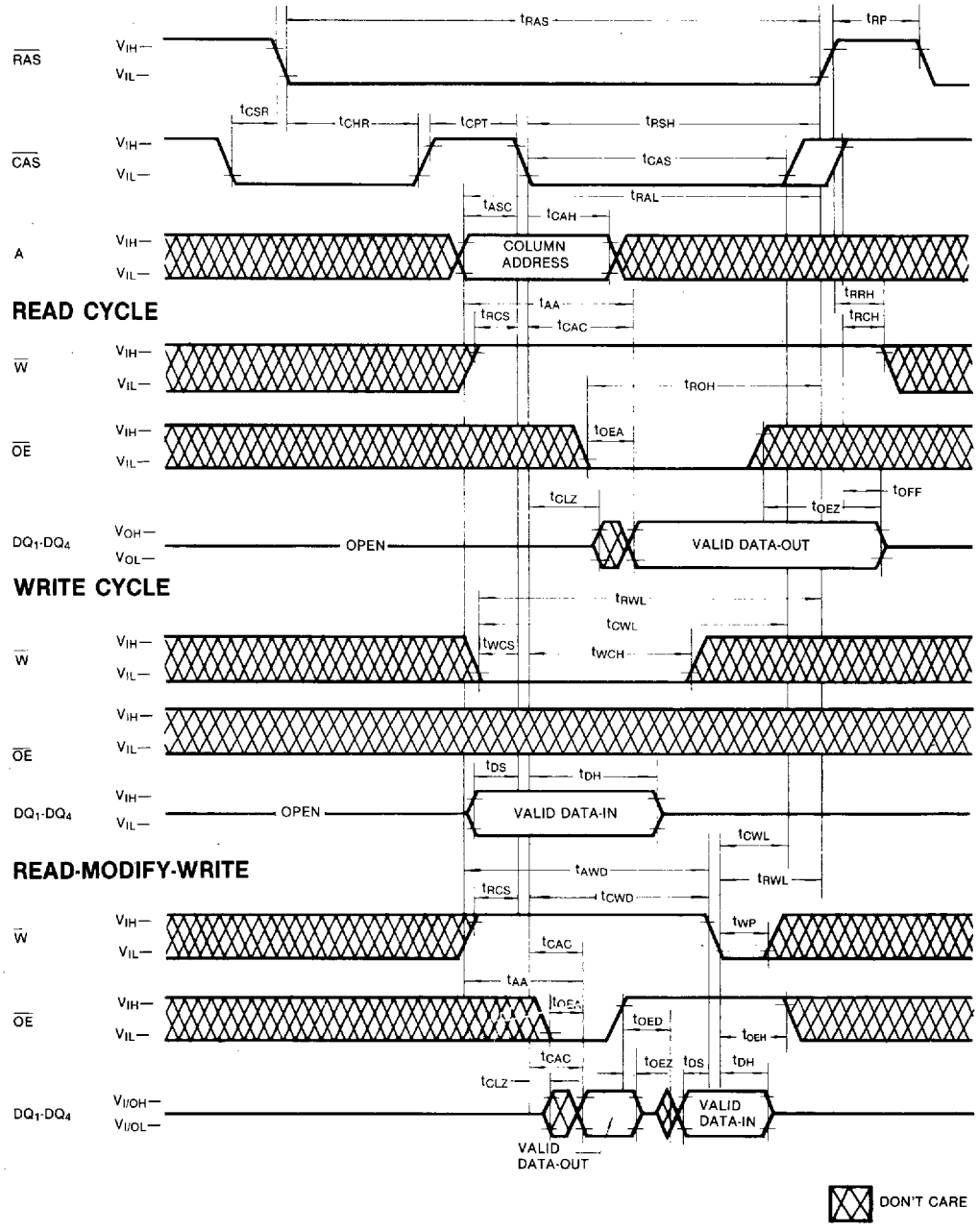


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device operation

The KM44C256C/CL/CSL contains 1,048,576 memory locations organzed as 262,144 four-bit words. Eighteen address bits are required to address a paricular 4-bit word in the memory array. Since the KM44C256C/CL-/CSL has only 9 address input pins,time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column adress strobe($\overline{CAS}$), and the valid row and column address inputs.

Operation of the KM44C256C/CL/CSL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C256C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C256C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max), then the access time to valid data is specified by t_{RAC}(min). However if $\overline{CAS}$ goes low after t_{RCD}(max), or if the column address becomes valid after t_{RAD}(max.), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

The KM44C256C/CL/CSL has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, OE must be low for the period of time defined by to t_{OEA} and t_{OEZ}.

Write

The KM44C256C/CL/CSL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pin is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in he Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contiain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C256C/CL/CSL's DQ pins.

Data Output

The KM44C256C/CL/CSL has a three-state output buffer which is controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever $\overline{CAS}$ or $\overline{OE}$ is high(V_{IH}), the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C256C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode

DEVICE OPERATION (Continued)

Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$ only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C256C/CL/CSL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8/64/128 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A_0~A_8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C256C/CL/CSL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C256C/CL/CSL hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C256C/CL/CSL by using read, write or read-modify write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the low address bits A_0 through A_8 are supplied by the on-chip refresh counter.

Fast Page Mode

The Fast page mode Provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. Then, while $\overline{RAS}$ is kept low to maintain the row address $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time requried to set up and strobe sequential row addresses for the same page

Power-up

If $\overline{RAS}$=V_{SS} during power-up, the KM44C256C/CL/CSL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current. An initial pause of 200 μ sec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C256C/CL/CSL inputs act like unteminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used,series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C256-C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transisient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS

DEVICE OPERATION (Continued)

run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

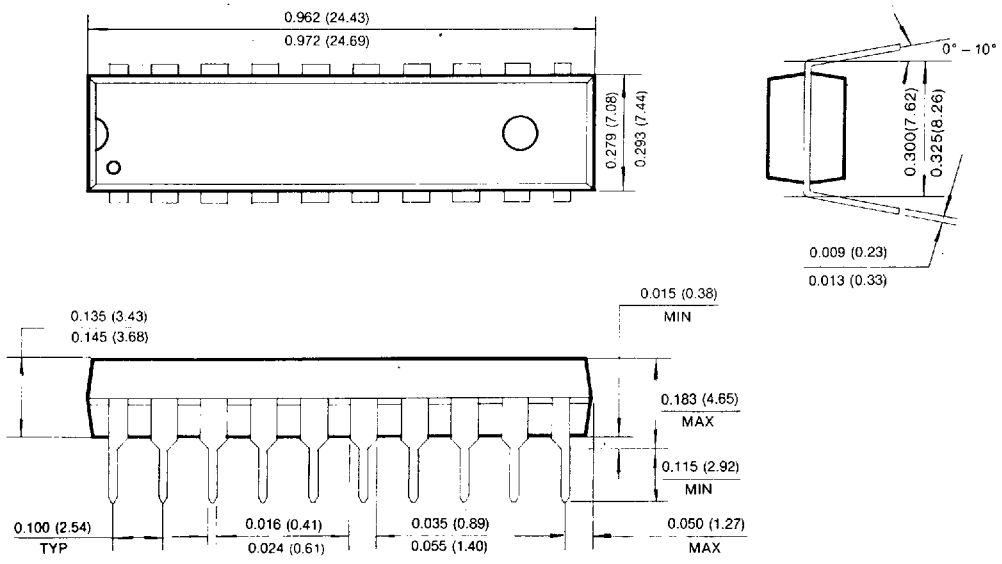
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM44C256C/CL/CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C256C/CL/CSL and they supply much of the current used by the KM44C256-C/CL/CSL during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (Millimeters)

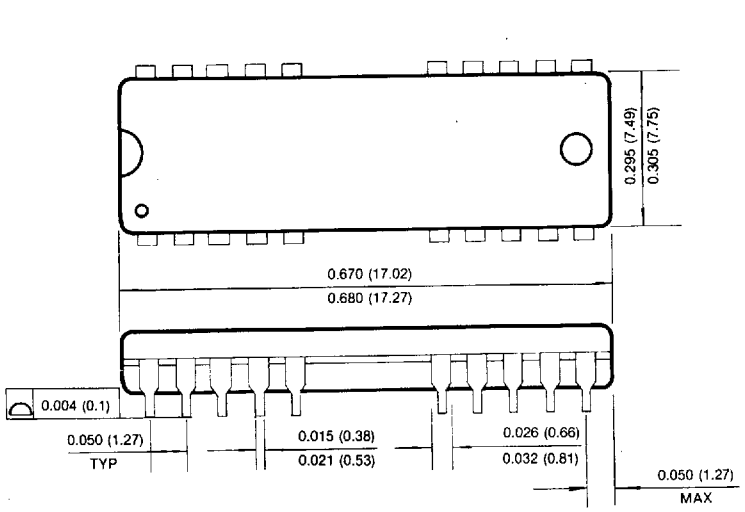


SAMSUNG ELECTRONICS

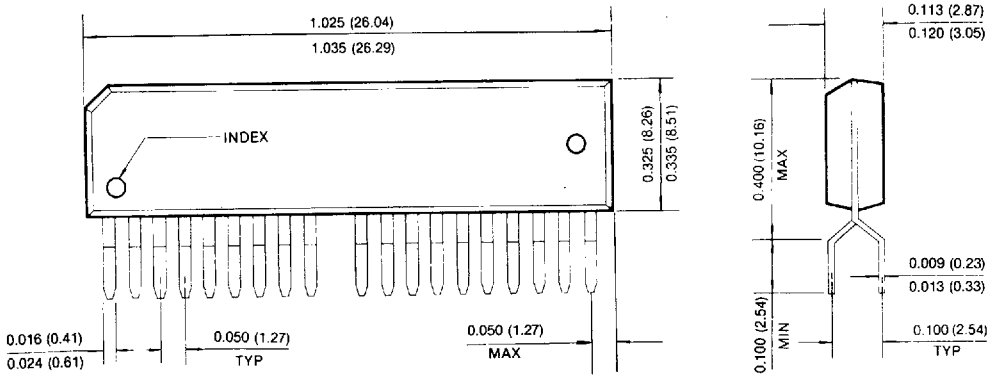
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

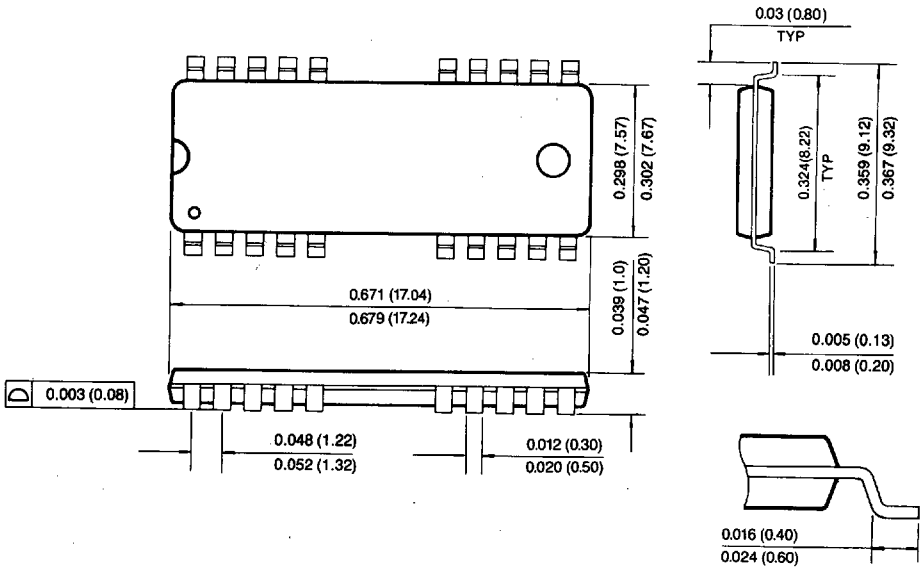


SAMSUNG ELECTRONICS

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)